BACKUP-BATTERY SUPERVISORS FOR RAM RETENTION

FEATURES

- **Supply Current of 40 μA (Max)**
- **Battery-Supply Current of 100 nA (Max)**
- **Precision Supply Voltage Monitor 3.3 V, 5 V, Other Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Voltage Monitor For Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal (TPS3619)**
- **Pin-For-Pin Compatible With MAX819, MAX703, and MAX704**
- **8-Pin MSOP Package**
- **Temperature Range -40°C to 85°C**

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery-Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

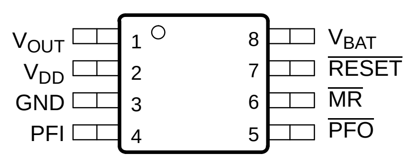
DESCRIPTION

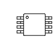
The TPS3619 and TPS3620 families of supervisory circuits monitor and control processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on, $\overline{RESET}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{RESET}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above V_{IT}. When the supply voltage drops below $V_{IT,}$ the output becomes active (low) again.

The product spectrum is designed for supply voltages of 3.3 V and 5 V. The TPS3619 and TPS3620 are available in an 8-pin MSOP package and are characterized for operation over a temperature range of -40°C to 85°C.

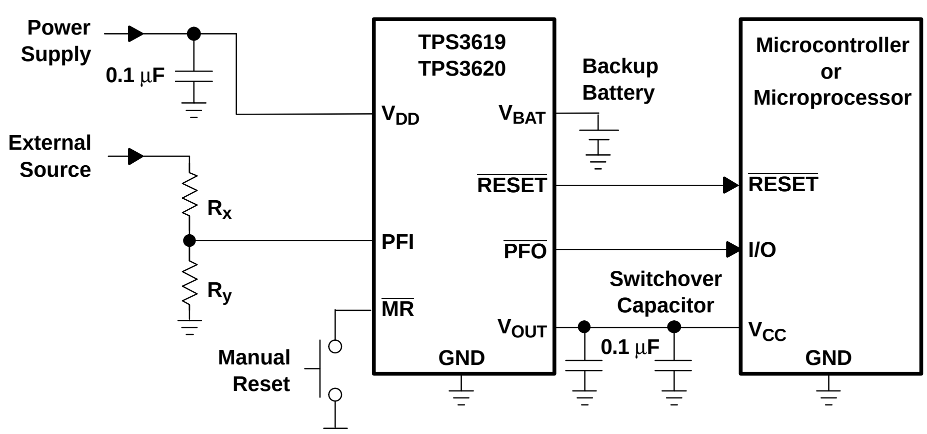
DGK PACKAGE
(TOP VIEW)





ACTUAL SIZE
3,05 mm x 4,98 mm

TYPICAL OPERATING CIRCUIT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

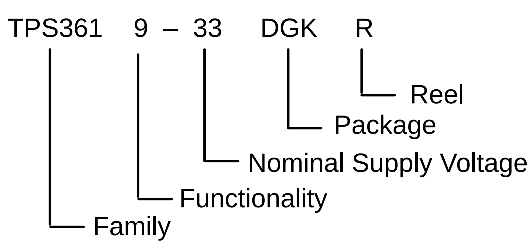
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS3619-33	-40°C to 85°C	AFL	TPS3619-33DGK	Tube, 80
			TPS3619-33DGKR	Tape and Reel, 2500
TPS3619-50		AFM	TPS3619-50DGK	Tube, 80
			TPS3619-50DGKR	Tape and Reel, 2500
TPS3620-33		ANL	TPS3620-33DGKT	Tape and Reel, 250
			TPS3620-33DGKR	Tape and Reel, 2500
TPS3620-50		ANM	TPS3620-50DGKT	Tape and Reel, 250
			TPS3620-50DGKR	Tape and Reel, 2500

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

STANDARD AND APPLICATION SPECIFIC VERSIONS



DEVICE NAME	NOMINAL VOLTAGE(1), V_{NOM}
TPS3619-33 DGK	3.3 V
TPS3619-50 DGK	5.0 V
TPS3620-33 DGK	3.3 V
TPS3620-50 DGK	5.0 V

(1) For other threshold voltage versions, contact the local TI sales office for availability and lead-time.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

		UNIT
Supply voltage:	V_{DD}(2)	7 V
	$\overline{MR}$ and PFI pins(2)	-0.3 V to (V_{DD} + 0.3 V)
Continuous output current:	V_{OUT}, I_O	400 mA
	All other pins, I_O(2)	±10 mA
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A		-40°C to 85°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A= 70°C POWER RATING	T_A = 85°C POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage, V_{IL}		0.3 x V_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at $\overline{MR}$		100	ns/V
Slew rate at V_{DD} or V_{BAT},Δ t/ΔV		1	V/µs
Operating free-air temperature range, T_A	-40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V,	I_{OH} = -400 µA	V_{DD} - 0.2 V			V
			V_{DD} = 3.3 V,	I_{OH} = -2 mA	V_{DD} - 0.4 V			
			V_{DD} = 5 V,	I_{OH} = -3 mA	V_{DD} - 0.4 V			
		$\overline{PFO}$	V_{DD} = 1.8 V,	I_{OH} = -20 µA	V_{DD} - 0.3 V			V
			V_{DD} = 3.3 V,	I_{OH} = -80 µA	V_{DD} - 0.4 V			
			V_{DD} = 5 V,	I_{OH} = -120 µA	V_{DD} - 0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{DD} = 1.8 V,	I_{OL} = -400 µA			0.2	V
			V_{DD} = 3.3 V,	I_{OL} = 2 mA			0.4	
			V_{DD} = 5 V,	I_{OL} = 3 mA			0.4	
V_{res}	Powerup reset voltage (see (1))		I_{OL} = 20 µA, V_{BAT} > 1.1 V or V_{DD} > 1.1 V				0.4	V
V_{OUT}	Normal mode		I_{OUT} = 8.5 mA, V_{BAT} = 0 V	V_{DD} = 1.8 V	V_{DD} - 50 V			V
			I_{OUT} = 125 mA, V_{BAT} = 0 V	V_{DD} = 3.3 V	V_{DD} - 150 V			
			I_{OUT} = 200 mA, V_{BAT} = 0 V	V_{DD} = 5 V	V_{DD} - 200 V			
	Battery-backup mode		I_{OUT} = 0.5 mA, V_{BAT} = 1.5 V	V_{DD} = 0 V	V_{BAT} - 20 mV			V
			I_{OUT} = 7.5 mA, V_{BAT} = 3.3 V		V_{BAT} - 113 mV			
$r_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V			0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{DD} = 3.3 V			8	15	
V_{IT-}	Negative-going input threshold voltage (see (2))	TPS3619-33	T_A = -40°C to 85°C		2.88	2.93	3	V
		TPS3619-50			4.46	4.55	4.64	
V_{PFI}		PFI			1.13	1.15	1.17	

(1) The lowest supply voltage at which RESET becomes active. $t_{r,VDD} \geq$ 15 µs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V			20		mV
			2.5 V < V_{IT} < 3.5 V			40		
			3.5 V < V_{IT} < 5.5 V			60		
		PFI				12		
		VBSW (see (3))	V_{DD} = 1.8 V			55		
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 x V_{DD}	V_{DD} = 5 V	-33		-76	µA
I_{IL}	Low-level input current		$\overline{MR}$ = 0 V		-110		-255	
I_I	Input current	PFI			-25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V	V_{DD} = 1.8 V			-0.3	mA
				V_{DD} = 3.3 V			-1.1	
				V_{DD} = 5 V			-2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}				40	µA
			V_{OUT} = V_{BAT}				40	
$I_{(BAT)}$	V_{BAT} supply current		V_{OUT} = V_{DD}		-0.1		0.1	µA
			V_{OUT} = V_{BAT}				0.5	
C_i	Input capacitance		V_I = 0 V to 5 V			5		pF

(3) For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}.

TIMING REQUIREMENTS

at R_L = 1 MΩ, C_L = 50 pF, T_A = -40°C to 85°C

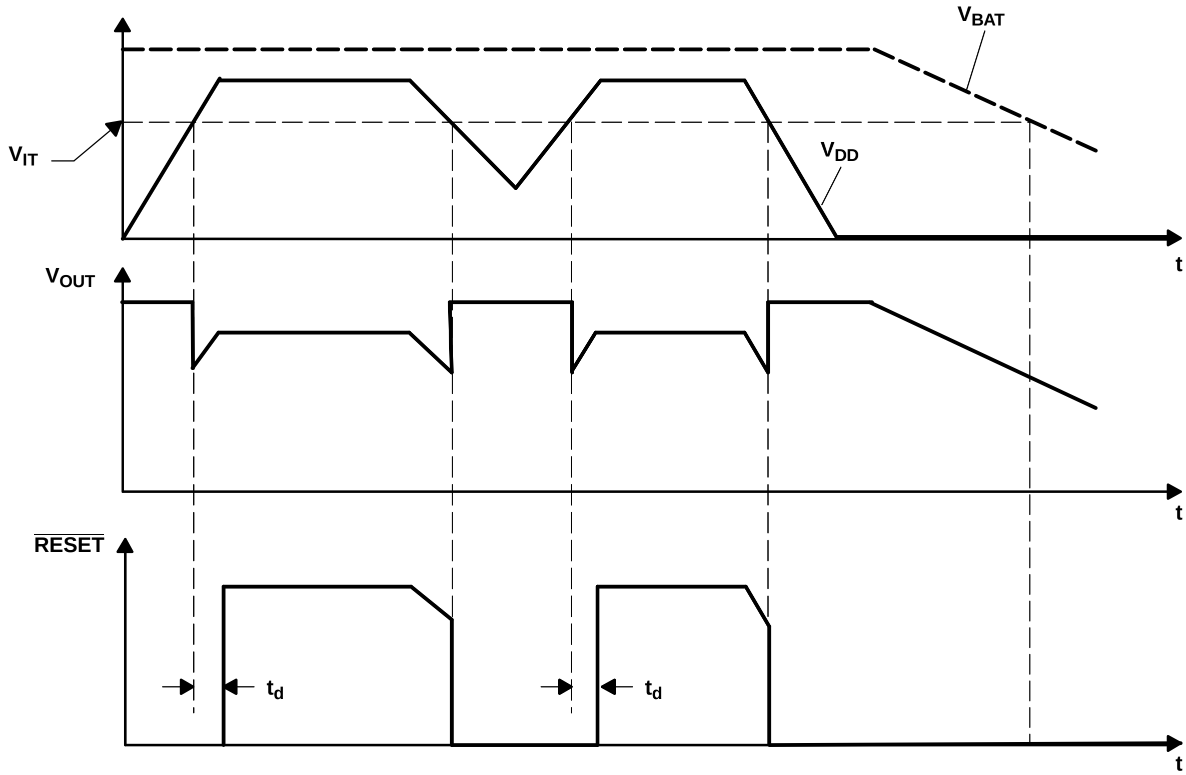
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	V_{IH} = V_{IT} + 0.2 V, V_{IL} = V_{IT} - 0.2 V	6			µs
		at $\overline{MR}$	V_{DD} = V_{IT} + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns

SWITCHING CHARACTERISTICS

at R_L = 1 MΩ, C_L= 50 pF, T_A= -40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ V_{IT}+ 0.2 V, $\overline{MR}$ ≥ 0.7 x V_{DD} See timing diagram	60	100	140	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	V_{DD} to $\overline{RESET}$	V_{IL} = V_{IT} - 0.2 V, V_{IH} = V_{IT}+ 0.2 V		2	5	µs
		PFI to $\overline{PFO}$ delay	V_{IL} = V_{PFI} - 0.2 V, V_{IH} = V_{PFI}+ 0.2 V		3	5	
		$\overline{MR}$ to $\overline{RESET}$	V_{DD} ≥ V_{IT}+ 0.2 V, V_{IL}= 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}		0.1	1	

TIMING DIAGRAM



FUNCTION TABLE

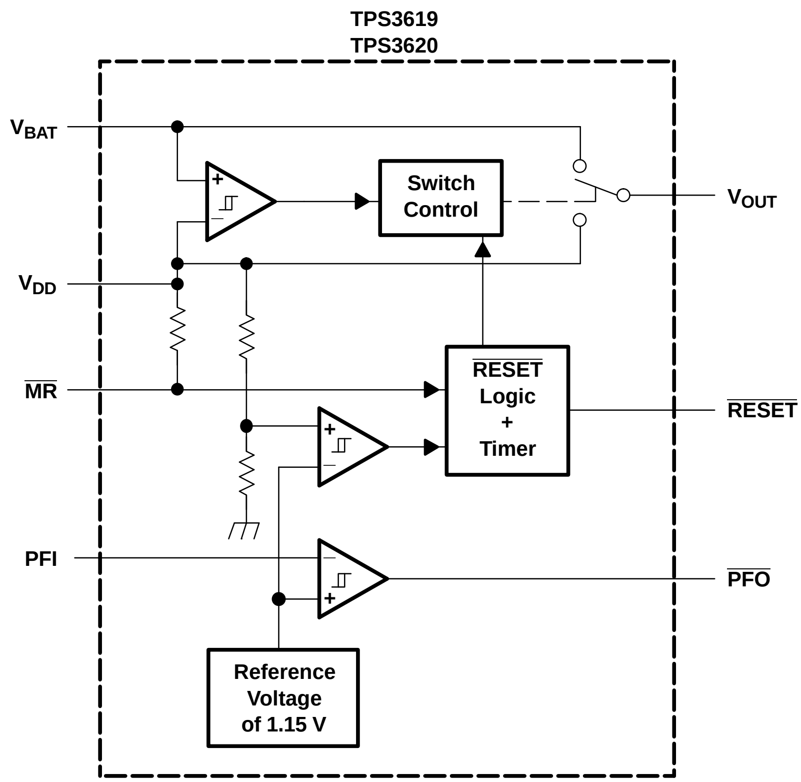
V_{DD} > V_{IT}	V_{DD} > V_{BAT}	$\overline{MR}$	V_{OUT}	$\overline{RESET}$
0	0	0	V_{BAT}	0
0	0	1	V_{BAT}	0
0	1	0	V_{DD}	0
0	1	1	V_{DD}	0
1	0	0	V_{DD}	0
1	0	1	V_{DD}	1
1	1	0	V_{DD}	0
1	1	1	V_{DD}	1

PFI > V_{PFI}	$\overline{PFO}$
0	0
1	1
CONDITION.: V_{DD} > V_{DD}_MIN	

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	3	I	Ground
$\overline{MR}$	6	I	Manual reset input
PFI	4	I	Power-fail comparator input
$\overline{PFO}$	5	O	Power-fail comparator output
$\overline{RESET}$	7	O	Active-low reset output
V_{BAT}	8	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

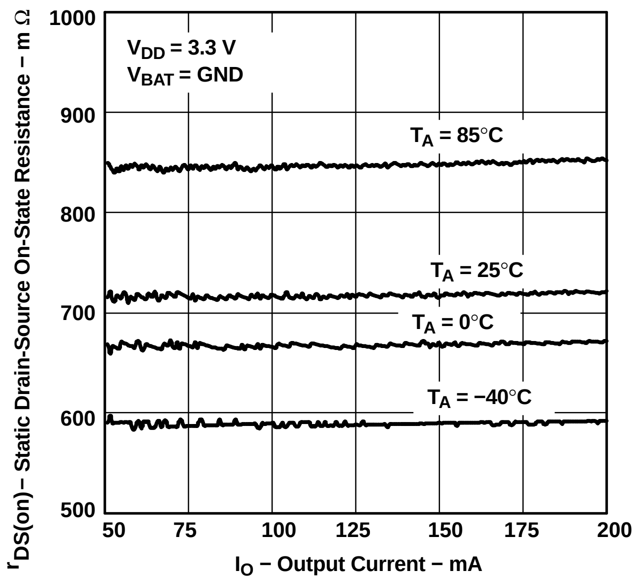


Figure 1.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

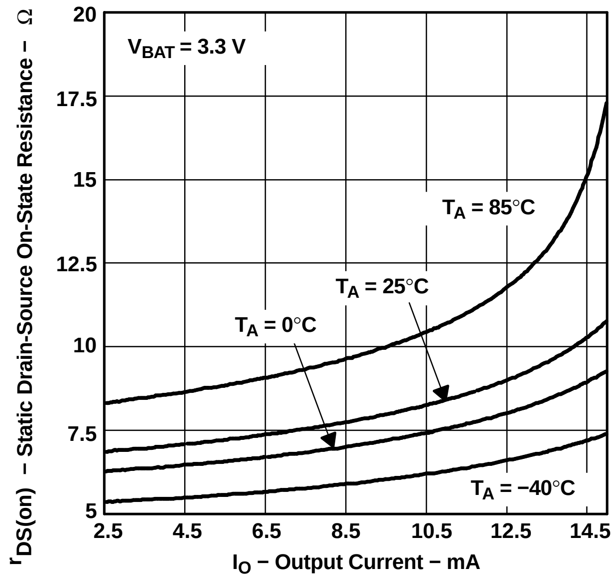


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

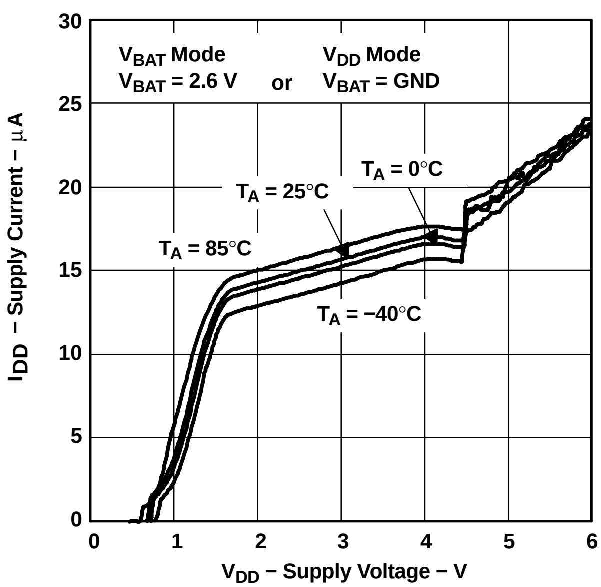


Figure 3.

NORMALIZED THRESHOLD AT RESET vs FREE-AIR TEMPERATURE

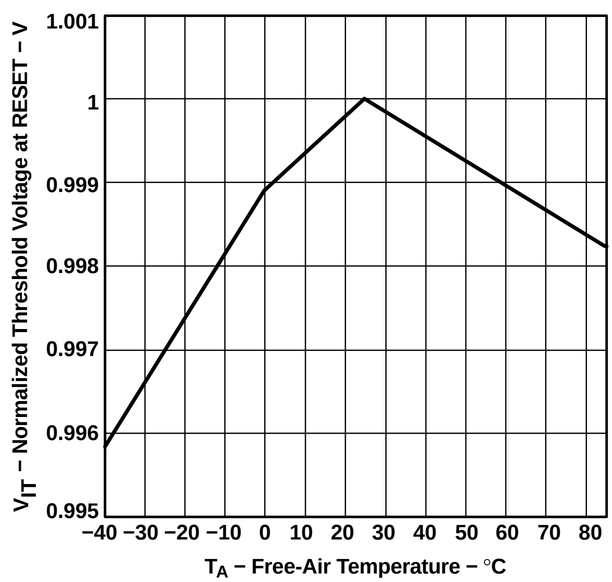


Figure 4.

TYPICAL CHARACTERISTICS (continued)

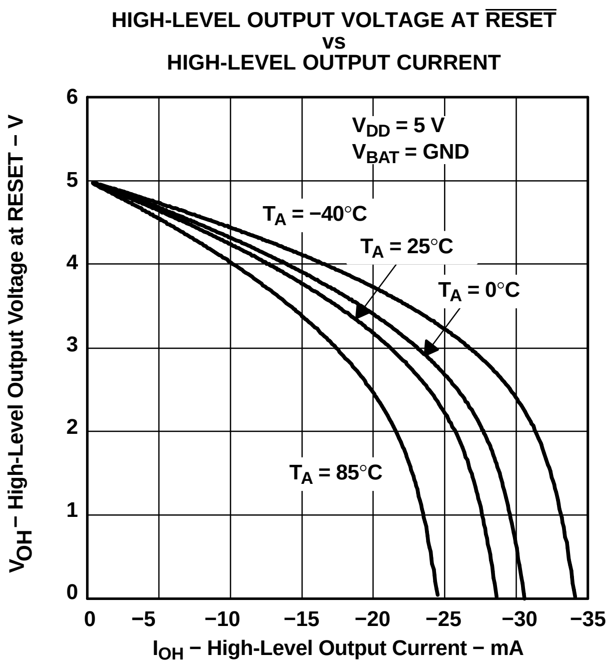


Figure 5.

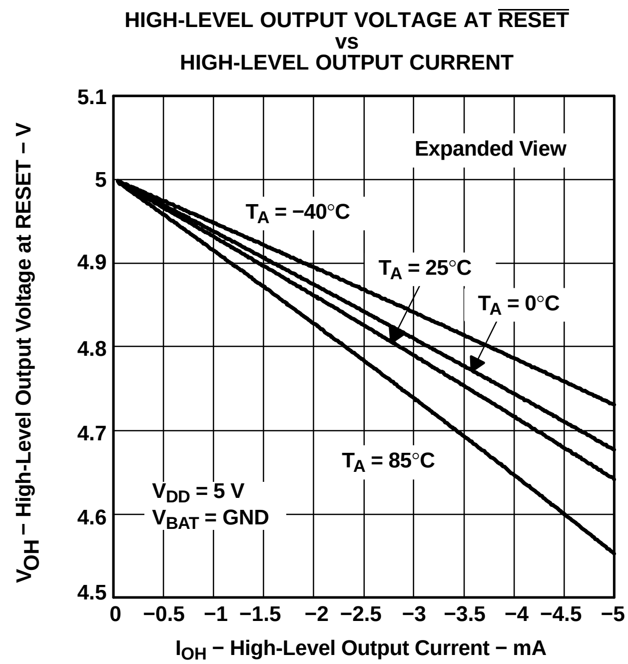


Figure 6.

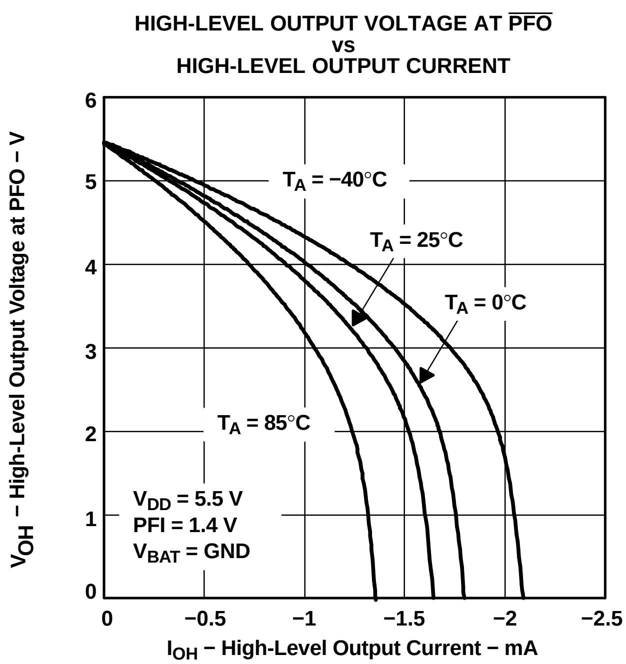


Figure 7.

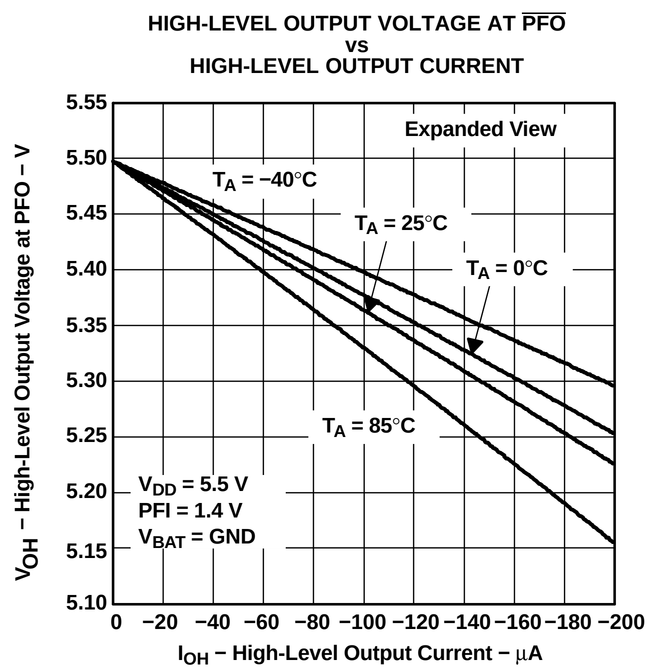


Figure 8.

TYPICAL CHARACTERISTICS (continued)

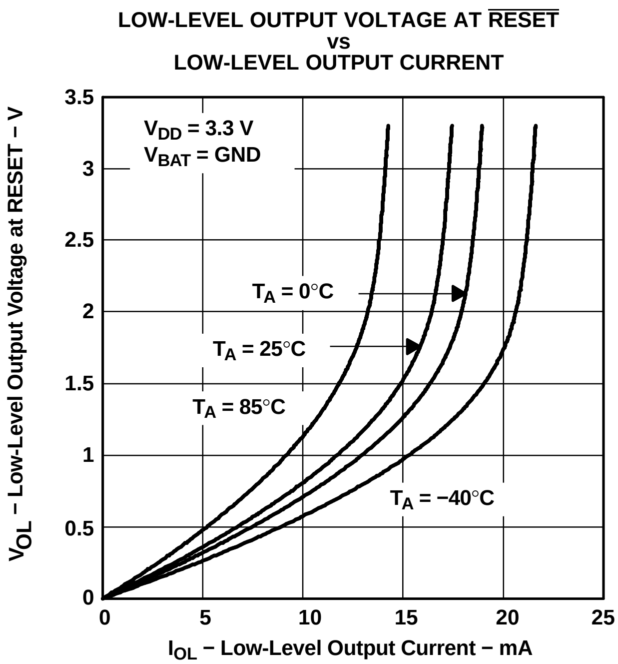


Figure 9.

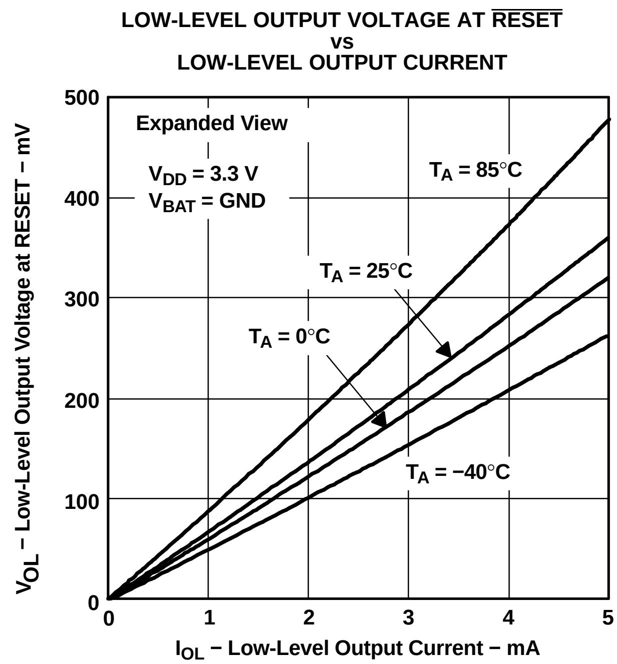


Figure 10.

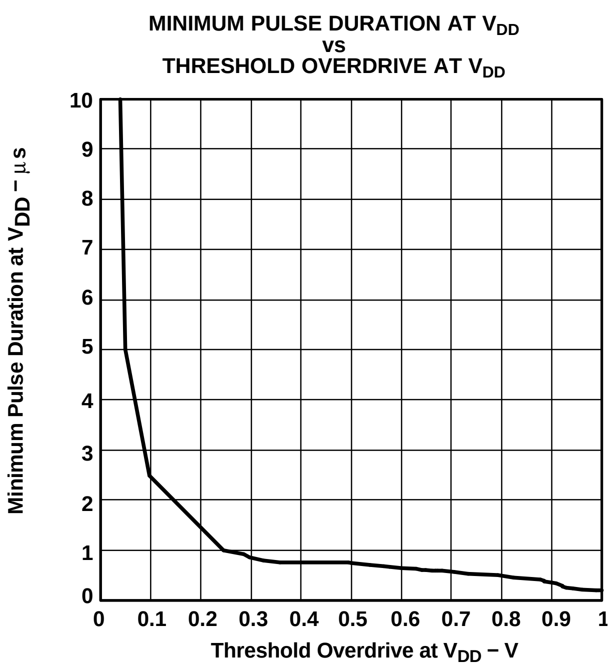


Figure 11.

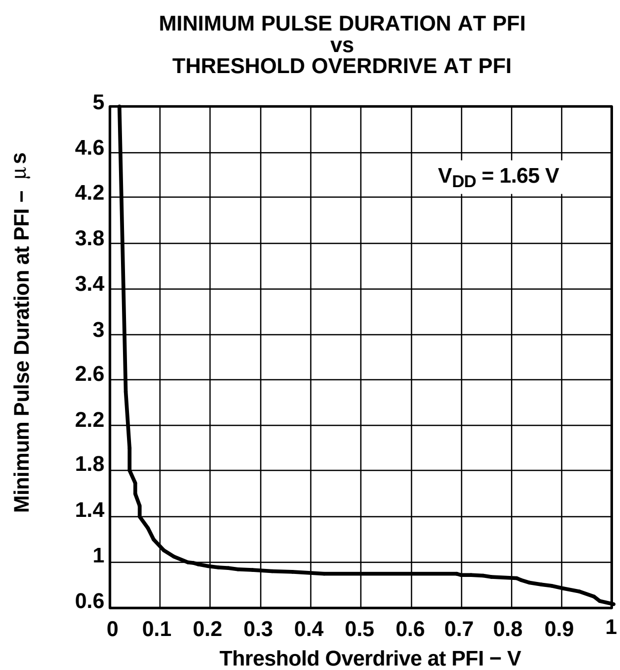


Figure 12.

DETAILED DESCRIPTION

Battery Freshness Seal (TPS3619)

The battery freshness seal of the TPS3619 family disconnects the backup-battery from internal circuitry until it is needed. This function prevents the backup-battery from being discharged unitl the final product is put to use. The following steps explain how to enable the freshness seal mode.

1. Connect V_{BAT} (V_{BAT} > V_{BAT} min)
2. Ground $\overline{PFO}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply (V_{DD} > V_{IT}) and keep connected for 5 ms < t < 35 ms

The battery freshness seal mode is automatically removed by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

Power-Fail Comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold $V_{IT(PFI)}$ of typical 1.15 V, the power-fail output ($\overline{PFO}$) goes low. If $V_{IT(PFI)}$ goes above $V_{(PFI)}$, plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to assure that the current in the PFI pin can be ignored compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, PFI should be connected to ground and $\overline{PFO}$ left unconnected.

Backup-Battery Switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE

V_{DD}> V_{BAT}	V_{DD}> V_{IT}	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

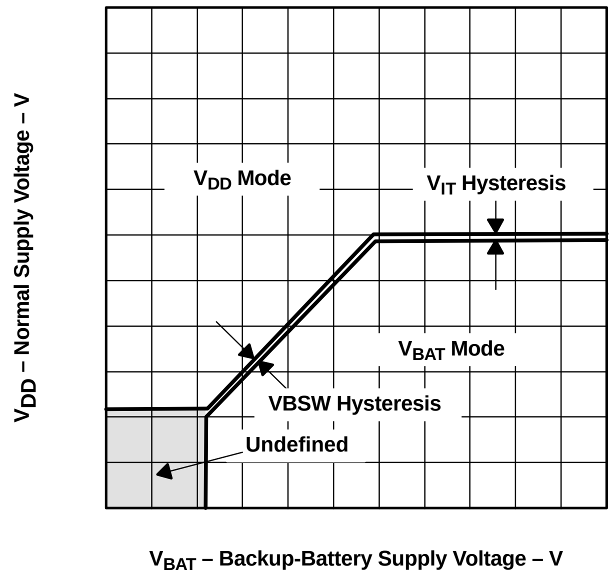


Figure 13. Normal Supply Voltage vs Backup-Battery Supply Voltage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3619-33DGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-33DGKG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-33DGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-33DGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-50DGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-50DGKG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-50DGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3619-50DGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-33DGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-33DGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-33DGKT	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-33DGKTG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-50DGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-50DGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-50DGKT	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3620-50DGKTG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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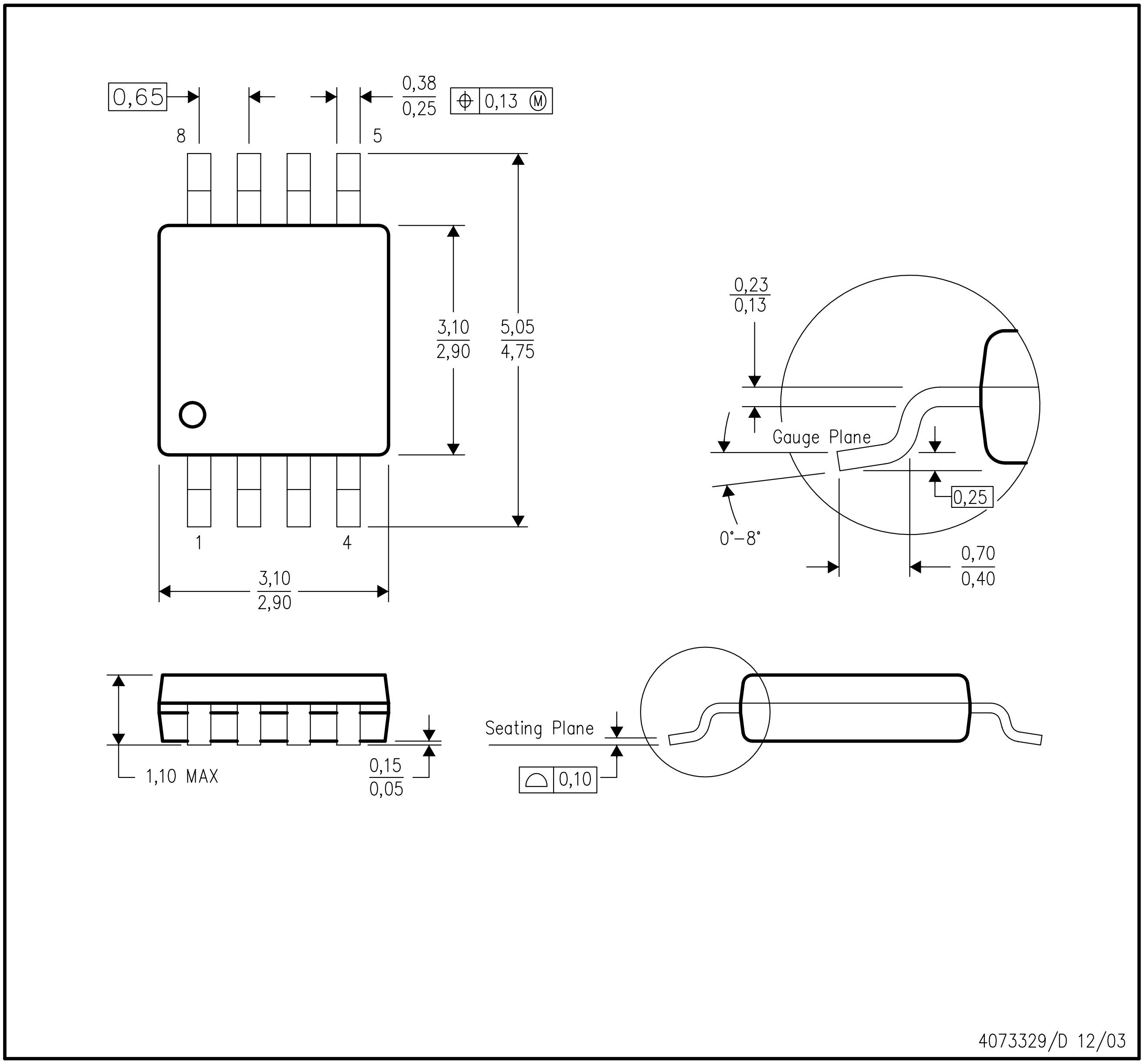
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.