



128K X 36, 256K X 18
3.3V Synchronous SRAMs
2.5V I/O, Pipelined Outputs,
Burst Counter, Single Cycle Deselect

IDT71V25761
IDT71V25781

Features

- ◆ 128K x 36, 256K x 18 memory configurations
- ◆ Supports high system speed:
Commercial:
 - 200MHz 3.1ns clock access time*Commercial and Industrial:*
 - 183MHz 3.3ns clock access time
 - 166MHz 3.5ns clock access time
- ◆ $\overline{\text{LBO}}$ input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control ($\overline{\text{GW}}$), byte write enable ($\overline{\text{BWE}}$), and byte writes ($\overline{\text{BWx}}$)
- ◆ 3.3V core power supply
- ◆ Power down controlled by ZZ input
- ◆ 2.5V I/O
- ◆ Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array

Description

The IDT71V25761/781 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V25761/781 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V25761/781 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{\text{ADV}}=\text{LOW}$), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{\text{LBO}}$ input pin.

The IDT71V25761/781 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array (FBGA).

Pin Description Summary

A0-A17	Address Inputs	Input	Synchronous
$\overline{\text{CE}}$	Chip Enable	Input	Synchronous
CS0, $\overline{\text{CS}}_1$	Chip Selects	Input	Synchronous
$\overline{\text{OE}}$	Output Enable	Input	Asynchronous
$\overline{\text{GW}}$	Global Write Enable	Input	Synchronous
$\overline{\text{BWE}}$	Byte Write Enable	Input	Synchronous
$\overline{\text{BW}}_1$, $\overline{\text{BW}}_2$, $\overline{\text{BW}}_3$, $\overline{\text{BW}}_4^{(1)}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{\text{ADV}}$	Burst Address Advance	Input	Synchronous
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{\text{ADSP}}$	Address Status (Processor)	Input	Synchronous
$\overline{\text{LBO}}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O0-I/O31, I/OP1-I/OP4	Data Input / Output	I/O	Synchronous
VDD, VDDQ	Core Power, I/O Power	Supply	N/A
VSS	Ground	Supply	N/A

5297 tbl 01

NOTE:

1. $\overline{\text{BW}}_3$ and $\overline{\text{BW}}_4$ are not applicable for the IDT71V25781.

OCTOBER 2000

Pin Definitions⁽¹⁾

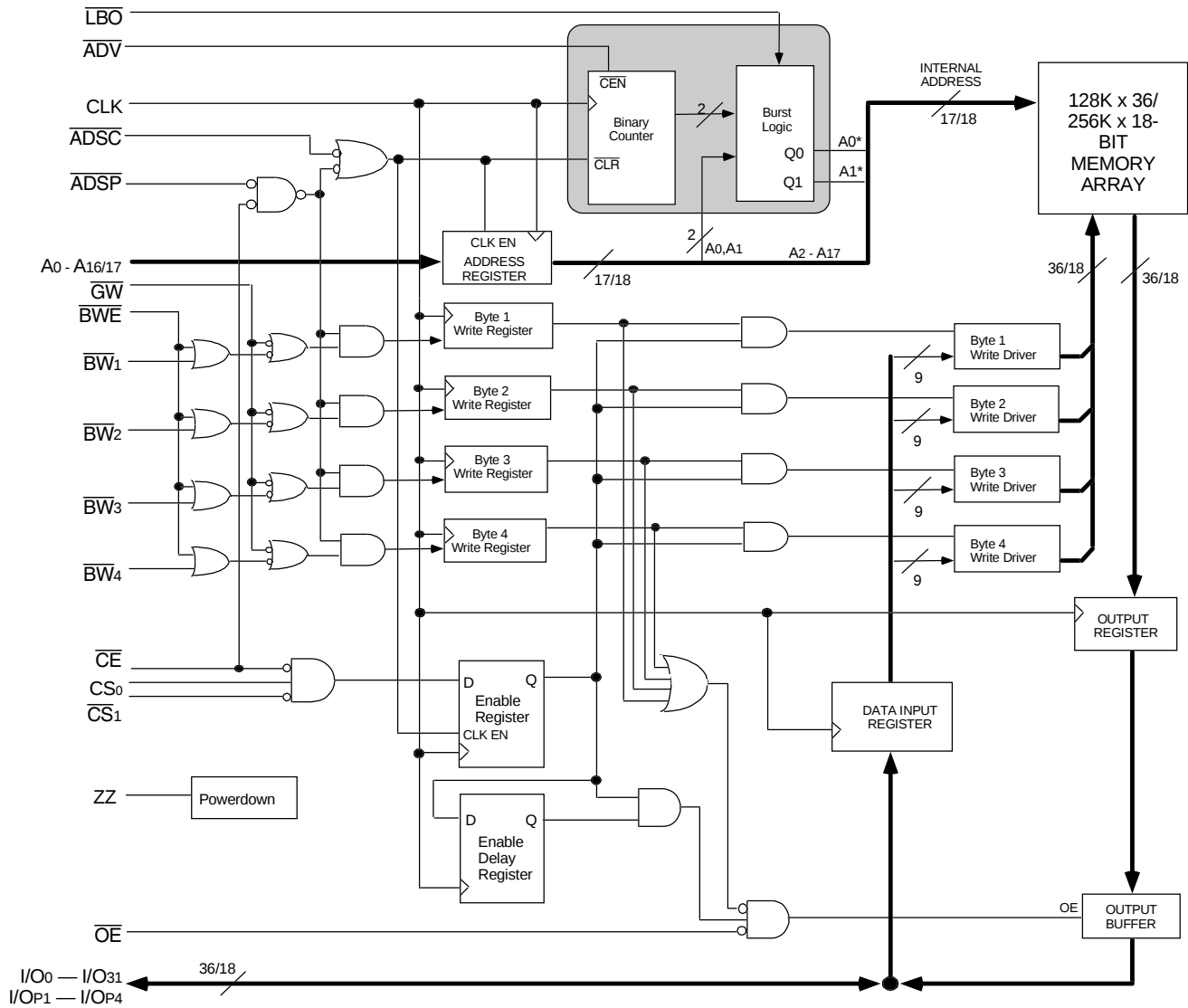
Symbol	Pin Function	I/O	Active	Description
A0-A17	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low.
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{\text{ADSP}}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$.
$\overline{\text{ADV}}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{\text{BWE}}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{\text{BW1}}\text{--}\overline{\text{BW4}}$. If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BWx}}$ inputs are passed to the next stage in the circuit. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle.
$\overline{\text{BW1}}\text{--}\overline{\text{BW4}}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{\text{BW1}}$ controls I/O0-7, I/OP1, $\overline{\text{BW2}}$ controls I/O8-15, I/OP2, etc. Any active byte write causes all outputs to be disabled.
$\overline{\text{CE}}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{\text{CE}}$ is used with CS0 and $\overline{\text{CS1}}$ to enable the IDT71V25761/781. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS0 is used with $\overline{\text{CE}}$ and $\overline{\text{CS1}}$ to enable the chip.
$\overline{\text{CS1}}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{\text{CS1}}$ is used with $\overline{\text{CE}}$ and CS0 to enable the chip.
$\overline{\text{GW}}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supersedes individual byte write enables.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{\text{LBO}}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{\text{LBO}}$ is HIGH, the interleaved burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear burst sequence is selected. $\overline{\text{LBO}}$ is a static input and must not change state while the device is operating.
$\overline{\text{OE}}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state.
VDD	Power Supply	N/A	N/A	3.3V core power supply.
VDDQ	Power Supply	N/A	N/A	2.5V I/O Supply.
VSS	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V25761/781 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

NOTE:

5297 tbl 02

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ^(3,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD}	V
V _{TERM} ^(4,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD} +0.5	V
V _{TERM} ^(5,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DDQ} +0.5	V
T _A ⁽⁷⁾	Commercial Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	2.0	W
I _{OUT}	DC Output Current	50	mA

5297 tbl 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- V_{DDQ} terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- T_A is the "instant on" case temperature.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature ⁽¹⁾	V _{SS}	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	2.5V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	2.5V±5%

NOTES:

5297 tbl 04

- T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V _{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage - Inputs	1.7	—	V _{DD} +0.3	V
V _{IH}	Input High Voltage - I/O	1.7	—	V _{DDQ} +0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	—	0.7	V

NOTES:

5297 tbl 05

- V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than t_{CYC/2}, once per cycle.
- V_{IL} (min) = -1.0V for pulse width less than t_{CYC/2}, once per cycle.

100 pin TQFP Capacitance

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	5	pF
C _{IO}	I/O Capacitance	V _{OUT} = 3dV	7	pF

5297 tbl 07

119 BGA Capacitance

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	7	pF
C _{IO}	I/O Capacitance	V _{OUT} = 3dV	7	pF

5297 tbl 07a

165 fBGA Capacitance

(T_A = +25°C, f = 1.0MHz)

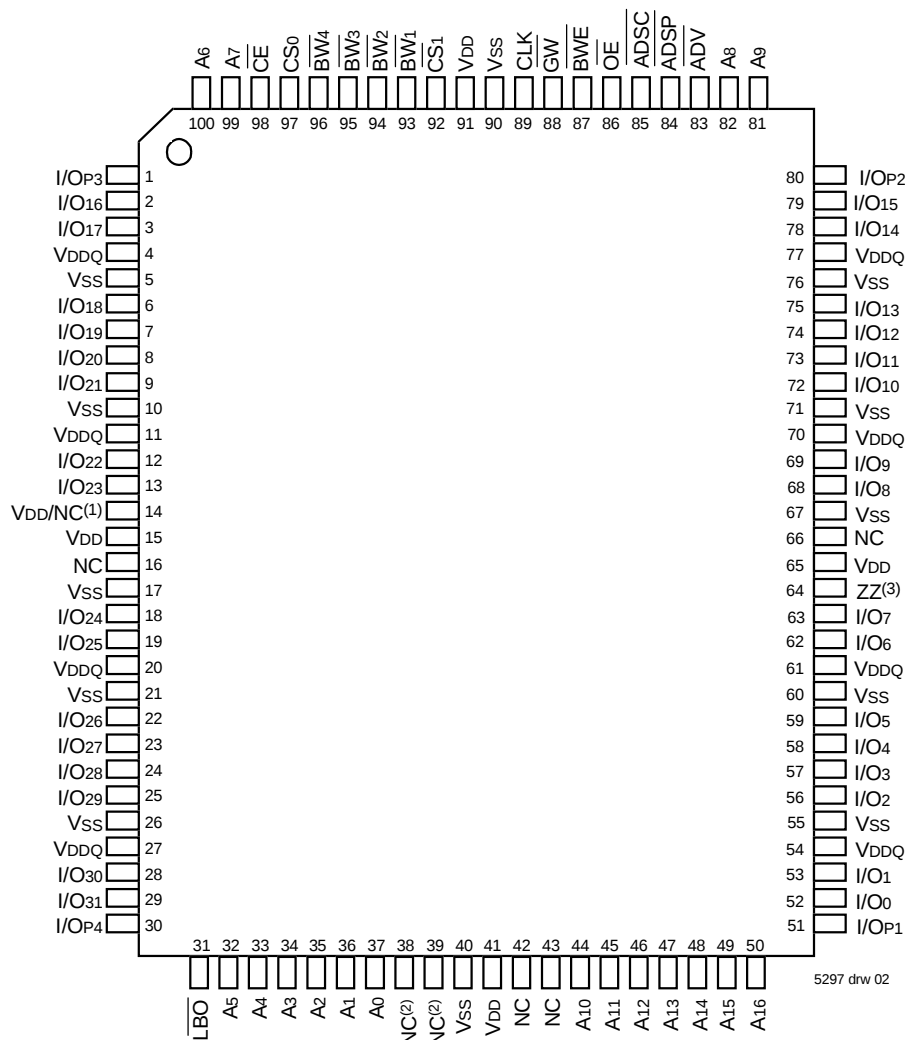
Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	TBD	pF
C _{IO}	I/O Capacitance	V _{OUT} = 3dV	TBD	pF

5297 tbl 07b

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration – 128K x 36



100 TQFP Top View

NOTES:

- Pin 14 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
- Pins 38 and 39 can be either NC or connected to VSS.
- Pin 64 can be left unconnected and the device will always remain in active mode.

Pinout diagram for the AD9250 100-pin QFN package. The diagram shows the top, bottom, left, and right pin connections. Pin 1 is at the top-left corner. The top edge contains pins 100 (A6) to 81 (A9). The right edge contains pins 80 (A10) to 51 (NC). The bottom edge contains pins 50 (A17) to 31 (LBO). The left edge contains pins 30 (NC) to 1 (NC). A circular notch is located on the top-left side of the package.

Pin	Signal	Pin	Signal
1	NC	51	NC
2	NC	52	NC
3	NC	53	NC
4	VDDQ	54	VDDQ
5	VSS	55	VSS
6	NC	56	NC
7	NC	57	NC
8	I/O8	58	I/O0
9	I/O9	59	I/O1
10	VSS	60	VSS
11	VDDQ	61	VDDQ
12	I/O10	62	I/O2
13	I/O11	63	I/O3
14	VDD/NC ⁽¹⁾	64	VDD
15	VDD	65	VDD
16	NC	66	NC
17	VSS	67	VSS
18	I/O12	68	I/O4
19	I/O13	69	I/O5
20	VDDQ	70	VDDQ
21	VSS	71	VSS
22	I/O14	72	I/O6
23	I/O15	73	I/O7
24	I/OP2	74	I/OP1
25	NC	75	NC
26	VSS	76	VSS
27	VDDQ	77	VDDQ
28	NC	78	NC
29	NC	79	NC
30	NC	80	A10
31	LBO	81	A9
32	A5	82	A8
33	A4	83	ADV
34	A3	84	ADSP
35	A2	85	ADSC
36	A1	86	OE
37	A0	87	BWE
38	NC ⁽²⁾	88	GW
39	NC ⁽²⁾	89	CLK
40	VSS	90	VSS
41	VDD	91	VDD
42	NC	92	CS1
43	NC	93	BW1
44	A11	94	BW2
45	A12	95	NC
46	A13	96	NC
47	A14	97	CS0
48	A15	98	CE
49	A16	99	A7
50	A17	100	A6

5297 drw 03

100 TQFP Top View

1. Pin 14 can either be directly connected to V_{DD} , or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pins 38 and 39 can be either NC or connected to V_{SS} .
3. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 128K x 36, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	ADSP	A8	A16	VDDQ
B	NC	CS ₀	A3	ADSC	A9	CS ₁	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	CE	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	OE	VSS	I/O12	VDDQ
G	I/O20	I/O21	BW ₃	ADV	BW ₂	I/O11	I/O10
H	I/O22	I/O23	VSS	GW	VSS	I/O9	I/O8
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	BW ₄	NC ⁽²⁾	BW ₁	I/O4	I/O5
M	VDDQ	I/O28	VSS	BWE	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/O0	I/OP1
R	NC	A5	LBO	VDD	VDD / NC ⁽¹⁾	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ ⁽³⁾
U	VDDQ	DNU ⁽⁴⁾	DNU ⁽⁴⁾	DNU ^(2,4)	DNU ⁽⁴⁾	DNU ⁽⁴⁾	VDDQ

5297 drw 04

Top View

Pin Configuration – 256K x 18, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	ADSP	A8	A16	VDDQ
B	NC	CS ₀	A3	ADSC	A9	CS ₁	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/O7	NC
E	NC	I/O9	VSS	CE	VSS	NC	I/O6
F	VDDQ	NC	VSS	OE	VSS	I/O5	VDDQ
G	NC	I/O10	BW ₂	ADV	VSS	NC	I/O4
H	I/O11	NC	VSS	GW	VSS	I/O3	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O2
L	I/O13	NC	VSS	NC ⁽²⁾	BW ₁	I/O1	NC
M	VDDQ	I/O14	VSS	BWE	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O0	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/OP1
R	NC	A5	LBO	VDD	VDD / NC ⁽¹⁾	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ ⁽³⁾
U	VDDQ	DNU ⁽⁴⁾	DNU ⁽⁴⁾	DNU ^(2,4)	DNU ⁽⁴⁾	DNU ⁽⁴⁾	VDDQ

5297 drw 05

Top View

NOTES:

1. R5 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. L4 and U4 can be either NC or connected to VSS.
3. T7 can be left unconnected and the device will always remain in active mode.
4. DNU = Do not use; Pins U2, U3, U4, U5 and U6 are reserved for respective JTAG Pins: TMS, TDI, TCK, TDO and $\overline{\text{TRST}}$. Within the current version, these pins are left unconnected.

Pin Configuration – 128K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽⁴⁾	A7	$\overline{CE}_1$	$\overline{BW}_3$	$\overline{BW}_2$	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	NC
B	NC	A6	CS0	$\overline{BW}_4$	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC ⁽⁴⁾
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VDD ⁽¹⁾	NC ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ ⁽³⁾
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	DNU ⁽⁵⁾	NC ⁽⁴⁾	NC ⁽²⁾	VSS	VDDQ	NC	I/OP1
P	NC	NC ⁽⁴⁾	A5	A2	DNU ⁽⁵⁾	A1	DNU ⁽⁵⁾	A10	A13	A14	NC ⁽⁴⁾
R	$\overline{LBO}$	NC ⁽⁴⁾	A4	A3	DNU ⁽⁵⁾	A0	DNU ⁽⁵⁾	A11	A12	A15	A16

5297 tbl 17

Pin Configuration – 256K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽⁴⁾	A7	$\overline{CE}_1$	$\overline{BW}_2$	NC	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	A10
B	NC	A6	CS0	NC	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC ⁽⁴⁾
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VDD ⁽¹⁾	NC ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ ⁽³⁾
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	DNU ⁽⁵⁾	NC ⁽⁴⁾	NC ⁽²⁾	VSS	VDDQ	NC	NC
P	NC	NC ⁽⁴⁾	A5	A2	DNU ⁽⁵⁾	A1	DNU ⁽⁵⁾	A11	A14	A15	NC ⁽⁴⁾
R	$\overline{LBO}$	NC ⁽⁴⁾	A4	A3	DNU ⁽⁵⁾	A0	DNU ⁽⁵⁾	A12	A13	A16	A17

5297 tbl 17a

NOTES:

- H1 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
- H2 and N7 can be either NC or connected to VSS.
- H11 can be left unconnected and the device will always remain in active mode.
- Pins P11, N6, B11, A1, R2 and P2 are reserved for 9M, 18M, 36M, 72M, 144M and 288M respectively.
- DNU = Do not use; Pins P5, P7, R5, R7 and N5 are reserved for respective JTAG Pins: TDI, TDO, TMS, TCK and $\overline{TRST}$ on future revisions. Within this current version, these pins are not connected.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{IL} $	Input Leakage Current	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	5	μA
$ I_{LZZ} $	ZZ and $\overline{LBO}$ Input Leakage Current ⁽¹⁾	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	30	μA
$ I_{LO} $	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{DDQ}$, Device Deselected	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +6mA$, $V_{DD} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -6mA$, $V_{DD} = \text{Min.}$	2.0	—	V

5297 tbl 08

NOTE:

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

Symbol	Parameter	Test Conditions	200MHz	183MHz		166MHz		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, $f = f_{MAX}^{(2)}$	360	340	350	320	330	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, $f = 0^{(2,3)}$	30	30	35	30	35	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, $f = f_{MAX}^{(2,3)}$	130	120	130	110	120	mA
I_{ZZ}	Full Sleep Mode Supply Current	$ZZ \geq V_{HD}$, $V_{DD} = \text{Max.}$	30	30	35	30	35	mA

5297 tbl 09

NOTES:

1. All values are maximum guaranteed values.
2. At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.
3. For I/Os $V_{HD} = V_{DDQ} - 0.2V$, $V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V$, $V_{LD} = 0.2V$.

AC Test Conditions ($V_{DDQ} = 2.5V$)

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	$(V_{DDQ}/2)$
Output Timing Reference Levels	$(V_{DDQ}/2)$
AC Test Load	See Figure 1

5297 tbl 10

AC Test Load

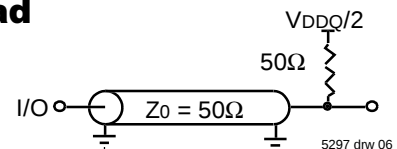
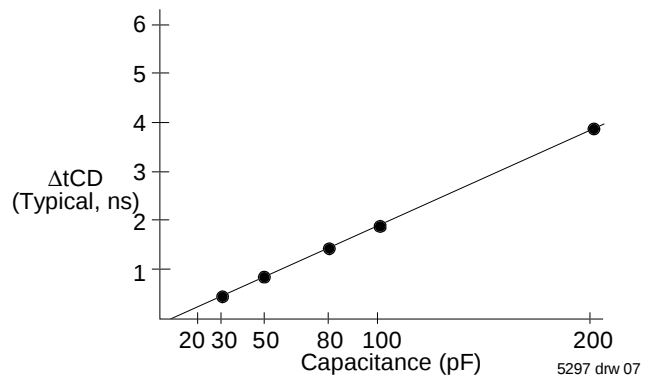


Figure 1. AC Test Load



5297 drw 07

Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table^(1,3)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_x$	$\overline{OE}$ (2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	-	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	-	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	-	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	-	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	-	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	-	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	-	DIN

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ = low for this table.

5297 tbl 11

Synchronous Write Function Truth Table^(1,2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 ⁽³⁾	H	L	L	H	H	H
Write Byte 2 ⁽³⁾	H	L	H	L	H	H
Write Byte 3 ⁽³⁾	H	L	H	H	L	H
Write Byte 4 ⁽³⁾	H	L	H	H	H	L

5297 tbl 12

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. $\overline{BW}_3$ and $\overline{BW}_4$ are not applicable for the IDT71V2578.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table⁽¹⁾

Operation ⁽²⁾	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5297 tbl 13

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LB0}=V_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

5297 tbl 14

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LB0}=V_{SS}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

5297 tbl 15

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics

(V_{DD} = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	200MHz ⁽⁵⁾		183MHz		166MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	5	—	5.5	—	6	—	ns
t _{CH} ⁽¹⁾	Clock High Pulse Width	2	—	2.2	—	2.4	—	ns
t _{CL} ⁽¹⁾	Clock Low Pulse Width	2	—	2.2	—	2.4	—	ns
Output Parameters								
t _{CD}	Clock High to Valid Data	—	3.1	—	3.3	—	3.5	ns
t _{DC}	Clock High to Data Change	1.0	—	1.0	—	1.0	—	ns
t _{CLZ} ⁽²⁾	Clock High to Output Active	0	—	0	—	0	—	ns
t _{CHZ} ⁽²⁾	Clock High to Data High-Z	1.5	3.1	1.5	3.3	1.5	3.5	ns
t _{OE}	Output Enable Access Time	—	3.1	—	3.3	—	3.5	ns
t _{OLZ} ⁽²⁾	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t _{OHZ} ⁽²⁾	Output Enable High to Output High-Z	—	3.1	—	3.3	—	3.5	ns
Set Up Times								
t _{SA}	Address Setup Time	1.2	—	1.5	—	1.5	—	ns
t _{SS}	Address Status Setup Time	1.2	—	1.5	—	1.5	—	ns
t _{SD}	Data In Setup Time	1.2	—	1.5	—	1.5	—	ns
t _{SW}	Write Setup Time	1.2	—	1.5	—	1.5	—	ns
t _{SAV}	Address Advance Setup Time	1.2	—	1.5	—	1.5	—	ns
t _{SC}	Chip Enable/Select Setup Time	1.2	—	1.5	—	1.5	—	ns
Hold Times								
t _{HA}	Address Hold Time	0.4	—	0.5	—	0.5	—	ns
t _{HS}	Address Status Hold Time	0.4	—	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.4	—	0.5	—	0.5	—	ns
t _{HW}	Write Hold Time	0.4	—	0.5	—	0.5	—	ns
t _{HAV}	Address Advance Hold Time	0.4	—	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.4	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t _{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t _{ZZR} ⁽³⁾	ZZ Recovery Time	100	—	100	—	100	—	ns
t _{CFG} ⁽⁴⁾	Configuration Set-up Time	20	—	22	—	24	—	ns

4876 tbl 16

NOTES:

1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{\text{LB0}}$ input. $\overline{\text{LB0}}$ is a static input and must not change during normal operation.
5. Commercial temperature range only.

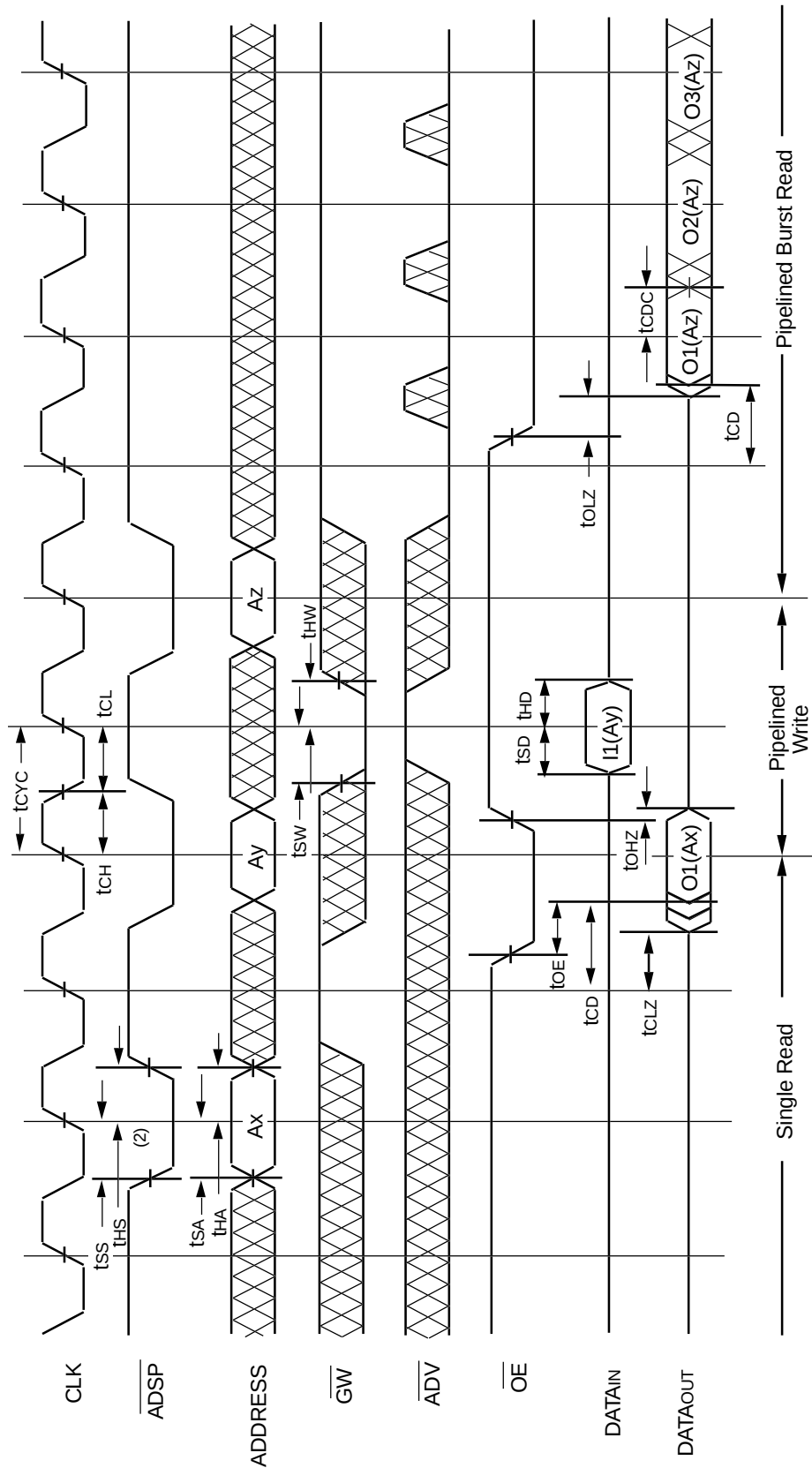
Timing Waveform of Pipeline Read Cycle^(1,2)



NOTES:

1. $O1_Ax$ represents the first output from the external address Ax . $O1_Ay$ represents the first output from the external address Ay . $O2_Ay$ represents the next output data in the burst sequence of the base address Ay , etc. where $A0$ and $A1$ are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is $\overline{LOW}$ and $\overline{LBO}$ is Don't Care for this cycle.
3. $CS0$ timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are $\overline{LOW}$ on this waveform, $CS0$ is $HIGH$.

Timing Waveform of Combined Pipelined Read and Write Cycles^(1,2,3)

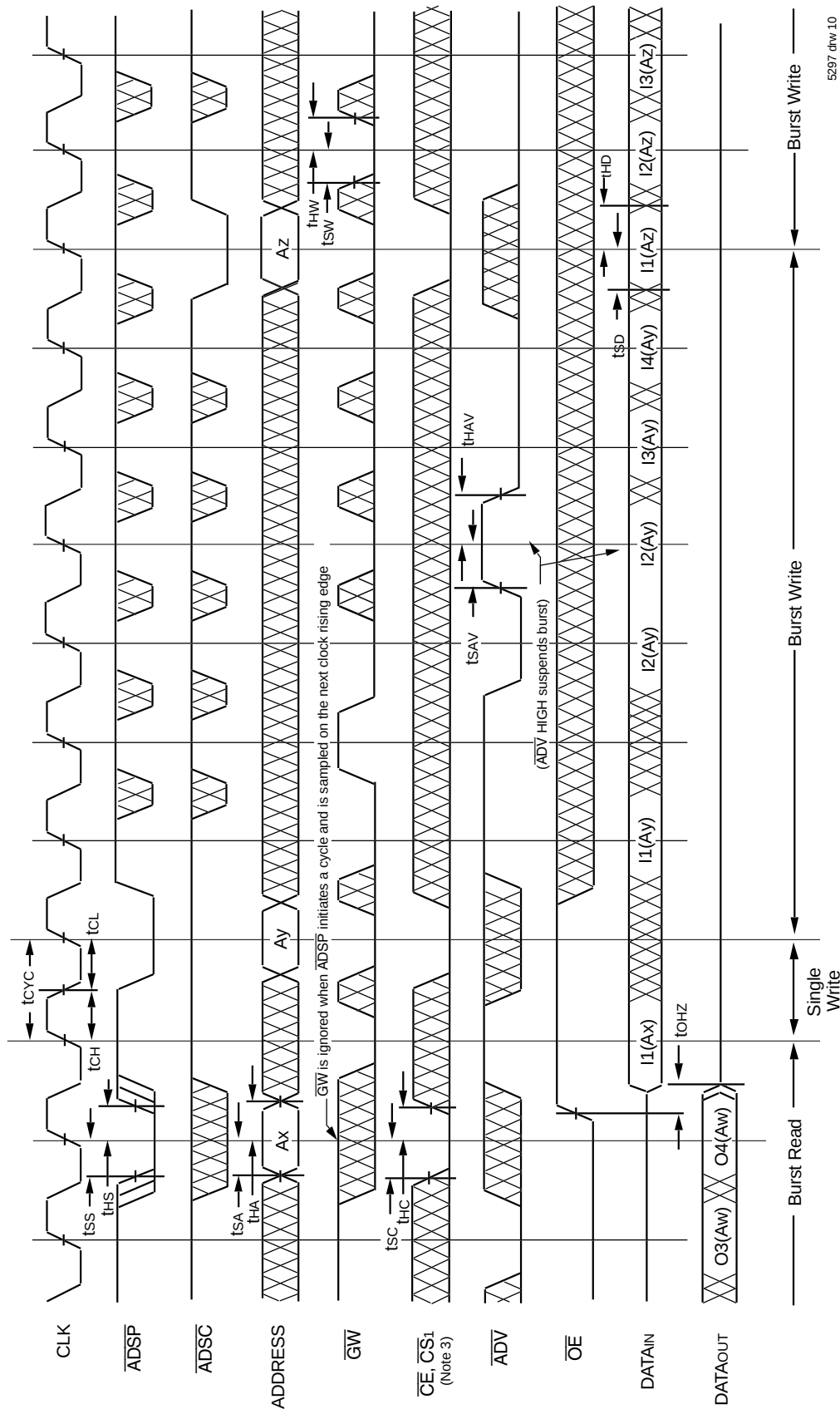


5297 drw 09

NOTES:

1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS1}$ are LOW, $\overline{CS0}$ is HIGH.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. O1 (Ay) represents the first output from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.

Timing Waveform of Write Cycle No. 1 — $\overline{GW}$ Controlled^(1,2,3)

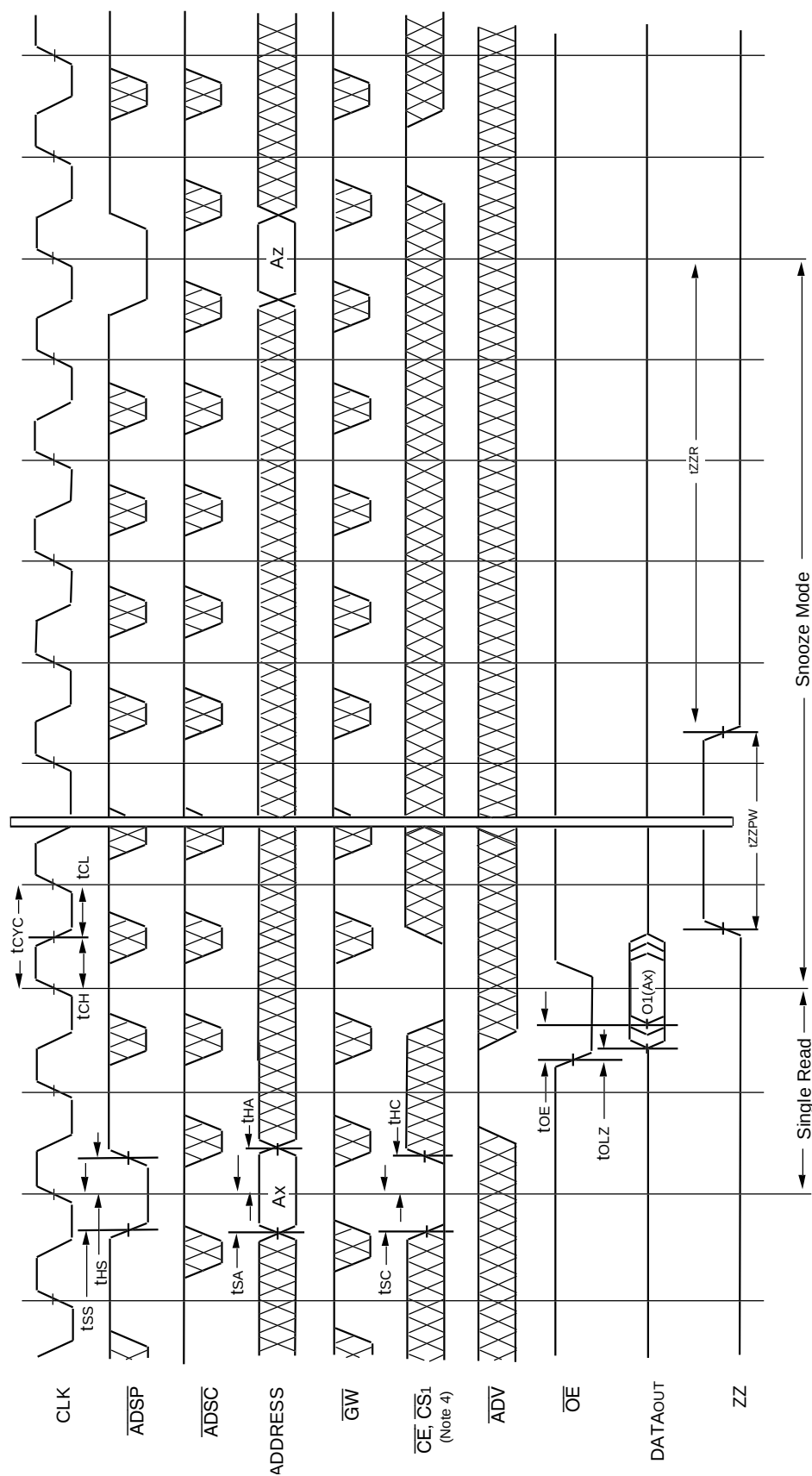


NOTES:

1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. $O4(Aw)$ represents the final output data in the burst sequence of the base address Aw . $I1(Ax)$ represents the first input from the external address Ay . $I2(Ay)$ represents the next input data in the burst sequence of the base address Ay , etc. where $A0$ and $A1$ are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input $I2(Ay)$ this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

5297 dw 10

Timing Waveform of Sleep (ZZ) and Power-Down Modes^(1,2,3)

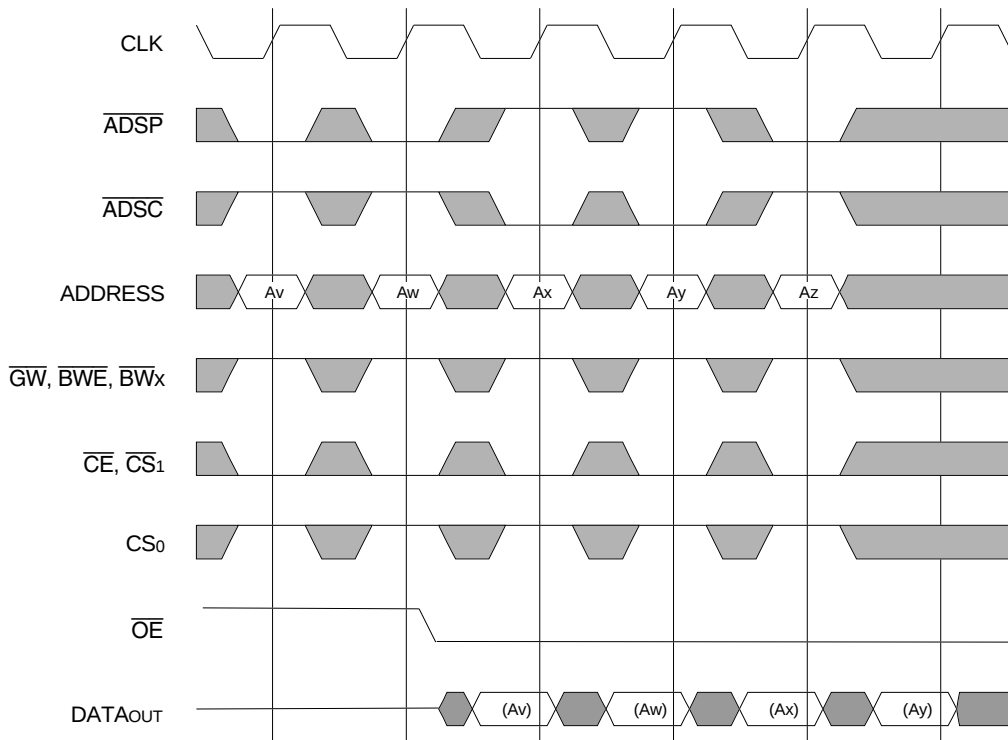


5297 drw 12

NOTES:

1. Device must power up in deselected Mode.
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform

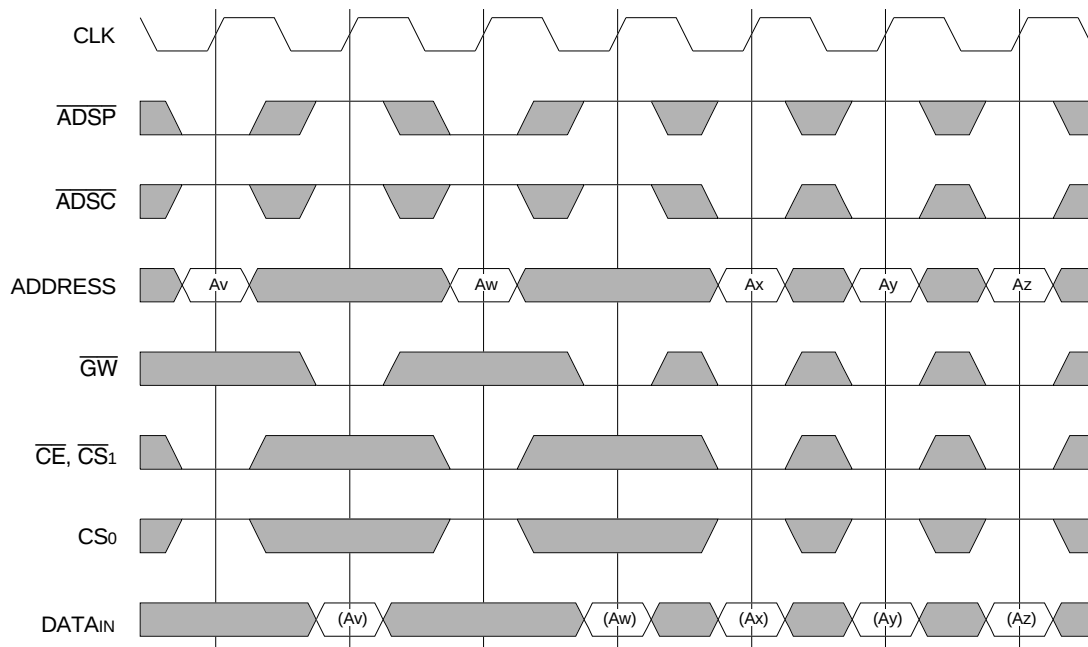


NOTES:

1. ZZ input is LOW, $\overline{\text{ADV}}$ is HIGH and $\overline{\text{LB0}}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ function identically and are therefore interchangeable.

5297 drw 14

Non-Burst Write Cycle Timing Waveform

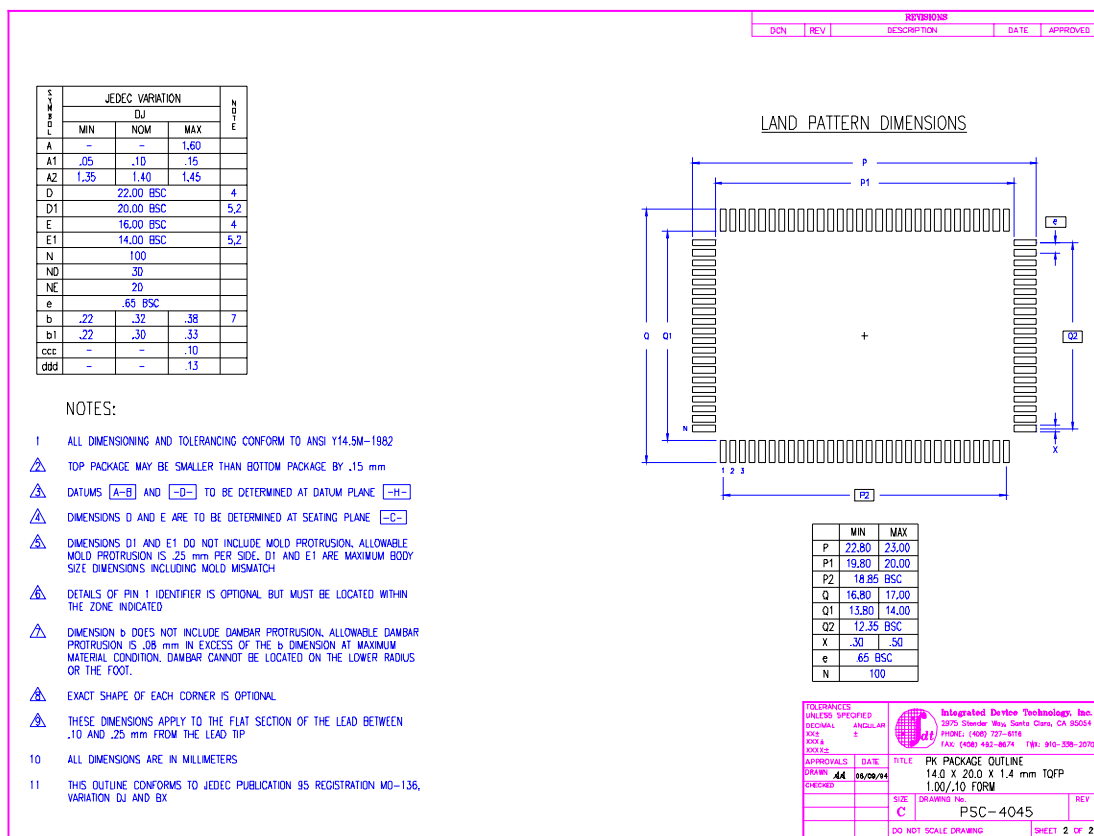
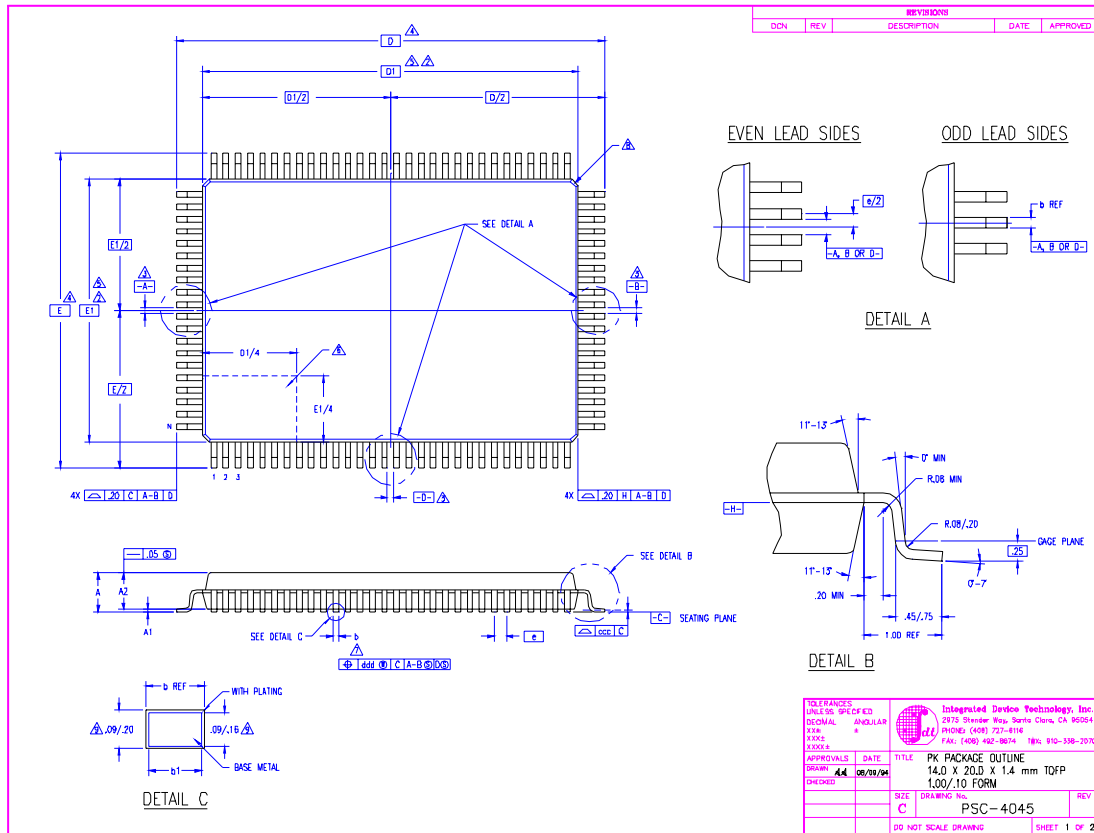


NOTES:

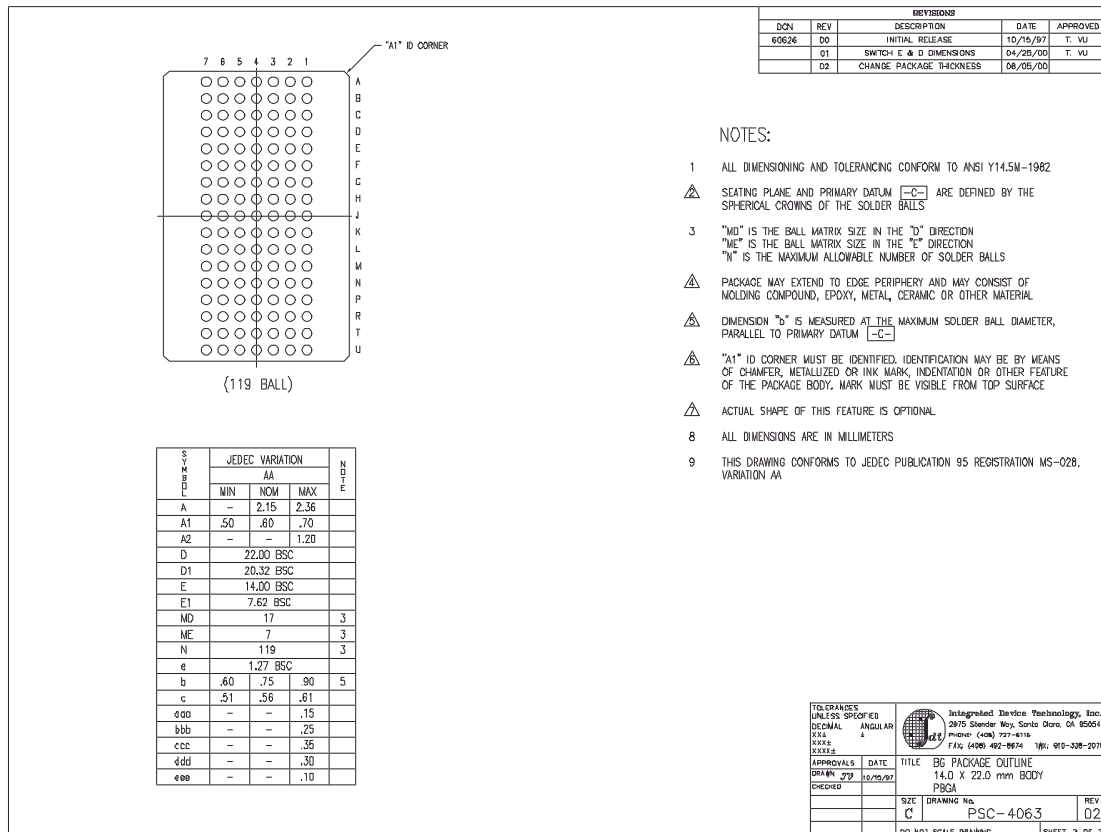
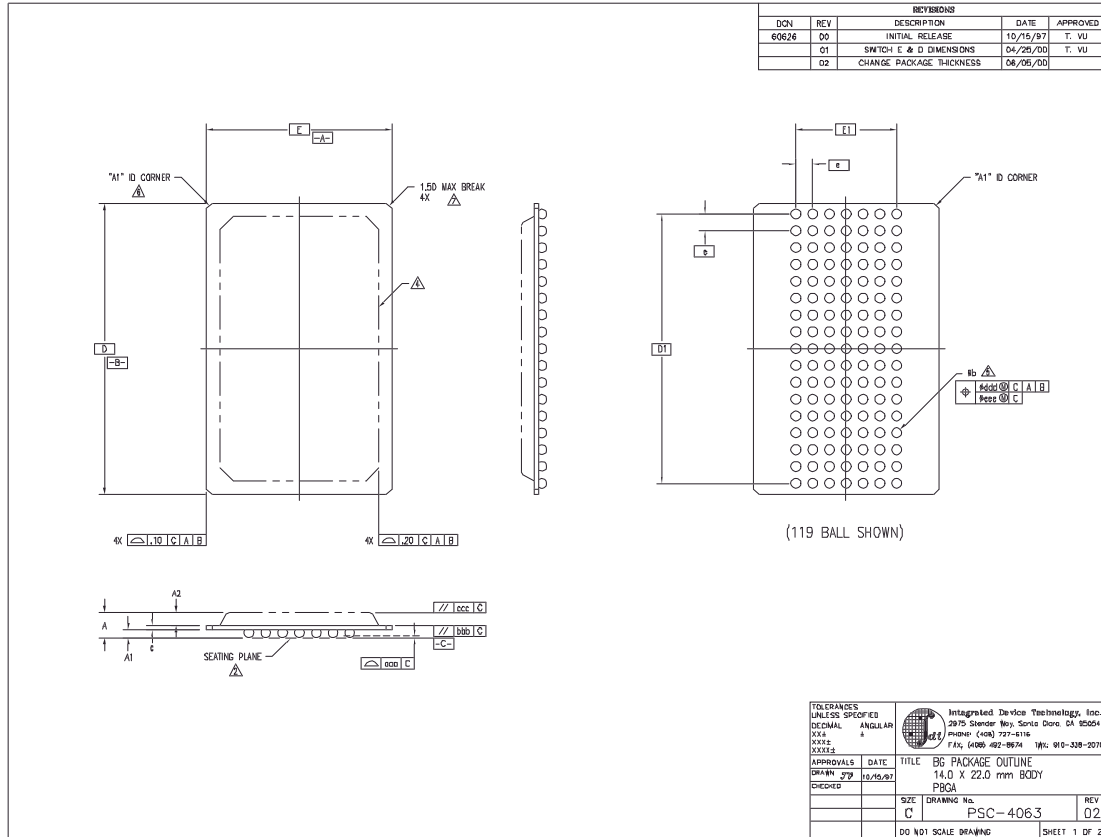
1. ZZ input is LOW, $\overline{\text{ADV}}$ and $\overline{\text{OE}}$ are HIGH, and $\overline{\text{LB0}}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only $\overline{\text{GW}}$ writes are shown, the functionality of $\overline{\text{BWE}}$ and $\overline{\text{BWx}}$ together is the same as $\overline{\text{GW}}$.
4. For write cycles, $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ have different limitations.

5297 drw 15

100-Pin Plastic Thin Quad Flatpack(TQFP) Package Diagram Outline



119 Ball Grid Array (BGA) Package Diagram Outline



REVIEWS

DGN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	

The figure shows three views of the BQ package outline:

- Top View:** A square grid representing the solder ball array. Dimensions include overall width and length, and specific features like the "A1" ID corner.
- Side View:** Shows the profile of the package body and the seating plane of the balls.
- Ball Matrix:** A detailed view of the 16x16 ball grid, labeled with letters A-R and numbers 1-16.

TOLERANCES UNLESS SPECIFIED

DECIMAL	ANGULAR
.XX	.XX°

INTEGRATED DEVICE TECHNOLOGY, INC.
 2975 Slender Way, Santa Clara, CA 95054
 PHONE: (408) 727-6116 FAX: (408) 492-8674 TEL: 910-338-2075

APPROVALS DATE
DRAWN BY 05/01/00
CHECKED

TITLE BQ PACKAGE OUTLINE
SIZE 13.0 X 15.0 mm BODY
FPBGA
PSC-4086

DO NOT SCALE DRAWING SHEET 1 OF 2

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- "B" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
- "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
- "N" REPRESENTS THE BALLCOUNT NUMBER
- DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM [C]
- SEATING PLANE AND PRIMARY DATUM [C] ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
- "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
- IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN MILLIMETERS

(165 BALL)

SOLDER BALL	JEDEC VARIATION	NOM	MAX	MIN
A	NOT YET REGISTERED	-	-	1.20
A1		.50	.35	.40
A2		.78	.85	.92
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b		.35	.45	.50
CENTER BALL MATRIX	N/A			

REVIEWS

DGN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	

This is a duplicate of the first figure, showing the same technical drawing of the BQ package outline with dimensions, tolerances, and company information.

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- "B" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
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(165 BALL)

SOLDER BALL	JEDEC VARIATION	NOM	MAX	MIN
A	NOT YET REGISTERED	-	-	1.20
A1		.50	.35	.40
A2		.78	.85	.92
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b		.35	.45	.50
CENTER BALL MATRIX	N/A			

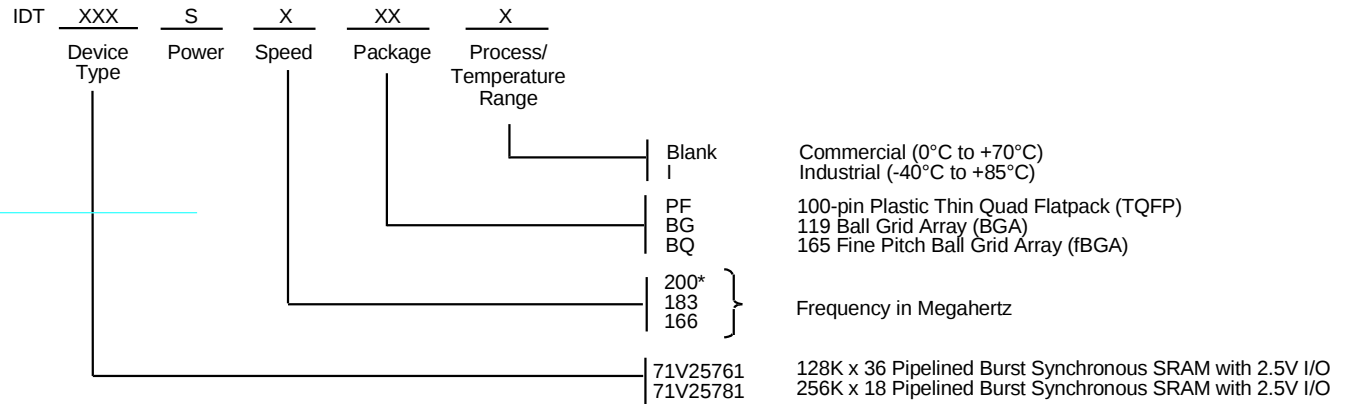
INTEGRATED DEVICE TECHNOLOGY, INC.
 2975 Slender Way, Santa Clara, CA 95054
 PHONE: (408) 727-6116 FAX: (408) 492-8674 TEL: 910-338-2075

APPROVALS DATE
DRAWN BY 05/01/00
CHECKED

TITLE BQ PACKAGE OUTLINE
SIZE 13.0 X 15.0 mm BODY
FPBGA
PSC-4086

DO NOT SCALE DRAWING SHEET 2 OF 2

Ordering Information



*Commercial temperature range only.

Datasheet Document History

12/31/99		Created new datasheet from 71V2576 and 71V2578 datasheets
	Pg. 1, 4, 8, 19	Added Industrial Temperature range offerings
04/04/00	Pg. 18	Added 100pin TQFP Package Diagram Outline
	Pg. 4	Add capacitance table for BGA package; Add Industrial temperature to table; Insert note to Absolute Max Ratings and Recommended Operating Temperature tables
06/01/00		Add new package offering, 13 x 15mm 165 fBGA
	Pg. 20	Correct BG119 Package Diagram Outline
07/15/00	Pg. 7	Add note reference to BG119 pinout
	Pg. 8	Add DNU note to BQ165 pinout
	Pg. 20	Update BG119 Package Diagram Outline Dimensions
10/25/00		Remove Preliminary from datasheet
	Pg. 8	Add reference note to pin N5 in BQ165 pinout, reserved for JTAG, $\overline{\text{TRST}}$



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