

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

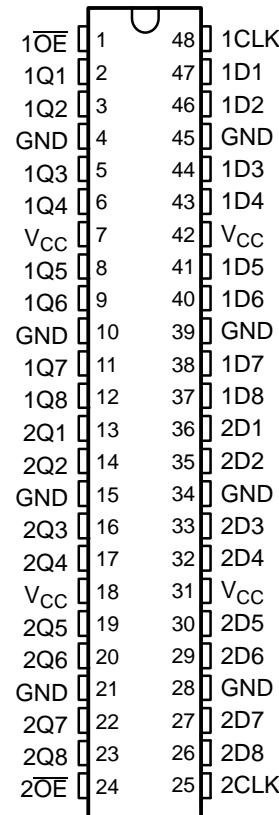
DESCRIPTION/ORDERING INFORMATION

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Tape and reel	SN74LVC16374AGRDR	LD374A
	FBGA – ZRD (Pb-free)		SN74LVC16374AZRDR	
	SSOP – DL	Tube	SN74LVC16374ADL	LVC16374A
		Tape and reel	SN74LVC16374ADLR	
	TSSOP – DGG	Tape and reel	SN74LVC16374ADGGR	LVC16374A
			74LVC16374ADGGRG4	
	TVSOP – DGV	Tape and reel	SN74LVC16374ADGVR	LD374A
			74LVC16374ADGVRE4	
	VFBGA – GQL	Tape and reel	SN74LVC16374AGQLR	LD374A
	VFBGA – ZQL (Pb-free)		SN74LVC16374AZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Widebus is a trademark of Texas Instruments.

SN74LVC16374A
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

SCAS728A—OCTOBER 2003—REVISED OCTOBER 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

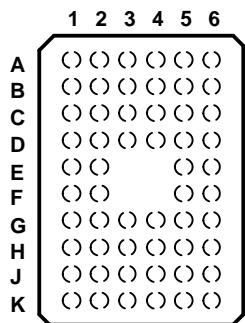
\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**GQL OR ZQL PACKAGE
(TOP VIEW)**

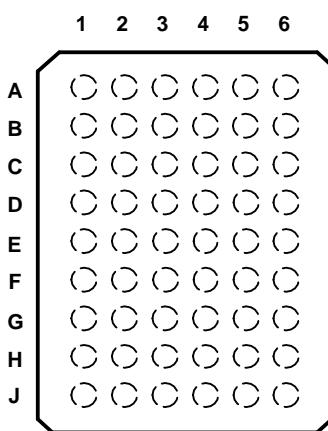


**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	$1\overline{OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	$2\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

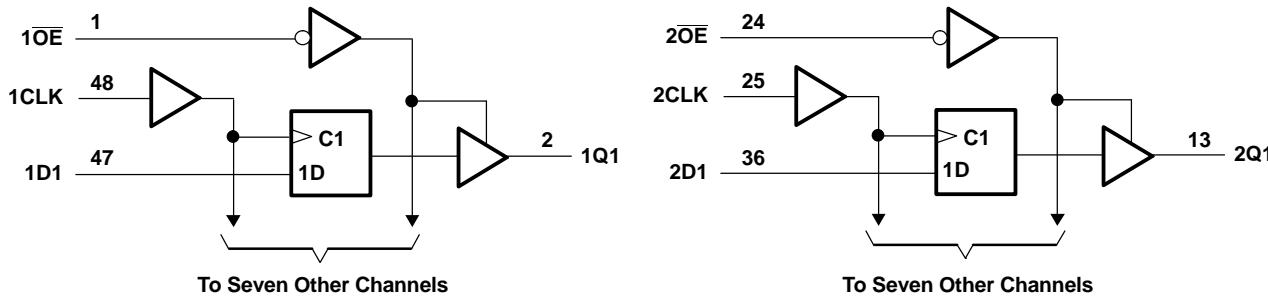
	1	2	3	4	5	6
A	1Q1	NC	$1\overline{OE}$	1CLK	NC	1D1
B	1Q3	1Q2	NC	NC	1D2	1D3
C	1Q5	1Q4	V_{CC}	V_{CC}	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V_{CC}	V_{CC}	2D4	2D5
H	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	$2\overline{OE}$	2CLK	NC	2D8

(1) NC – No internal connection

**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through each V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC16374A
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8		
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$		-4	mA
		$V_{CC} = 2.3\text{ V}$		-8	
		$V_{CC} = 2.7\text{ V}$		-12	
		$V_{CC} = 3\text{ V}$		-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
		$V_{CC} = 2.3\text{ V}$		8	
		$V_{CC} = 2.7\text{ V}$		12	
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μ A	1.65 V to 3.6 V	V _{CC}	-0.2		V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -8 mA	2.3 V		1.7		
	I _{OH} = -12 mA	2.7 V		2.2		
	I _{OH} = -24 mA	3 V		2.4		
	I _{OH} = -24 mA	3 V		2.2		
V _{OL}	I _{OL} = 100 μ A	1.65 V to 3.6 V		0.2		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.7		
	I _{OL} = 12 mA	2.7 V		0.4		
	I _{OL} = 24 mA	3 V		0.55		
I _I	V _I = 0 to 5.5 V	3.6 V		\pm 5	μ A	
I _{off}	V _I or V _O = 5.5 V	0		\pm 10	μ A	
I _{OZ}	V _O = 0 to 5.5 V	3.6 V		\pm 10	μ A	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	20		μ A
	3.6 V \leq V _I \leq 5.5 V ⁽²⁾			20		
ΔI_{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V		500	μ A
C _i	V _I = V _{CC} or GND		3.3 V		5	pF
C _o	V _O = V _{CC} or GND		3.3 V		6.5	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 1.8 V \pm 0.15 V	V _{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V \pm 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		150		150		150		MHz
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑		2.4		1.6		1.9		ns
t _h	Hold time, data after CLK↑		0.8		1		1.1		ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V \pm 0.15 V		V _{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V \pm 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		150		MHz
t _{pd}	CLK	Q	1	6.5	1	4.3	1	4.9	1.5	4.5	ns
t _{en}	\overline{OE}	Q	1	6.7	1	4.7	1	5.3	1.5	4.6	ns
t _{dis}	\overline{OE}	Q	1	10.7	1	5	1	6.1	1.5	5.5	ns
t _{sk(o)}									1		ns

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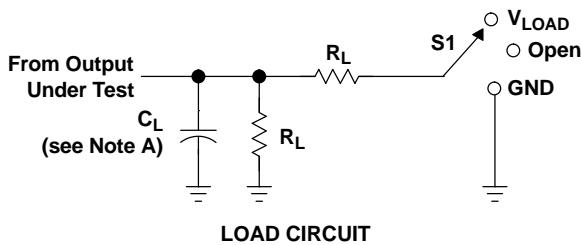


Operating Characteristics

$T_A = 25^\circ\text{C}$

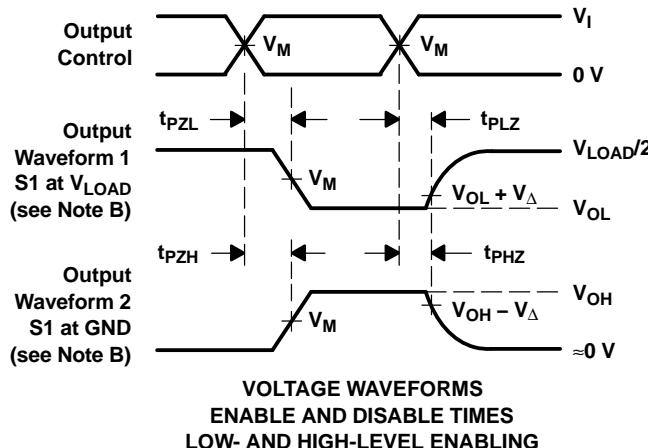
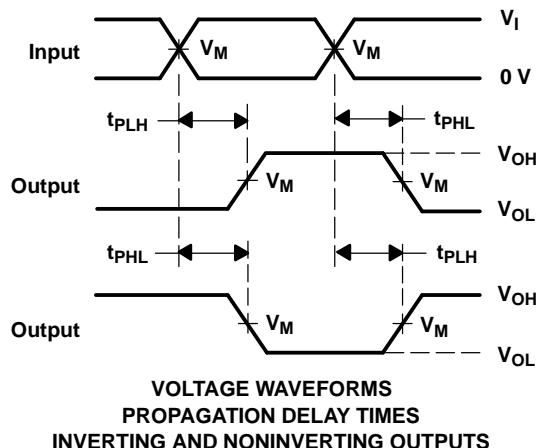
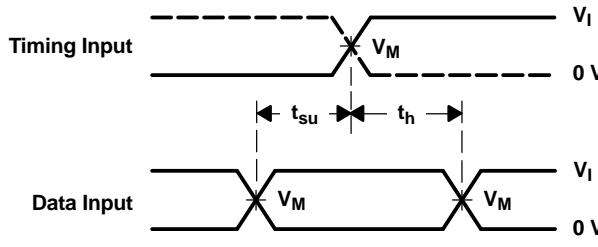
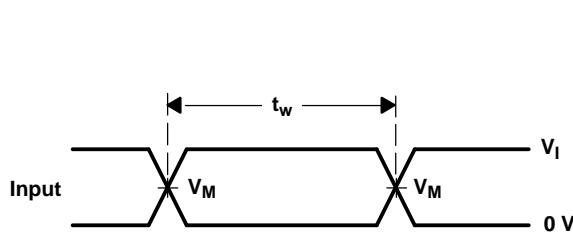
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per flip-flop	Outputs enabled	47	52	58	pF
	Outputs disabled	21	23	24	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	V_{CC}	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74LVC16374ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
74LVC16374ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD374A	Samples
74LVC16374ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD374A	Samples
SN74LVC16374ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
SN74LVC16374ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD374A	Samples
SN74LVC16374ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
SN74LVC16374ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
SN74LVC16374ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
SN74LVC16374ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16374A	Samples
SN74LVC16374AGRDR	OBsolete	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	LD374A	
SN74LVC16374AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LD374A	Samples
SN74LVC16374AZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LD374A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

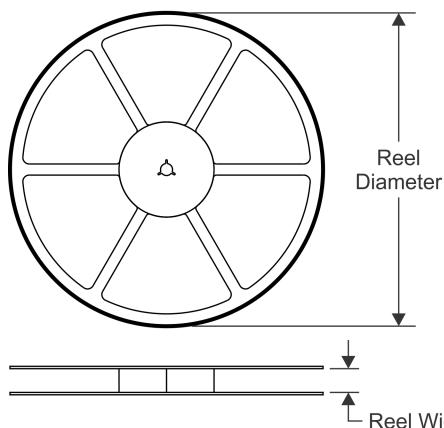
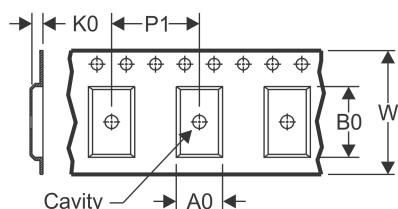
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

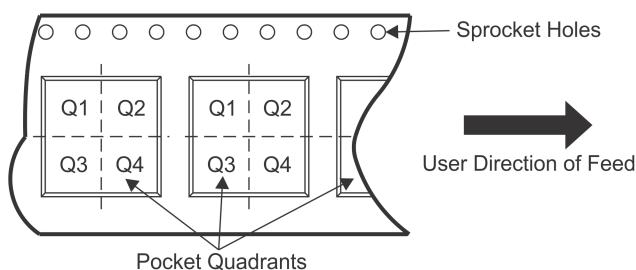
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC16374ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVC16374ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVC16374ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVC16374AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVC16374AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

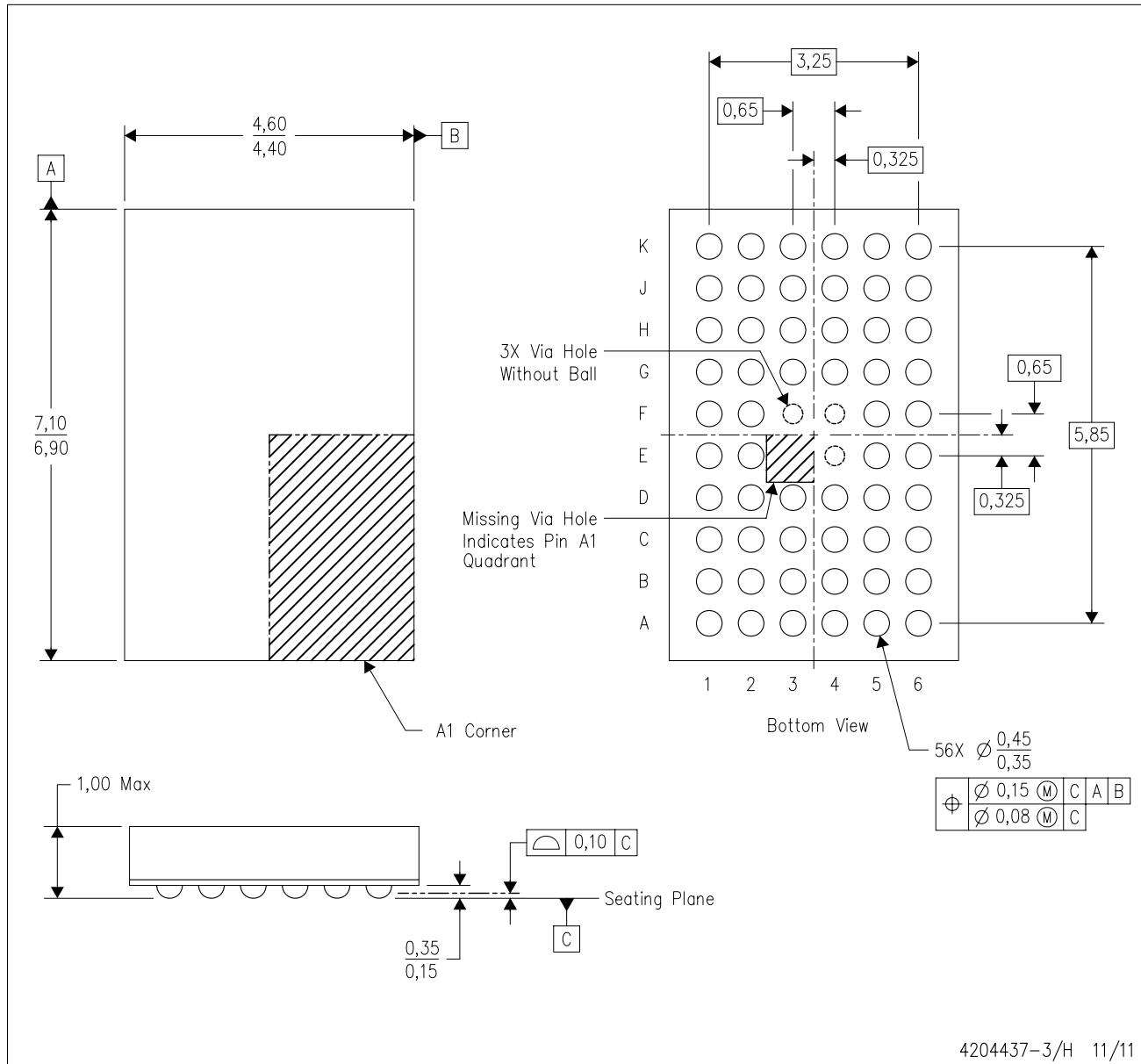
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC16374ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVC16374ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVC16374ADLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVC16374AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74LVC16374AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

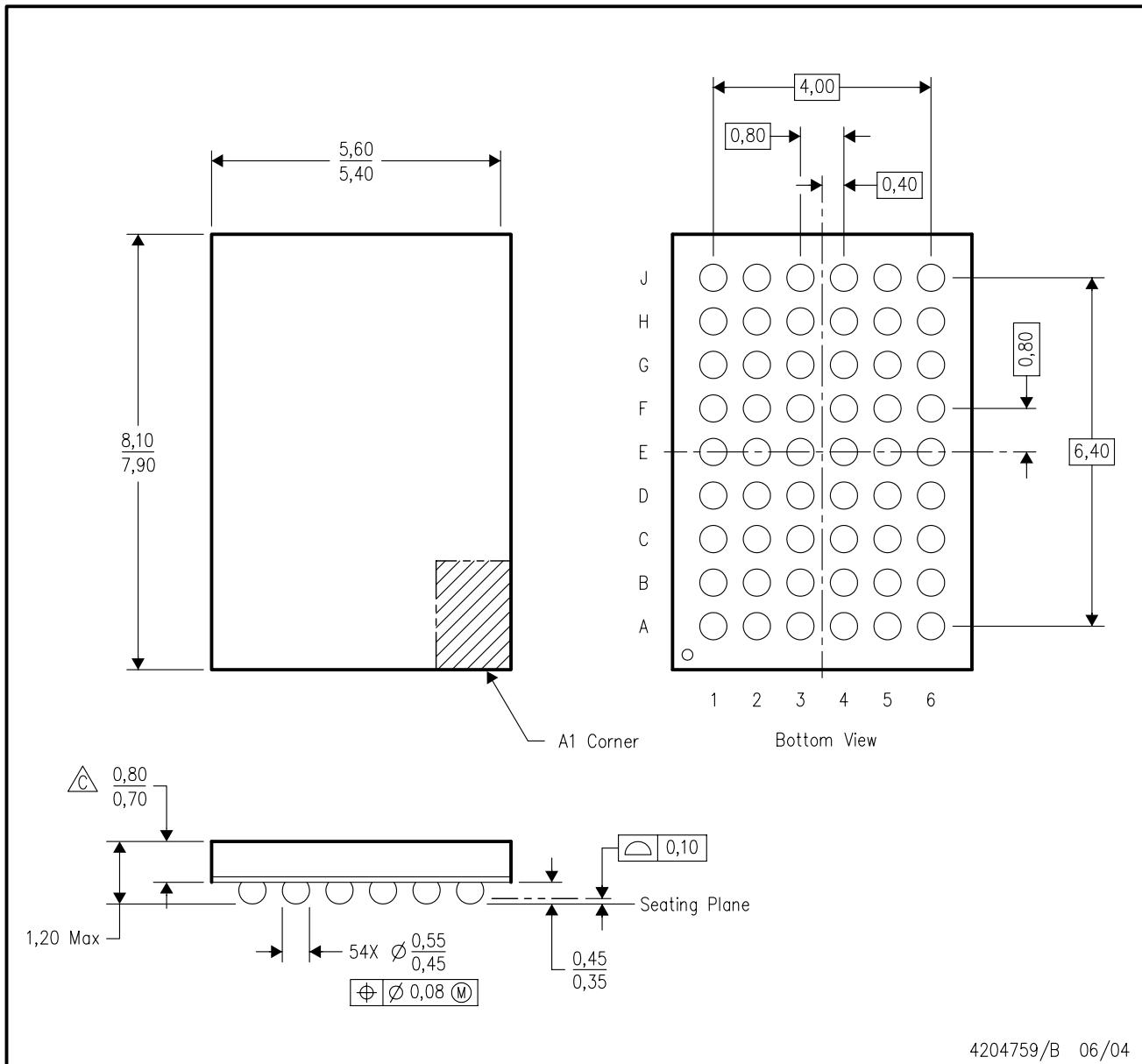


NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is Pb-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



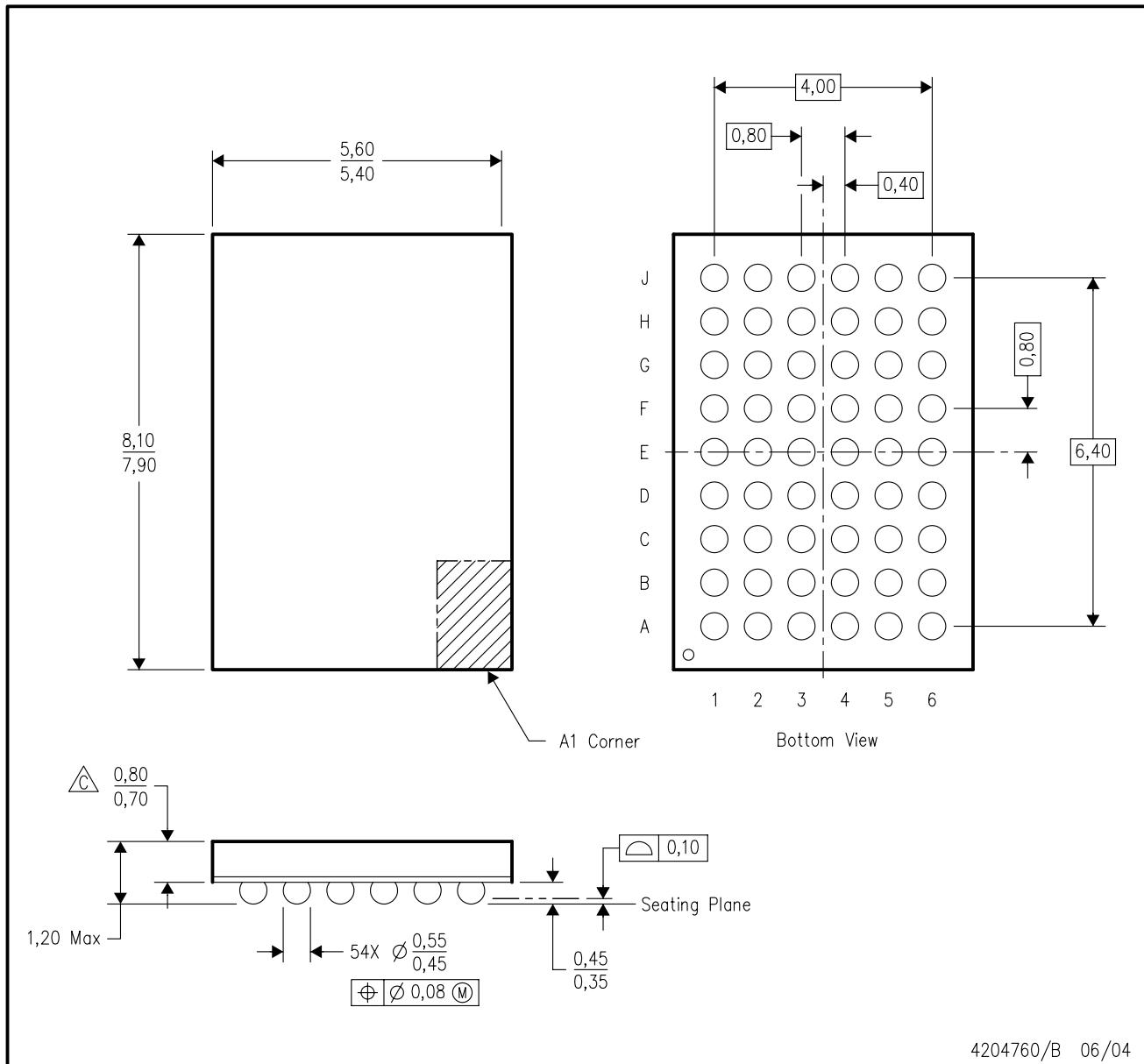
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

 Falls within JEDEC M0-205 variation D

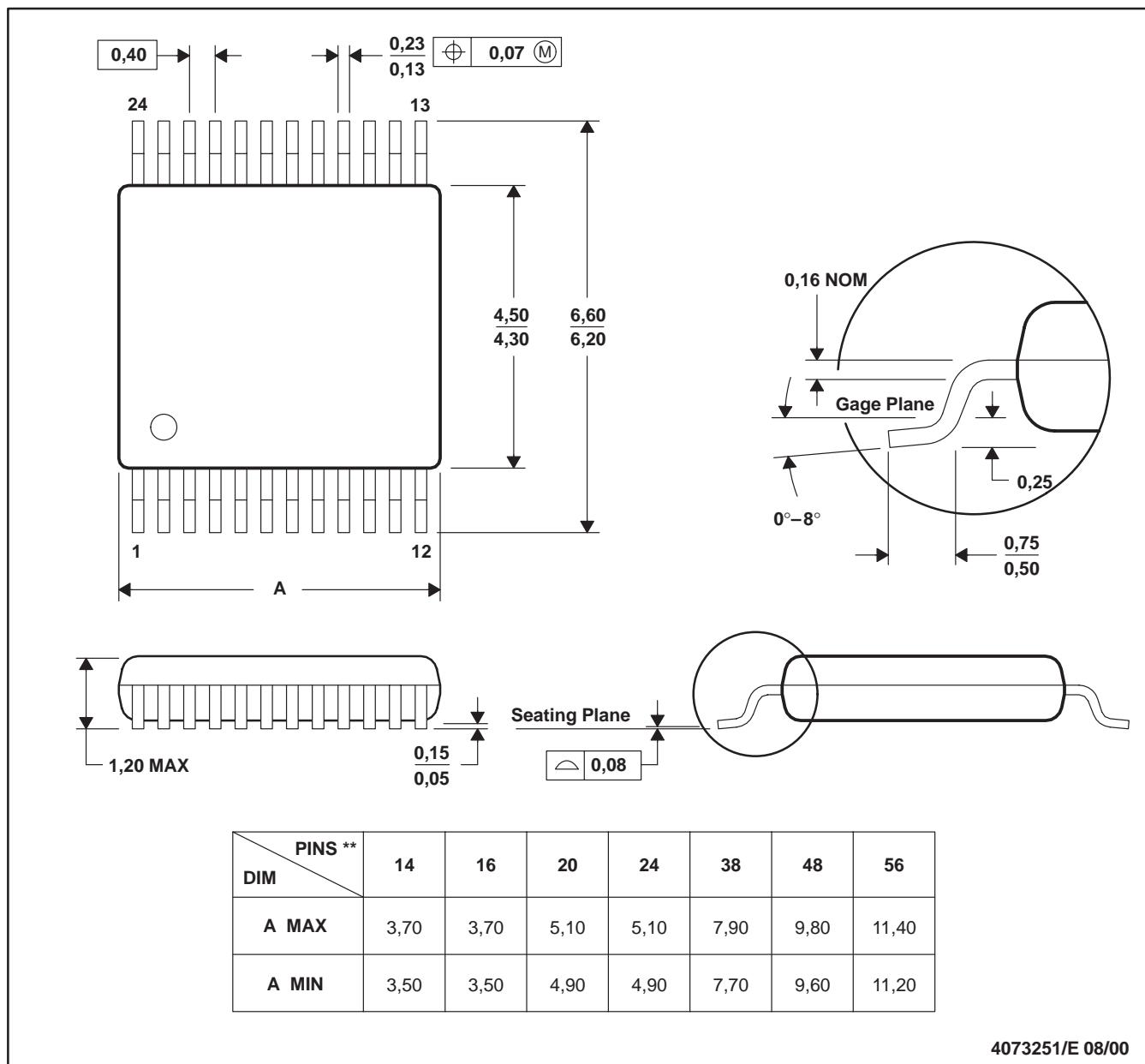
D. This package is lead-free. Refer to the

D. This package is lead-free. Refer to the S4 GRD package (drawing 4204759) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

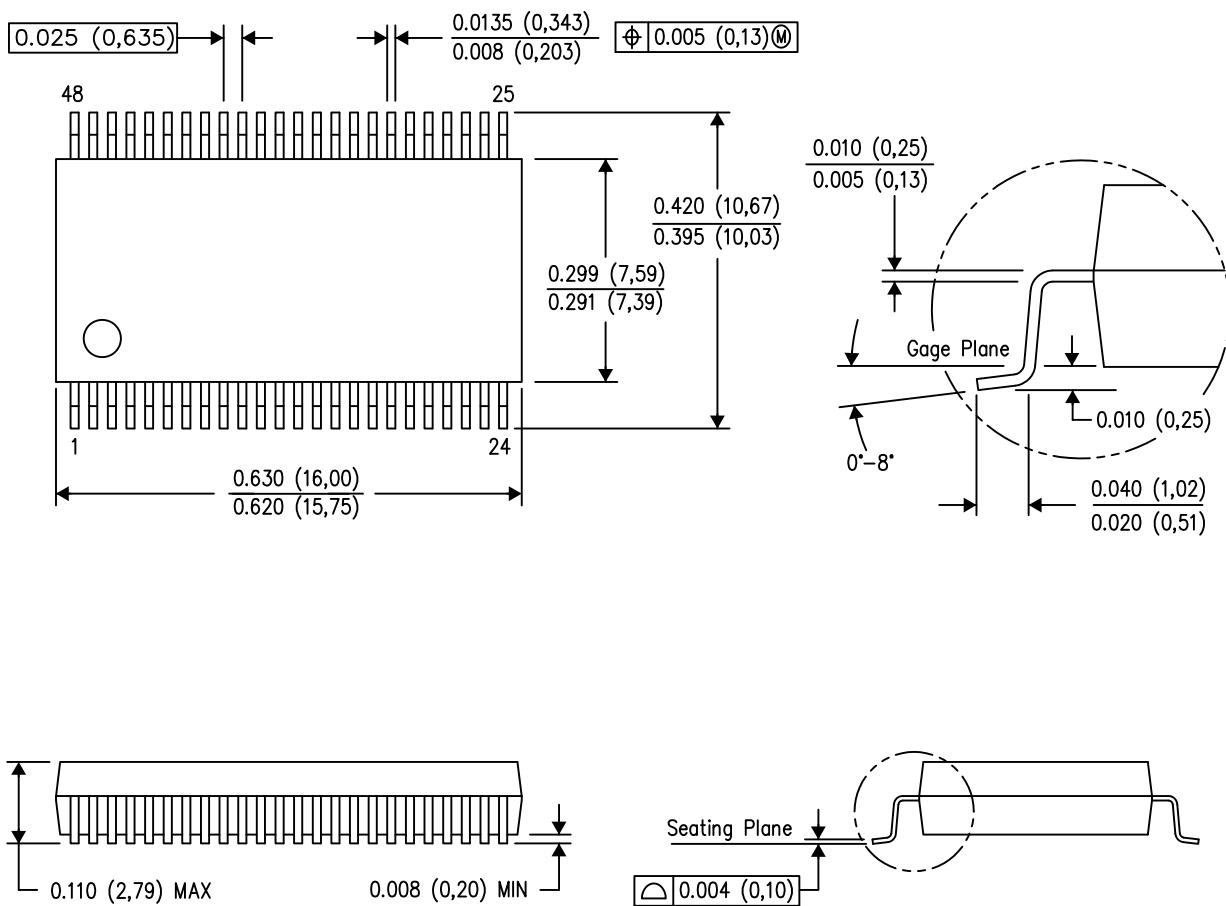
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

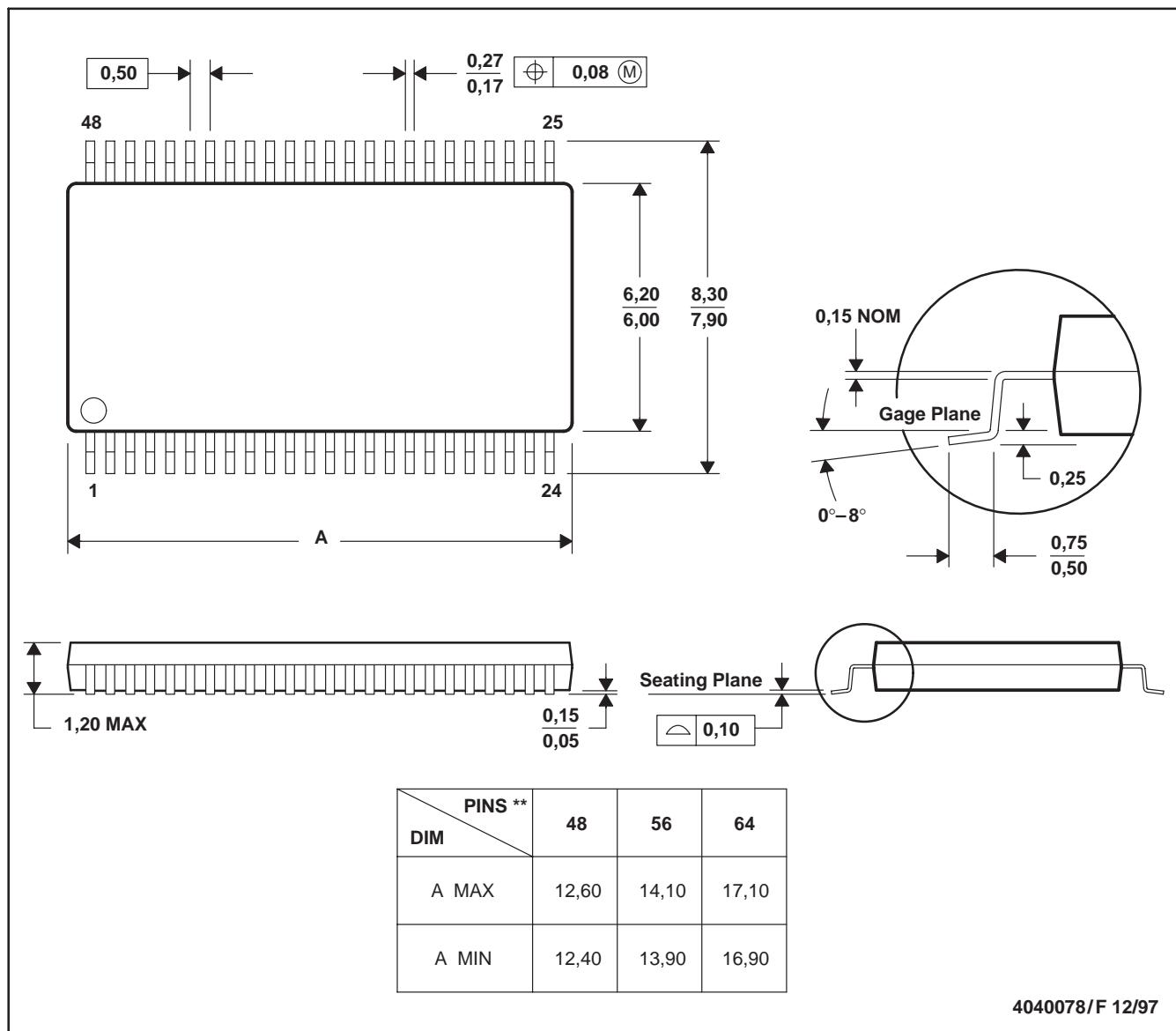
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC M0-118

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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