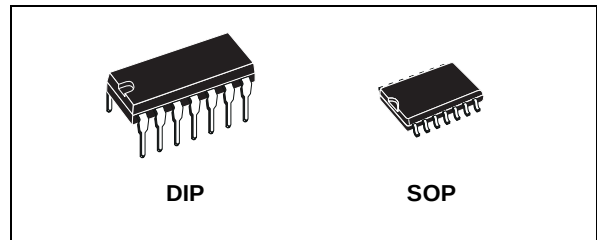


GATED J-K MASTER SLAVE FLIP-FLOP

- 16MHz TOGGLE RATE (Typ.) at $V_{DD} - V_{SS} = 10V$
- GATED INPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

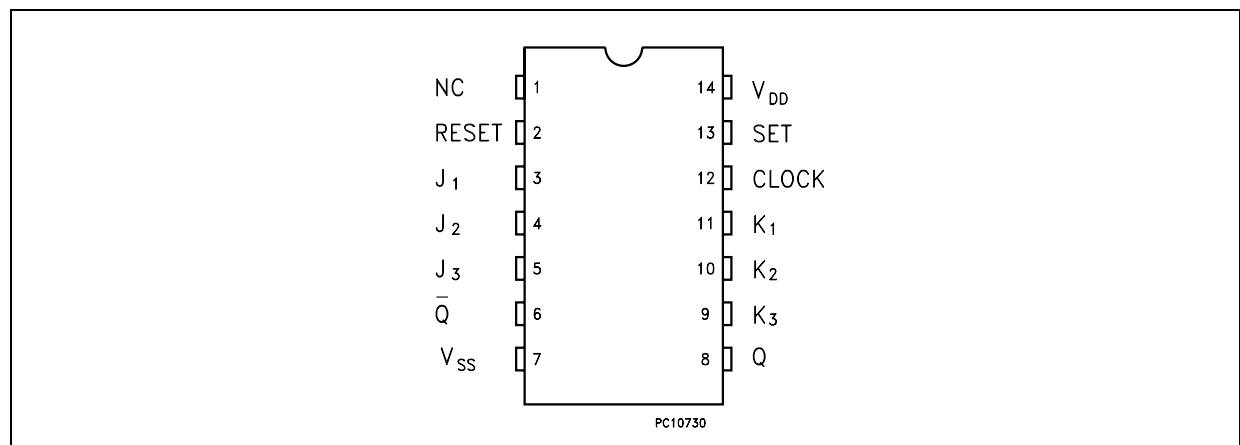
PACKAGE	TUBE	T & R
DIP	HCF4095BEY	
SOP	HCF4095BM1	HCF4095M013TR

DESCRIPTION

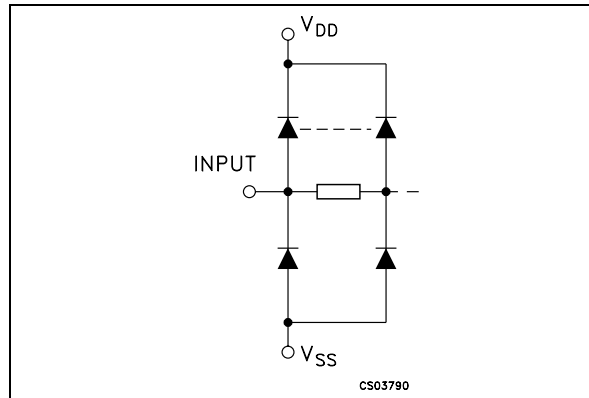
HCF4095B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4095B is J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K input control transfers

information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\bar{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 4, 5	J1 to J3	J Inputs
11, 10, 9	K1 to K3	K Inputs
8	Q	Q Output
6	Q	Q Output
13	SET (S)	Set Inputs(Active High)
2	RESET (R)	Reset Inputs(Active High)
12	CLOCK	Clock Inputs
1	NC	Not Connected
7	V _{SS}	Negative Supply Voltage
14	V _{DD}	Positive Supply Voltage

TRUTH TABLE : SYNCHRONOUS OPERATION (S=0 R=0)

INPUTS BEFORE POSITIVE CLOCK TRANSITION		OUTPUTS AFTER POSITIVE CLOCK TRANSITION	
J*	K*	Q	$\bar{Q}$
L	L	NO CHANGE	
L	H	L	H
H	L	H	L
H	H	TOGGLES	

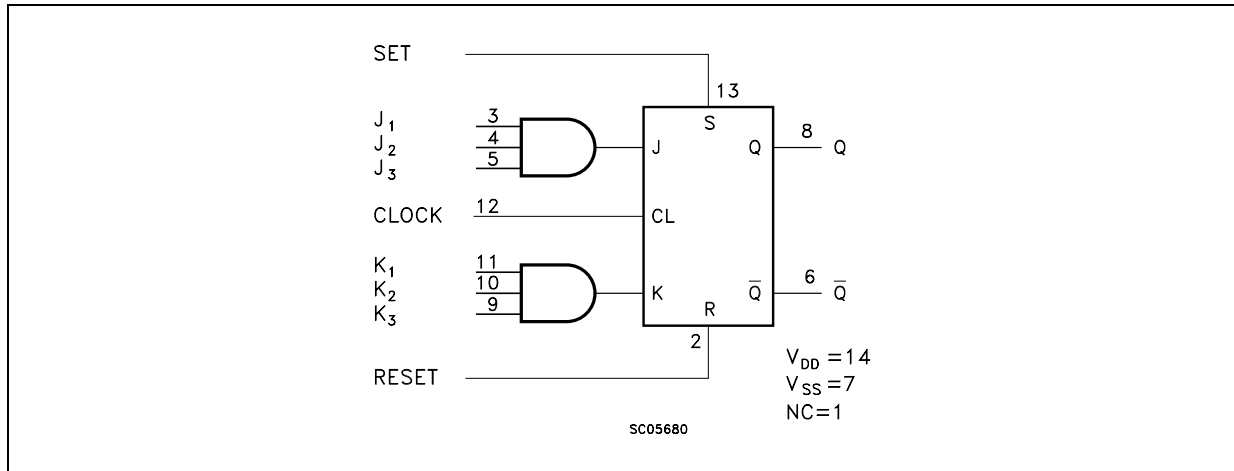
(*) : J=J1 • J2 • J3, K=K1 • K2 • K3

TRUTH TABLE : ASYNCHRONOUS OPERATION (J and K DON'T CARE)

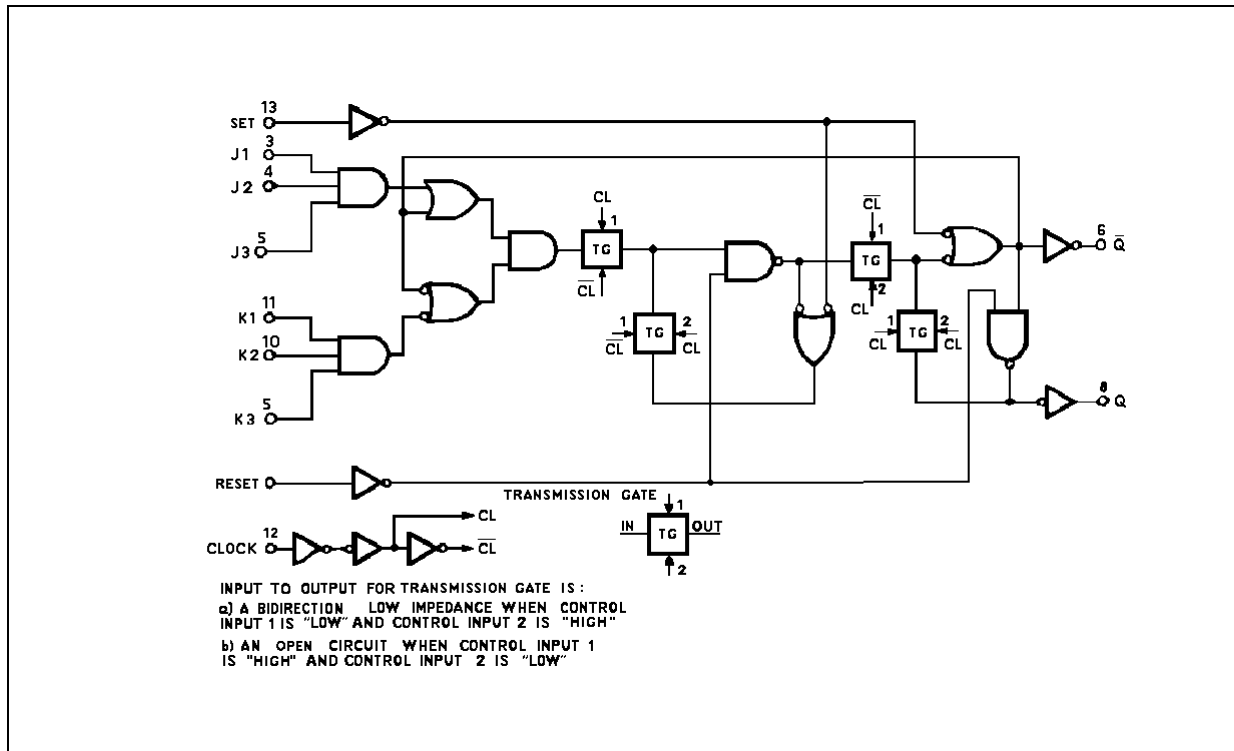
INPUTS BEFORE POSITIVE CLOCK TRANSITION		OUTPUTS AFTER POSITIVE CLOCK TRANSITION	
S	R	Q	$\bar{Q}$
L	L	NO CHANGE	
L	H	L	H
H	L	H	L
H	H	L	L

(*) : L = V_{ss}, H = V_{dd}

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value								Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I _L	Quiescent Current	0/5			5		0.02	1		30		30	μA	
		0/10			10		0.02	2		60		60		
		0/15			15		0.02	4		120		120		
		0/20			20		0.04	20		600		600		
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V	
		0/10		<1	10	9.95			9.95		9.95			
		0/15		<1	15	14.95			14.95		14.95			
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V	
		10/0		<1	10		0.05			0.05		0.05		
		15/0		<1	15		0.05			0.05		0.05		
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V	
			1/9	<1	10	7			7		7			
			1.5/13.5	<1	15	11			11		11			
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V	
			9/1	<1	10			3		3		3		
			13.5/1.5	<1	15			4		4		4		
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			

Symbol	Parameter	Test Condition				Value								Unit
		V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA	
C _I	Input Capacitance		Any Input				5	7.5					pF	

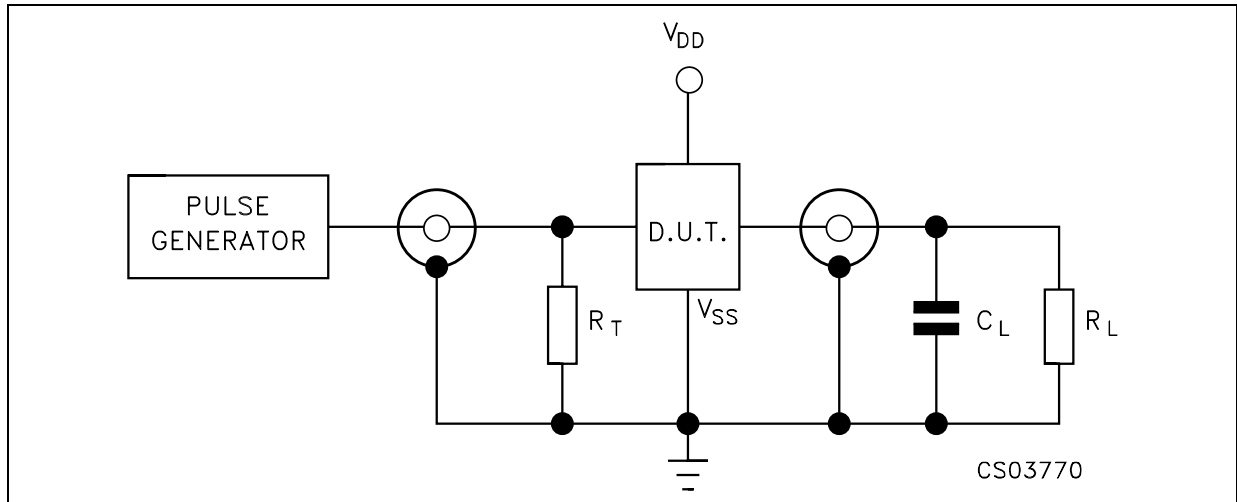
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200K Ω , t_r = t_f = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)		Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	5			250	500	ns
		10			100	200	
		15			75	150	
t _{PLH} t _{PHL}	Propagation Delay Time (Set or Reset)	5			150	300	ns
		10			75	150	
		15			50	100	
t _{TLH} t _{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f _{CL}	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		8	16		
		15		12	24		
t _W	Clock Pulse Width	5		140	70		ns
		10		60	30		
		15		40	20		
t _r , t _f	Clock input Rise or Fall Time	5				15	μ s
		10				5	
		15				5	
t _W	Set or Reset Pulse Width	5		200	100		ns
		10		100	50		
		15		50	25		
t _{setup}	Data Setup Time	5		400	200		ns
		10		160	80		
		15		100	50		

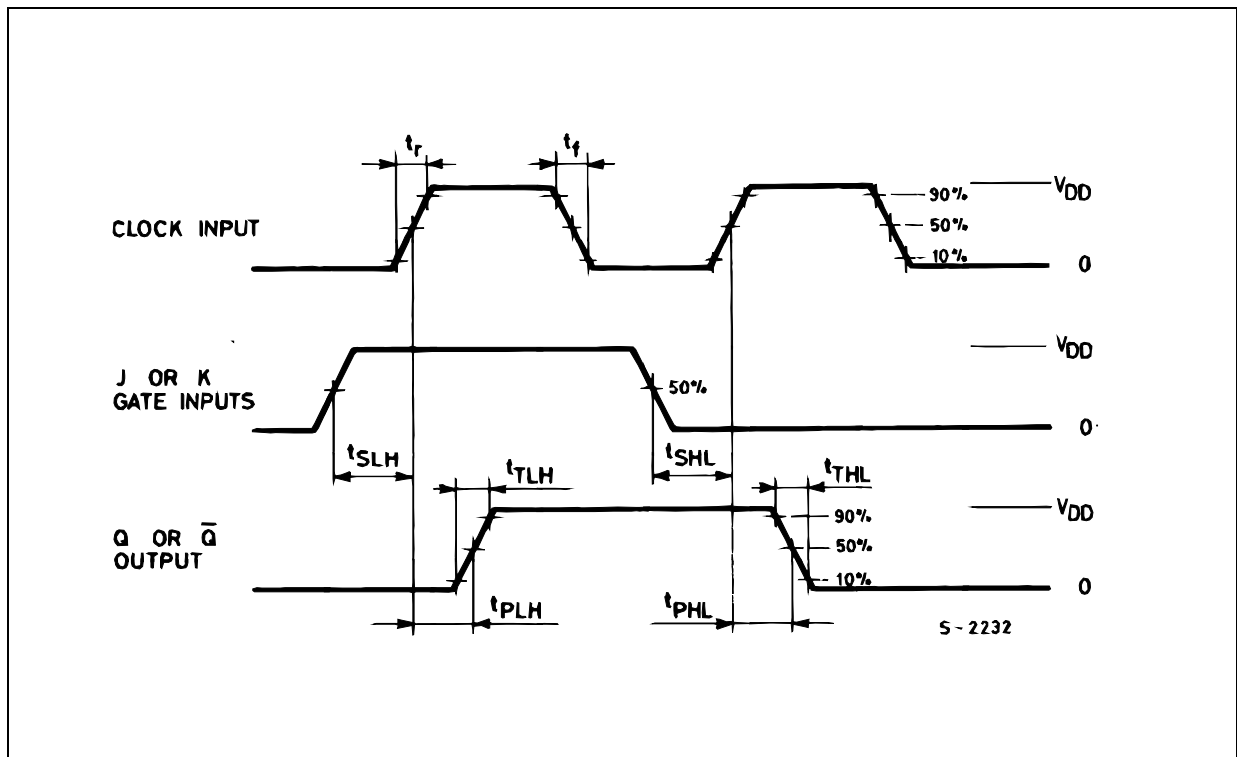
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TEST CIRCUIT

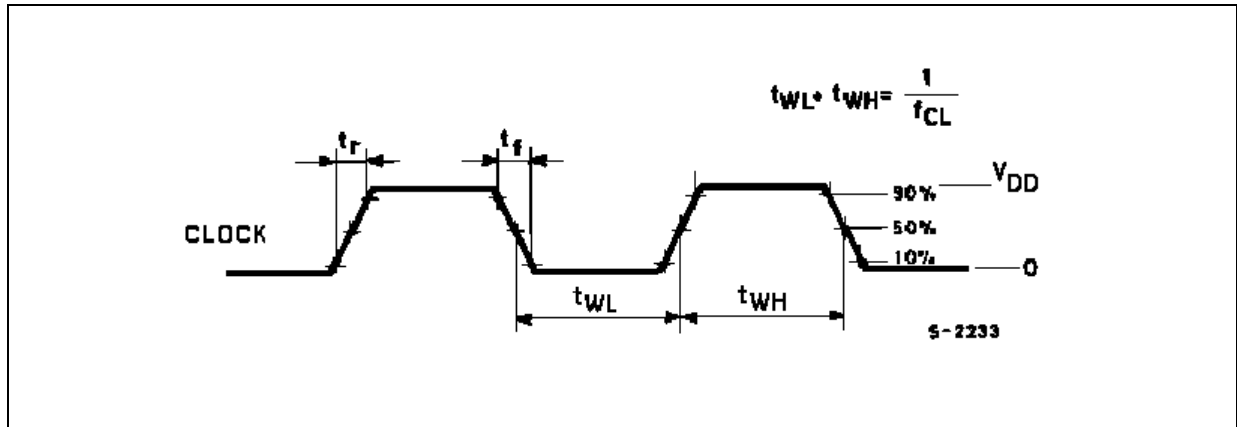


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{k}\Omega$
 $R_T = Z_{\text{OUT}}$ of pulse generator (typically 50Ω)

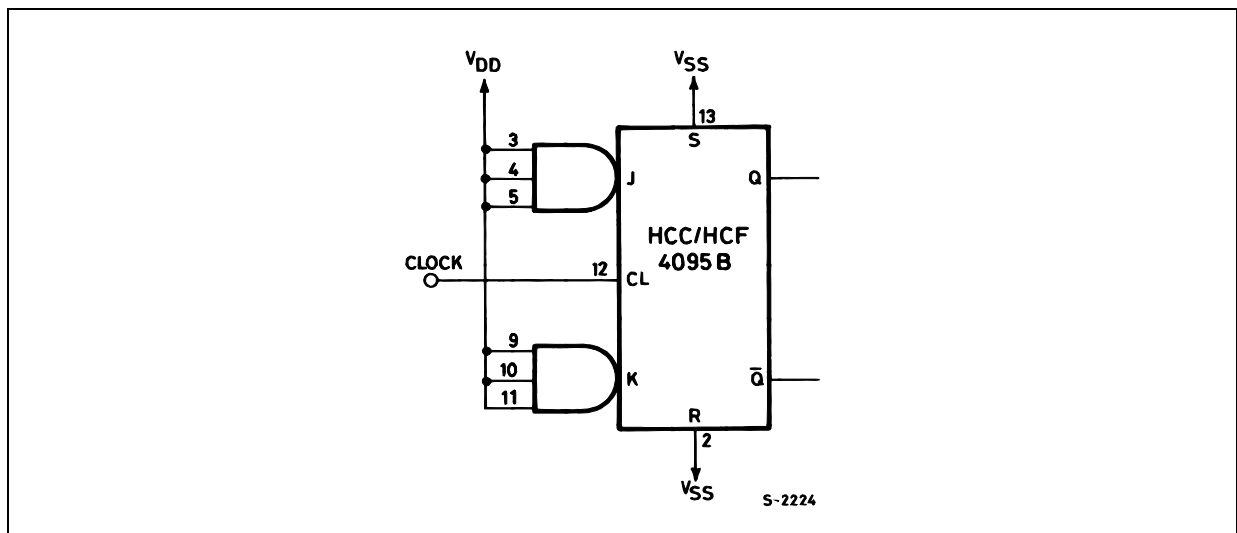
WAVEFORM : PROPAGATION DELAY, TRANSITION AND SETUP TIME



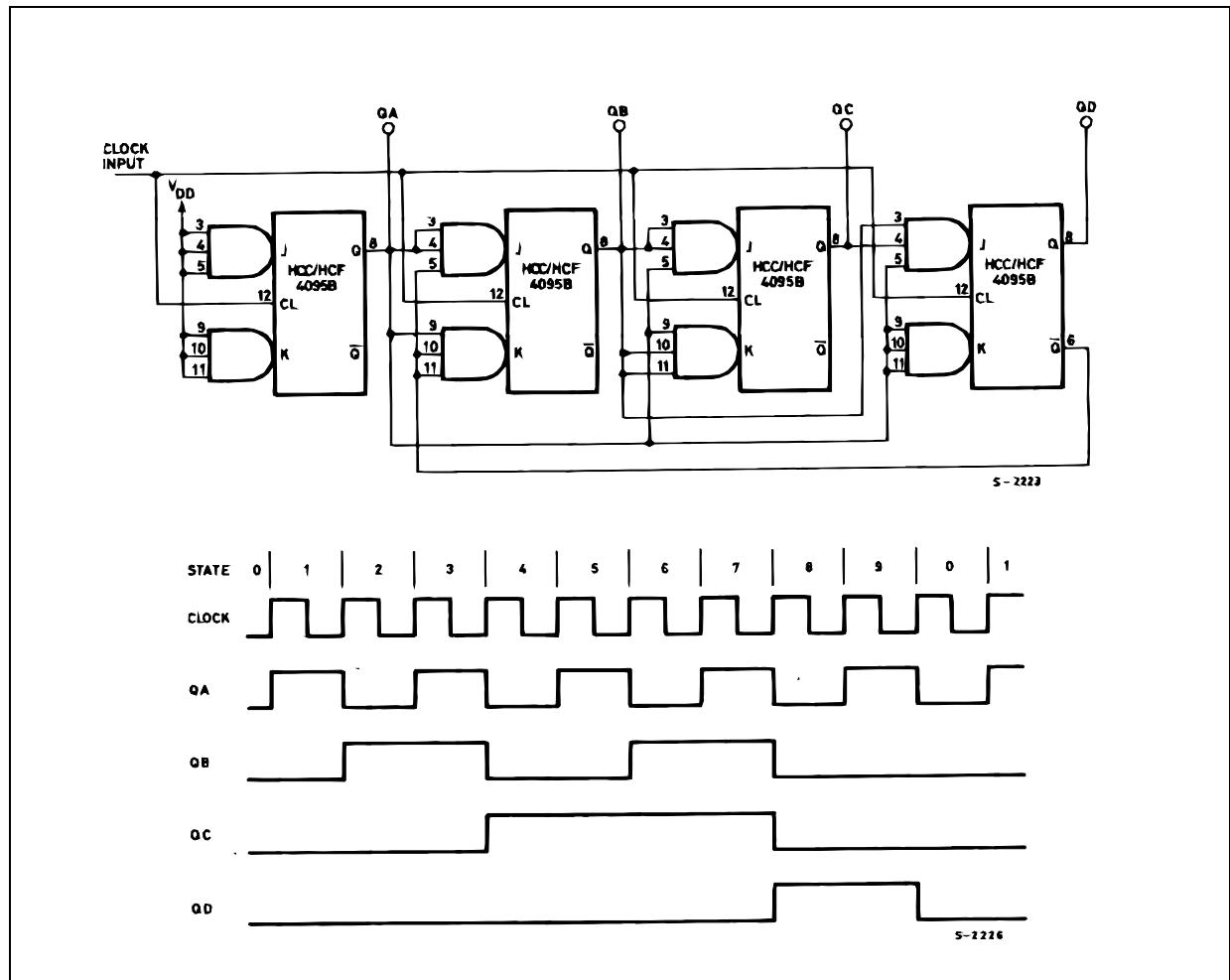
WAVEFORM : CLOCK PULSE, RISE AND FALL TIME



TYPICAL APPLICATION: T-TYPE FLIP-FLOP



TYPICAL APPLICATION: SYNCHRONOUS BINARY DIVIDE BY TEN COUNTER



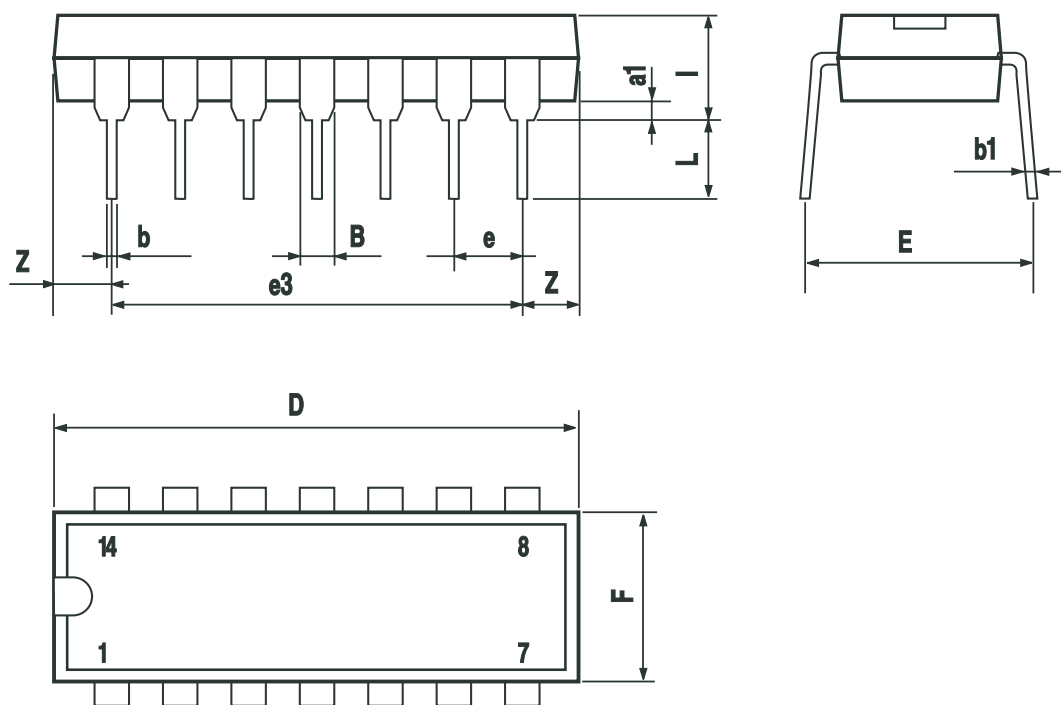
TRUTH TABLE

STATE	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: In all units the Set and Reset are Connected to V_{SS} .

Plastic DIP-14 MECHANICAL DATA

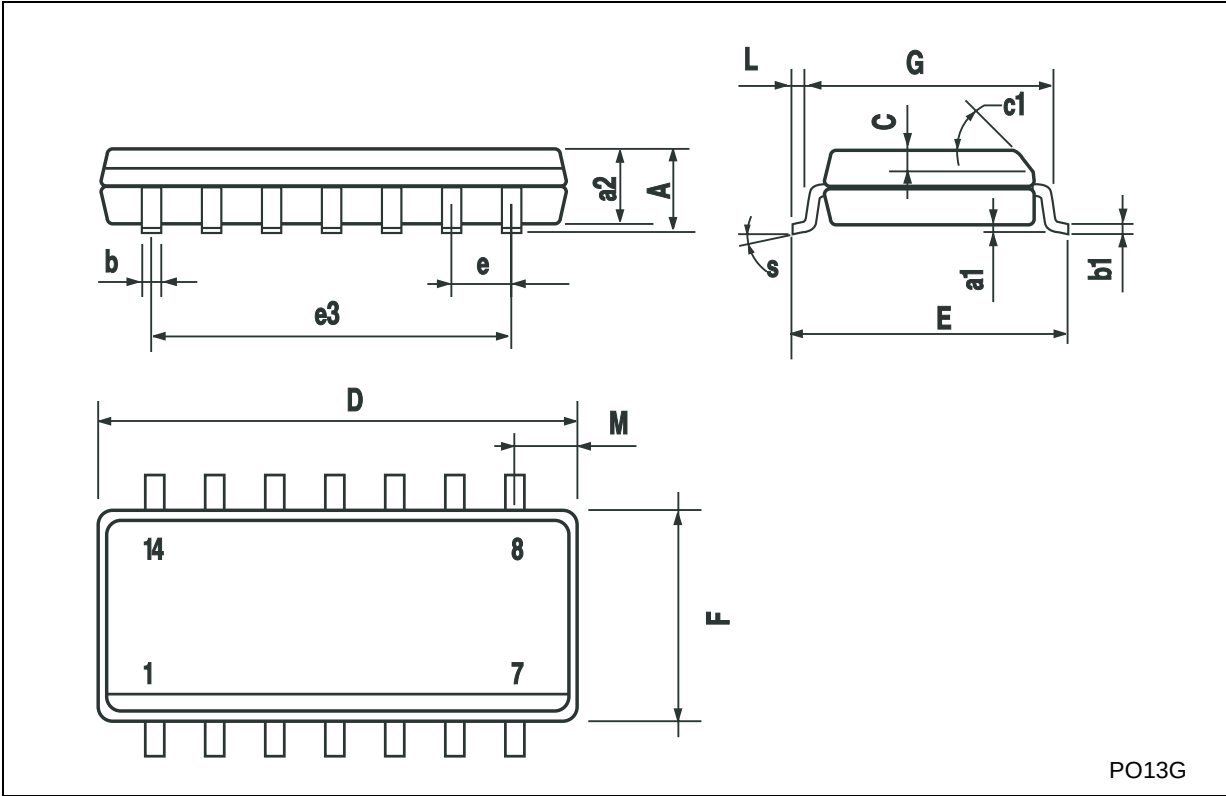
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G



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