

AMP03
FEATURES

High CMRR: 100 dB Typ
 Low Nonlinearity: 0.001% Max
 Low Distortion: 0.001% Typ
 Wide Bandwidth: 3 MHz Typ
 Fast Slew Rate: 9.5 V/ μ s Typ
 Fast Settling (0.01%): 1 μ s Typ
 Low Cost

APPLICATIONS

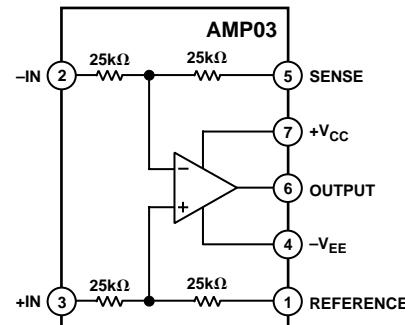
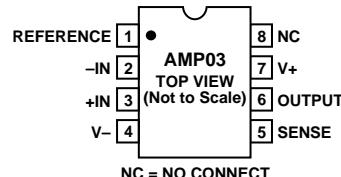
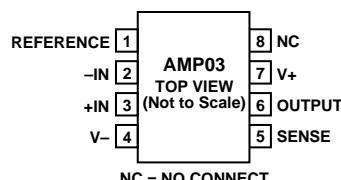
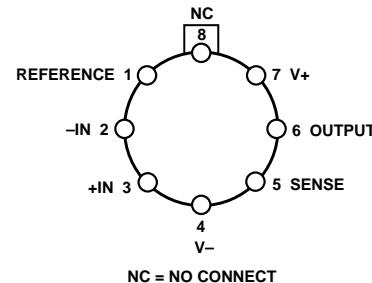
Summing Amplifiers
Instrumentation Amplifiers
Balanced Line Receivers
Current-Voltage Conversion
Absolute Value Amplifier
4 mA-20 mA Current Transmitter
Precision Voltage Reference Applications
Lower Cost and Higher Speed Version of INA105

GENERAL DESCRIPTION

The AMP03 is a monolithic unity-gain, high speed differential amplifier. Incorporating a matched thin-film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications.

The differential amplifier topology of the AMP03 serves to both amplify the difference between two signals and provide extremely high rejection of the common-mode input voltage. By providing common-mode rejection (CMR) of 100 dB typical, the AMP03 solves common problems encountered in instrumentation design. As an example, the AMP03 is ideal for performing either addition or subtraction of two signals without using expensive externally-matched precision resistors. The large common-mode rejection is made possible by matching the internal resistors to better than 0.002% and maintaining a thermally symmetric layout. Additionally, due to high CMR over frequency, the AMP03 is an ideal general amplifier for buffering signals in a noisy environment into data acquisition systems.

The AMP03 is a higher speed alternative to the INA105. Featuring slew rates of 9.5 V/ μ s, and a bandwidth of 3 MHz, the AMP03 offers superior performance for high speed current sources, absolute value amplifiers and summing amplifiers than the INA105.

FUNCTIONAL BLOCK DIAGRAM

PIN CONNECTIONS
**8-Lead Plastic DIP
(P Suffix)**

**8-Lead SOIC
(S Suffix)**

**Header
(J Suffix)**

REV. E

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AMP03—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	AMP03F			AMP03B			AMP03G			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0$ V	-400	10	400	-700	20	700	-750	25	750	µV
Gain Error		No Load, $V_{IN} = \pm 10$ V, $R_S = 0$ Ω		0.00004	0.008		0.00004	0.008		0.001	0.008	%
Input Voltage Range	IVR	(Note 1)	±10			±10			±10			V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10$ V	85	100		80	95		80	95		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6$ V to ± 18 V		0.6	10		0.6	10		0.7	10	µV/V
Output Swing	V_O	$R_L = 2$ kΩ	±12	±13.7		±12	±13.7		±12	±13.7		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground		+45/-15			+45/-15			+45/-15		mA
Small-Signal Bandwidth (-3 dB)	BW	$R_L = 2$ kΩ		3			3			3		MHz
Slew Rate	SR	$R_L = 2$ kΩ	6	9.5		6	9.5		6	9.5		V/µs
Capacitive Load Drive Capability	C_L	No Oscillation		300			300			300		pF
Supply Current	I_{SY}	No Load		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES

¹Input voltage range guaranteed by CMR test.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for B Grade)

Parameter	Symbol	Conditions	AMP03B			Units
			Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0$ V	-1500	150	1500	µV
Gain Error		No Load, $V_{IN} = \pm 10$ V, $R_S = 0$ Ω		0.0014	0.02	%
Input Voltage Range	IVR		±20			V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10$ V	75	95		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6$ V to ± 18 V		0.7	20	µV/V
Output Swing	V_O	$R_L = 2$ kΩ	±12	±13.7		V
Slew Rate	SR	$R_L = 2$ kΩ		9.5		V/µs
Supply Current	I_{SY}	No Load		3.0	4.0	mA

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for F and G Grades)

Parameter	Symbol	Conditions	AMP03F			AMP03G			Units
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0$ V	-1000	100	1000	-2000	200	2000	µV
Gain Error		No Load, $V_{IN} = \pm 10$ V, $R_S = 0$ Ω		0.0008	0.015		0.002	0.02	%
Input Voltage Range	IVR		±20			±20			V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10$ V	80	95		75	90		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6$ V to ± 18 V		0.7	15		1.0	15	µV/V
Output Swing	V_O	$R_L = 2$ kΩ	±12	±13.7		±12	±13.7		V
Slew Rate	SR	$R_L = 2$ kΩ		9.5			9.5		V/µs
Supply Current	I_{SY}	No Load		2.6	4.0		2.6	4.0	mA

Specifications subject to change without notice.

WAFER TEST LIMITS (@ $V_S = \pm 15$ V, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	AMP03BC Limit	Units
Offset Voltage	V_{OS}	$V_S = \pm 18$ V	0.5	mV max
Gain Error		No Load, $V_{IN} = \pm 10$ V, $R_S = 0 \Omega$	0.008	% max
Input Voltage Range	IVR		± 10	V min
Common-Mode Rejection	CMR	$V_{CM} = \pm 10$ V	80	dB min
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6$ V to ± 18 V	8	$\mu\text{V/V}$ max
Output Swing	V_O	$R_L = 2 \text{ k}\Omega$	± 12	V max
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	$+45/-15$	mA min
Supply Current	I_{SY}	No Load	3.5	mA max

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	± 18 V
Input Voltage ²	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range		
P, J Package	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Operating Temperature Range		
AMP03B	-55°C to $+125^\circ\text{C}$
AMP03F, AMP03G	-40°C to $+85^\circ\text{C}$

Package Type	θ_{JA}^3	θ_{JC}	Units
Header (J)	150	18	$^\circ\text{C}/\text{W}$
8-Lead Plastic DIP (P)	103	43	$^\circ\text{C}/\text{W}$
8-Lead SOIC (S)	155	40	$^\circ\text{C}/\text{W}$

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

²For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.

³ θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for header and plastic DIP packages and for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE¹

Model	Temperature Range	Package Description	Package Option ²
AMP03GP	-40°C to $+85^\circ\text{C}$	8-Lead Plastic DIP	N-8
AMP03BJ	-40°C to $+85^\circ\text{C}$	Header	H-08B
AMP03FJ	-40°C to $+85^\circ\text{C}$	Header	H-08B
AMP03BJ/883C	-55°C to $+125^\circ\text{C}$	Header	H-08B
AMP03GS	-40°C to $+85^\circ\text{C}$	8-Lead SOIC	SO-8
AMP03GS-REEL	-40°C to $+85^\circ\text{C}$	8-Lead SOIC	SO-8
5962-9563901MGA	-55°C to $+125^\circ\text{C}$	Header	H-08B
AMP03GBC		Die	

NOTES

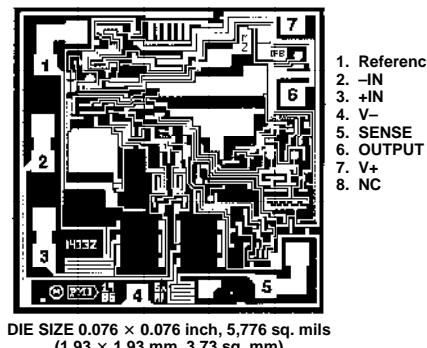
¹Burn-in is available on commercial and industrial temperature range parts in plastic DIP and header packages.

²For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 data sheet.

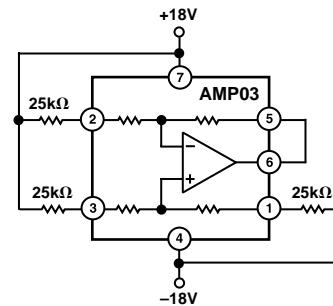
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AMP03 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

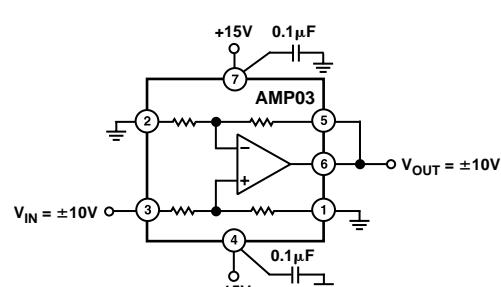
DICE CHARACTERISTICS



BURN-IN CIRCUIT



SLEW RATE TEST CIRCUIT



AMP03—Typical Performance Characteristics

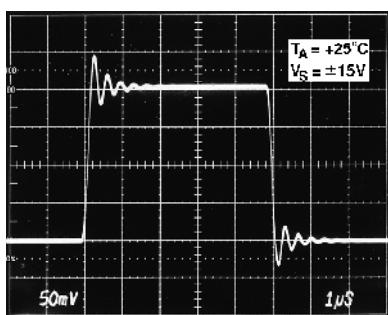


Figure 1. Small Signal Transient Response

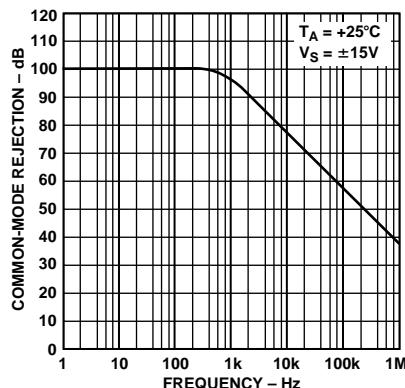


Figure 2. Common-Mode Rejection vs. Frequency

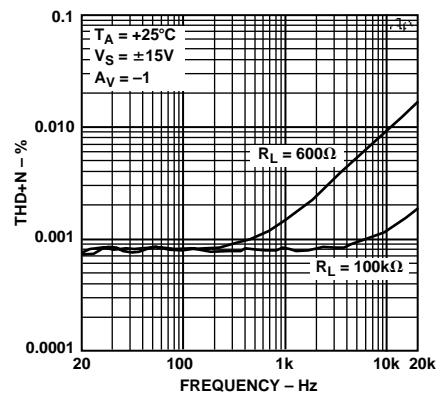


Figure 3. Total Harmonic Distortion vs. Frequency

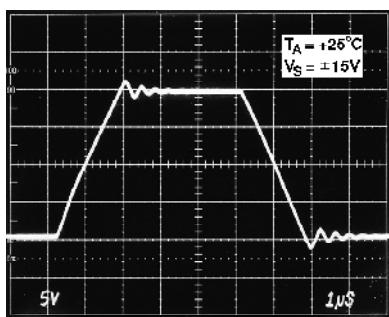


Figure 4. Large Signal Transient Response

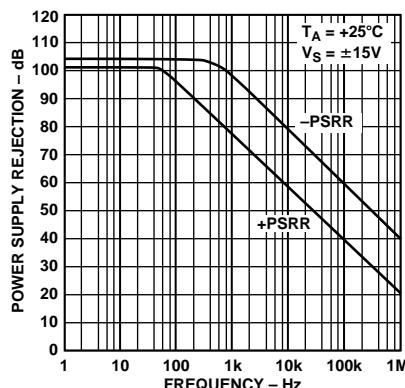


Figure 5. Power Supply Rejection vs. Frequency

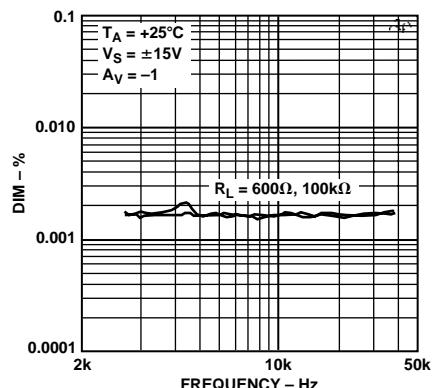


Figure 6. Dynamic Intermodulation Distortion vs. Frequency

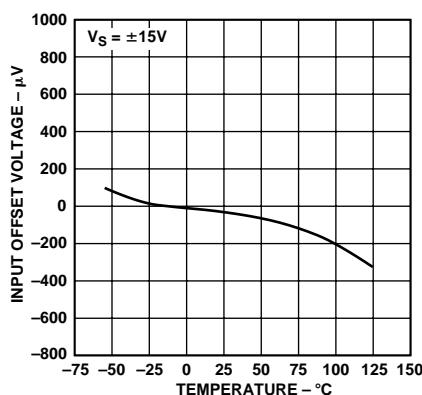


Figure 7. Input Offset Voltage vs. Temperature

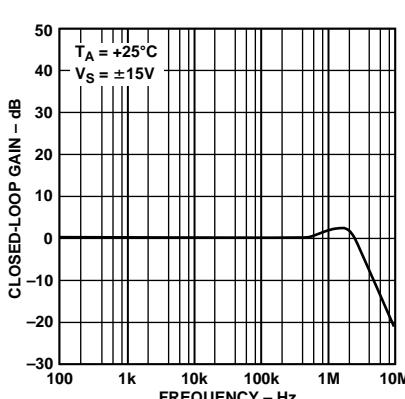


Figure 8. Closed-Loop Gain vs. Frequency

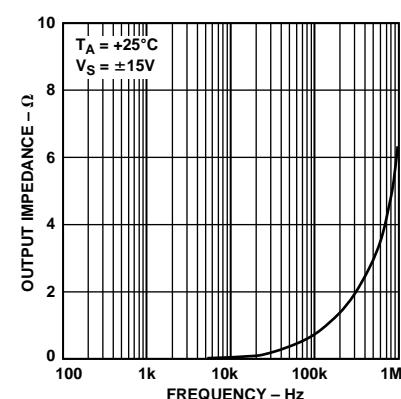


Figure 9. Closed-Loop Output Impedance vs. Frequency

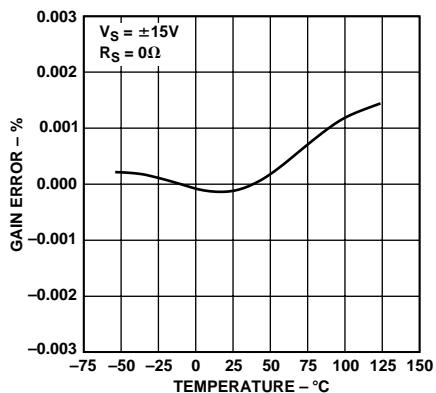


Figure 10. Gain Error vs. Temperature

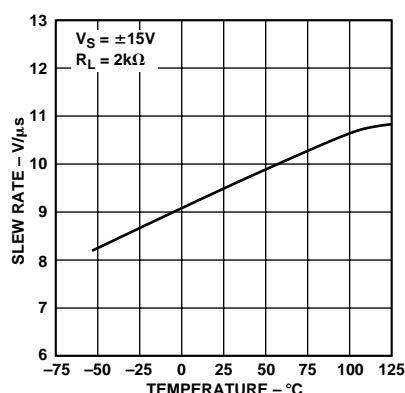


Figure 11. Slew Rate vs. Temperature

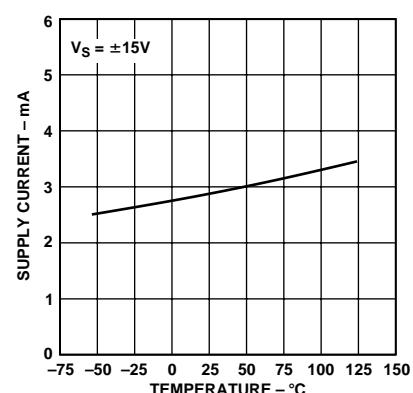


Figure 12. Supply Current vs. Temperature

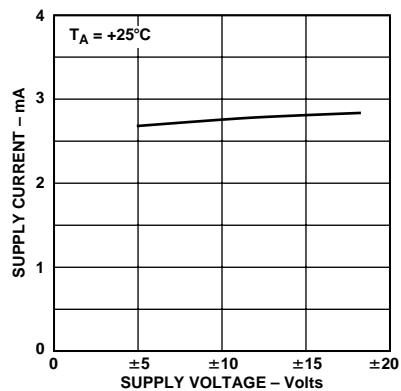


Figure 13. Supply Current vs. Supply Voltage

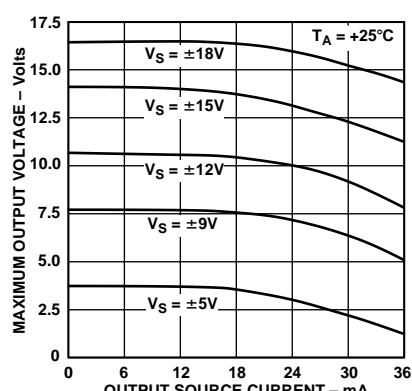


Figure 14. Maximum Output Voltage vs. Output Current (Source)

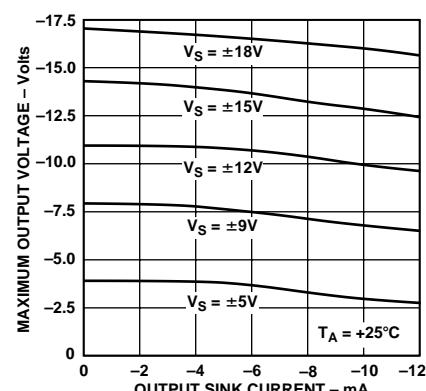


Figure 15. Maximum Output Voltage vs. Output Current (Sink)

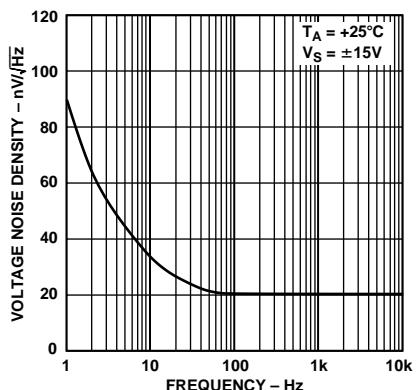


Figure 16. Voltage Noise Density vs. Frequency

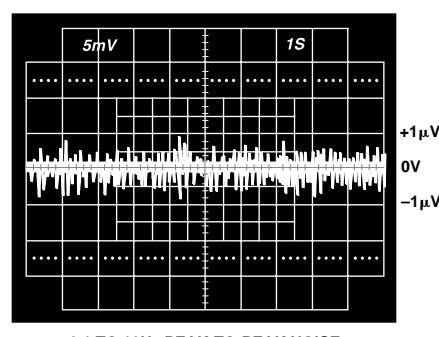


Figure 17. Low Frequency Voltage Noise

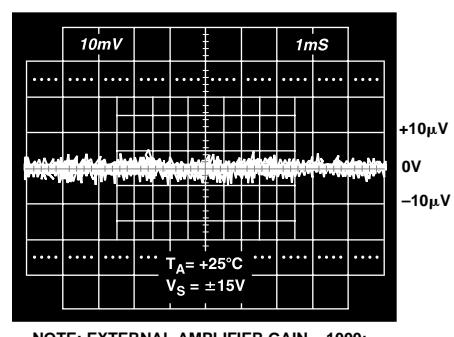


Figure 18. Voltage Noise from 0 kHz to 1 kHz

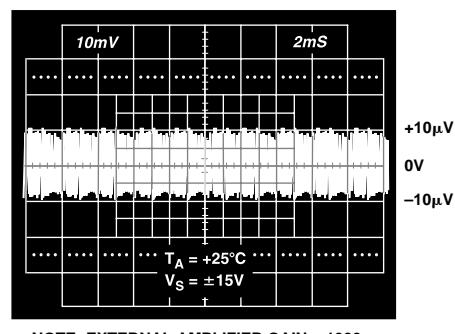


Figure 19. Voltage Noise from 0 kHz to 10 kHz

AMP03

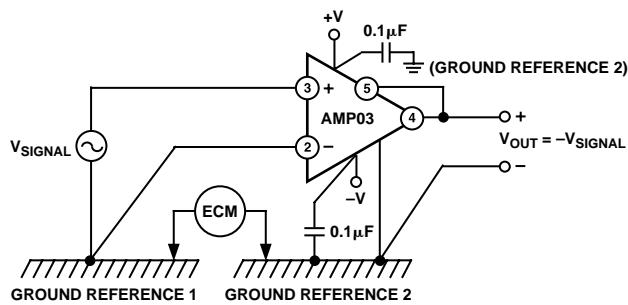


Figure 20. AMP03 Serves to Reject Common-Mode Voltages in Instrumentation Systems. Common-Mode Voltages Occur Due to Ground Current Returns. V_{SIGNAL} and E_{CM} Must Be Within the Common-Mode Range of AMP03.

APPLICATIONS INFORMATION

The AMP03 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate and high CMR, proper decoupling and grounding techniques must be employed. Figure 20 illustrates the use of $0.1 \mu F$ decoupling capacitors and proper ground connections.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the AMP03, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR—even a 5Ω imbalance will degrade CMR by 20 dB. Also, the matching of the reactive source impedance must be matched in order to preserve the CMRR over frequency.

APPLICATION CIRCUITS

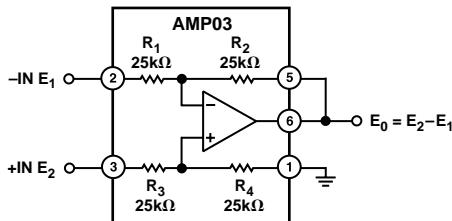


Figure 21. Precision Difference Amplifier. Rejects Common-Mode Signal $= (E_1 + E_2)/2$ by 100 dB

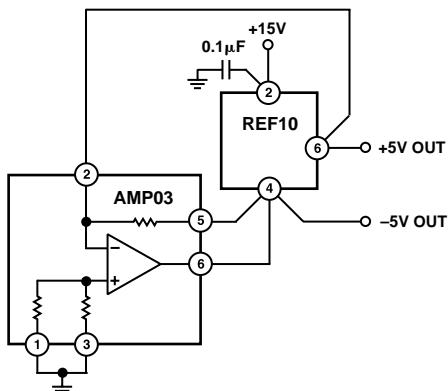


Figure 24. ± 5 V Precision Voltage Reference

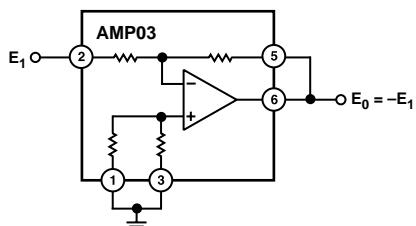


Figure 22. Precision Unity-Gain Inverting Amplifier

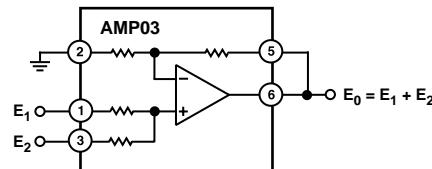


Figure 25. Precision Summing Amplifier

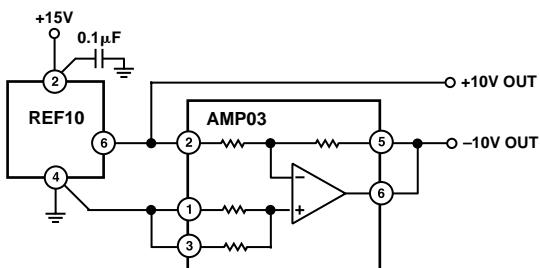


Figure 23. ± 10 V Precision Voltage Reference

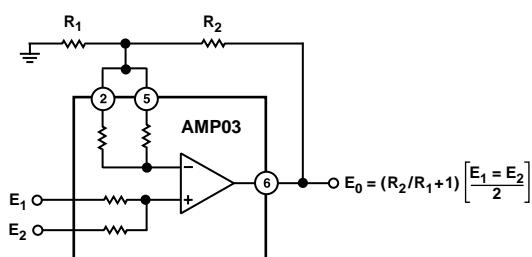


Figure 26. Precision Summing Amplifier with Gain

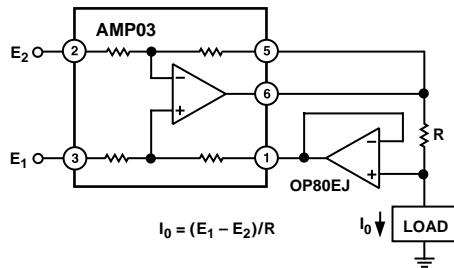


Figure 27. Differential Input Voltage-to-Current Converter for Low I_{OUT} . OP80EJ Maintains 250 fA Max Input Current, Allowing I_0 to Be Less Than 1 pA

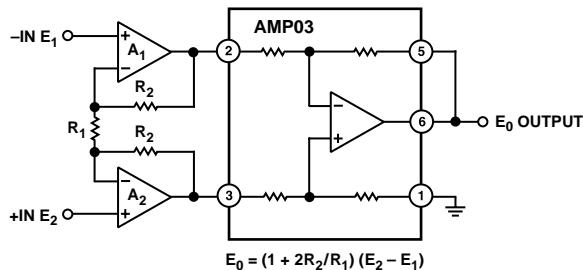
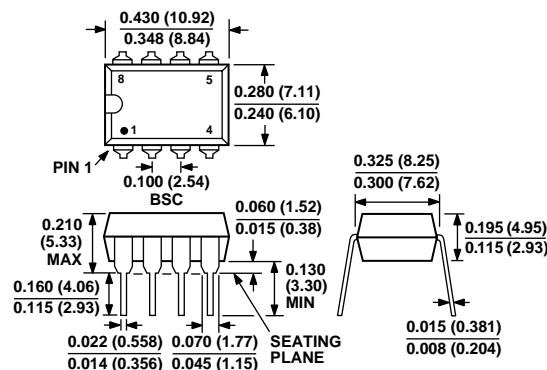


Figure 28. Suitable Instrumentation Amplifier Requirements Can Be Addressed by Using an Input Stage Consisting of A_1 , A_2 , R_1 and R_2 . The Following Matrix Suggests a Suitable Amplifier.

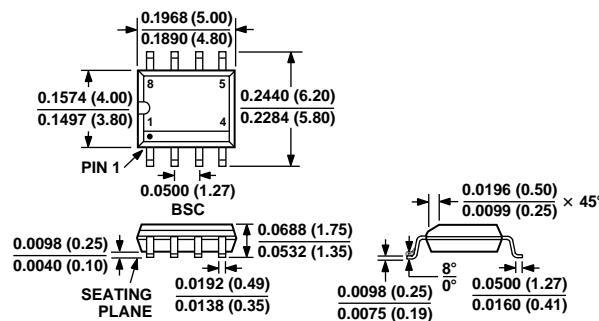
System Design Requirement	Suggested Op Amp For A1 and A2
Source Impedance Low, Need Low Voltage Noise Performance	OP27, OP37 OP227 (Dual Matched) OP270 (Dual) OP271 OP470 OP471
Source Impedance High ($R_S \geq 15 \text{ k}\Omega$). Need Low Current Noise	OP80 OP41 OP43 OP249 OP97
Require Ultrahigh Input Impedance	OP80 OP97 OP41 OP43
Need Wider Bandwidth and High Speed	OP42 OP43 OP249

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

**8-Lead Plastic DIP
(N-8)**



**8-Lead SOIC
(SO-8)**



**8-Lead Metal Can
(H-08B)**

