# CY28RS480

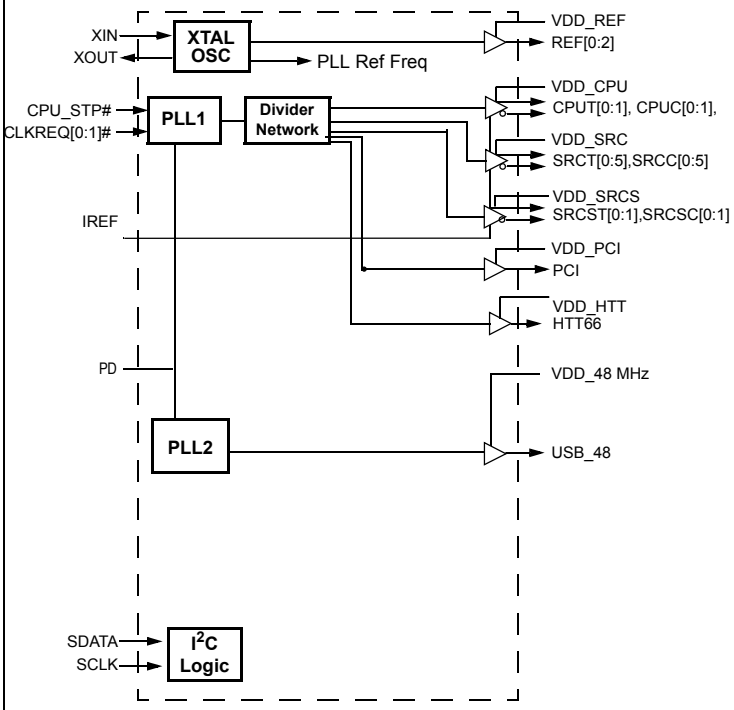
# Clock Generator for ATI® RS480 Chipset

## Features

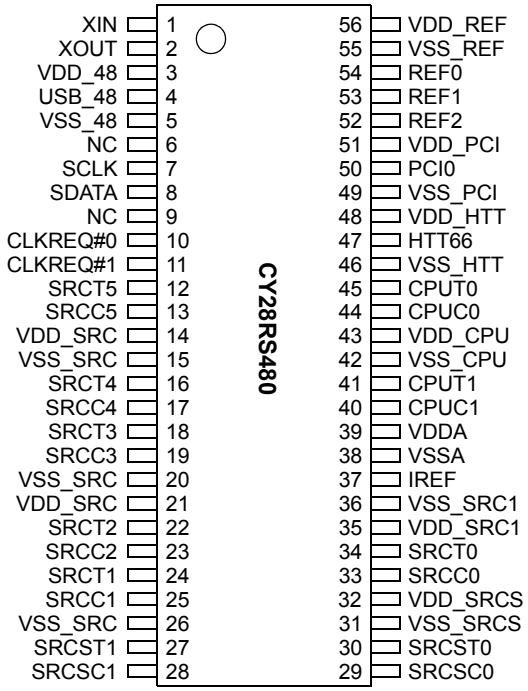
- **Supports AMD® CPU**
- **200-MHz differential CPU clock pairs**
- **100-MHz differential SRC clocks**
- **48-MHz USB clock**
- **33-MHz PCI clock**
- **66-MHz HyperTransport™ clock**
- **I²C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V power supply**
- **56-pin SSOP and TSSOP packages**

| CPU | SRC | HTT66 | PCI | REF | USB_48 |
|---|---|---|---|---|---|
| x2 | x8 | x1 | x1 | x 3 | x 1 |

## Block Diagram




## Pin Configuration




**56 SSOP/TSSOP**

## Pin Description

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 41,40,45,44 | CPUT/C | O, DIF | **Differential CPU clock outputs**. AMD K8 buffer (200 Mhz). |
| 50 | PCI0 | O | **33-MHz clock output**. |
| 37 | IREF | I | A precision resistor attached to this pin is connected to the internal current reference. |
| 52, 53, 54 | REF[2:0] | O, SE | **14.318-MHz REF clock output**. Intel® Type-5 buffer. |
| 7 | SCLK | I,PU | **SMBus-compatible SCLOCK**.This pin has an internal pull-up, but is tri-stated in power-down. |
| 8 | SDATA | I/O,PU | **SMBus-compatible SDATA**.This pin has an internal pull-up, but is tri-stated in power-down. |
| 27, 28, 30, 29 | SRCST/C[1:0] | O, DIF | **Differentials Selectable serial reference clock**. Intel Type-X buffer. Includes overclock support through SMBUS |
| 12, 13, 16, 17, 18, 19, 22, 23, 24, 25, 34, 33 | SRCT/C[5:0] | O, DIF | **100-MHz differential serial reference clock**. Intel Type-X buffer. |
| 10,11 | CLKREQ#[0:1] | I, SE, PD | **Output Enable control for SRCT/C**. Output enable control required by Minicard specification. This pin has an internal pull-down. 0 = Selected SRC outputs are enabled, 1 = Selected SRC outputs are disabled |
| 4 | USB_48 | O, SE | **48-MHz clock output**. Intel Type-3A buffer. |
| 47 | HTT66 | O, SE | **66-MHz clock output**. Intel Type-5 buffer. |
| 3 | VDD_48 | PWR | 3.3V power supply for USB outputs |
| 43 | VDD_CPU | PWR | 3.3V power supply for CPU outputs |
| 51 | VDD_PCI | PWR | 3.3V power supply for PCI outputs |
| 56 | VDD_REF | PWR | 3.3V power supply for REF outputs |
| 48 | VDD_HTT | PWR | 3.3V power supply for Hyper Transport outputs |
| 14, 21 | VDD_SRC | PWR | 3.3V power supply for SRC outputs |
| 35 | VDD_SRC1 | PWR | 3.3V power supply for SRC outputs |
| 32 | VDD_SRCS | PWR | 3.3V power supply for SRCS outputs |
| 39 | VDDA | PWR | 3.3V Analog Power for PLLs |
| 5 | VSS_48 | GND | Ground for USB outputs |
| 42 | VSS_CPU | GND | Ground for CPU outputs |
| 49 | VSS_PCI | GND | Ground for PCI outputs |
| 55 | VSS_REF | GND | Ground for REF outputs |
| 15, 20, 26 | VSS_SRC | GND | Ground for SRC outputs |
| 36 | VSS_SRC1 | GND | Ground for SRC outputs |
| 31 | VSS_SRCS | GND | Ground for SRCS outputs |
| 46 | VSS_HTT | GND | Ground for HyperTransport outputs |
| 38 | VSSA | GND | Analog Ground |
| 1 | XIN | I | 14.318-MHz Crystal Input |
| 2 | XOUT | O | 14.318-MHz Crystal Output |
| 6, 9 | NC | | No Connects |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

| Bit | Description |
|---|---|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:5) | Chip select address, set to ‘00’ to access device |
| (4:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address – 7 bits | 8:2 | Slave address – 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code – 8 bits | 18:11 | Command Code – 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address – 7 bits |
| 36:29 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2 – 8 bits | 37:30 | Byte Count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| .... | Data Byte /Slave Acknowledges | 46:39 | Data byte 1 from slave – 8 bits |
| .... | Data Byte N – 8 bits | 47 | Acknowledge |
| .... | Acknowledge from slave | 55:48 | Data byte 2 from slave – 8 bits |
| .... | Stop | 56 | Acknowledge |
| | | .... | Data bytes from slave / Acknowledge |
| | | .... | Data Byte N from slave – 8 bits |
| | | .... | NOT Acknowledge |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address – 7 bits | 8:2 | Slave address – 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |

**Table 3. Byte Read and Byte Write Protocol** (continued)

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 18:11 | Command Code – 8 bits | 18:11 | Command Code – 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte – 8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address – 7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave – 8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

## Control Registers

**Byte 0:Control Register 0**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | SRC[T/C]5 | SRC[T/C]5 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 6 | 1 | SRC[T/C]4 | SRC[T/C]4 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 5 | 1 | SRC[T/C]3 | SRC[T/C]3 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 4 | 1 | SRC[T/C]2 | SRC[T/C]2 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 3 | 1 | SRC[T/C]1 | SRC[T/C]1 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 2 | 1 | SRC [T/C]0 | SRC[T/C]0 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 1 | 1 | SRCS[T/C]1 | SRCS[T/C]1 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 0 | 1 | SRCS[T/C]0 | SRCS[T/C]0 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |

**Byte 1: Control Register 1**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | REF2 | REF2 Output Enable<br>0 = Disable, 1 = Enable |
| 6 | 1 | REF1 | REF1 Output Enable<br>0 = Disable, 1 = Enable |
| 5 | 1 | REF0 | REF0 Output Enable<br>0 = Disable, 1 = Enable |
| 4 | 1 | PCI0 | PCI0 Output Enable<br>0 = Disable, 1 = Enable |
| 3 | 1 | USB_48 | USB_48MHz Output Enable<br>0 = Disable, 1 = Enable |
| 2 | 1 | RESERVED | RESERVED |
| 1 | 1 | CPU[T/C]1 | CPU[T/C]1 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |
| 0 | 1 | CPU[T/C]0 | CPU[T/C]0 Output Enable<br>0 = Disable (Hi-Z), 1 = Enable |

**Byte 2: Control Register 2**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | CPUT/C<br>SRCT/C | Spread Spectrum Selection<br>'0' = –0.35%<br>'1' = –0.50% |
| 6 | 1 | USB_48 | 48-MHz Output Drive Strength<br>0 = 2x, 1 = 1x |
| 5 | 1 | PCI | 33-MHz Output Drive Strength<br>0 = 2x, 1 = 1x |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 0 | CPU<br>SRC | CPU/SRC Spread Spectrum Enable<br>0 = Spread off, 1 = Spread on |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Byte 3: Control Register 3**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | CLKREQ# | CLKREQ# drive mode<br>0 = SRC clocks driven when stopped, 1 = SRC clocks tri-state when stopped |
| 6 | 0 | CPU | CPU pd drive mode<br>0 = CPU clocks driven when power-down, 1 = CPU clocks tri-state |
| 5 | 1 | SRC | SRC pd drive mode<br>0 = SRC clocks driven when power-down, 1 = SRC clocks tri-state |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 1 | Reserved | Reserved |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | HTT66 | HTT66 Output Drive Strength0 = High drive, 1 = Low drive. |

**Byte 4: Control Register 4**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | SRC[T/C]5 | SRC[T/C]5 CLKREQ0 control<br>1 = SRC[T/C]5 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]5 free running |
| 6 | 0 | SRC[T/C]4 | SRC[T/C]4 CLKREQ#0 control<br>1 = SRC[T/C]4 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]4 free running |
| 5 | 0 | SRC[T/C]3 | SRC[T/C]3 CLKREQ#0 control<br>1 = SRC[T/C]3 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]3 free running |
| 4 | 0 | SRC[T/C]2 | SRC[T/C]2 CLKREQ#0 control<br>1 = SRC[T/C]2 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]2 free running |
| 3 | 0 | SRC[T/C]1 | SRC[T/C]1 CLKREQ#0 control<br>1 = SRC[T/C]1 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]1 free running |
| 2 | 0 | SRC[T/C]0 | SRC[T/C]0 CLKREQ#0 control<br>1 = SRC[T/C]1 stoppable by CLKREQ#0 pin<br>0 = SRC[T/C]1 free running |
| 1 | 1 | HTT66 | HTT66 Output enable<br>0 = Disabled, 1 = Enabled |

**Byte 4: Control Register 4** (continued)

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 0 | 1 | Reserved | Reserved |

**Byte 5: Control Register 5**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | SRC[T/C]5 | SRC[T/C]5 CLKREQ#1 control<br>1 = SRC[T/C]5 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]5 free running |
| 6 | 0 | SRC[T/C]4 | SRC[T/C]4 CLKREQ#1 control<br>1 = SRC[T/C]4 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]4 free running |
| 5 | 0 | SRC[T/C]3 | SRC[T/C]3 CLKREQ#1 control<br>1 = SRC[T/C]3 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]3 free running |
| 4 | 0 | SRC[T/C]2 | SRC[T/C]2 CLKREQ#1 control<br>1 = SRC[T/C]2 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]2 free running |
| 3 | 0 | SRC[T/C]1 | SRC[T/C]1 CLKREQ#1 control<br>1 = SRC[T/C]1 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]1 free running |
| 2 | 0 | SRC[T/C]0 | SRC[T/C]0 CLKREQ#1 control<br>1 = SRC[T/C]1 stoppable by CLKREQ#1 pin<br>0 = SRC[T/C]1 free running |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Byte 6: Control Register 6**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | TEST_SEL | REF/N or Three-state Select<br>1 = REF/N Clock, 0 = Three-state |
| 6 | 0 | TEST_MODE | Test Clock Mode Entry Control<br>1 = REF/N or Tri-state mode, 0 = Normal operation |
| 5 | 0 | REF | REF Output drive strength<br>0 = Low drive, 1 = High drive |
| 4 | 1 | Reserved | Reserved |
| 3 | HW | Reserved | Reserved |
| 2 | HW | Reserved | Reserved |
| 1 | HW | Reserved | Reserved |
| 0 | HW | Reserved | Reserved |

**Byte 7: Vendor ID**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | | Revision Code Bit 3 |
| 6 | 0 | | Revision Code Bit 2 |
| 5 | 0 | | Revision Code Bit 1 |
| 4 | 1 | | Revision Code Bit 0 |
| 3 | 1 | | Vendor ID Bit 3 |
| 2 | 0 | | Vendor ID Bit 2 |
| 1 | 0 | | Vendor ID Bit 1 |
| 0 | 0 | | Vendor ID Bit 0 |

**Table 4. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|---|---|---|---|---|---|---|---|---|---|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

## Crystal Recommendations

The CY28RS480 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28RS480 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

## Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

*Figure 1* shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

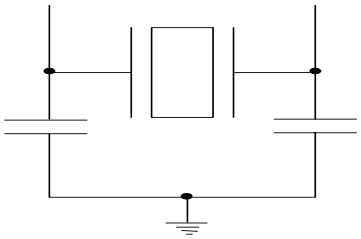


**Figure 1. Crystal Capacitive Clarification**

## Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

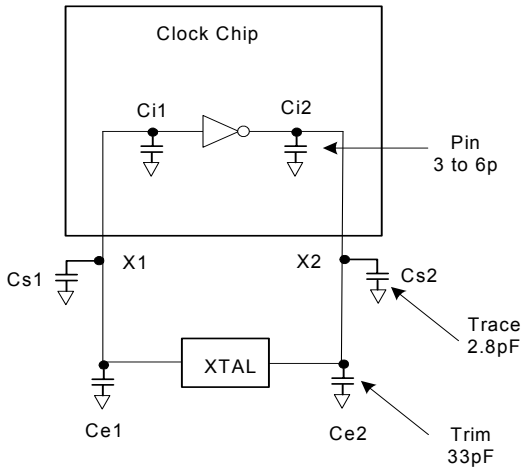



**Figure 2. Crystal Loading Example**

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

**Load Capacitance (each side)**

$$Ce = 2 * CL - (Cs + Ci)$$

**Total Capacitance (as seen by the crystal)**

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .....Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs .....Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

CL .....Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs .....Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

### CLK_REQ[0:1]# Description

The CLKREQ#[1:0] signals are active low input used for clean stopping and starting selected SRC outputs. The outputs controlled by CLKREQ#[1:0] are determined by the settings in register bytes 4 and 5. The CLKREQ# signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

### CLK_REQ[0:1]# Deassertion [Low to High Transition]

The impact of deasserting the CLKREQ#[1:0] pins is all DIF outputs that are set in the control registers to stoppable via assertion of CLKREQ#[1:0] are to be stopped after their next transition. When the control register CLKREQ# drive mode bit is programmed to ‘0’, the final state of all stopped SRC signals is SRCT clock = High and SRCC = Low. There is to be no change to the output drive current values, SRCT will be driven high with a current value equal 6 x Iref,. When the control register CLKREQ# drive mode bit is programmed to ‘1’, the final state of all stopped DIF signals is low, both SRCT clock and SRCC clock outputs will not be driven.

### CLK_REQ[0:1]# Assertion [High to Low Transition]

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the Assertion to active outputs is between 2–6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. If the CLKREQ# drive mode bit is programmed to ‘1’ three-state), the all stopped SRC outputs must be driven high within 10 ns of CLKREQ#[1:0] Assertion to a voltage greater than 200 mV.

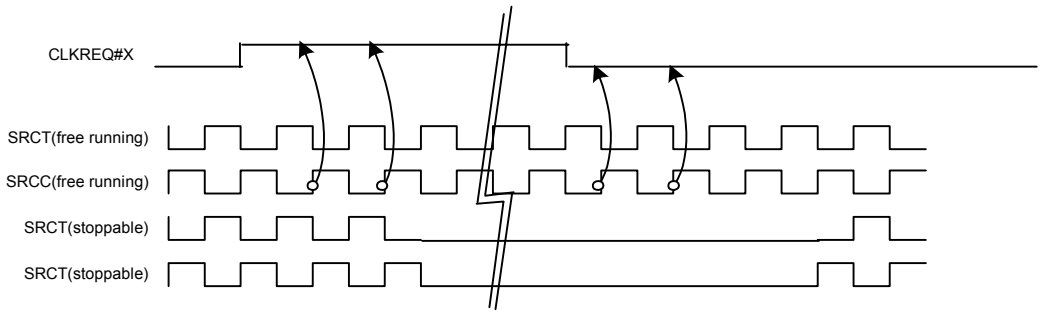



**Figure 3. CLK_REQ#[0:1] Assertion/Deassertion Waveform**

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | –0.5 | 4.6 | V |
| $V_{DDA}$ | Analog Supply Voltage | | –0.5 | 4.6 | V |
| $V_{IN}$ | Input Voltage | Relative to $V_{SS}$ | –0.5 | $V_{DD}$+0.5 | VDC |
| $T_S$ | Temperature, Storage | Non-functional | –65 | +150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | 70 | °C |
| $T_J$ | Temperature, Junction | Functional | – | 150 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| $Ø_{JC}$ | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | – | 20 | °C/W |
| $Ø_{JA}$ | Dissipation, Junction to Ambient | JEDEC (JESD 51) | – | 60 | °C/W |
| UL-94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |
| **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required. | | | | | |

## DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VDD_REF, VDD_CPU, VDD_PCI, VDD_SRC, VDD_SRC1, VDD_SRCS VDD_48 | 3.3V Operating Voltage | 3.3V ± 5% | 3.135 | 3.465 | V |
| $V_{ILSMBUS}$ | Input Low Voltage | SDATA, SCLK | – | 1.0 | V |
| $V_{IHSMBUS}$ | Input High Voltage | SDATA, SCLK | 2.2 | - | V |
| $V_{IL}$ | Input Low Voltage | VDD | $V_{SS}$–0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{DD}$+0.3 | V |
| $I_{IL}$ | Input Leakage Current | Except pull-ups or pull-downs $0<V_{IN}<V_{DD}$ | –5 | 5 | mA |
| $V_{OL}$ | Output Low Voltage | IOL = 1 mA | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | IOH = 1 mA | 2.4 | – | V |
| $I_{OZ}$ | High-Impedance Output Current | | –10 | 10 | µA |
| $C_{IN}$ | Input Pin Capacitance | | 3 | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | 3 | 5 | pF |
| $L_{IN}$ | Pin Inductance | | – | 7 | nH |
| $V_{XIH}$ | Xin High Voltage | | $0.7*V_{DD}$ | $V_{DD}$ | V |
| $V_{XIL}$ | Xin Low Voltage | | 0 | $0.3*V_{DD}$ | V |
| $I_{DD}$ | Dynamic Supply Current | At max load and frequency | – | 450 | mA |
| $IPD_D$ | Power Down Supply Current | PD asserted, Outputs driven | – | 75 | mA |
| $IPD_T$ | Power Down Supply Current | PD asserted, Outputs Hi-Z | – | 12 | mA |

## AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **Crystal** | | | | | |
| $T_{DC}$ | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| $T_{PERIOD}$ | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |

## AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $T_R$ / $T_F$ | XIN Rise and Fall Times | Measured between $0.3V_{DD}$ and $0.7V_{DD}$ | – | 10.0 | ns |
| $T_{CCJ}$ | XIN Cycle to Cycle Jitter | As an average over 1-μs duration | – | 500 | ps |
| $L_{ACC}$ | Long-term Accuracy | Over 150 ms | – | 300 | ppm |
| **CPU Outputs** | | | | | |
| TR/TF | Output Slew Rate | Measured @ test load using VOCM ±400 mV, 0.85 to 1.65 | 2 | 7 | V/ns |
| $V_{DIFF}$ | Differential Voltage | Measured at load single ended | 0.4 | 2.3 | V |
| TSKEW | Any CPU to CPU Clock Skew | Measured at crossing point $V_{OX}$ | – | 250 | ps |
| _ $V_{DIFF}$ | Change in VDIFF_DC Magnitude | Measured at load single ended | –150 | 150 | mV |
| $V_{CM}$ | Common Mode Voltage | Measured at load single ended | 1.05 | 1.45 | V |
| _ $V_{CM}$ | Change in $V_{CM}$ | Measured at load single ended | –200 | 200 | mV |
| $T_{DC}$ | Duty Cycle | Measured at $V_{OX}$ | 45 | 55 | % |
| $T_{JCYC}$ | Cycle to Cycle Jitter | Measured at $V_{OX}$ | 0 | 200 | ps |
| **SRC** | | | | | |
| $T_{DC}$ | SRCT and SRCC Duty Cycle | Measured at crossing point $V_{OX}$ | 45 | 55 | % |
| $T_{PERIOD}$ | 100-MHz SRCT and SRCC Period | Measured at crossing point $V_{OX}$ | 9.997001 | 10.00300 | ns |
| $T_{PERIODSS}$ | 100-MHz SRCT and SRCC Period, SSC | Measured at crossing point $V_{OX}$ | 9.997001 | 10.05327 | ns |
| $T_{PERIODAbs}$ | 100-MHz SRCT and SRCC Absolute Period | Measured at crossing point $V_{OX}$ | 10.12800 | 9.872001 | ns |
| $T_{PERIODSSAbs}$ | 100-MHz SRCT and SRCC Absolute Period, SSC | Measured at crossing point $V_{OX}$ | 9.872001 | 10.17827 | ns |
| $T_{SKEW}$ | Any SRCT/C to SRCT/C Clock Skew | Measured at crossing point $V_{OX}$ | – | 250 | ps |
| TSKEW | Any SRCS clock to Any SRCS clock Skew | Measured at crossing point $V_{OX}$ | – | 250 | ps |
| $T_{CCJ}$ | SRCT/C Cycle to Cycle Jitter | Measured at crossing point $V_{OX}$ | – | 125 | ps |
| $L_{ACC}$ | SRCT/C Long Term Accuracy | Measured at crossing point $V_{OX}$ | – | 300 | ppm |
| $T_R$ / $T_F$ | SRCT and SRCC Rise and Fall Times | Measured from $V_{OL}$ = 0.175 to $V_{OH}$ = 0.525V | 175 | 700 | ps |
| $T_{RFM}$ | Rise/Fall Matching | Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$ | – | 20 | % |
| $\Delta T_R$ | Rise TimeVariation | | – | 125 | ps |
| $\Delta T_F$ | Fall Time Variation | | – | 125 | ps |
| $V_{HIGH}$ | Voltage High | Math averages *Figure 5* | 660 | 850 | mv |
| $V_{LOW}$ | Voltage Low | Math averages *Figure 5* | –150 | – | mv |
| $V_{OX}$ | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| $V_{OVS}$ | Maximum Overshoot Voltage | | – | $V_{HIGH}$ + 0.3 | V |
| $V_{UDS}$ | Minimum Undershoot Voltage | | –0.3 | – | V |
| $V_{RB}$ | Ring Back Voltage | See *Figure 5.* Measure SE | – | 0.2 | V |
| **HTT66 HyperTransport Output** | | | | | |
| F66 | Operating Frequency | | – | 66.67 | MHz |
| TDC | Duty Cycle | Measured at 1.5V | 45 | 55 | % |
| TR/TF | Slew Rate | Measured at 20% and 60% | 0.9 | 6.5 | V/ns |
| TCCJ | Cycle to Cycle jitter | Measured at 1.5V | – | 450 | ps |
| TSKEW | HTT66 clock to PCI clock Skew | Measurement at 1.5V | – | 500 | ps |

## AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **PCI** | | | | | |
| $T_{DC}$ | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Spread Disabled PCI Period | Measurement at 1.5V | 29.99100 | 30.00900 | ns |
| $T_{PERIODSS}$ | Spread Enabled PCI Period, SSC | Measurement at 1.5V | 29.9910 | 30.15980 | ns |
| $T_{PERIODAbs}$ | Spread Disabled PCI Period | Measurement at 1.5V | 29.49100 | 30.50900 | ns |
| $T_{PERIODSSAbs}$ | Spread Enabled PCI Period, SSC | Measurement at 1.5V | 29.49100 | 30.65980 | ns |
| $T_{HIGH}$ | PCI high time | Measurement at 2.4V | 12.0 | – | ns |
| $T_{LOW}$ | PCI low time | Measurement at 0.4V | 12.0 | – | ns |
| $T_R$ / $T_F$ | PCI rise and fall times | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| $T_{CCJ}$ | PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 500 | ps |
| **USB** | | | | | |
| $T_{DC}$ | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Period | Measurement at 1.5V | 20.83125 | 20.83542 | ns |
| $T_{PERIODAbs}$ | Absolute Period | Measurement at 1.5V | 20.48125 | 21.18542 | ns |
| $T_{HIGH}$ | USB high time | Measurement at 2.4V | 8.094 | 10.036 | ns |
| $T_{LOW}$ | USB low time | Measurement at 0.4V | 7.694 | 9.836 | ns |
| $T_R$ / $T_F$ | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | V/ns |
| $T_{CCJ}$ | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| $T_{LTJ}$ | Long Term Jitter | Measurement at 1.5V@1 us | – | TBD | ps |
| **REF** | | | | | |
| $T_{DC}$ | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | REF Period | Measurement at 1.5V | 69.8203 | 69.8622 | ns |
| $T_{PERIODAbs}$ | REF Absolute Period | Measurement at 1.5V | 68.82033 | 70.86224 | ns |
| $T_R$ / $T_F$ | REF Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| $T_{CCJ}$ | REF Cycle to Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| **ENABLE/DISABLE and SET-UP** | | | | | |
| $T_{STABLE}$ | Clock Stabilization from Power-up | | – | 1.8 | ms |
| $T_{SS}$ | Stopclock Set-up Time | | 10.0 | – | ns |
| $T_{SH}$ | Stopclock Hold Time | | 0 | – | ns |

## Test and Measurement Set-up

### For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

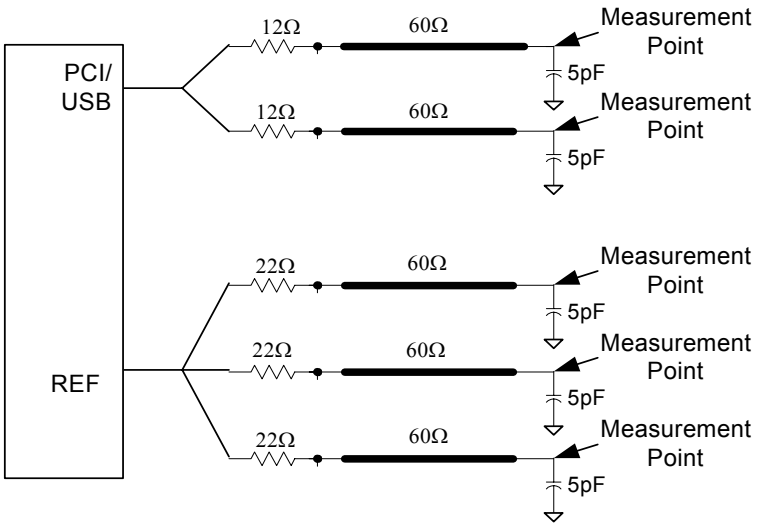



**Figure 4. Single-ended Load Configuration**

### For Differential CPU and SRC Output Signals

The following diagram shows the test load configuration for the differential SRC outputs.

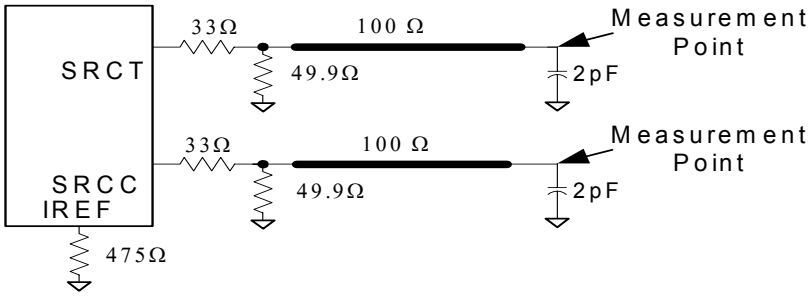



**Figure 5. 0.7V Load Configuration**

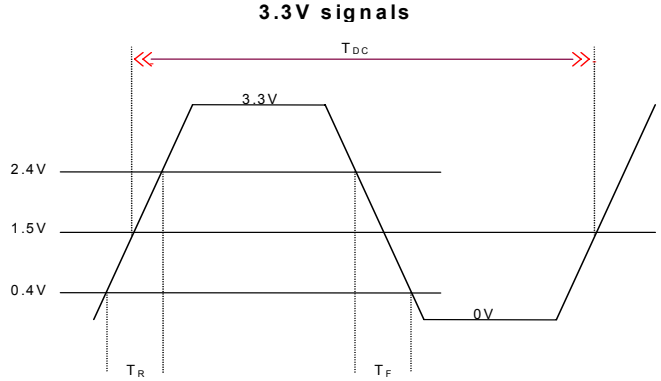



**Figure 6. Single-ended Output Signals (for AC Parameters Measurement)**

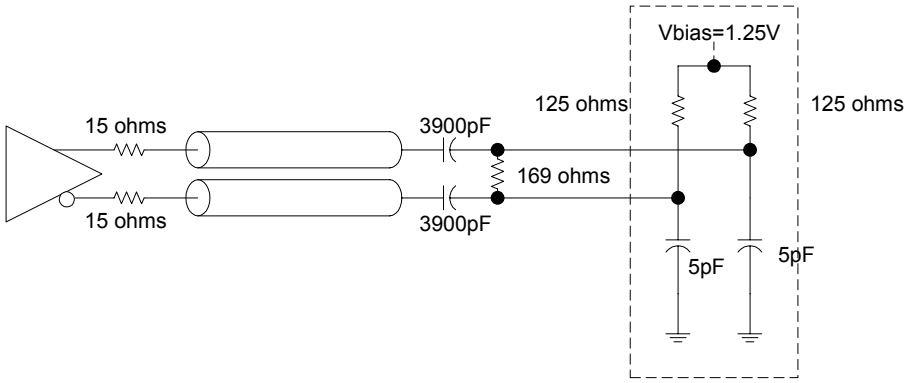


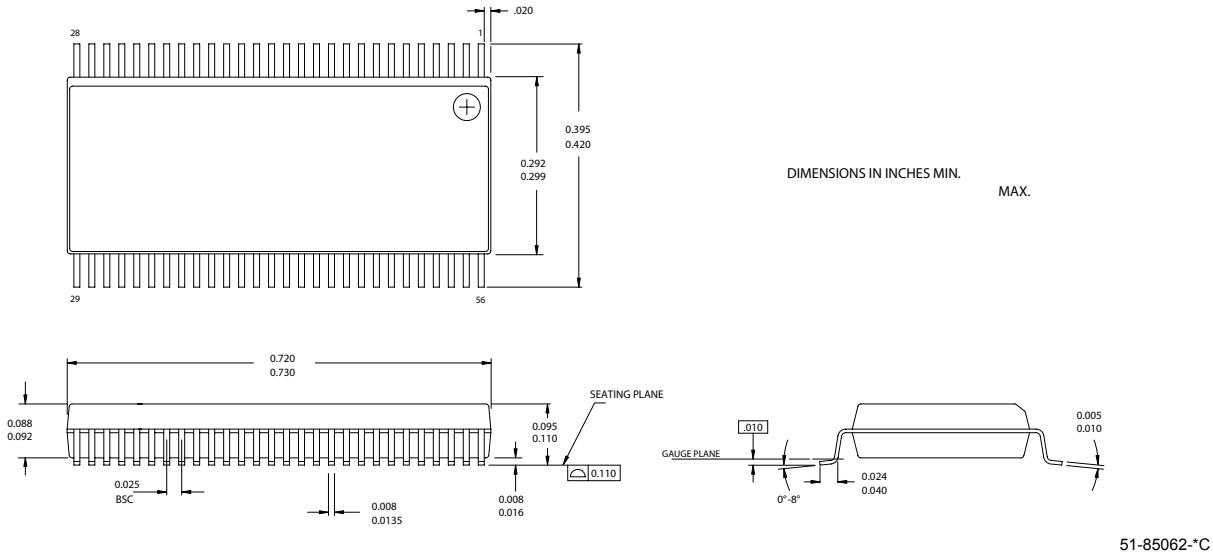

**Figure 7. CPU Output Load Configuration**

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| **Lead-free** | | |
| CY28RS480OXC | 56-pin SSOP | Commercial, 0° to 70°C |
| CY28RS480OXCT | 56-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |
| CY28RS480ZXC | 56-pin TSSOP | Commercial, 0° to 70°C |
| CY28RS480ZXCT | 56-pin TSSOP – Tape and Reel | Commercial, 0° to 70°C |

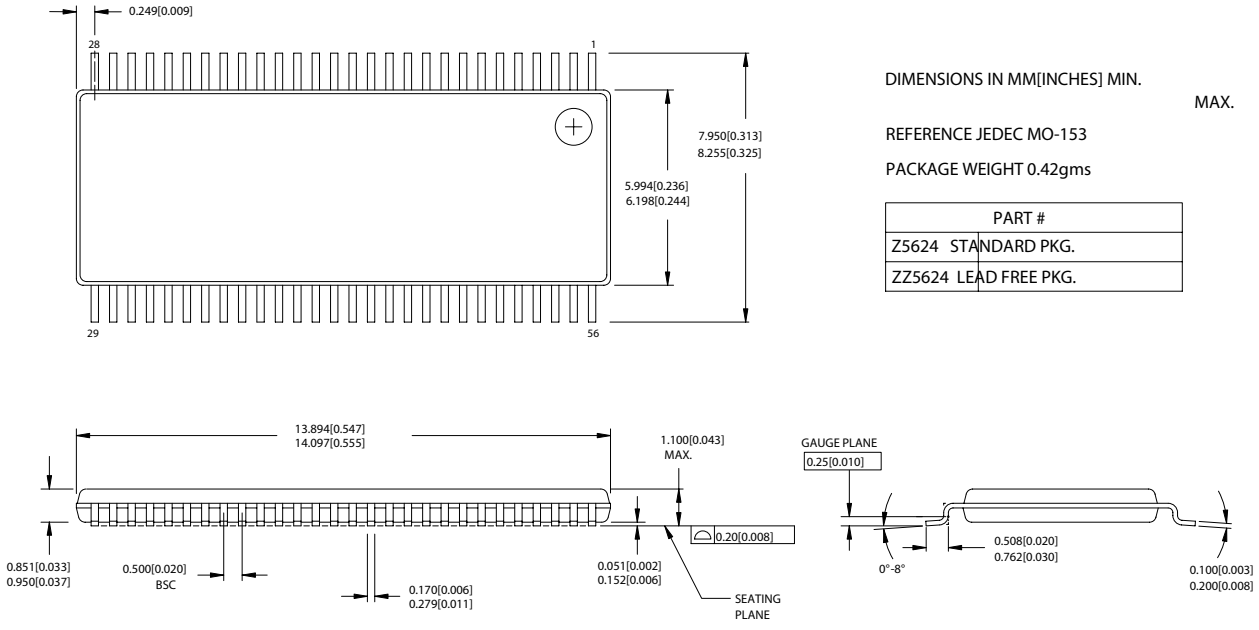
## Package Drawing and Dimensions

**56-Lead Shrunk Small Outline Package O56**



## Package Drawing and Dimensions (continued)

**56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56**




DIMENSIONS IN MM[INCHES] MIN.

MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.42gms

| PART # |
|---|
| Z5624 STANDARD PKG. |
| ZZ5624 LEAD FREE PKG. |

51-85060-*C

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## Document History Page

| Document Title: CY28RS480 Clock Generator for ATI® RS480 Chipset<br>Document Number: 38-07638 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 204582 | See ECN | RGL | New data sheet |
| *A | 215828 | See ECN | RGL | Minor change: posted to external web site |
| *B | 267850 | See ECN | RGL | Changed pins 10 and 11 from internal Pull up to Pull down<br>Changed polarity of CLKREQ#<br>Added register byte 3 bits [1:3] for CPU Stop control<br>Changed the Slew rate to max of 6.5V/ns<br>Changed the IDD max load from 400 to 450 mA<br>Changed the IPD Outputs Driven from 70 to 75 mA<br>Changed the CPU Duty Cycle from 45 to 53 to 45 to 55%<br>Changed the HTT66 Cycle to cycle jitter from 300 to 450 ps<br>Fixed the Single-ended loading diagram |
| *C | 325360 | See ECN | RGL | Fixed the ordering information table to match the parts in the DevMaster |