

General Description

The AO4830 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

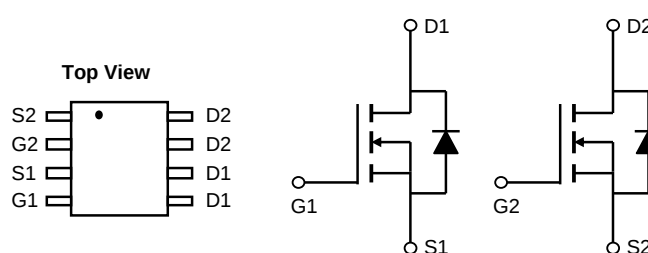
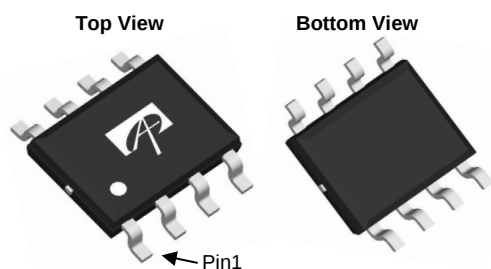
Product Summary

V_{DS} (V) = 80V
 I_D = 3.5A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 75m Ω (V_{GS} = 10V)

100% UIS Tested
100% Rg Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	3.5	A
$T_A=25^\circ\text{C}$		2.9	
Pulsed Drain Current ^C	I_{DM}	18	A
Avalanche Current ^C	I_{AR}	16	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	12.8	mJ
Power Dissipation ^B	P_D	2	W
$T_A=25^\circ\text{C}$		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		74	90	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±30V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	3.5	4.2	5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	18			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.5A T _J =125°C		62 113.0	75 135	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3.5A		15		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
I _{SM}	Pulsed Body-diode Current ^C				18	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz	510	640	770	pF
C _{oss}	Output Capacitance		28	40	52	pF
C _{rss}	Reverse Transfer Capacitance		12	20	30	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =40V, I _D =3.5A	8	11	13	nC
Q _{g(4.5V)}	Total Gate Charge		4	5.5	7	
Q _{gs}	Gate Source Charge		4	5	6	nC
Q _{gd}	Gate Drain Charge		0.7	1.2	1.7	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =40V, R _L =8Ω, R _{GEN} =3Ω		7.2		ns
t _r	Turn-On Rise Time			2.2		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =3.5A, dI/dt=300A/μs	14	20	26	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.5A, dI/dt=300A/μs	35	50	65	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

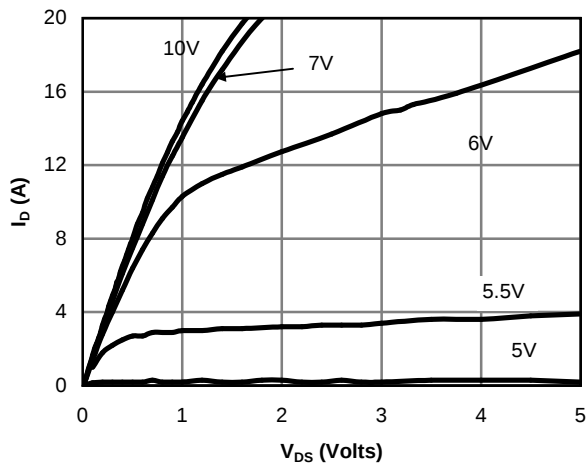


Fig 1: On-Region Characteristics (Note E)

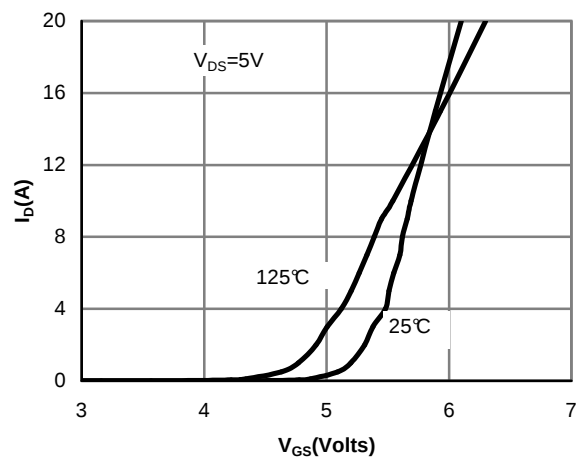


Figure 2: Transfer Characteristics (Note E)

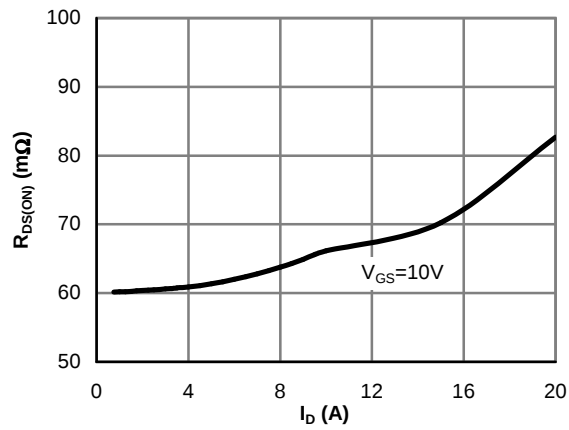


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

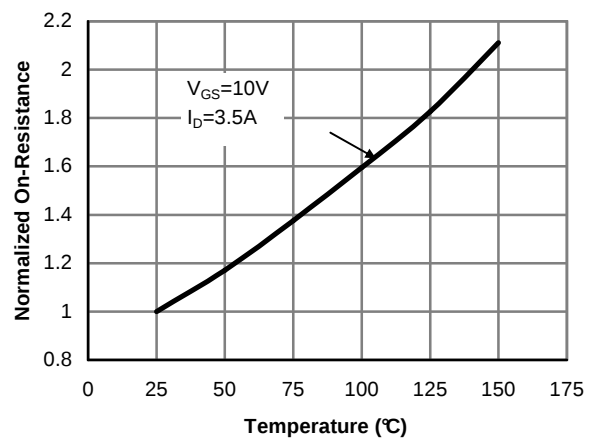


Figure 4: On-Resistance vs. Junction Temperature (Note E)

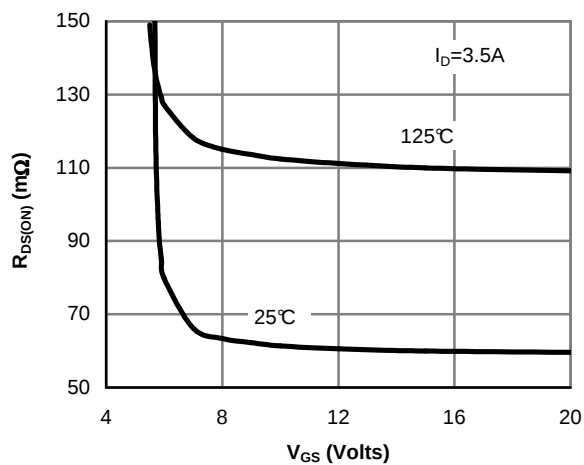


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

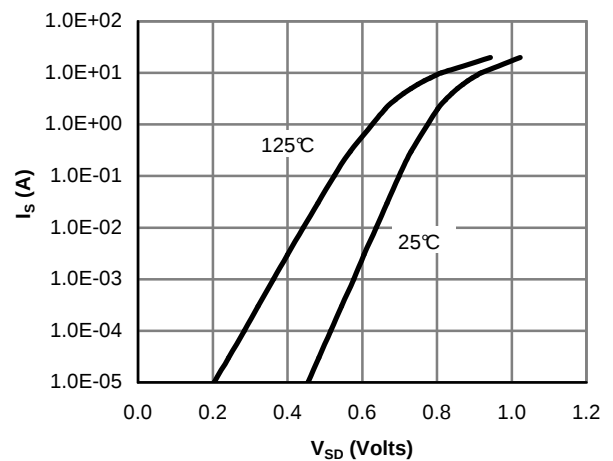


Figure 6: Body-Diode Characteristics (Note E)

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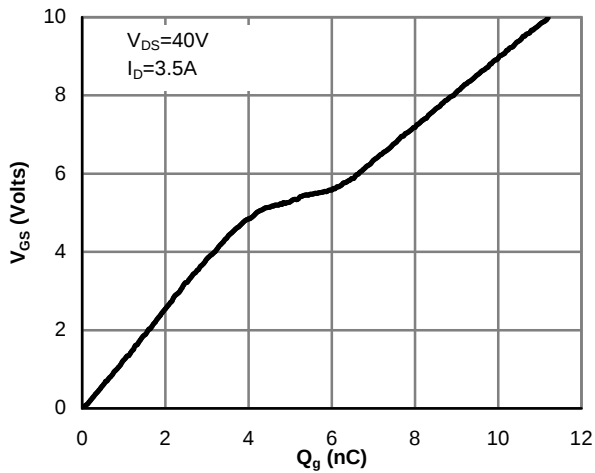


Figure 7: Gate-Charge Characteristics

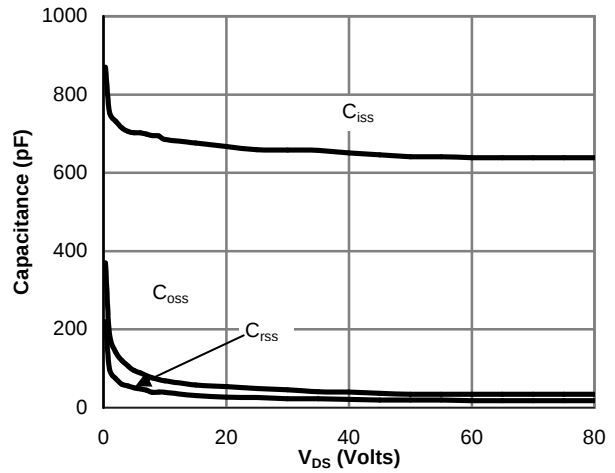


Figure 8: Capacitance Characteristics

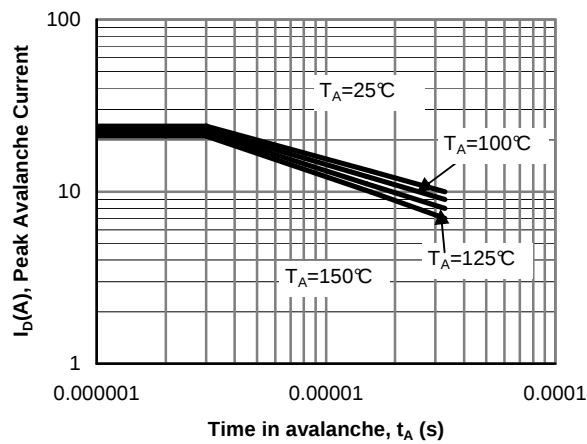


Figure 12: Single Pulse Avalanche capability

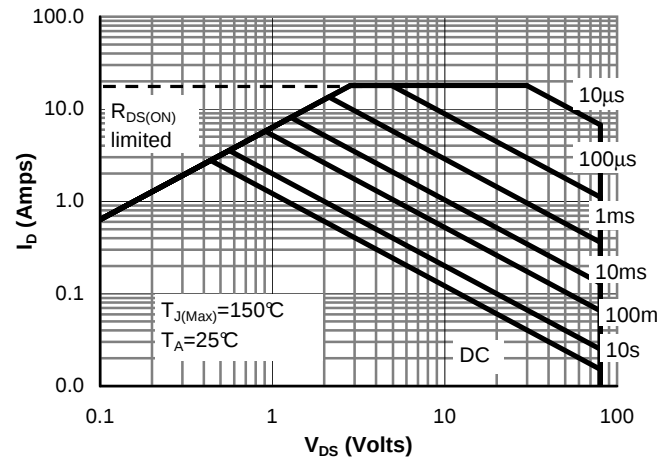


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

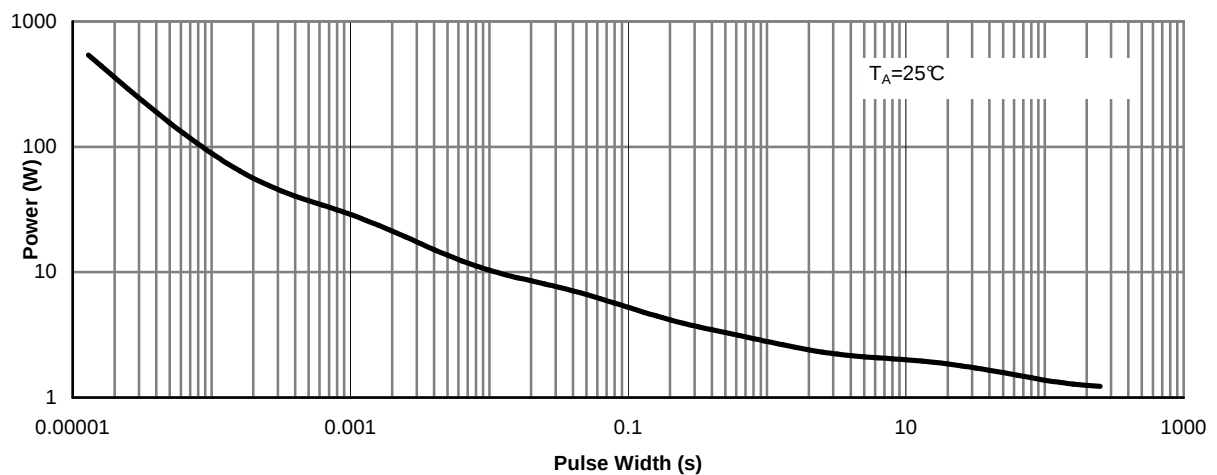


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

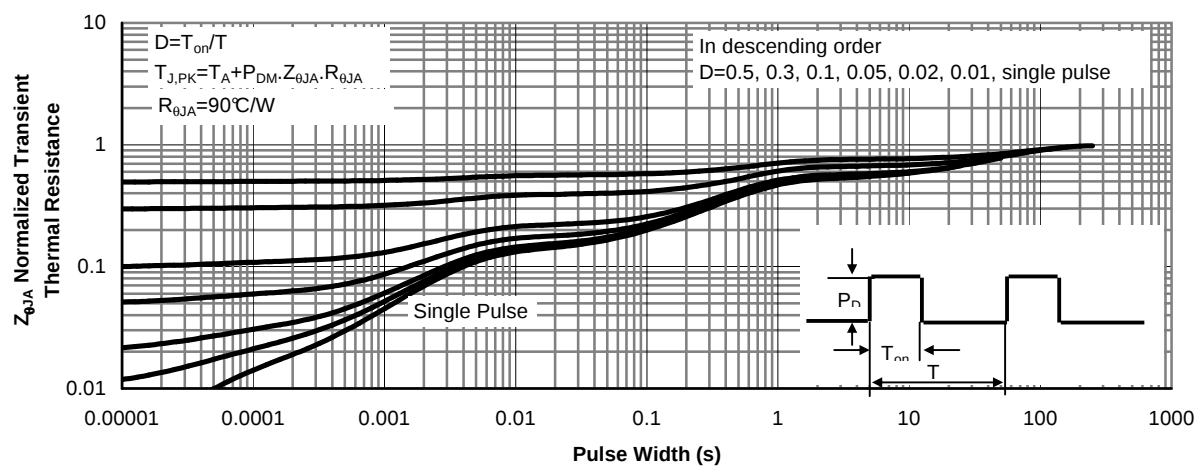
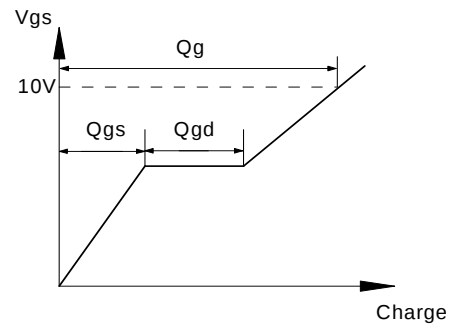
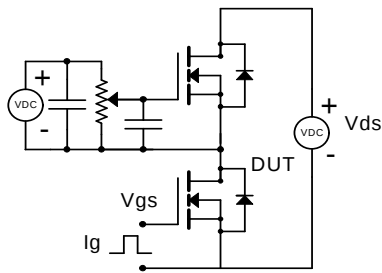
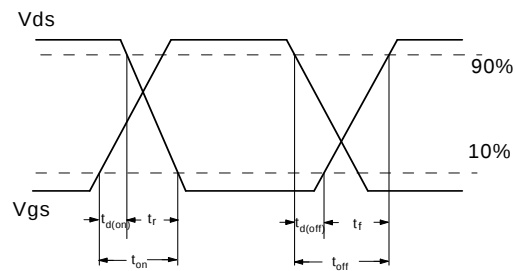
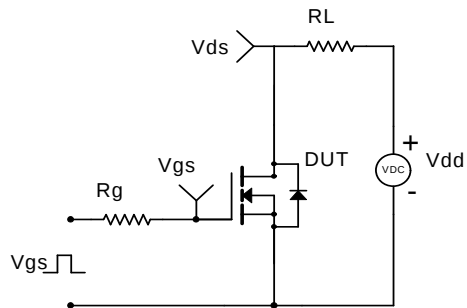


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

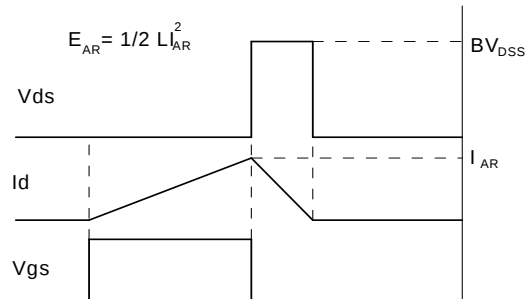
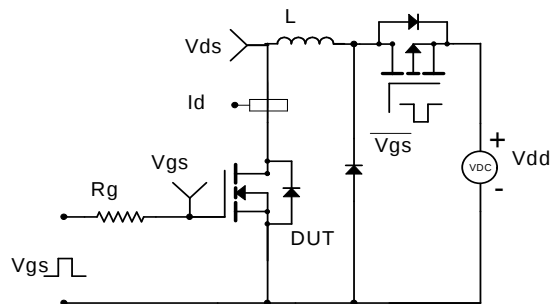
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

