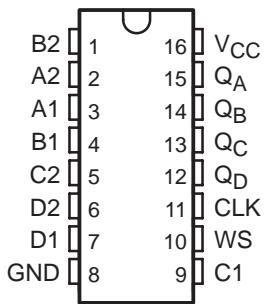


- Selects One of Two 4-Bit Data Sources and Synchronously Stores Data With System Clock
- Applications:
 - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
 - Implements Separate Registers Capable of Parallel Exchange of Contents, Yet Retains External Load Capability
 - Has Universal-Type Register for Implementing Various Shift Patterns, Including Compound Left-Right Capability
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

D OR N PACKAGE
(TOP VIEW)



description

The SN74AS298A is a quadruple 2-input multiplexer with storage that provides essentially the equivalent functional capabilities of two separate MSI functions (SN74AS157 and 'AS175A) in a 16-pin package.

When the word-select (WS) input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to WS causes the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

The SN74AS298A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | OUTPUTS [†] | | | |
|--------|-----|----------------------|-----------------|-----------------|-----------------|
| WS | CLK | Q _A | Q _B | Q _C | Q _D |
| L | ↓ | a1 | b1 | c1 | d1 |
| H | ↓ | a2 | b2 | c2 | d2 |
| X | H | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |

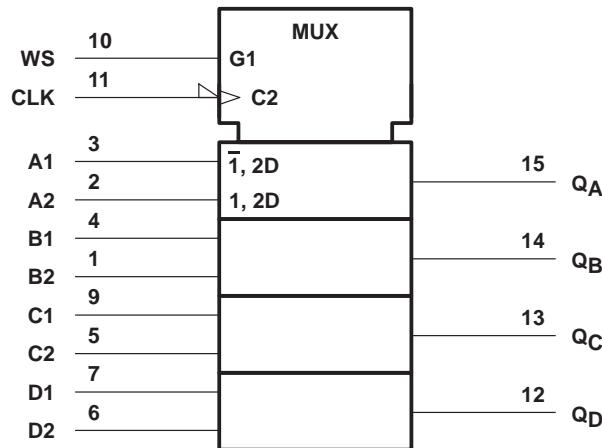
[†] a1, a2, etc. = the level of steady-state input at A1, A2, etc.

Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of CLK

SN74AS298A
QUADRUPLE 2-INPUT MULTIPLEXER
WITH STORAGE

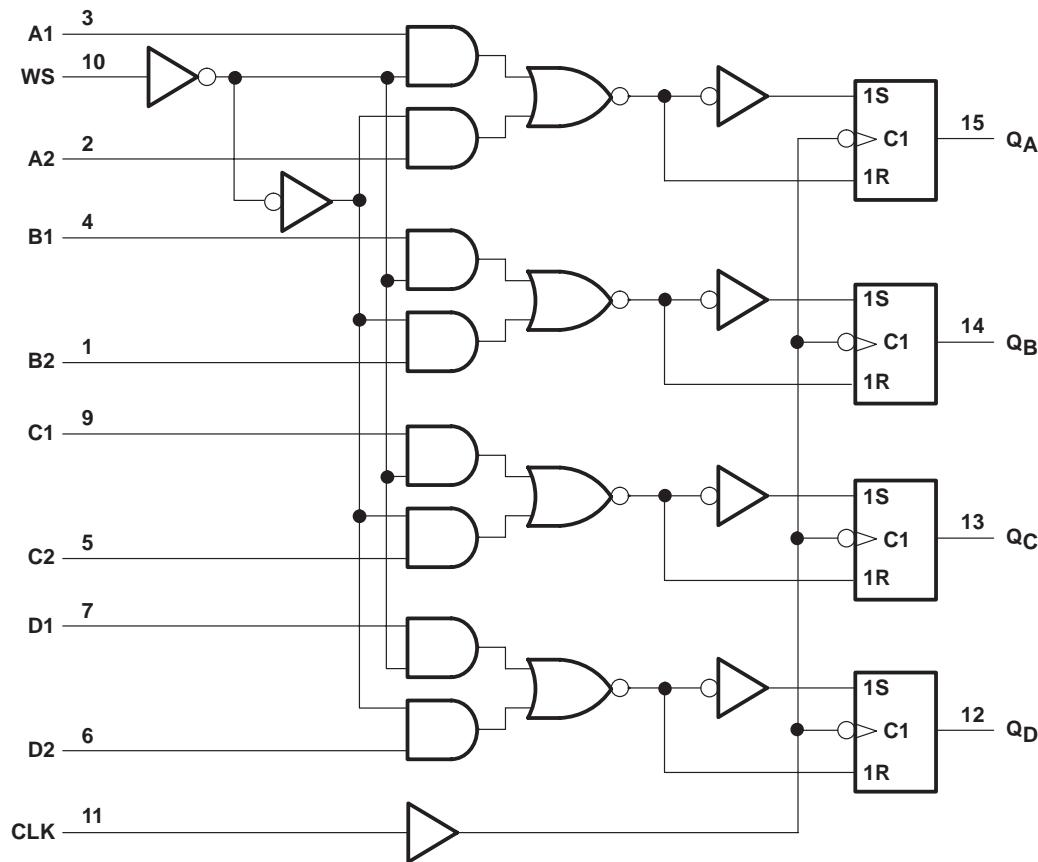
SDAS219B - DECEMBER 1983 - REVISED DECEMBER 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range | 65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | -2 | mA |
| I_{OL} | Low-level output current | | | 20 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP [‡] | MAX | UNIT |
|-----------|---|---------------------------------|------------------|------|------|
| V_{IK} | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5$ V, $I_{OL} = 20$ mA | 0.35 | 0.5 | | V |
| I_I | $V_{CC} = 5.5$ V, $V_I = 7$ V | | 0.1 | | mA |
| I_{IH} | WS | | 40 | | |
| | All others | $V_{CC} = 5.5$ V, $V_I = 2.7$ V | 20 | | μA |
| I_{IL} | WS | | -0.75 | | |
| | All others | $V_{CC} = 5.5$ V, $V_I = 0.4$ V | -0.5 | | mA |
| $I_O^§$ | $V_{CC} = 5.5$ V, $V_O = 2.25$ V | -30 | -112 | | mA |
| I_{CCH} | $V_{CC} = 5.5$ V | | 21 | 33 | mA |
| I_{CCL} | $V_{CC} = 5.5$ V | | 22 | 36 | mA |

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------|---------------------------------|------|-----|------|
| f_{clock} | Clock frequency | 0 | 62 | MHz |
| t_w | Pulse duration, CLK high or low | 8 | | ns |
| t_{su} | Setup time before CLK↓ | Data | 4.5 | ns |
| | | WS | 13 | |
| t_h | Hold time after CLK↓ | Data | 3.5 | ns |
| | | WS | 1 | |

SN74AS298A

QUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE

SDAS219B - DECEMBER 1983 - REVISED DECEMBER 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|------------------|-----------------|----------------|-----|-----|------|
| f_{max} | | | 62 | | MHz |
| t_{PLH} | CLK | Q | 2 | 9 | ns |
| t_{PHL} | | | 1 | 11 | |

APPLICATION INFORMATION

This versatile multiplexer can be connected to operate as a shift register that can shift n places in a single clock pulse.

Figure 1 illustrates a BCD shift register that shifts an entire 4-bit BCD digit in one clock pulse.

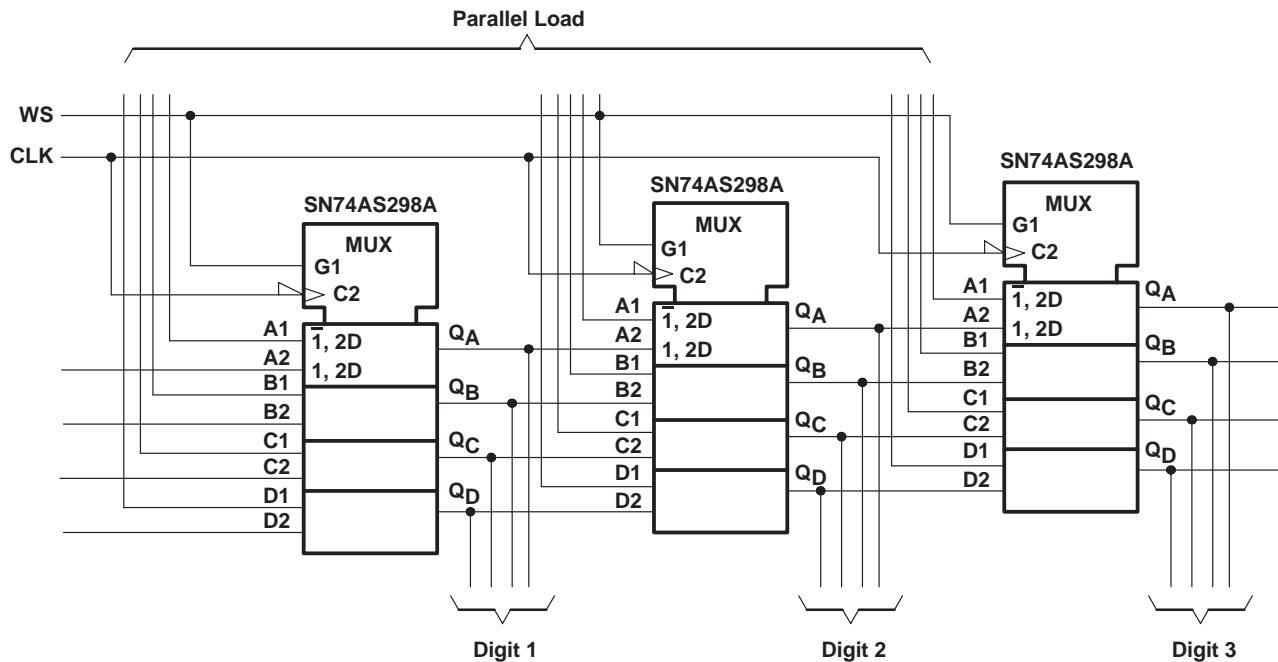


Figure 1. BCD Shift Register

When WS is high and the registers are clocked, the content of register 1 is transferred (shifted) to register 2, etc., effectively shifting the BCD digits one position. This application also retains a parallel-load capability, which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented is a register designed specifically for supporting multiplier or division operations (see Figure 2).

When WS is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When WS is high and the registers are clocked, the data is shifted two places.

APPLICATION INFORMATION

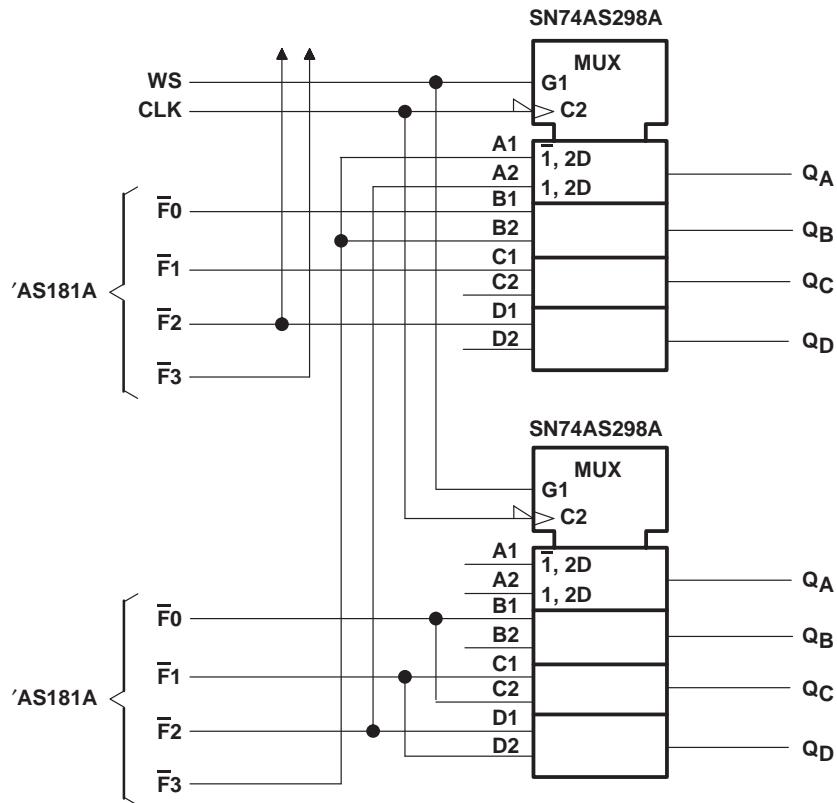


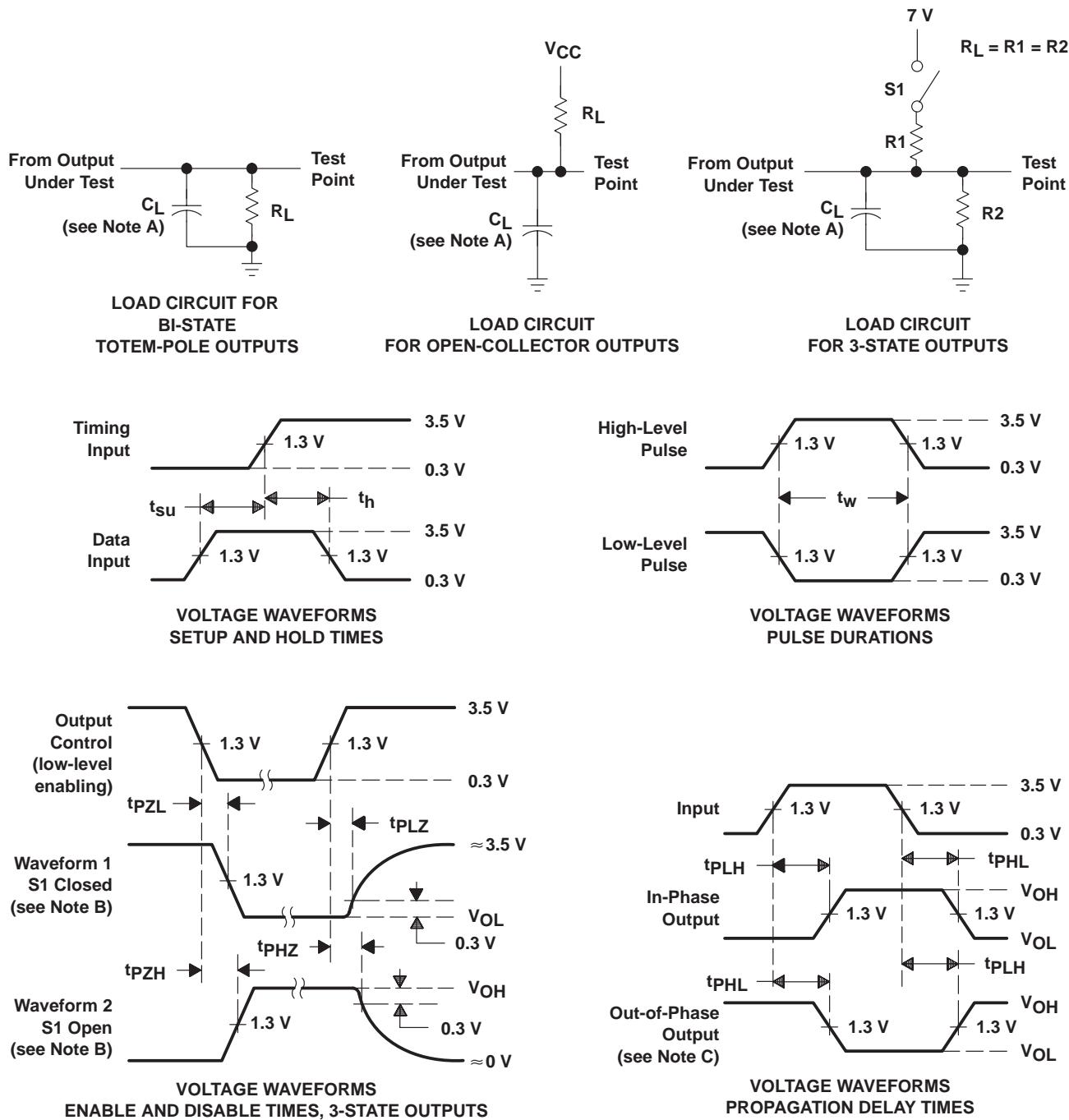
Figure 2. 1-Place/2-Place Shift Register

SN74AS298A

QUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE

SDAS219B - DECEMBER 1983 - REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AS298AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AS298ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AS298ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AS298AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74AS298ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74AS298ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AS298ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AS298ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

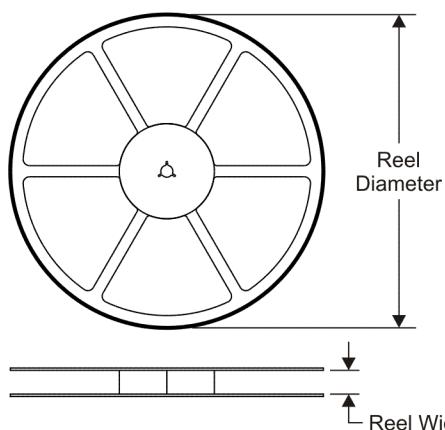
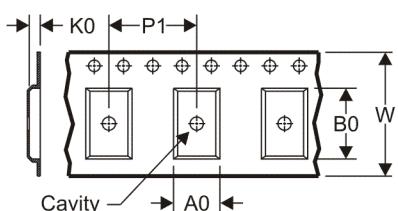
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

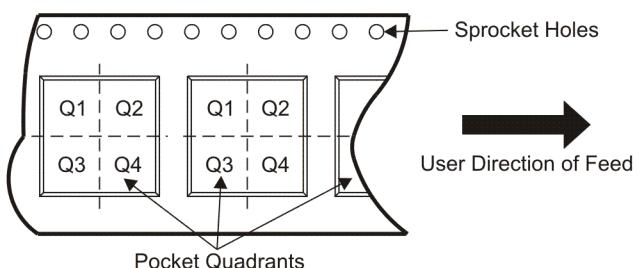
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|-------|---|
| A_0 | Dimension designed to accommodate the component width |
| B_0 | Dimension designed to accommodate the component length |
| K_0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P_1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A_0 (mm) | B_0 (mm) | K_0 (mm) | P_1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|------------|------------|------------|------------|----------|---------------|
| SN74AS298ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

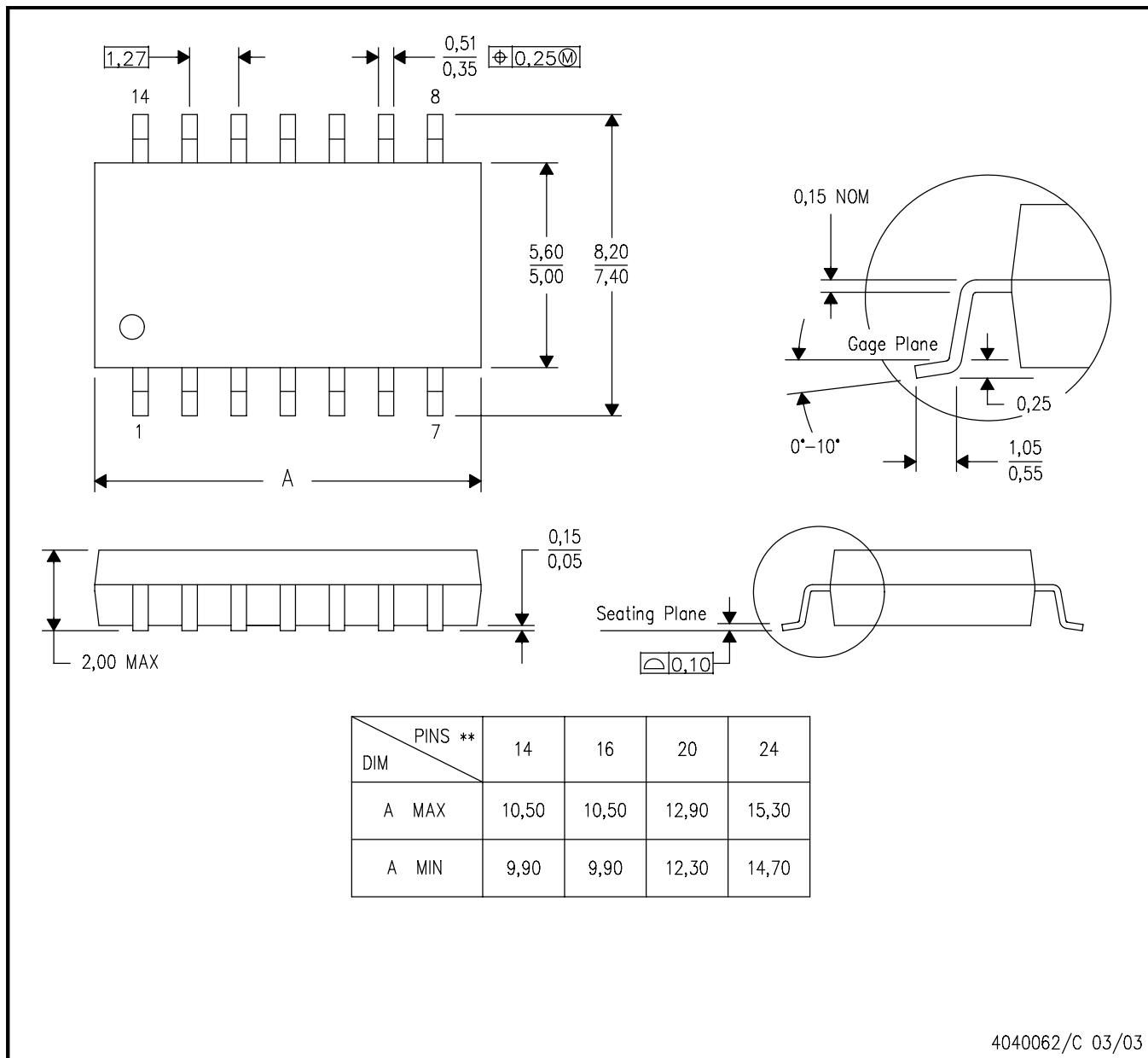
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AS298ANSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

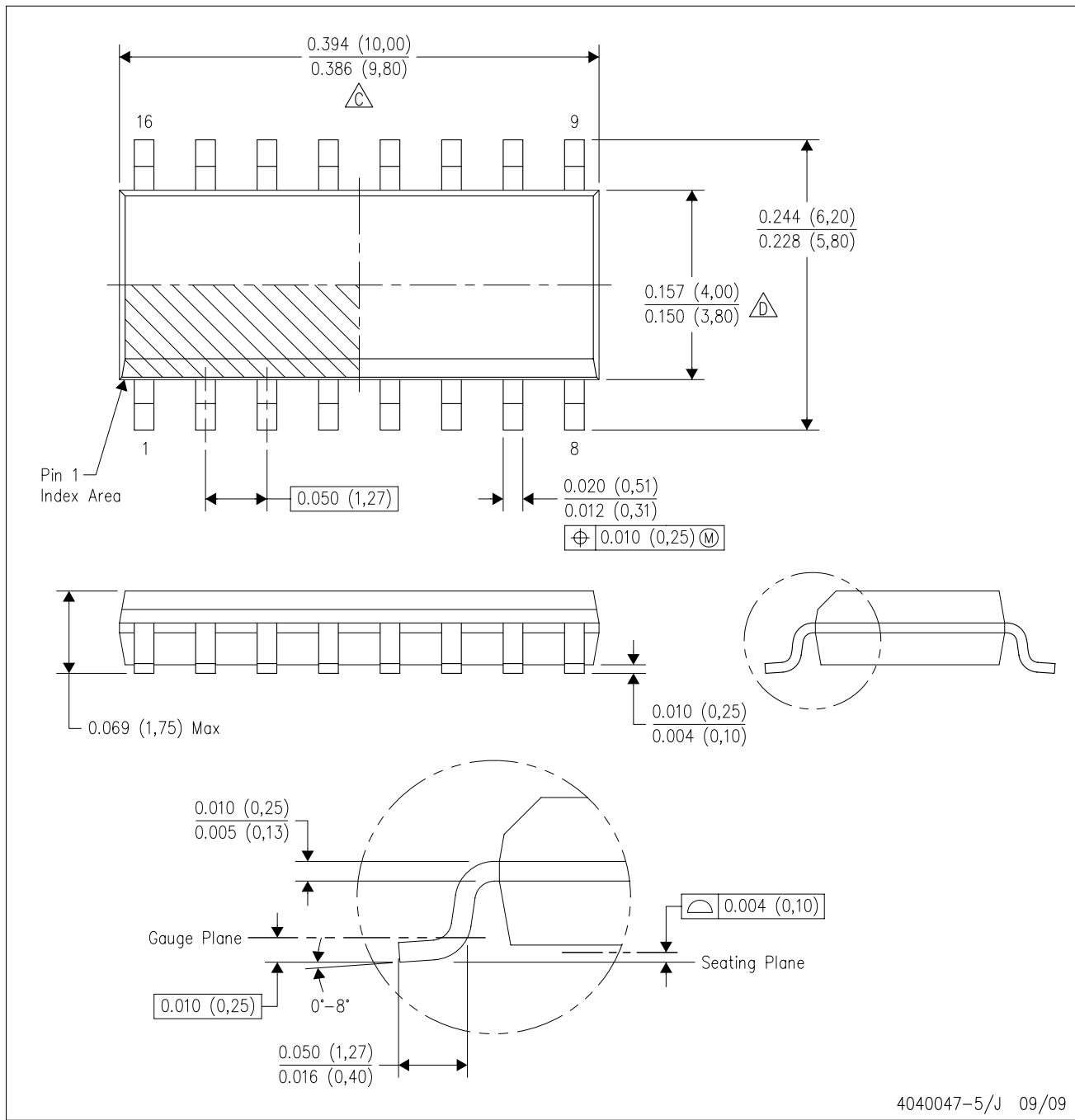


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

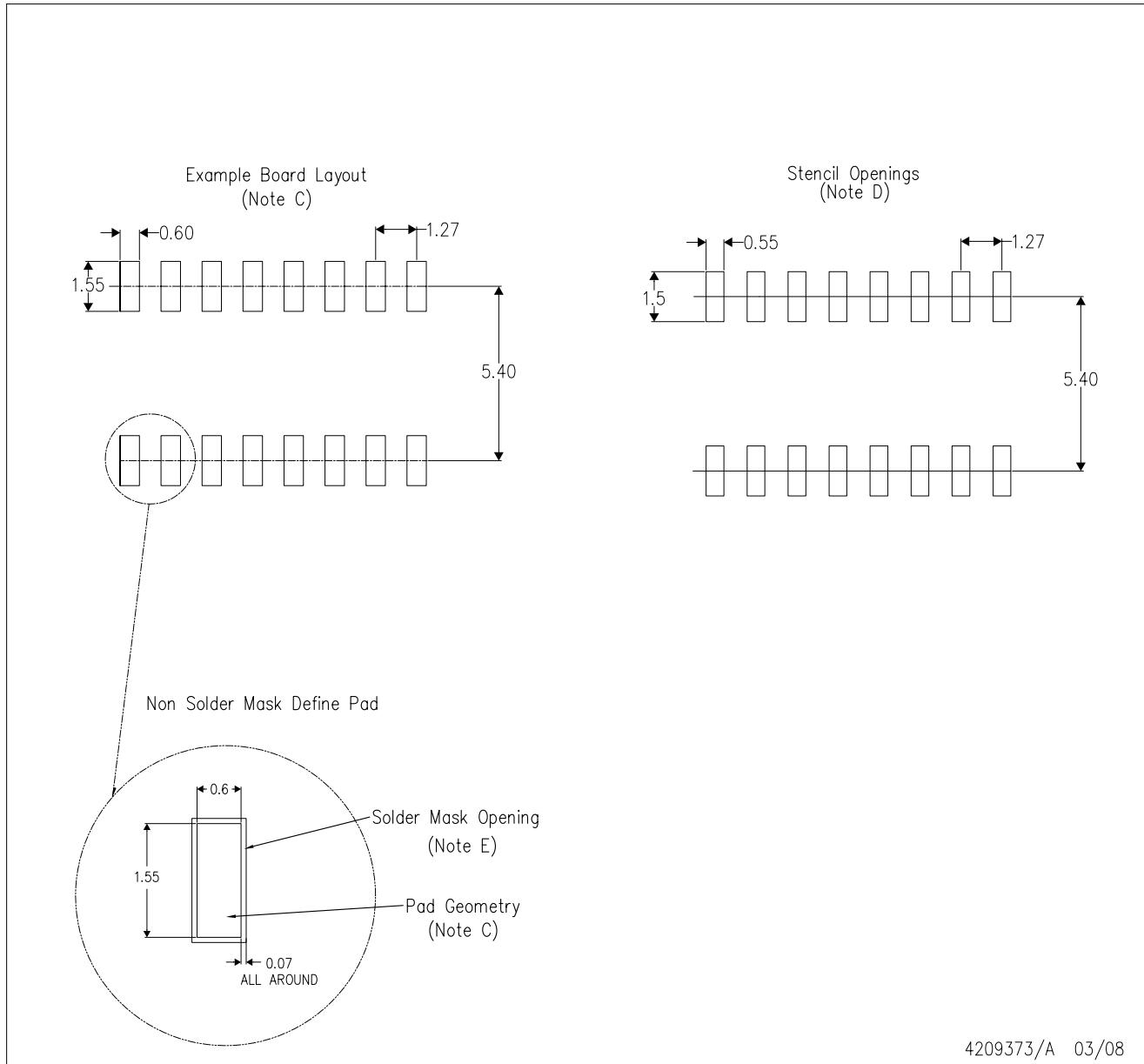
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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