ULTRA-COMPACT REAL-TIME CLOCK IC

RS5C314

EK-082-9908

OUTLINE

The RS5C314 is a CMOS type real-time clock which is connected to the CPU via three signal lines and capable of serial transmission of clock and calendar data to the CPU. The RS5C314 can generate various interrupt clock pulses lasting for long periods (one month). Driving an oscillation circuit at constant voltage, the circuit undergoes few voltage fluctuations and consequently realizes low current consumption (TYP. 0.7µA at 3 V). It also provides an oscillator halt sensing function for application to data validity at power-on and other occasions. Integrated into an ultra-compact and ultra-thin 8pin SSOP (0.65mm pitch), the RS5C314 is the optimum choice for equipment requiring small size and low power consumption.

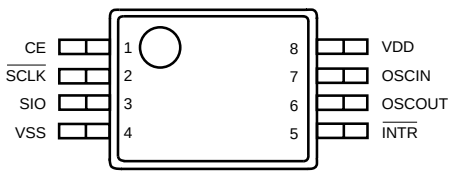
There is RS5C313 reversing the logic of serial clock for series goods.

FEATURES

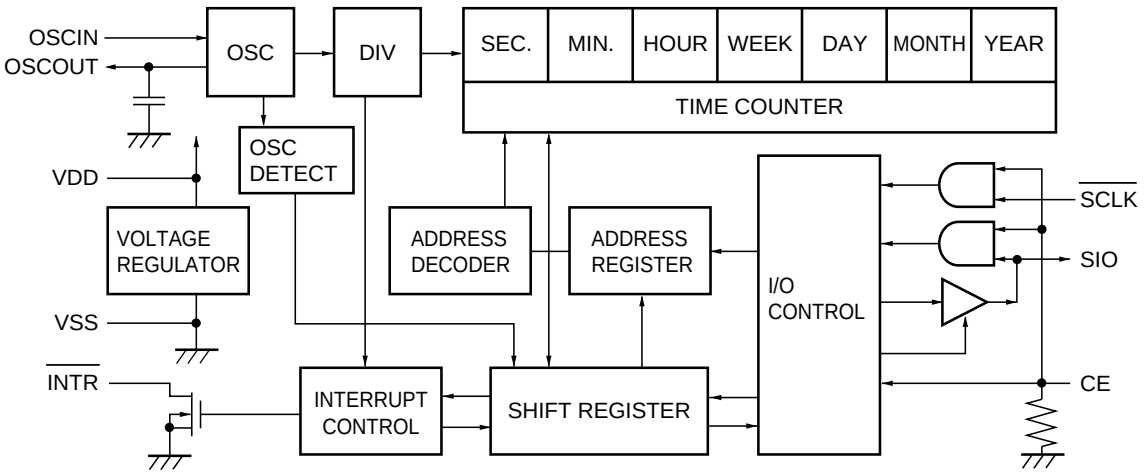
- Time Keeping Supply Voltage: 1.6 to 6.0 V
- Operating Supply Voltage: 2.7 to 6.0 V
- Low Current Consumption: TYP. 0.7µA (MAX. of 1.5µA) at 3V
- Connection to the CPU via only three pins: CE, $\overline{\text{SCLK}}$, and SIO (for addressing and data read and write operations)
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in binary-coded decimal (BCD) code
- Generation of interrupt pulses to the CPU with cycles ranging from 1 month to 1/1024 Hz, interrupt flags, and interrupt halt
- Software-based alarming through clock-interlocked interrupt operation
- Oscillator halt sensing to judge internal data validity
- Second digit adjustment by ±30 seconds
- 12-hour or 24-hour time display selectable
- Automatic leap year recognition up to the year 2099
- CMOS logic
- Package: 8pin SSOP (0.65mm pitch)

PIN CONFIGURATION

• 8pin SSOP



BLOCK DIAGRAM

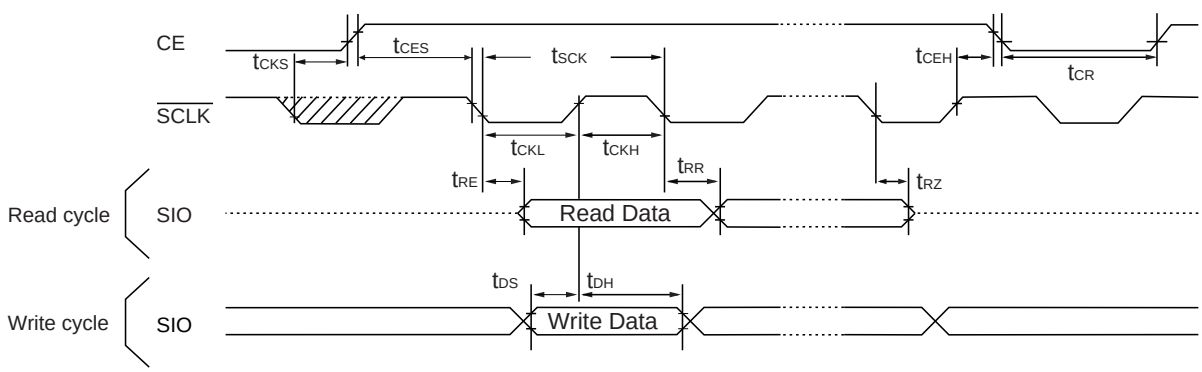


A DIFFERENCE WITH RS5C313

The logic of serial clock is point that it become that RS5C313 reverses RS5C314 with $\overline{SCLK}$ for SCLK and difference point of RS5C314 and RS5C313, describe is the master of by it being different in the following 3 items

(Give RS5C313 application manual absolutely reference in electric characteristic / the thing AC/DC requirements rating / recommendation gesture a maximum.)

1. Timing Chart



Input/output conditions

$V_{IH} = 0.8 \times V_{DD}$
$V_{IL} = 0.2 \times V_{DD}$
$V_{OH} = 0.8 \times V_{DD}$
$V_{OL} = 0.2 \times V_{DD}$

*) The ability that is fair in “H” or “L” slanted line department

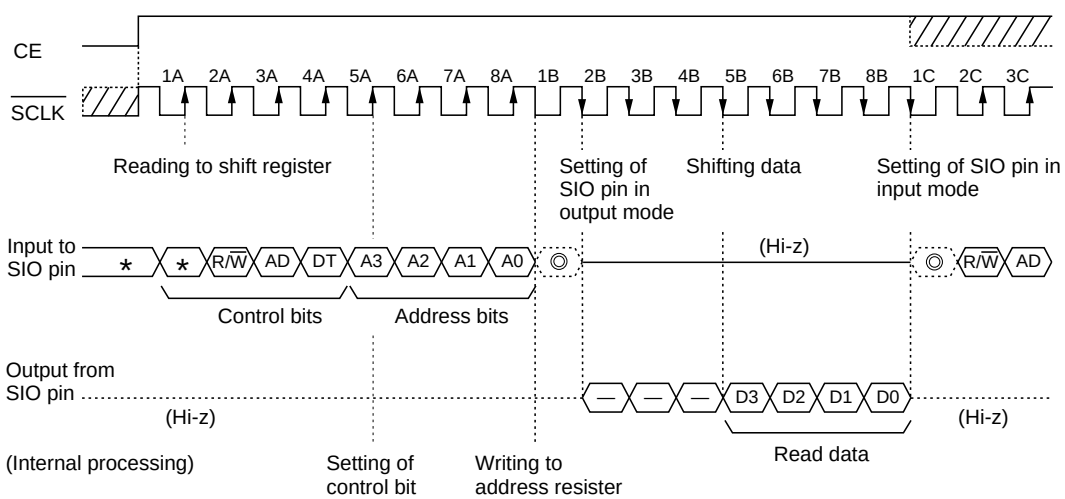
2. Read Data

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the $\overline{\text{SCLK}}$ pin.
The input data are registered in synchronization with the rising edge of the $\overline{\text{SCLK}}$. When the data is read, the read cycle shall be set by control bits.

- Control bits
  - R/$\overline{\text{W}}$: Establishes the read mode when set to 1, and the write mode when set to 0.
  - AD: Writes succeeding address bits (A3 to A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  - DT: Writes data bits (D3 to D0) to the counter or the register specified by the address register which has written just before when set to 1 with the R/$\overline{\text{W}}$ and AD bits set equally to 0 and performs no such write operation in any other case.
- Address bits
  - A3 to A0: Inputs the bits MSB to LSB in the address table describing the functions.

2.1 Read Cycle Flow

1. The CE pin is switched from the low level to the high level.
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/$\overline{\text{W}}$ and AD are set equally to 1 while a control bit DT is set to 0.
3. The SIO pin enters the output mode at the falling edge of the shift clock pulse 2B from the $\overline{\text{SCLK}}$ pinwhile the four read bits (MSB→LSB) at designated addresses are output at the falling edge of the shift clock pulse 5B (see the figure below).
4. Then, the SIO pin returns to the input mode at the falling edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from the high level to the low level (after t_{CEH} from the rising edge of the eighth shift clock pulse from the $\overline{\text{SCLK}}$ pin). (Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at the high level.)



) In the above figure, the "" mark indicates arbitrary data; the "—" mark indicates unknown data; the "◎" mark indicates data which are available when the SIO pin is held at the high, low, or Hiz level ; and the diagonaliy shaded area indicates high or low.

3. Write Data

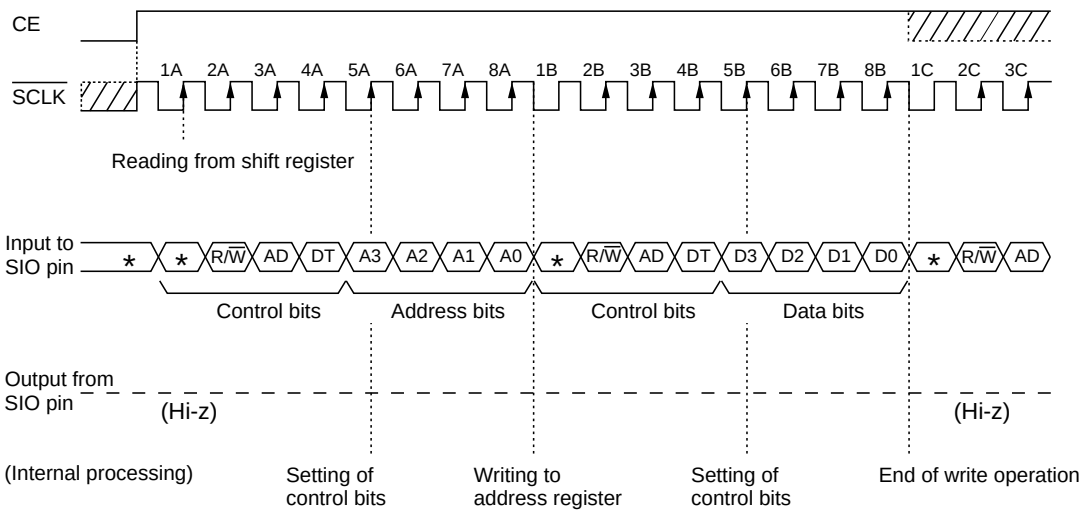
Writing data to the real-time clock requires inputting setting data (control bits and address bits) to the SIO pin and then establishing the write mode by using a control bit R/$\overline{W}$ in the same manner as in read operation.

*) Control bits and address bits are described in the previous section on read cycle.

• Data bits D3 to D0 : inputs writing data to the counter or the register describing the functions in order of MSB to LSB.

3.1 Write Cycle Flow

1. The CE pin is switched from the low level to the high level.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and DT are set equally to 0 while a control bit AD is set to 1 (at the shift clock pulses 1A to 8A from the $\overline{SCLK}$ pin).
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/$\overline{W}$ and AD are set equally to 0 while a control bit DT is set to 1 (at the shift clock pulses 1B to 8B from the $\overline{SCLK}$ pin).
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/$\overline{W}$, AD, and DT are set equally to 0 (at the rising edge of the fifth shift clock pulse and later from the $\overline{SCLK}$ pin) or the CE pin is switched from the high level to the low level (after t_{CEH} from the rising edge of the eighth shift clock pulse from the $\overline{SCLK}$ pin).



) In the above figure, the "" mark indicates arbitrary data; and the diagonally shaded area indicates the high or low level.

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