ISL6443A

300kHz Dual, 180° Out-of-Phase, Step-Down PWM and Single Linear Controller

FN6600
Rev 3.00
Sep 4, 2015

The ISL6443A is a high-performance, triple-output controller optimized for converting wall adapter, battery or network intermediate bus DC input supplies into the system supply voltages required for a wide variety of applications. Each output is adjustable down to 0.8V. The two PWMs are synchronized at 180° out-of-phase, thus reducing the RMS input current and ripple voltage.

The ISL6443A incorporates several protection features. An adjustable overcurrent protection circuit monitors the output current by sensing the voltage drop across the lower MOSFET. Hiccup mode overcurrent operation protects the DC/DC components from damage during output overload/short circuit conditions. Each PWM has an independent logic-level shutdown input ($\overline{SD1}$ and $\overline{SD2}$).

A single PGOOD signal is issued when soft-start is complete on both PWM controllers and their outputs are within 10% of the set point and the linear regulator output is greater than 75% of its setpoint. Thermal shutdown circuitry turns off the device if the junction temperature exceeds +150°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6443AIRZ*	6443A IRZ	-40 to +85	28 Ld 5x5 QFN	L28.5x5
ISL6443AIVZ* **(No longer available, recommended replacement: ISL6443AIRZ)**	6443A IVZ	-40 to +85	28 Ld TSSOP	M28.173

Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

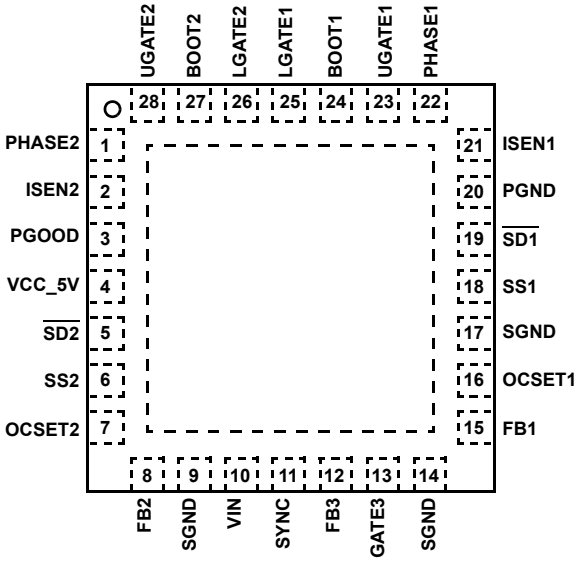
- Wide Input Supply Voltage Range
  - Variable 5.6V to 24V
  - Fixed 4.5V to 5.6V
- Three Independently Programmable Output Voltages
- Switching Frequency 300kHz
- Out-of-Phase PWM Controller Operation
  - Reduces Required Input Capacitance and Power Supply Induced Loads
- No External Current Sense Resistor
  - Uses Lower MOSFET’s $r_{DS(ON)}$
- Bidirectional Frequency Synchronization for Synchronizing Multiple ISL6443As
- Programmable Soft-Start
- Extensive Circuit Protection Functions
  - PGOOD
  - UVLO
  - Overcurrent
  - Over-temperature
  - Independent Shutdown for Both PWMs
- Excellent Dynamic Response
  - Voltage Feed-Forward with Current Mode Control
- QFN Packages:
  - QFN - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and has a Thinner Profile
- Pb-Free (RoHS Compliant)

Applications

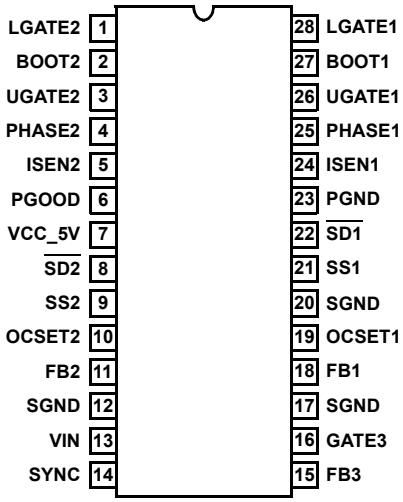
- Power Supplies with Multiple Outputs
- xDSL Modems/Routers
- DSP, ASIC, and FPGA Power Supplies
- Set-Top Boxes
- Dual Output Supplies for DSP, Memory, Logic, µP Core and I/O
- Telecom Systems

Pinouts

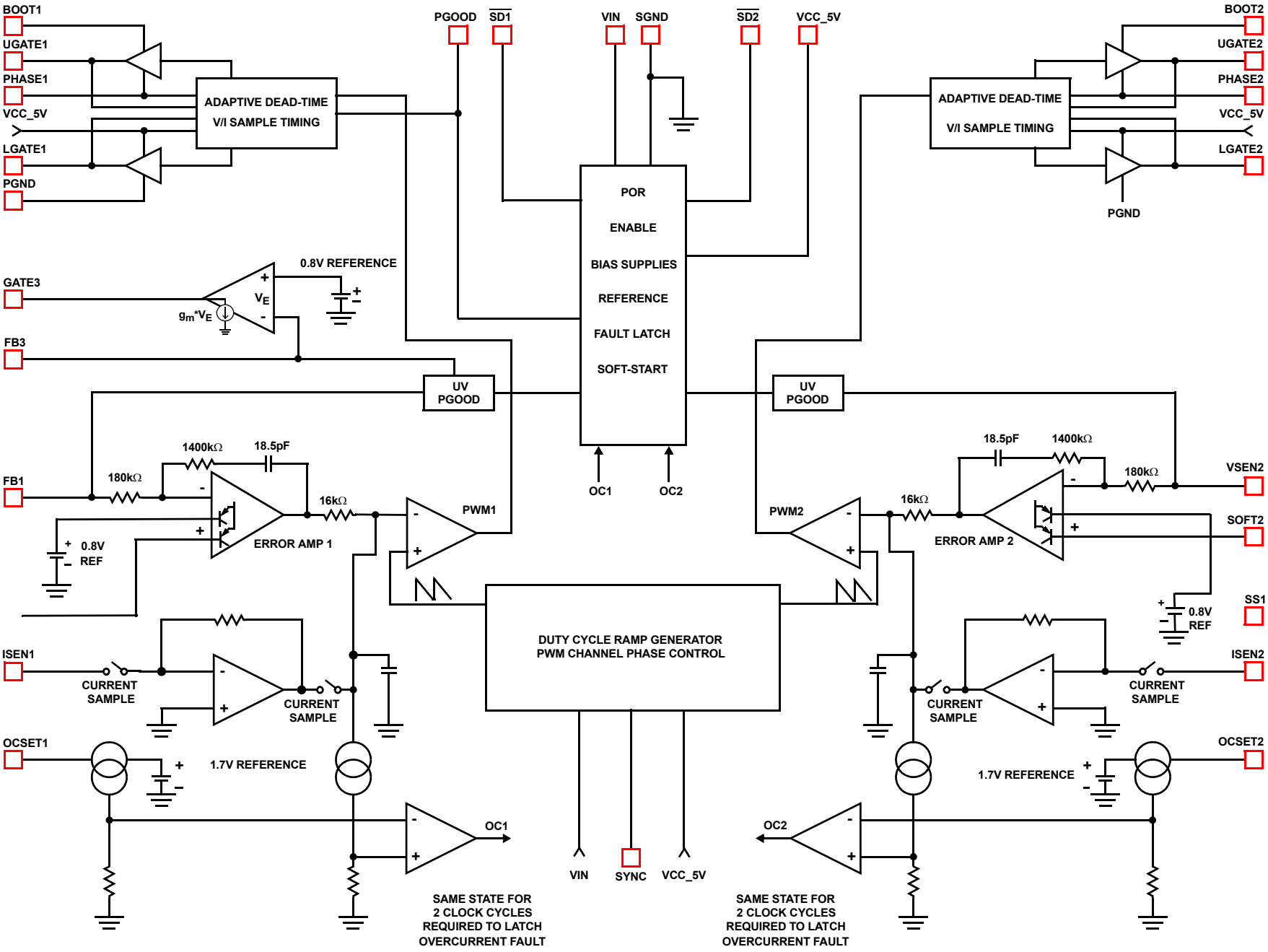
ISL6443A
(28 LD QFN)
TOP VIEW



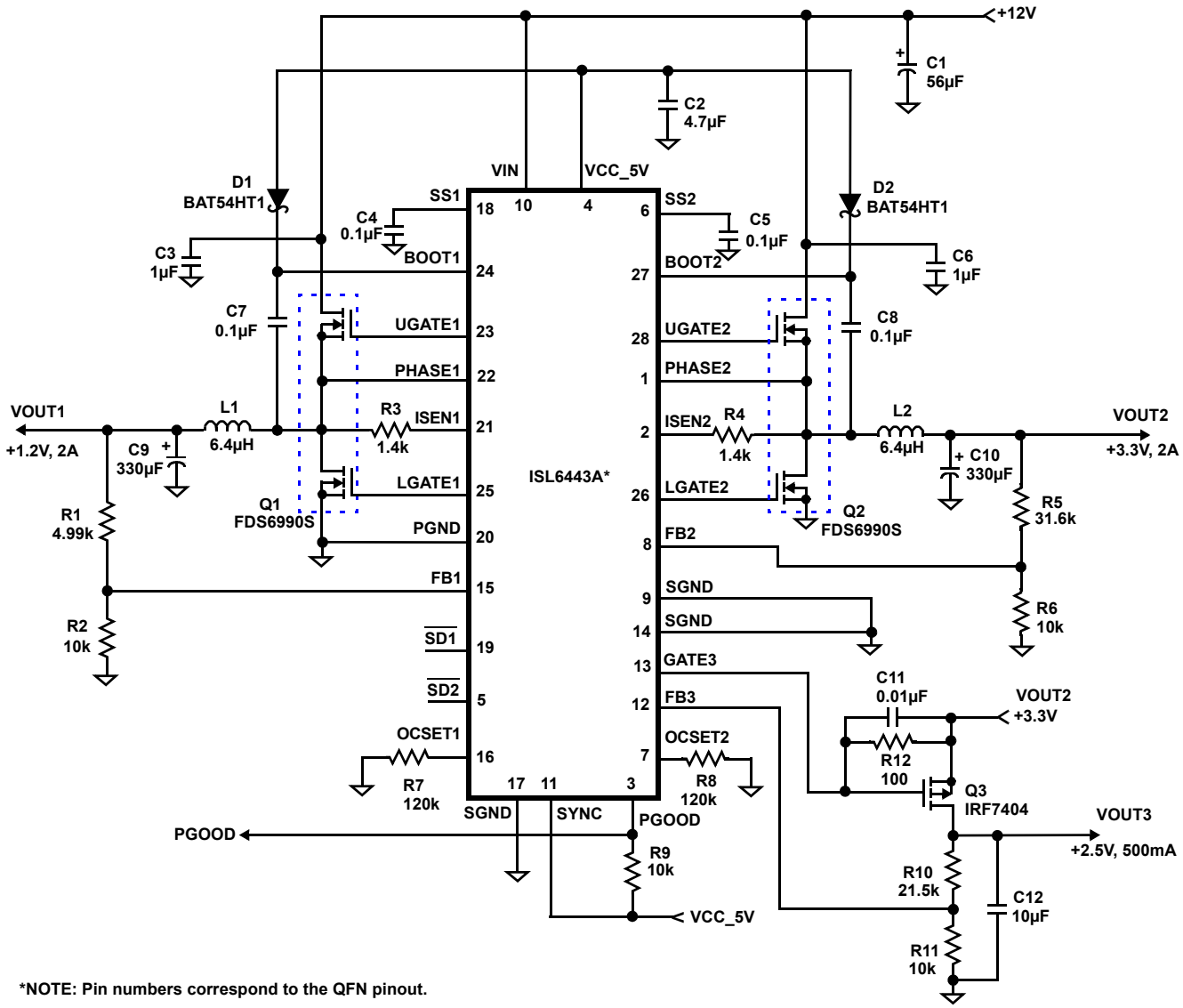
ISL6443A
(28 LD TSSOP)
TOP VIEW



Block Diagram



Typical Application Schematic



*NOTE: Pin numbers correspond to the QFN pinout.

Absolute Maximum Ratings

Supply Voltage (VCC_5V Pin) . . . . . .-0.3V to +7V
Input Voltage (V_{IN} Pin). . . . . .+27V
BOOT1, 2 and UGATE1, 2. . . . . .+35V
PHASE1, 2 and ISEN1, 2
. . . . . .-5V (<100ns, 10µJ)/-0.3V (DC) to +27V
BOOT1, 2 with Respect to PHASE1, 2 . . . . . +6.5V
UGATE1, 2. . . . . .(PHASE1, 2 - 0.3V) to (BOOT1, 2 + 0.3V)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Lead QFN (Notes 1, 2)	36	4
28 Lead TSSOP (Note 1)	75	NA

Maximum Junction Temperature . . . . . .-55°C to +150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Temperature Range. . . . . .-40°C to +85°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3 and “Typical Application Schematic” on page 4. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, T_A = -40°C to +85°C (Note 7), Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN SUPPLY					
Input Voltage Range		5.6	12	24	V
Input Voltage Range	V_{IN} = VCC (Note 4)	4.5	5.0	5.6	V
VCC_5V SUPPLY (Note 4)					
Input Voltage		4.5	5.0	5.6	V
Output Voltage	V_{IN} > 5.6V, I_L = 20mA	4.5	5.0	5.5	V
Maximum Output Current	V_{IN} = 12V	60	-	-	mA
SUPPLY CURRENT					
Shutdown Current (Note 5)	$\overline{SD1}$ = $\overline{SD2}$ = GND	-	50	375	µA
Operating Current (Note 6)		-	2.0	4.0	mA
REFERENCE SECTION					
Nominal Reference Voltage		-	0.8	-	V
Reference Voltage Tolerance		-1.0	-	1.0	%
POWER-ON RESET					
Rising VCC_5V Threshold		4.25	4.45	4.5	V
Falling VCC_5V Threshold		3.95	4.2	4.4	V
OSCILLATOR					
Total Frequency Variation		260	300	340	kHz
Peak-to-Peak Sawtooth Amplitude (Note 7)	V_{IN} = 12V	-	1.6	-	V
	V_{IN} = 5V	-	0.667	-	V
Ramp Offset (Note 7)		-	1.0	-	V
SYNC Input Rise/Fall Time (Note 7)		-	5.0	-	ns
SYNC Frequency Range		4.16	4.8	5.44	MHz
SYNC Input HIGH Level		3.5	-	-	V
SYNC Input LOW Level		-	-	1.5	V

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3 and “Typical Application Schematic” on page 4. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, T_A = -40°C to +85°C (Note 7), Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Input Minimum Pulse Width (Note 7)		-	15.0	-	ns
SYNC Output HIGH Level		V_{CC} - 0.6V	-	-	V
SHUTDOWN1/SHUTDOWN2					
HIGH Level (Converter Enabled)	Internal Pull-up (3µA)	2.0	-	-	V
LOW Level (Converter Disabled)		-	-	0.8	V
PWM CONVERTERS					
Output Voltage		-	0.8	-	V
FB Pin Bias Current		-	-	150	nA
Maximum Duty Cycle	C_{OUT} = 1000pF, T_A = +25°C	93	-	-	%
Minimum Duty Cycle		-	4	-	%
PWM CONTROLLER ERROR AMPLIFIERS					
DC Gain (Note 7)		-	88	-	dB
Gain-Bandwidth Product (Note 7)		-	15	-	MHz
Slew Rate (Note 7)		-	2.0	-	V/µs
PWM CONTROLLER GATE DRIVERS (Note 7)					
Sink/Source Current		-	400	-	mA
Upper Drive Pull-Up Resistance	VCC_5V = 4.5V	-	8	-	Ω
Upper Drive Pull-Down Resistance	VCC_5V = 4.5V	-	3.2	-	Ω
Lower Drive Pull-Up Resistance	VCC_5V = 4.5V	-	8	-	Ω
Lower Drive Pull-Down Resistance	VCC_5V = 4.5V	-	1.8	-	Ω
Rise Time	C_{OUT} = 1000pF	-	18	-	ns
Fall Time	C_{OUT} = 1000pF	-	18	-	ns
LINEAR CONTROLLER					
Drive Sink Current		50	-	-	mA
FB3 Feedback Threshold	I = 21mA	-	0.8	-	V
Undervoltage Threshold	V_{FB}	-	75	-	%
FB3 Input Leakage Current		-	45	150	nA
Amplifier Transconductance	V_{FB} = 0.8V, I = 21mA	-	2	-	A/V
POWER GOOD AND CONTROL FUNCTIONS					
PGOOD LOW Level Voltage	Pull-up = 100kΩ	-	0.1	0.5	V
PGOOD Leakage Current		-	-	±1.0	µA
PGOOD Upper Threshold, PWM 1 and 2	Fraction of set point	105	-	120	%
PGOOD Lower Threshold, PWM 1 and 2	Fraction of set point	80	-	95	%
PGOOD for Linear Controller		70	75	80	%
ISEN AND CURRENT LIMIT					
Full Scale Input Current (Note 8)		-	32	-	µA
Overcurrent Threshold (Note 8)	R_{OCSET} = 110kΩ	-	64	-	µA
OCSET (Current Limit) Voltage		-	1.7	-	V

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3 and “Typical Application Schematic” on page 4. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, T_A = -40°C to +85°C (Note 7), Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START					
Soft-Start Current		-	5	-	µA
PROTECTION					
Thermal Shutdown	Rising	-	150	-	°C
	Hysteresis	-	20	-	°C

NOTES:

4. In normal operation, where the device is supplied with voltage on the V_{IN} pin, the VCC_5V pin provides a 5V output capable of 60mA (min). When the VCC_5V pin is used as a 5V supply input, the internal LDO regulator is disabled and the V_{IN} input pin must be connected to the VCC_5V pin. (Refer to “Pin Descriptions” on page 10 for more details.)
5. This is the total shutdown current with V_{IN} = VCC_5V = PVCC = 5V.
6. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
7. Limits should be considered typical and are not production tested.
8. Established by characterization. The full scale current of 32µA is recommended for optimum current sample and hold operation. See “Feedback Loop Compensation” on page 13.

Typical Performance Curves

Oscilloscope Plots are Taken Using the ISL6443A EVAL Evaluation Board, VIN = 12V Unless Otherwise Noted.

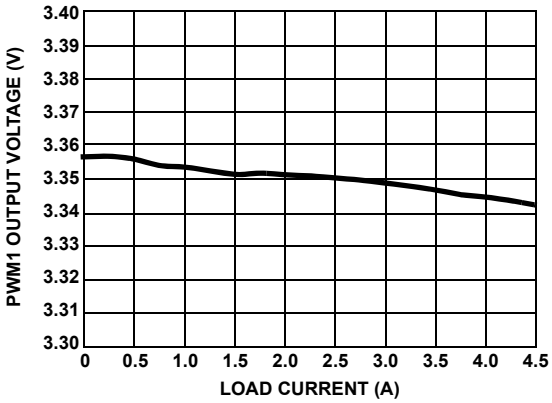


FIGURE 1. PWM1 LOAD REGULATION

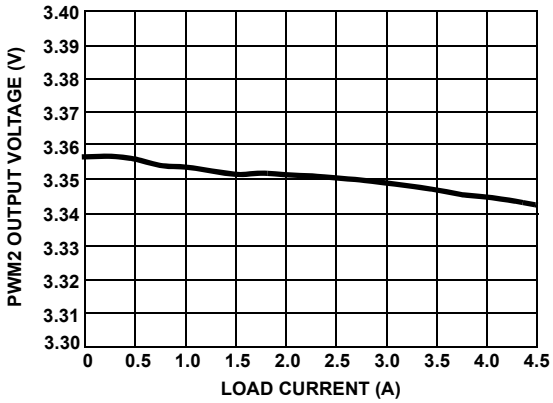


FIGURE 2. PWM2 LOAD REGULATION

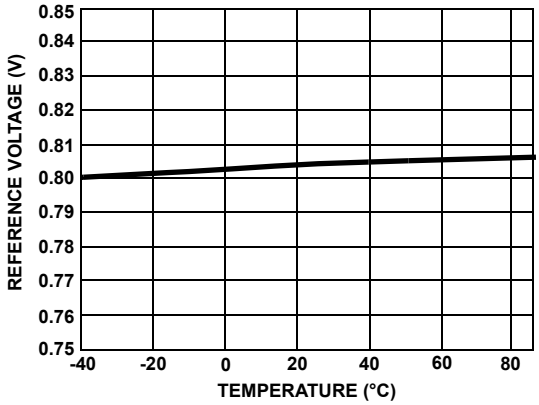


FIGURE 3. REFERENCE VOLTAGE VARIATION OVER TEMPERATURE

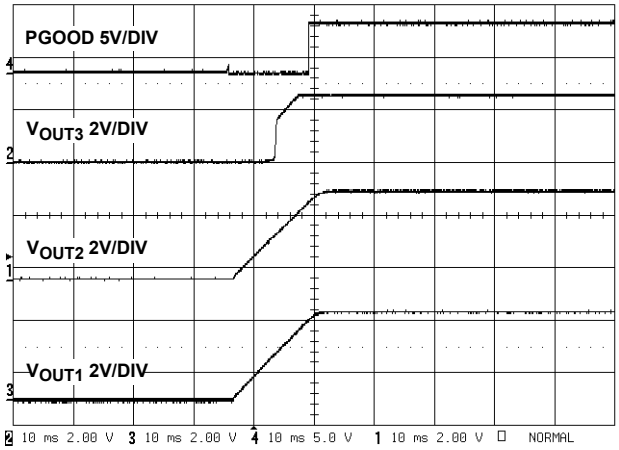


FIGURE 4. SOFT-START WAVEFORMS WITH PGOOD

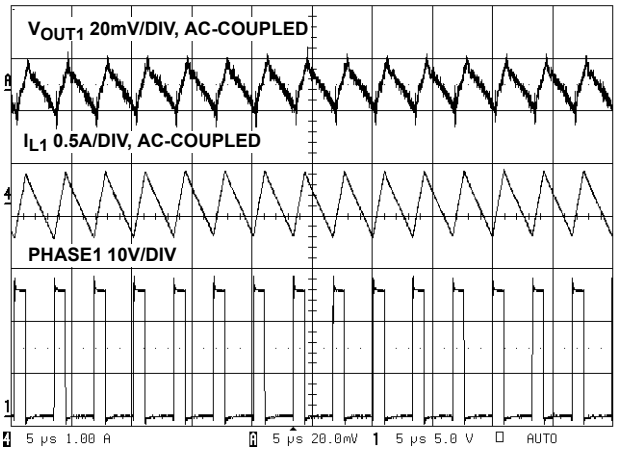


FIGURE 5. PWM1 WAVEFORMS

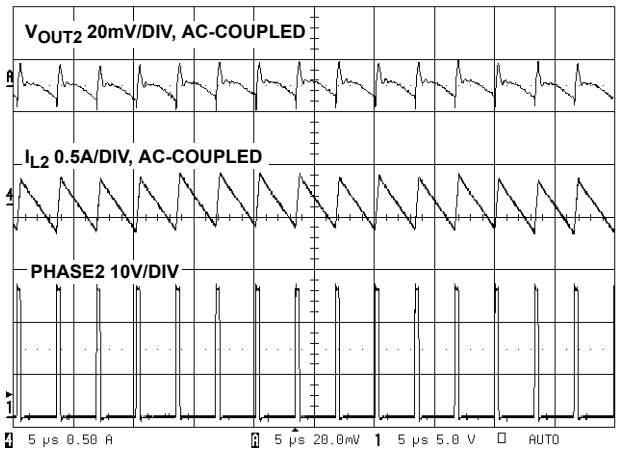


FIGURE 6. PWM2 WAVEFORMS

Typical Performance Curves Oscilloscope Plots are Taken Using the ISL6443A EVAL Evaluation Board, VIN = 12V Unless Otherwise Noted. **(Continued)**

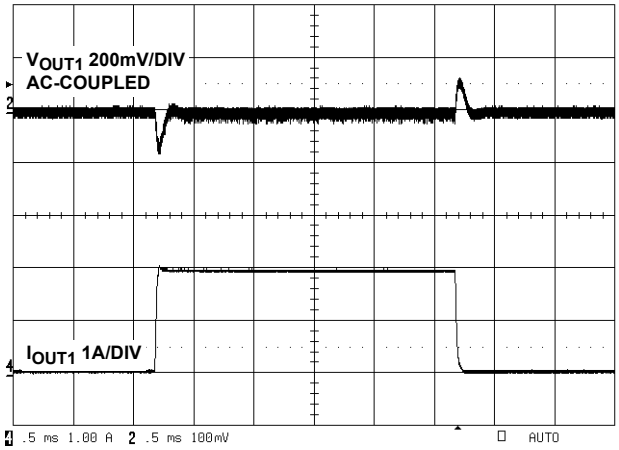


FIGURE 7. LOAD TRANSIENT RESPONSE V_{OUT1} (3.3V)

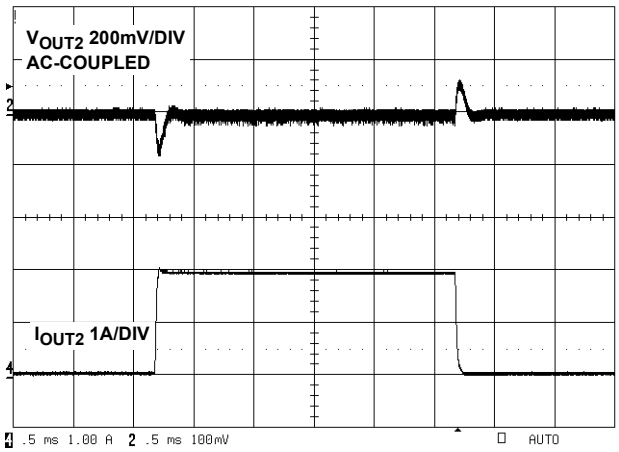


FIGURE 8. LOAD TRANSIENT RESPONSE V_{OUT2} (3.3V)

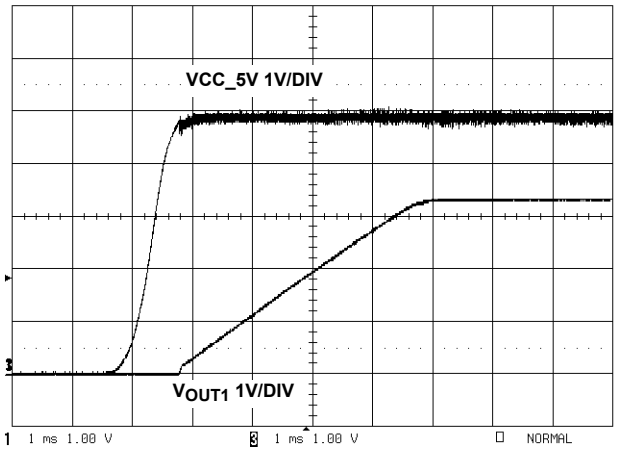


FIGURE 9. PWM SOFT-START WAVEFORM

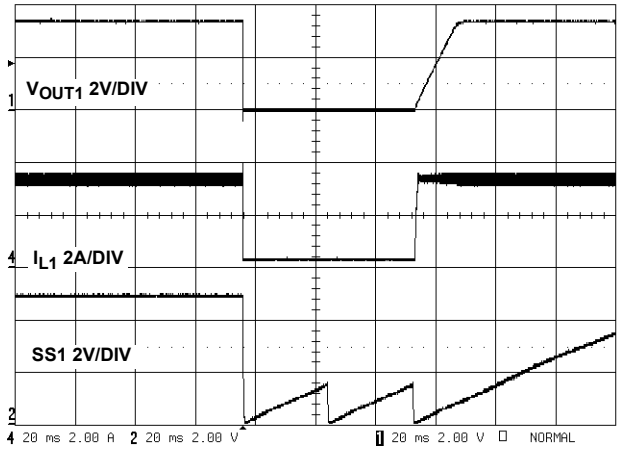


FIGURE 10. OVERCURRENT HICCUP MODE OPERATION

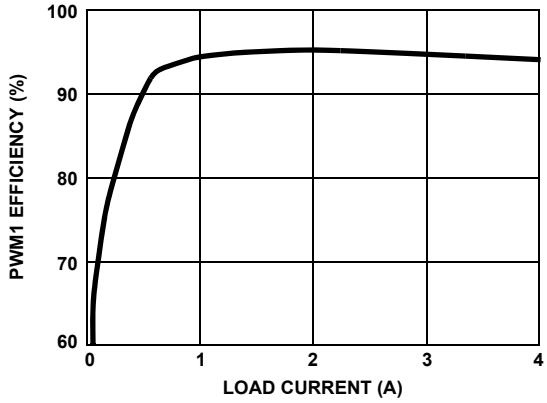


FIGURE 11. PWM1 EFFICIENCY vs LOAD (3.3V), V_{IN} = 12V

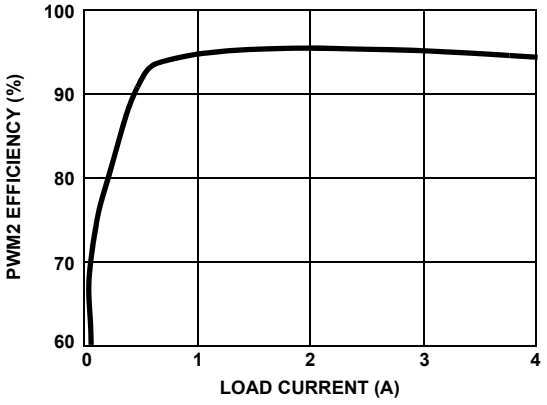


FIGURE 12. PWM2 EFFICIENCY vs LOAD (3.3V), V_{IN} = 12V

Pin Descriptions

BOOT2, BOOT1 - These pins power the upper MOSFET drivers of each PWM converter. Connect these pins to the junction of the bootstrap capacitor and the cathode of the bootstrap diode. The anode of the bootstrap diode is connected to the VCC_5V pin.

UGATE2, UGATE1 - These pins provide the gate drive for the upper MOSFETs.

PHASE2, PHASE1 - These pins are connected to the junction of the upper MOSFETs source, output filter inductor and lower MOSFETs drain.

LGATE2, LGATE1 - These pins provide the gate drive for the lower MOSFETs.

PGND - This pin provides the power ground connection for the lower gate drivers for both PWM1 and PWM2. This pin should be connected to the sources of the lower MOSFETs and the (-) terminals of the external input capacitors.

FB3, FB2, FB1 - These pins are connected to the feedback resistor divider and provide the voltage feedback signals for the respective controller. They set the output voltage of the converter. In addition, the PGOOD circuit uses these inputs to monitor the output voltage status.

ISEN2, ISEN1 - These pins are used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.

PGOOD - This is an open drain logic output used to indicate the status of the output voltages. This pin is pulled low when either of the two PWM outputs is not within 10% of the respective nominal voltage, or if the linear controller output is less than 75% of it's nominal value.

Table 1 shows detailed status of PGOOD which can be classified into 4 cases under different combinations of SD1 and SD2 inputs.

The first case is when both SD1 and SD2 are HIGH. PGOOD will be HIGH if all FB pins from the 3 REQUIRED outputs are within regulation AND soft-starts (SS1 AND SS2) are complete.

The other two cases are when either of SD1 or SD2 is LOW which means the system wants to shut down one of the PWM outputs but still wants to keep another output working. PGOOD will be HIGH if all the FB pins from the 2 REQUIRED outputs are within regulation AND soft-start (SS1/SS2) is complete.

The last case is when both of the SD1 and SD2 are LOW. PGOOD will be low.

SGND - (Pin 20 on the TSSOP; Pin 17 on the QFN)
This is the small-signal ground, common to all 3 controllers, and must be routed separately from the high current ground (PGND). All voltage levels are measured with respect to this pin. A small ceramic capacitor should be connected right next to this pin for noise decoupling.

VIN - Use this pin to power the device with an external supply voltage with a range of 5.6V to 24V. For 5V ±10% operation, connect this pin to VCC_5V.

VCC_5V - This pin is the output of the internal 5V linear regulator. This output supplies the bias for the IC, the low side gate drivers, and the external boot circuitry for the high side gate drivers. The IC may be powered directly from a single 5V (±10%) supply at this pin. When used as a 5V supply input, this pin must be externally connected to V_{IN}. The VCC_5V pin must be always de-coupled to power ground with a minimum of 4.7µF ceramic capacitor, placed very close to the pin.

SYNC - This pin may be used to synchronize two or more ISL6443A controllers. This pin requires a 1k resistor to ground if used; connect directly to VCC_5V if not used.

SS1, SS2 - These pins provide a soft-start function for their respective PWM controllers. When the chip is enabled, the regulated 5µA pull-up current source charges the capacitor connected from this pin to ground. The error amplifier reference voltage ramps from 0V to 0.8V while the voltage on the soft-start pin ramps from 0V to 0.8V.

$\overline{SD1}$, $\overline{SD2}$ - These pins provide an enable/disable function for their respective PWM output. The output is enabled when this pin is floating or pulled HIGH, and disabled when the pin is pulled LOW.

GATE3 - This pin is the open drain output of the linear regulator controller.

OCSET2, OCSET1 - A resistor from this pin to ground sets the overcurrent threshold for the respective PWM.

TABLE 1. DETAILED STATUS OF PGOOD

SD1	SD2	LDO > 75%?	90% < FB1 < 110%?	90% < FB2 < 110%?	SS1 COMPLETED?	SS2 COMPLETED?	PGOOD
1	1	Y	Y	Y	Y	Y	1
1	0	Y	Y	x	Y	x	1
0	1	Y	x	Y	x	Y	1
0	0	x	x	x	x	x	0

"x" means "don't care".

Functional Description

General Description

The ISL6443A integrates control circuits for two synchronous buck converters and one linear controller. The two synchronous bucks operate out-of-phase to substantially reduce the input ripple and thus reduce the input filter requirements. The chip has four control lines (SS1, $\overline{SD1}$, SS2, and $\overline{SD2}$), which provide independent control for each of the synchronous buck outputs.

The buck PWM controllers employ a free-running frequency of 300kHz. The current mode control scheme with an input voltage feed-forward ramp input to the modulator provides excellent rejection of input voltage variations and provides simplified loop compensations.

The linear controller can drive either a PNP or PFET to provide ultra low-dropout regulation with programmable voltages.

Internal 5V Linear Regulator (VCC_5V)

All ISL6443A functions are internally powered from an on-chip, low dropout 5V regulator. The maximum regulator input voltage is 24V. Bypass the regulator's output (VCC_5V) with a 4.7µF capacitor to ground. The dropout voltage for this LDO is typically 600mV, so when VIN is greater than 5.6V, VCC_5V is typically 5V. The ISL6443A also employs an undervoltage lockout circuit that disables both regulators when VCC_5V falls below 4.4V.

The internal LDO can source over 60mA to supply the IC, power the low side gate drivers and charge the external boot capacitor. When driving large FETs (especially at 300kHz frequency), little or no regulator current may be available for external loads.

For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA. Also, at higher input voltages with larger FETs, the power dissipation across the internal 5V will increase. Excessive dissipation across this regulator must be avoided to prevent the junction temperature from rising. Larger FETs can be used with 5V ±10% input applications. The thermal overload protection circuit will be triggered if the VCC_5V output is short circuited. Connect VCC_5V to V_{IN} for 5V ±10% input applications.

Soft-Start Operation

When soft-start is initiated, the voltage on the SS pin of the enabled PWM channels starts to ramp gradually, due to the 5µA current sourced into the external capacitor. The output voltage follows the soft-start voltage.

When the SS pin voltage reaches 0.8V, the output voltage of the enabled PWM channel reaches the regulation point, and the soft-start pin voltage continues to rise. At this point the PGOOD and fault circuitry is enabled. This completes the soft-start sequence. Any further rise of SS pin voltage does not affect the output voltage. By varying the values of the soft-start capacitors, it is possible to provide sequencing of the main outputs at start-up. The soft-start time can be obtained from Equation 1:

$$t_{SOFT} = 0.8V\left(\frac{C_{SS}}{5\mu A}\right) \quad \text{(EQ. 1)}$$

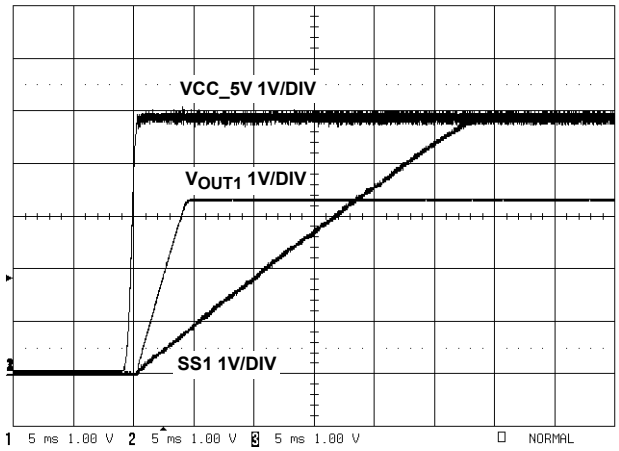


FIGURE 13. SOFT-START OPERATION

The soft-start capacitors can be chosen to provide start-up tracking for the two PWM outputs. This can be achieved by choosing the soft-start capacitors such that the soft-start capacitor ratio equals the respective PWM output voltage ratio. For example, if one uses PWM1 = 1.2V and PWM2 = 3.3V, then the soft-start capacitor ratio should be, C_{SS1}/C_{SS2} = 1.2/3.3 = 0.364. Figure 14 shows that soft-start waveform with C_{SS1} = 0.01µF and C_{SS2} = 0.027µF.

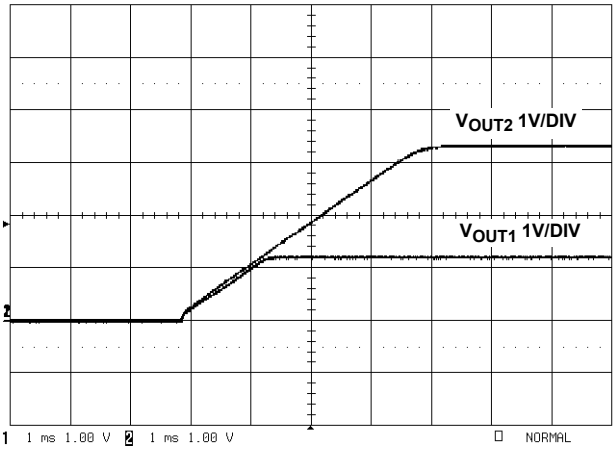


FIGURE 14. PWM1 AND PWM2 OUTPUT TRACKING DURING START-UP

Output Voltage Programming

A resistive divider from the output to ground sets the output voltage of either PWM channel. The center point of the divider shall be connected to FBx pin. The output voltage value is determined by Equation 2.

$$V_{OUTx} = 0.8V\left(\frac{R_1 + R_2}{R_2}\right) \quad \text{(EQ. 2)}$$

where R_1 is the top resistor of the feedback divider network and R_2 is the resistor connected from FBx to ground.

Out-of-Phase Operation

The two PWM controllers in the ISL6443A operate 180° out-of-phase to reduce input ripple current. This reduces the input capacitor ripple current requirements, reduces power supply-induced noise and improves EMI. This effectively helps to lower component cost, save board space and reduce EMI.

Dual PWMs typically operate in-phase and turn on both upper FETs at the same time. The input capacitor must then support the instantaneous current requirements of both controllers simultaneously, resulting in increased ripple voltage and current. The higher RMS ripple current lowers the efficiency due to the power loss associated with the ESR of the input capacitor. This typically requires more low-ESR capacitors in parallel to minimize the input voltage ripple and ESR-related losses, or to meet the required ripple current rating.

With dual synchronized out-of-phase operation, the high-side MOSFETs of the ISL6443A turn on 180° out-of-phase. The instantaneous input current peaks of both regulators no longer overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating, allowing fewer or less expensive capacitors, and reducing the shielding requirements for EMI. The “Typical Performance Curves Oscilloscope Plots are Taken Using the ISL6443A EVAL Evaluation Board, VIN = 12V Unless Otherwise Noted.” on page 8 show the synchronized 180° out-of-phase operation.

Input Voltage Range

The ISL6443A is designed to operate from input supplies ranging from 4.5V to 24V. However, the input voltage range can be effectively limited by the available maximum duty cycle (D_{MAX} = 93%).

$$V_{IN(min)} = \left(\frac{V_{OUT} + V_{d1}}{0.93}\right) + V_{d2} - V_{d1} \quad \text{(EQ. 3)}$$

where,

V_{d1} = Sum of the parasitic voltage drops in the inductor discharge path, including the lower FET, inductor and PC board.

V_{d2} = Sum of the voltage drops in the charging path, including the upper FET, inductor and PC board resistances.

The maximum input voltage and minimum output voltage is limited by the minimum on-time ($t_{ON(min)}$).

$$V_{IN(max)} \leq \frac{V_{OUT}}{t_{ON(min)} \times 300kHz} \quad \text{(EQ. 4)}$$

where, $t_{ON(min)}$ = 30ns

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals, which provides amplification, level shifting and shoot-through protection. The gate drivers have some circuitry that helps optimize the ICs performance over a wide range of operational conditions. As MOSFET switching times can vary dramatically from type to type and with input voltage, the gate control logic provides adaptive dead time by monitoring real gate waveforms of both the upper and the lower MOSFETs. Shoot-through control logic provides a 20ns deadtime to ensure that both the upper and lower MOSFETs will not turn on simultaneously and cause a shoot-through condition.

Gate Drivers

The low-side gate driver is supplied from VCC_5V and provides a peak sink/source current of 400mA. The high-side gate driver is also capable of 400mA current. Gate-drive voltages for the upper N-Channel MOSFET are generated by the flying capacitor boot circuit. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high side MOSFET driver. To limit the peak current in the IC, an external resistor may be placed between the UGATE pin and the gate of the external MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET’s input capacitance.

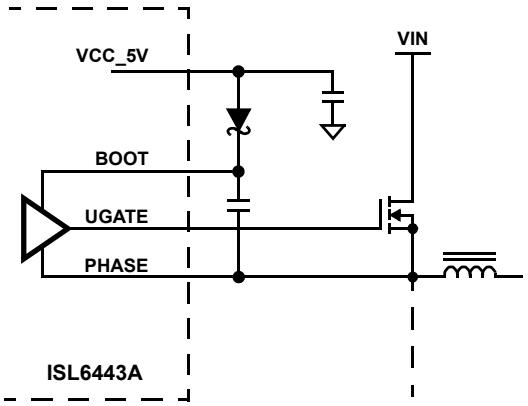


FIGURE 15. GATE DRIVER

At start-up, the low-side MOSFET turns on and forces PHASE to ground in order to charge the BOOT capacitor to 5V. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. This provides the necessary gate-to-source voltage to turn on the upper MOSFET, an action that boosts the 5V gate drive signal above V_{IN}. The current required to drive the upper MOSFET is drawn from the internal 5V regulator.

Protection Circuits

The converter output is monitored and protected against overload, short circuit and undervoltage conditions. A sustained overload on the output sets the PGOOD low and initiates hiccup mode.

Overcurrent Protection

Both PWM controllers use the lower MOSFET’s ON-resistance, $r_{DS(ON)}$, to monitor the current in the converter. The sensed voltage drop is compared with a threshold set by a resistor connected from the OCSETx pin to ground.

$$R_{OCSET} = \frac{(7)(R_{CS})}{(I_{OC})(r_{DS(on)})} \quad \text{(EQ. 5)}$$

where, I_{OC} is the desired overcurrent protection threshold, and R_{CS} is a value of the current sense resistor connected to the ISENx pin. If an overcurrent is detected for 2 consecutive clock cycles, then the IC enters a hiccup mode by turning off the gate drivers and entering into soft-start. The IC will cycle 2x through soft-start before trying to restart. The IC will continue to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start, so care must be taken to ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

Because of the nature of this current sensing technique, and to accommodate a wide range of $r_{DS(ON)}$ variations, the value of the overcurrent threshold should represent an overload current about 150% to 180% of the maximum operating current. If more accurate current protection is desired, place a current sense resistor in series with the lower MOSFET source.

Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +150°C is reached. Normal operation resumes when the die temperatures drops below +130°C through the initiation of a full soft-start cycle.

Implementing Synchronization

The SYNC pin may be used to synchronize two or more controllers. When the SYNC pins of two controllers are connected together, one controller becomes the master and the other controller synchronizes to the master. A pull-down resistor is required and must be sized to provide a low enough time constant to pass the SYNC pulse. Connect this pin to VCC_5V if not used. Figure 16 shows the SYNC pin waveform operating at 16x the switching frequency.

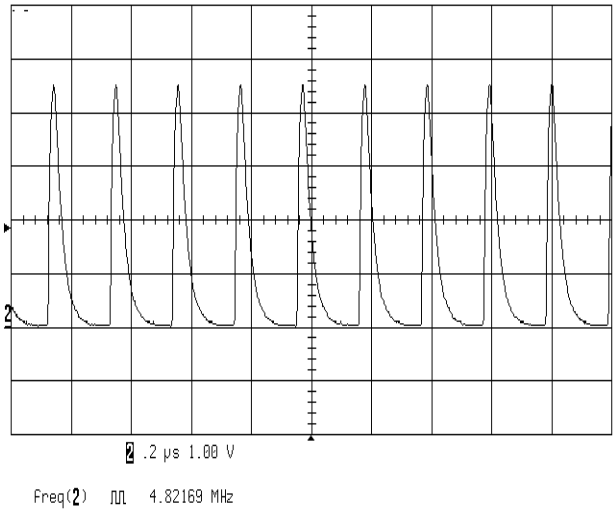


FIGURE 16. SYNC WAVEFORM

Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, both PWM controllers have internally compensated error amplifiers. To make internal compensation possible, several design measures were taken.

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided via the VIN pin. This keeps the modulator gain constant with variation in the input voltage. Second, the load current proportional signal is derived from the voltage drop across the lower MOSFET during the $\overline{PWM}$ time interval and is subtracted from the amplified error signal on the comparator input. This creates an internal current control loop. The resistor connected to the ISEN pin sets the gain in the current feedback loop. Equation 6 estimates the required value of the current sense resistor depending on the maximum operating load current and the value of the MOSFET's $r_{DS(ON)}$.

$$R_{CS} \geq \frac{(I_{MAX})(r_{DS(ON)})}{32\mu A} \quad \text{(EQ. 6)}$$

Choosing R_{CS} to provide 32µA of current to the current sample and hold circuitry is recommended but values down to 2µA and up to 100µA can be used.

Due to the current loop feedback, the modulator has a single pole response with -20dB slope at a frequency determined by the load.

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} \quad \text{(EQ. 7)}$$

where R_O is load resistance and C_O is load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 17 shows a Type 2 amplifier and its response along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies in between the zero and the pole.

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 6kHz \quad \text{(EQ. 8)}$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 600kHz \quad \text{(EQ. 9)}$$

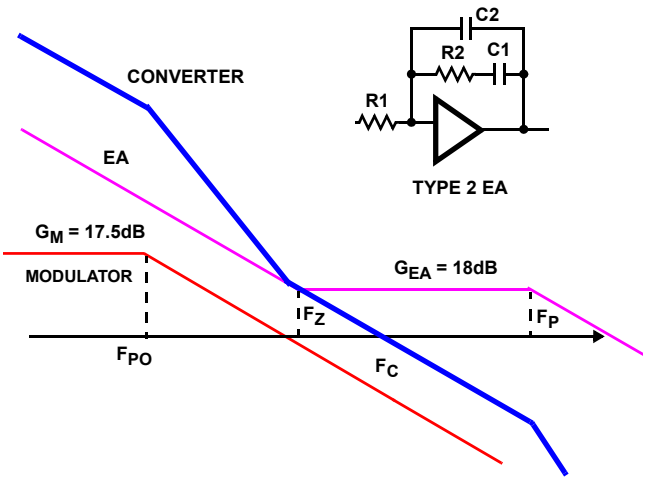


FIGURE 17. FEEDBACK LOOP COMPENSATION

The zero frequency, the amplifier high-frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase 'boost'.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase 'boost'. Some phase boost can also be achieved by connecting capacitor C_Z in parallel with the upper resistor R_1 of the divider that sets the output voltage value. Please refer to "Output Inductor Selection" and "Output Capacitor Selection" on page 16 for further details.

Linear Regulator

The linear regulator controller is a transconductance amplifier with a nominal gain of 2A/V. The N-Channel MOSFET output device can sink a minimum of 50mA. The reference voltage is 0.8V. With 0V differential at it's input, the controller sinks 21mA of current. An external PNP transistor or PFET pass element can be used. The dominant pole for the loop can be placed at the base of the PNP (or gate of the PFET), as a capacitor from emitter to base (source to gate of a PFET). Better load transient response is achieved, however, if the dominant pole is placed at the output, with a capacitor to ground at the output of the regulator.

Under no-load conditions, leakage currents from the pass transistors supply the output capacitors, even when the transistor is off. Generally this is not a problem since the feedback resistor drains the excess charge. However, charge may build up on the output capacitor making V_{LDO} rise above its set point. Care must be taken to ensure that the feedback resistor's current exceeds the pass transistors leakage current over the entire temperature range.

The linear regulator output can be supplied by the output of one of the PWMs. When using a PFET, the output of the linear regulator will track the PWM supply after the PWM output rises to a voltage greater than the threshold of the PFET pass device. The voltage differential between the PWM and the linear output will be the load current times the $r_{DS(ON)}$. Figure 18 shows the linear regulator (2.5V) start-up waveform and the PWM (3.3V) start-up waveform.

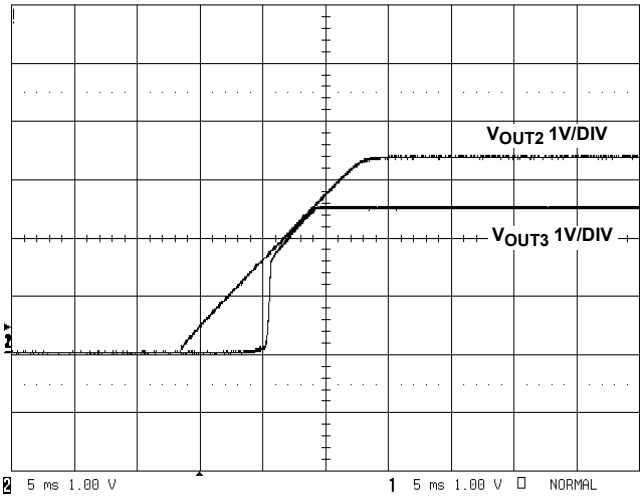


FIGURE 18. LINEAR REGULATOR START-UP WAVEFORM

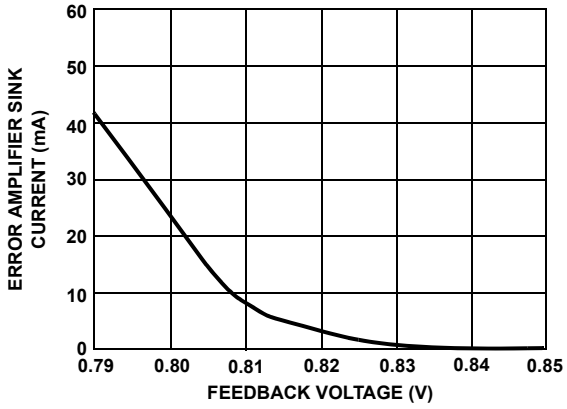


FIGURE 19. LINEAR CONTROLLER GAIN

Base-Drive Noise Reduction

The high-impedance base driver is susceptible to system noise, especially when the linear regulator is lightly loaded. Capacitively coupled switching noise or inductively coupled EMI onto the base drive causes fluctuations in the base current, which appear as noise on the linear regulator's output. Keep the base drive traces away from the step-down converter, and as short as possible, to minimize noise coupling. A resistor in series with the gate drivers reduces the switching noise generated by PWM. Additionally, a

bypass capacitor may be placed across the base-to-emitter resistor. This bypass capacitor, in addition to the transistor's input capacitor, could bring in a second pole that will destabilize the linear regulator. Therefore, the stability requirements determine the maximum base-to-emitter capacitance.

Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of a ISL6443A based DC/DC converter. The ISL6443A switches at a very high frequency and therefore the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also the peak gate drive current rises significantly in extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

There are two sets of critical components in a DC/DC converter using the ISL6443A. The switching power components and the small signal components. The switching power components are the most critical from a layout point of view because they switch a large amount of energy so they tend to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multi-layer printed circuit board is recommended.

Layout Considerations

1. The Input capacitors, Upper FET, Lower FET, Inductor and Output capacitor should be placed first. Isolate these power components on the topside of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitor very close to the MOSFETs.
2. Use separate ground planes for power ground and small signal ground. Connect the SGND and PGND together close to the IC. Do not connect them together anywhere else.
3. The loop formed by Input capacitor, the top FET and the bottom FET must be kept as small as possible.
4. Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and output capacitor are as short as possible with maximum allowable trace widths.
5. Place The PWM controller IC close to lower FET. The LGATE connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop current in this area.
6. Place VCC_5V bypass capacitor very close to VCC_5V pin of the IC and connect its ground to the PGND plane.
7. Place the gate drive components BOOT diode and BOOT capacitors together near controller IC
8. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper filled polygons or wide but short trace to connect the junction of upper FET, lower FET and output inductor. Also keep the PHASE node connection to the IC short. It is unnecessary to oversize the copper islands for PHASE node. Since the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise.
10. Route all high speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths, including feedback resistors, current limit setting resistors, and SYNC/SDx pull-down resistors should be connected to this SGND plane.
12. Ensure the feedback connection to the output capacitor is short and direct.

Component Selection Guidelines

MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements. Two N-Channel MOSFETs are used in each of the synchronous-rectified buck converters for the PWM1 and PWM2 outputs. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see Equations 10 and 11). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage. Equations 10 and 11 assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode.

$$P_{UPPER} = \frac{(I_O^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_O)(V_{IN})(t_{SW})(F_{SW})}{2} \quad \text{(EQ.10)}$$

$$P_{LOWER} = \frac{(I_O^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ.11)}$$

A large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by

calculating the temperature rise according to package thermal-resistance specifications.

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to it's new level. The ISL6443A will provide either 0% or 93% duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ.12)}$$

where, C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_O is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Equivalent Series Resistance) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 13:

$$V_{RIPPLE} = \Delta I_L(ESR) \quad \text{(EQ.13)}$$

where, I_L is calculated in "Output Inductor Selection" on page 16.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications at 300kHz for the bulk capacitors. In most cases, multiple small-case electrolytic capacitors perform better than a single large-case capacitor.

The stability requirement on the selection of the output capacitor is that the 'ESR zero' (f_Z) be between 1.2kHz and 30kHz. This range is set by an internal, single compensation zero at 6kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop. Therefore,

$$C_{OUT} = \frac{1}{2\Pi(ESR)(f_Z)} \quad \text{(EQ.14)}$$

In conclusion, the output capacitors must meet three criteria:

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.
3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

The recommended output capacitor value for the ISL6443A is between 150µF to 680µF, to meet stability criteria with external compensation. Use of aluminum electrolytic, POSCAP, or tantalum type capacitors is recommended. Use of low ESR ceramic capacitors is possible but would take more rigorous loop analysis to ensure stability.

Output Inductor Selection

The PWM converters require output inductors. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple voltage expression is given in "Output Capacitor Selection" on page 16 and the ripple current is approximated by Equation 15:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_S)(L)(V_{IN})} \quad \text{(EQ.15)}$$

For the ISL6443A, inductor values between 6.4µH to 10µH are recommended when using the "Typical Application Schematic" on page 4. Other values can be used but a thorough stability study should be done.

Input Capacitor Selection

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and 1.5x is a conservative guideline. The AC RMS Input current varies with the load. The total RMS current supplied by the input capacitance is:

$$I_{RMS} = \sqrt{I_{RMS1}^2 + I_{RMS2}^2} \quad \text{(EQ.16)}$$

where,

$$I_{RMSx} = \sqrt{DC - DC^2} \cdot I_O \quad \text{(EQ.17)}$$

DC is duty cycle of the respective PWM.

Depending on the specifics of the input power and its impedance, most (or all) of this current is supplied by the input capacitor(s). Figure 20 shows the advantage of having the PWM converters operating out-of-phase. If the converters were operating in-phase, the combined RMS current would be the algebraic sum, which is a much larger value as shown. The combined out-of-phase current is the square root of the sum of the square of the individual reflected currents and is significantly less than the combined in-phase current.

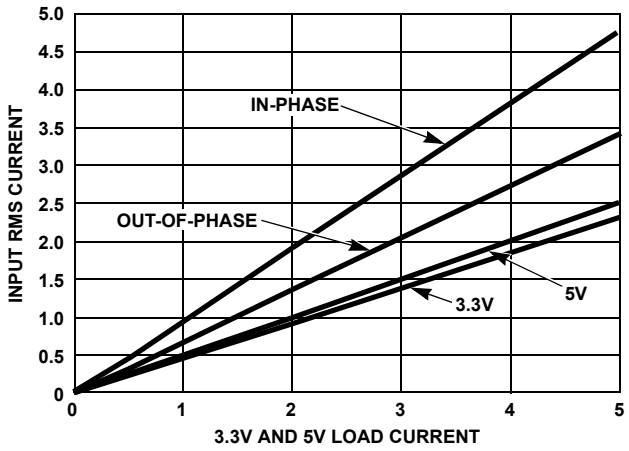


FIGURE 20. INPUT RMS CURRENT vs LOAD

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For board designs that allow through-hole components, the Sanyo OS-CON® series offer low ESR and good temperature performance. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX is surge-current tested.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 4, 2015	FN6600.3	Updated Ordering Information table on page 1. Added Revision History and About Intersil sections. Updated Package Outline Drawing M28.173 to the latest revision. -Rev 0 to Rev 1 changes - Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.

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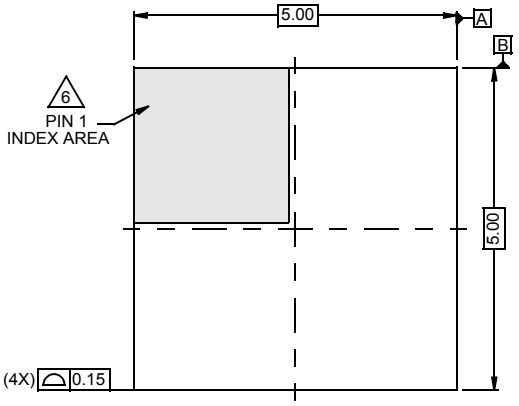
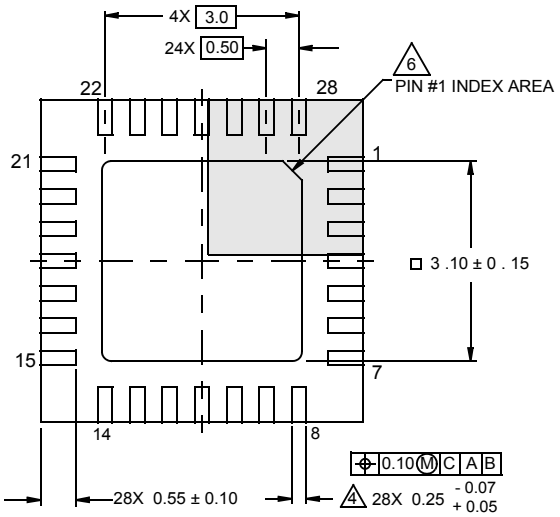
Package Outline Drawing

L28.5x5

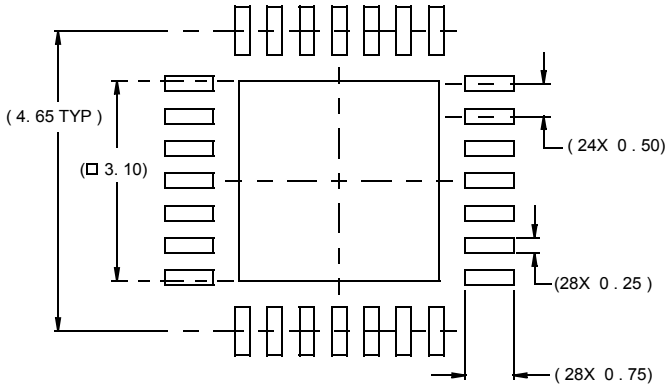
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/07



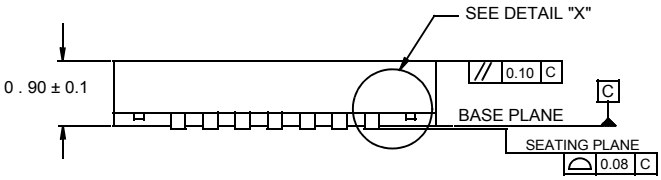
TOP VIEW



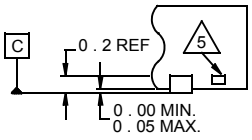
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

M28.173

28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
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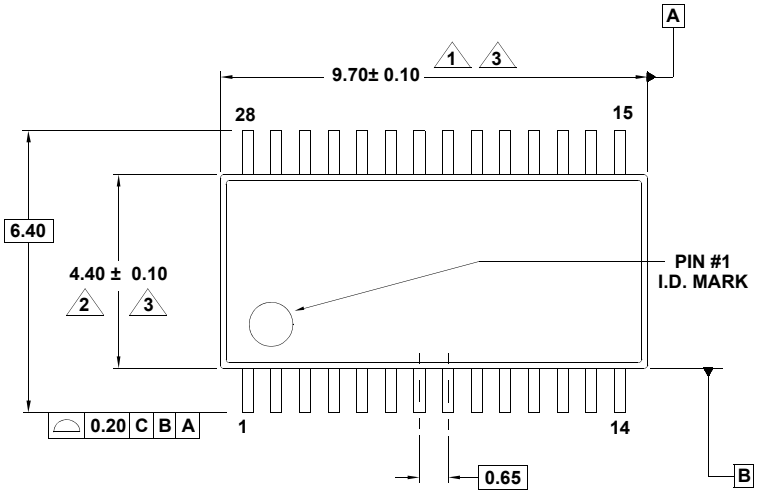
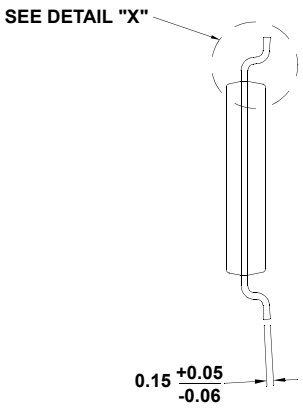
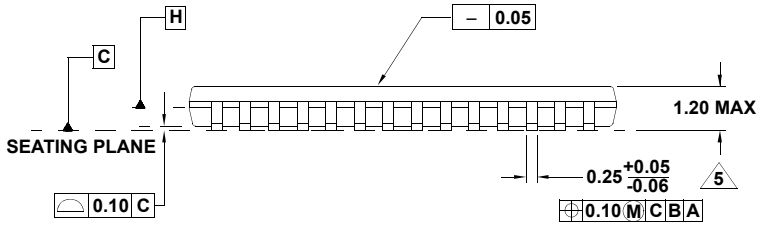


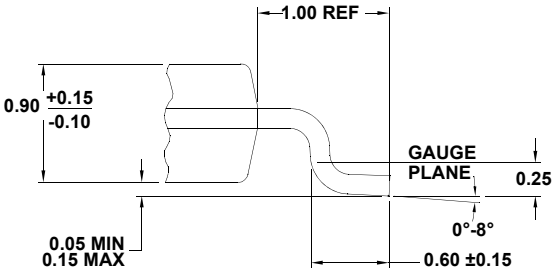
TOP VIEW



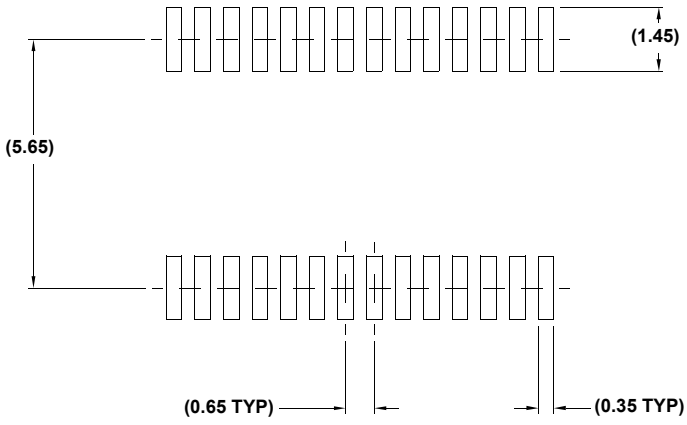
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.