FEB 8 1990

PRELIMINARY

MICRON TECHNOLOGY, INC.

MT45C8128

PSEUDO STATIC DRAM

128K x 8 PSDRAM

$\overline{CE}$/CS PSEUDO STATIC DRAM

FEATURES

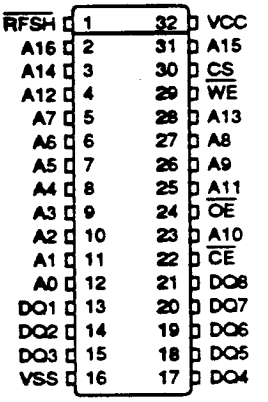
- Industry standard pin-out, timing, functions and package (pin compatible with 1MEG SRAM JEDEC pin-out)
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 0.5mW standby; 175mW active, typical
- All device pins are fully TTL and CMOS compatible
- CS selectable standby mode
- 512 cycle refresh in 8ms
- Refresh modes: AUTO, SELF and ADDRESS
- Internal refresh counter for AUTO refresh mode
- Internal refresh timer for SELF refresh mode
- Low standby current 200uA (maximum)

OPTIONS — MARKING

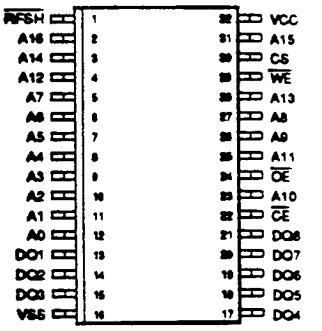
- Timing
  - 80ns access — -8
  - 100ns access — -10
  - 120ns access — -12
- Packages
  - Plastic DIP — None
  - Plastic SOIC — G
  - Plastic SOJ — DJ

PIN ASSIGNMENT (Top View)

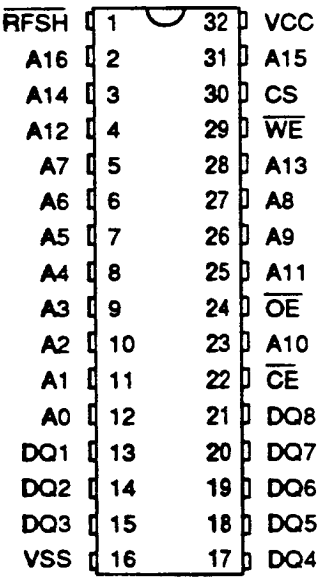
32 Pin SOJ*



32 Pin SOIC



32 Pin DIP*



*NOTE : These packages not released, consult factory

GENERAL DESCRIPTION

The MT45C8128 is a pseudo static, randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. The MT45C8128 is a low cost alternative to a 1MEG SRAM and a simpler design for small and medium size DRAM memory needs.

The pseudo static DRAM (PSDRAM) takes advantage of the best features of low cost DRAMs (low cost memory) and low power SRAMs (non-multiplexed address inputs, low power consumption and x8 organization). The PSDRAM incorporates a SELF refresh timer for easy refresh control.

The PSDRAM is identical to the 128K x 8 SRAM pinout, except the SRAM no connect pin (Pin 1 = NC) is replaced with the refresh pin ($\overline{RFSH}$). The $\overline{RFSH}$ control allows the PSDRAM to utilize AUTO and SELF refresh modes to refresh the DRAM cells, yet not interfere with its SRAM-like operation.

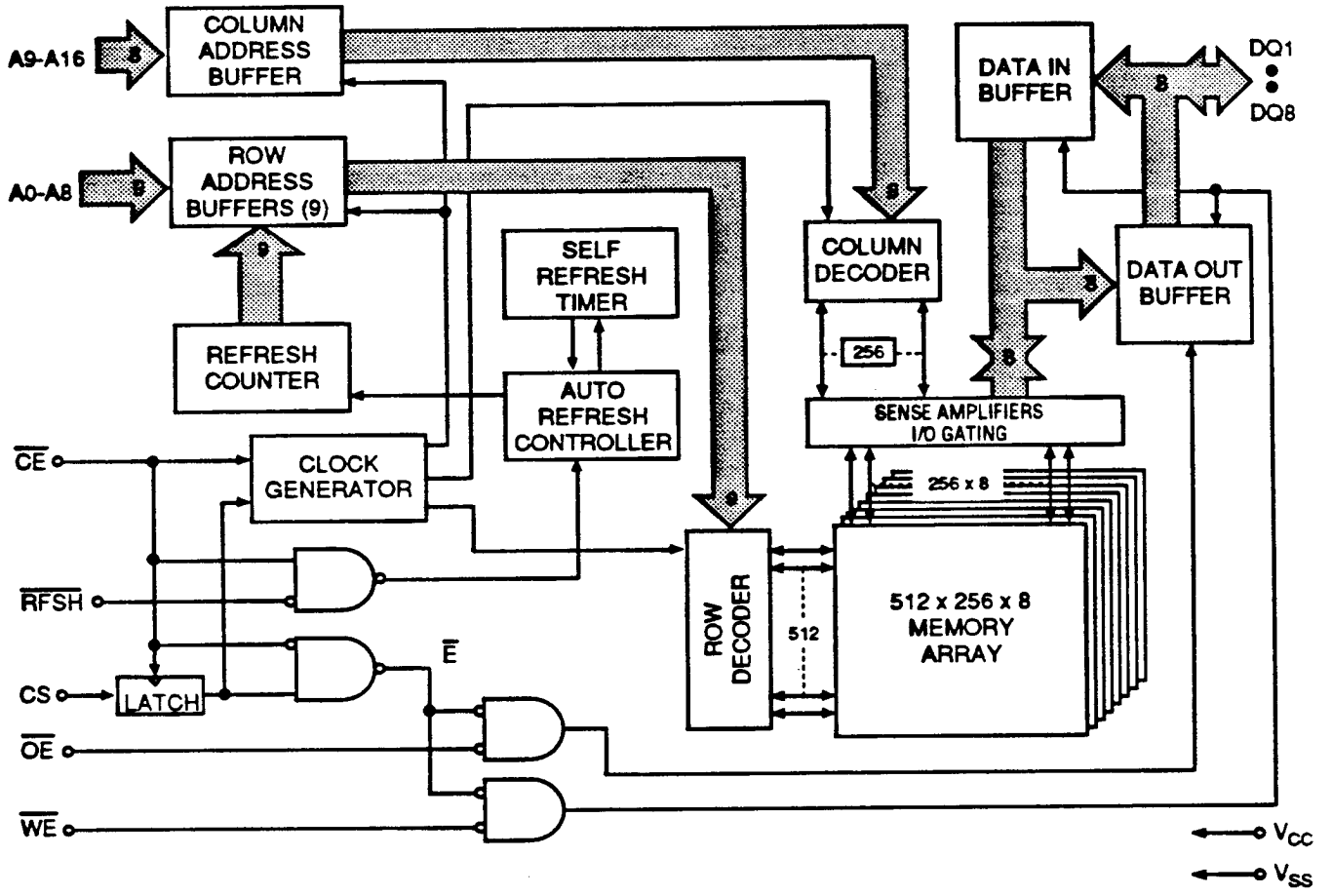


Figure 1
FUNCTIONAL BLOCK DIAGRAM
MT45C8128

PIN DESCRIPTIONS

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	$\overline{RFSH}$	Input	Refresh Input: $\overline{RFSH}$ pin activates one of two refresh cycles - AUTO or SELF refresh. $\overline{RFSH}$ going LOW while $\overline{CE}$ is HIGH will invoke the AUTO refresh mode (similar to DRAM CBR refresh). The SELF refresh mode will activate, via the internal refresh timer once the $\overline{RFSH}$ pin has been held LOW for at least 200us (AUTO refresh maximum is for 8us). The SELF refresh mode will typically refresh each row at a 100us cycle rate (512 cycles over 51.2ms).
12-5,27,26,23,25, 4,28,3,31,2	A0-A16	Input	Address Inputs: These inputs are clocked by the LOW going edge of $\overline{CE}$ when CS is active. A0 through A8 inputs address the Row Decoder and A9 through A16 inputs address the Column Decoder.
22	$\overline{CE}$	Input	Chip Enable: $\overline{CE}$ is the "master switch" allowing the device to perform either a READ or WRITE cycle, as long as it is held LOW. $\overline{CE}$ disabled (held HIGH) allows the device to enter the various refresh modes.
24	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ taken LOW activates the DQ output buffers, depending on the states of $\overline{CE}$ (must be LOW) and $\overline{WE}$. $\overline{OE}$ taken LOW during a READ cycle will activate the DQ outputs. $\overline{OE}$ taken LOW during a WRITE cycle will activate the DQ outputs while $\overline{WE}$ is held HIGH.
29	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ determines whether the device will be in a READ or WRITE cycle. $\overline{WE}$ held HIGH dictates a READ cycle and dictates a WRITE cycle when held LOW. $\overline{WE}$ will also tri-state (High-Z) the DQs while LOW for a WRITE cycle.
30	CS	Input	Chip Select: CS activates the device when a HIGH is latched in by the LOW going edge of $\overline{CE}$. CS will put the device in STANDBY mode when a LOW is latched in by the LOW going edge of $\overline{CE}$.
13-15,17-21	DQ1-DQ8	Input/ Output	Data Input/Output (DQ): These DQ pins are in one of three states, depending on the condition of the chip. WRITE cycles configure the DQs to be inputs (D) and READ cycles configure the I/Os to be Outputs (Q). The DQs will also be in the tri-state mode during certain portions of both READ and WRITE cycles, depending on the conditions of $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$. The DQs will be in the tri-state mode during a READ cycle until $\overline{OE}$ is taken LOW. The DQs will be in the tri-state mode during a WRITE cycle when $\overline{WE}$ is taken LOW, regardless of $\overline{OE}$. $\overline{CE}$ held HIGH will cause the DQs to be in the tri-state mode. $\overline{WE}$ going LOW simultaneously or prior to $\overline{CE}$ going LOW will cause the DQs to remain in tri-state.
32	Vcc	Supply	Power Supply: +5 Volts ± 10%
16	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT45C8128 PSDRAM operates in a similar manner to a 128K x 8 SRAM with the exception of the refresh and precharge (^tP) requirements. The MT45C8128 may be interchanged with the 128K x 8 SRAM in a system, provided that external circuitry has been added to the $\overline{RFSH}$ pin (NC on true SRAMs) to handle the refresh requirements.

Chip enable ($\overline{CE}$) taken LOW while chip select (CS) is HIGH will enable the device. This allows the device to perform either a READ, WRITE or READ-MODIFY-WRITE cycle depending on the state of write enable ($\overline{WE}$) and output enable ($\overline{OE}$).

A READ cycle is accomplished by holding $\overline{WE}$ and CS HIGH when $\overline{CE}$ and $\overline{OE}$ are taken LOW. A WRITE cycle is accomplished by holding CS HIGH when $\overline{WE}$ and $\overline{CE}$ are taken LOW ($\overline{OE}$ is don't care). A READ-MODIFY-WRITE cycle is a READ cycle except the $\overline{WE}$ pin is taken LOW after valid data has been read allowing the memory location being read to be rewritten with new data. CS held LOW when $\overline{CE}$ is brought LOW will put the device into a CS standby mode.

The PSDRAM must be fully refreshed every 8ms while in the operating mode. The refresh cycles may be executed in either burst mode (all at once) or distributive (spread throughout the 8ms period). Any READ, WRITE or READ-MODIFY-WRITE cycle will refresh the row being addressed. Additionally, the PSDRAM has three specific refresh modes available: ADDRESS, AUTO and SELF. The ADDRESS refresh is a READ cycle with $\overline{OE}$ held HIGH; the row being addressed is the row being refreshed (similar to the $\overline{RAS}$-ONLY refresh on a DRAM). The ADDRESS refresh cycle recognizes A0 through A9 to address the 512 rows requiring refresh (A10 through A16 are don't care).

The AUTO and SELF refresh modes utilyze the $\overline{RFSH}$ pin. The $\overline{RFSH}$ pin is the main functional difference between the PSDRAM and the SRAM. The $\overline{RFSH}$ pin is a don't care once $\overline{CE}$ is LOW (provided ^tRHC is met). The $\overline{RFSH}$ pin held HIGH once $\overline{CE}$ is taken HIGH (device inactive) will put the device into low power standby. $\overline{RFSH}$ taken back LOW will put the device into either AUTO or SELF refresh mode.

The PSDRAM enters AUTO refresh (similar to $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh of a DRAM) when $\overline{RFSH}$ is toggled from HIGH to LOW then back to HIGH. Each subsequent toggle of the $\overline{RFSH}$ pin will result in one ROW being refreshed (controlled by an internal refresh address counter). The LOW period of the $\overline{RFSH}$ toggle during AUTO refresh must not exceed 8µs.

The PSDRAM enters the SELF refresh mode once the $\overline{RFSH}$ pin has been held LOW continuously (somewhere between 8µs and 200µs) and will typically refresh all 512 rows in 51.2ms via an internal counter and timer. Once the SELF refresh cycle is terminated, an AUTO or ADDRESS refresh sequence of all 512 rows must be completed within 8ms, regardless of the length of time the PSDRAM was in SELF refresh. Until another SELF refresh cycle is initiated, AUTO or ADDRESS refresh cycles must be used thereafter to refresh all 512 rows within every 8ms period.

TRUTH TABLE

Function	$\overline{CE}$	CS	$\overline{WE}$	$\overline{OE}$	$\overline{RFSH}$	ADDRESS	DQs	NOTES
Standby	H	X	X	X	H	X	High-Z	
CS Standby	L	L	X	X	X	X	High-Z	
ADDR. Refresh	L	H	H	H	H	VALID	High-Z	1
AUTO Refresh	H	X	X	X	H→L→H	X	High-Z	2
SELF Refresh	H	X	X	X	H→L	X	High-Z	3
READ	L	H	H	L	H	VALID	Valid Data Out	
WRITE (#1)	L	H	L	H	H	VALID	Valid Data In	4
WRITE (#2)	L	H	L	X	H	VALID	Valid Data In	5
WRITE (#3)	L	H	L	L	H	VALID	Valid Data In	6
READ-WRITE	L	H→X	H→L	L→H	H	VALID	Valid Data Out, Valid Data In	

NOTES: 0. "X" means don't care.
1. A0 through A8 only (ROW), A9 through A16 are don't care. Also referred to as "$\overline{CE}$-only-refresh".
2. Each $\overline{RFSH}$ pulse (HIGH to LOW) results in the next AUTO Refresh Controlled ROW to be refreshed.
3. $\overline{RFSH}$ must be kept LOW for 200µs in order for the device to switch from AUTO to SELF refresh.
4. $\overline{OE}$ is fixed HIGH.
5. $\overline{OE}$ is clocked.
6. $\overline{OE}$ is fixed LOW.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, TA(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes : 1) ($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	Vcc+1	V	1,9
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1,9
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ Vcc, all other pins not under test = 0 volts)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	1

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; Vcc = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{CE}$ with Address Cycling: t_{RC} = $t_{RC(MIN)}$)	Icc	70	60	50	mA	3,4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{CE}$ = $\overline{RFSH}$ = V_{IH})	Isb1	1	1	1	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{CE}$ = $\overline{RFSH}$ = Vcc -0.2V)	Isb2	200	200	200	µA	3,4
SELF REFRESH CURRENT (TTL) Power supply standby current ($\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL})	Icc2	1	1	1	mA	3,4
SELF REFRESH CURRENT (CMOS) Power supply standby current ($\overline{CE}$ = Vcc -0.2V, $\overline{RFSH}$ = 0.2V)	Icc3	200	200	200	µA	3,4

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_{16}	C_{I1}		5	pF	2
Input Capacitance: $\overline{CE}$, CS, $\overline{RFSH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

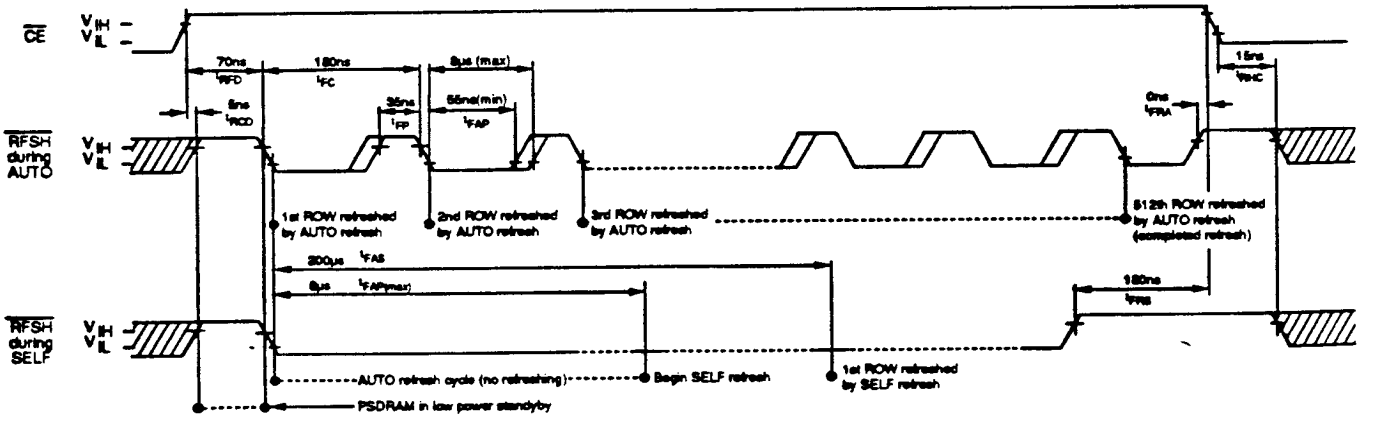
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	150		180		210		ns	
READ-WRITE cycle time	t_{RWC}	195		235		280		ns	
$\overline{CE}$ pulse width	t_{CE}	80	10,000	100	10,000	120	10,000	ns	
$\overline{CE}$ precharge time	t_P	60		70		80		ns	
$\overline{CE}$ access time	t_{CEA}		80		100		120	ns	
$\overline{OE}$ access time	t_{OEA}		30		35		45	ns	
$\overline{CE}$ to LOW-Z output	t_{CLZ}	10		10		10		ns	
$\overline{OE}$ to LOW-Z output	t_{OLZ}	0		0		0		ns	
Output active from end of WRITE	t_{WLZ}	0		0		0		ns	
Chip disable to HIGH-Z output	t_{CHZ}	0	25	0	30	0	35	ns	12
$\overline{OE}$ disable to HIGH-Z output	t_{OHZ}	0	25	0	30	0	35	ns	12
$\overline{WE}$ to HIGH-Z output	t_{WHZ}	0	25	0	30	0	35	ns	12
$\overline{OE}$ to disable output set-up time	t_{ODS}	0		0		0		ns	
$\overline{OE}$ to disable output hold time	t_{ODH}	10		10		10		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
Chip select set-up time	t_{CSS}	0		0		0		ns	
Chip select hold time	t_{CSH}	20		25		30		ns	
Write pulse width	t_{WP}	25		30		35		ns	
Write command hold time	t_{WCH}	80	10,000	100	10,000	120	10,000	ns	
Write command to $\overline{CE}$ lead time	t_{CWL}	25	10,000	30	10,000	35	10,000	ns	
Data set-up time from $\overline{WE}$	t_{DSW}	30		35		45		ns	13
Data set-up time from $\overline{CE}$	t_{DSC}	30		35		45		ns	13
Data hold time from $\overline{WE}$	t_{DHW}	0		0		0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	
Address set-up time	t_{ASC}	0		0		0		ns	14
Address hold time	t_{AHC}	20		25		30		ns	14
$\overline{RFSH}$ command hold time	t_{RHC}	15		15		15		ns	15
$\overline{RFSH}$ command delay time	t_{RCD}		5		5		5	ns	
AUTO refresh cycle time	t_{FC}	150		180		210		ns	16
$\overline{RFSH}$ delay time from $\overline{CE}$	t_{RFD}	60		70		80		ns	
$\overline{RFSH}$ pulse width (AUTO refresh)	t_{FAP}	55	8,000	55	8,000	55	8,000	ns	5,16
$\overline{RFSH}$ precharge time	t_{FP}	35		35		35		ns	15
$\overline{RFSH}$ pulse width (SELF refresh)	t_{FAS}	200		200		200		us	5,16
$\overline{CE}$ delay from $\overline{RFSH}$ (SELF refresh)	t_{FRS}	150		180		210		ns	15
$\overline{CE}$ delay from $\overline{RFSH}$ (AUTO refresh)	t_{FRA}	0		0		0		ns	15
Refresh period (512 cycles, A0-A8)	t_{REF}		8		8		8	ms	
Transition times (rise and fall)	t_T	3	50	3	50	3	50	ns	

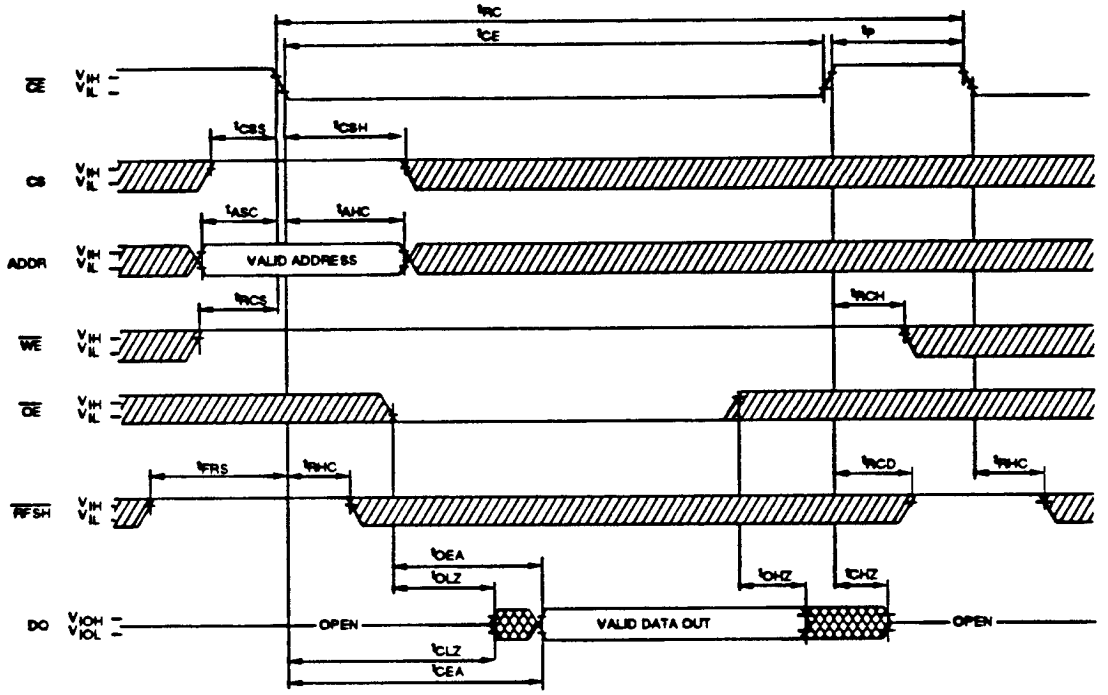
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{\Delta t}/_{\Delta v}$ with dv = 3V and Vcc = 5V.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs with $\overline{CE}$ HIGH followed by 8 pulses on $\overline{RFSH}$, or an initial pause of 1ms with $\overline{CE}$ HIGH while $\overline{RFSH}$ held LOW, are required after power-up before proper device operation is assured.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. Measured with a load equivalent to 2 TTL gates and 100pF.
12. The timing parameters ^tCHZ, ^tOHZ, ^tWHZ are referenced to the point at which the outputs tristate and are not referenced to valid output voltage levels. The rate of change and final output level will depend on the output loads connected to the outputs.
13. Valid data-in for a WRITE cycle is latched by the first rising edge of either $\overline{WE}$ or $\overline{CE}$.
14. Valid addresses are latched by the falling edge of $\overline{CE}$.
15. The timing parameter ^tFRS ($\overline{RFSH}$ HIGH setup to $\overline{CE}$ active) is required for the first operating cycle (READ,WRITE or READ-MODIFY-WRITE) once coming out of either a SELF refresh cycle or a power-up. Subsequent operating cycles do not require tFRS to be met and the setup/delay is determined by ^tFRA (AUTO refresh) or ^tP-^tRCD (operating cycles).
16. There are two refresh modes utilizing the internal AUTO REFRESH CONTROLLER and are controlled by the $\overline{RFSH}$ pin. Clocking of the $\overline{RFSH}$ pin will provide CBR-like refresh (AUTO), provided ^tFAP max.($\overline{RFSH}$ LOW period) is not violated. Once ^tFAP max. is exceeded, the device will enter SELF refresh and will have started SELF refresh by ^tFAS min.

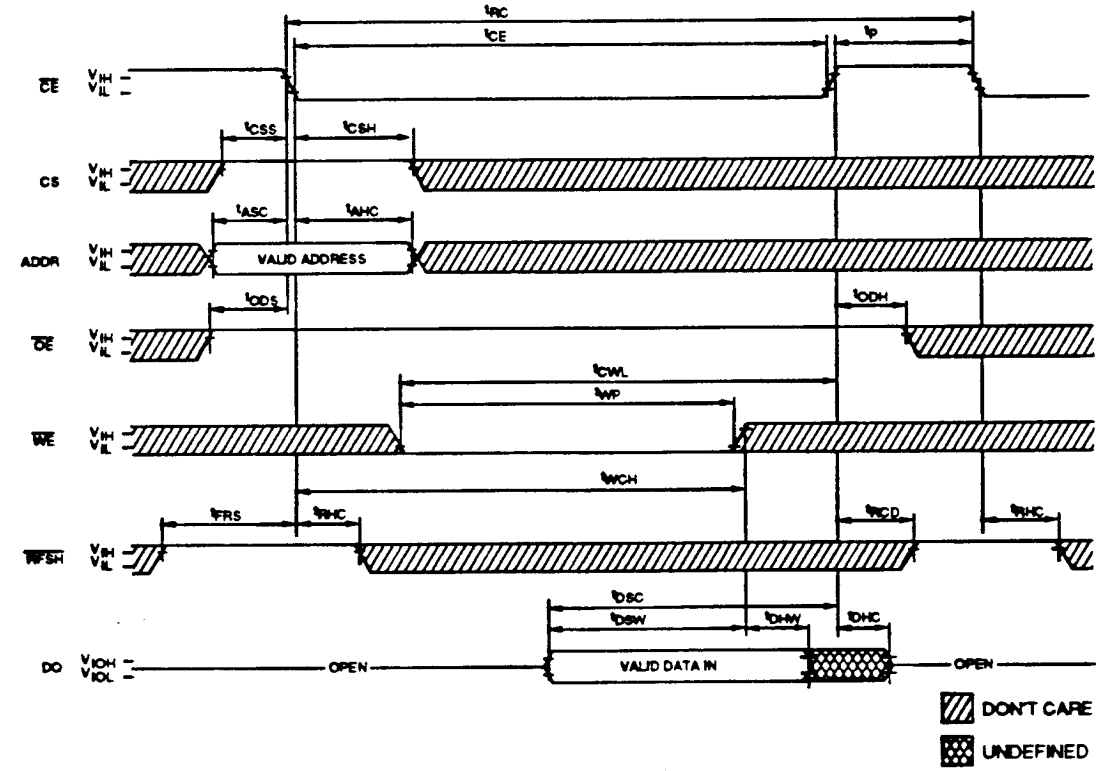
EXAMPLE OF AUTO vs SELF REFRESH CYCLES ON 100ns DEVICES



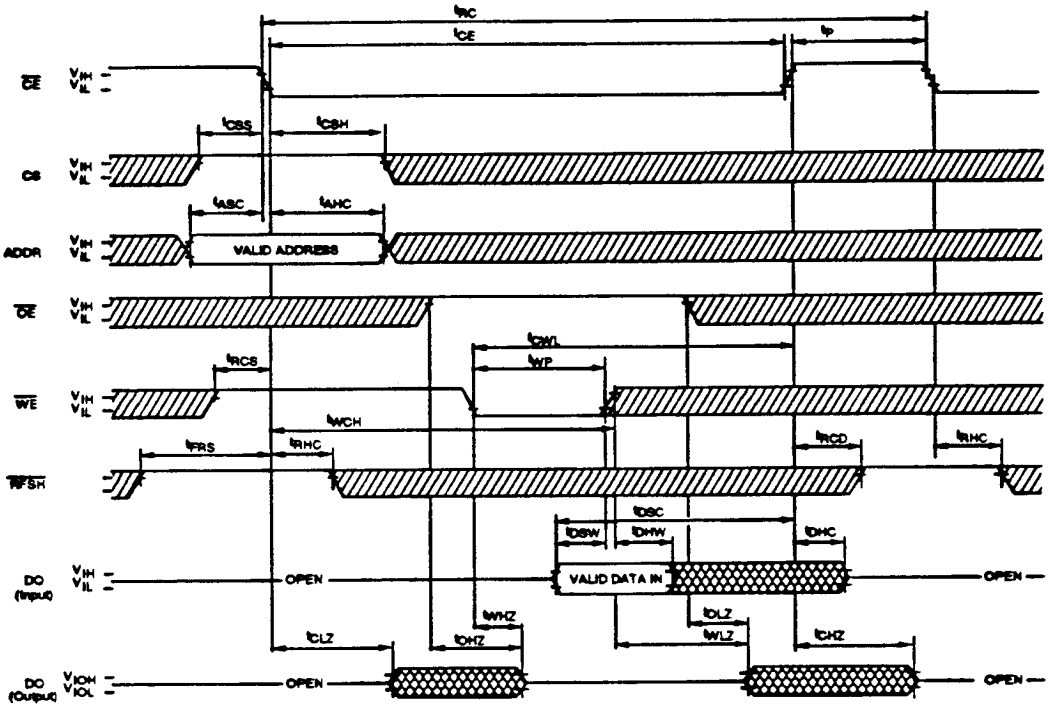
READ CYCLE



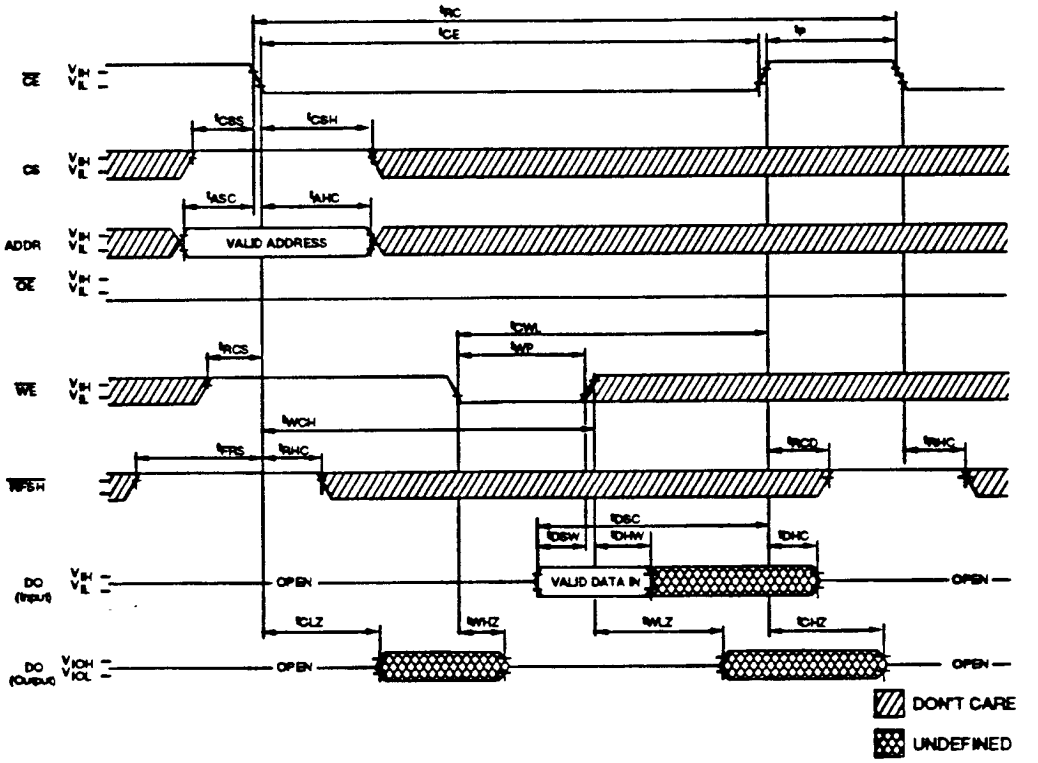
WRITE CYCLE #1 ($\overline{OE}$ HIGH)



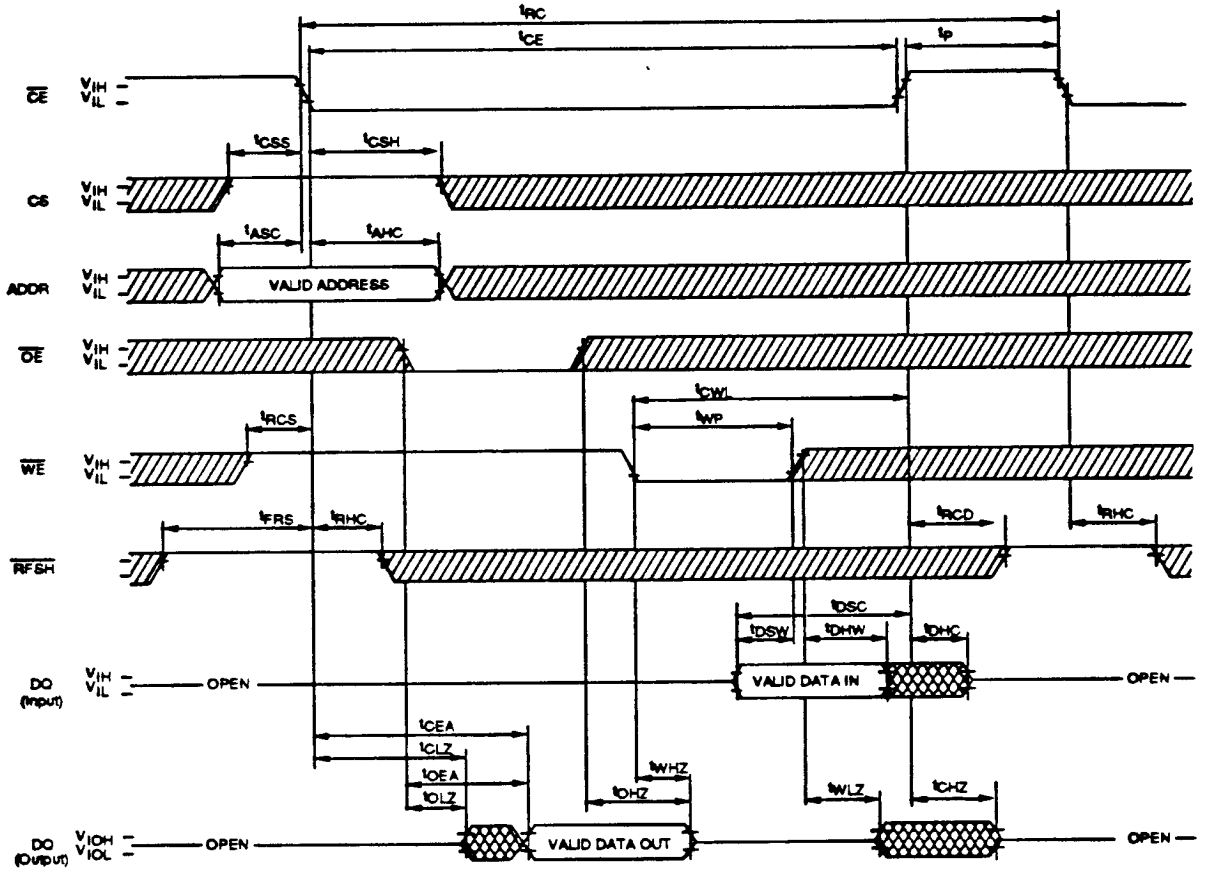
WRITE CYCLE #2 ($\overline{OE}$ CLOCKED)



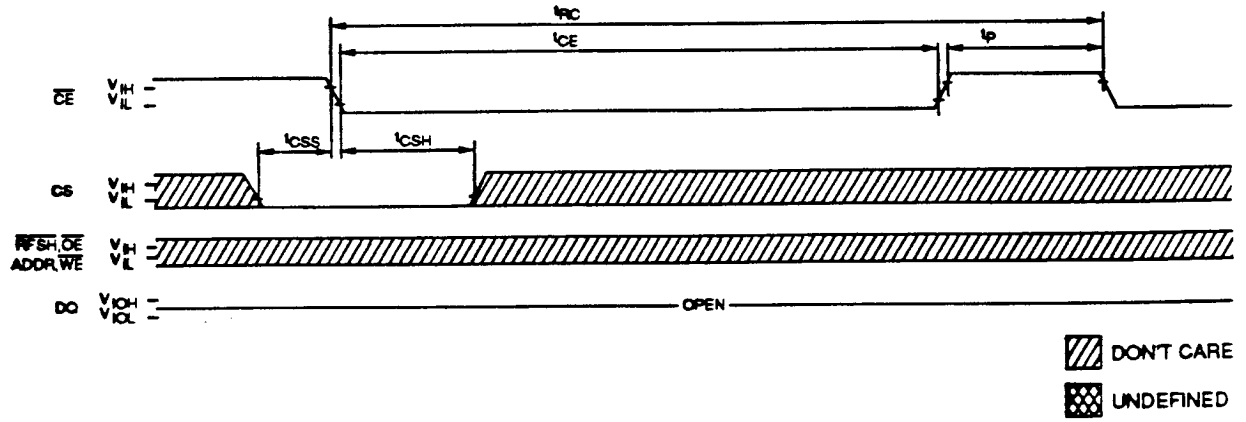
WRITE CYCLE #3 ($\overline{OE}$ LOW)



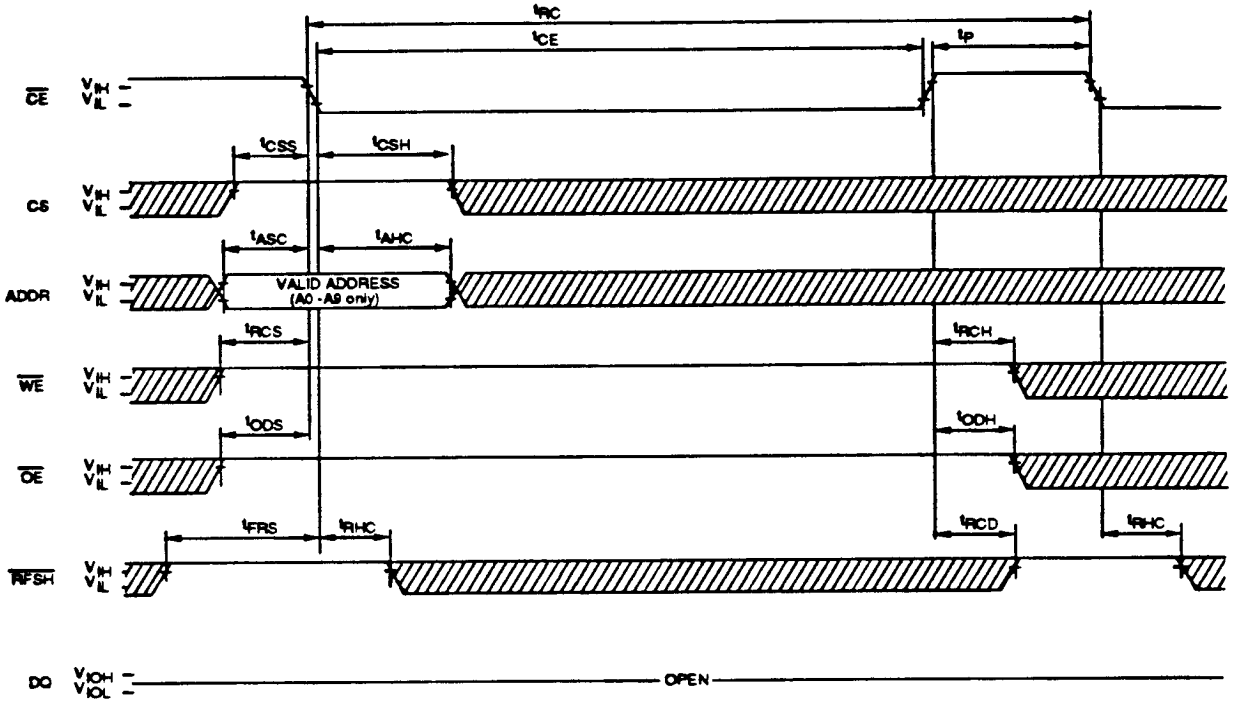
READ-MODIFY-WRITE CYCLE



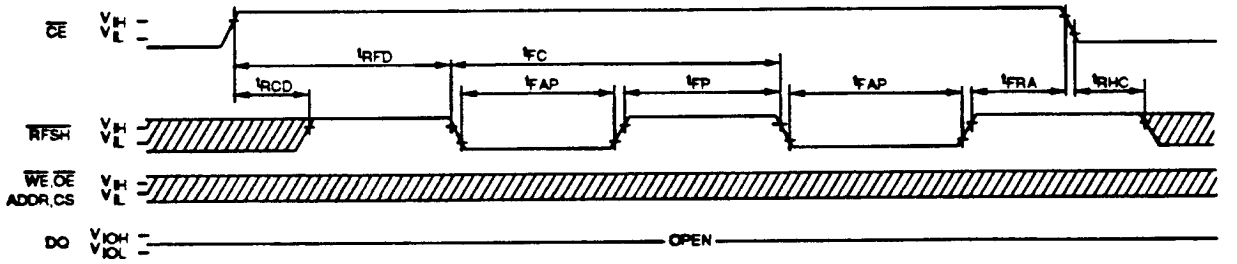
CS STANDBY CYCLE



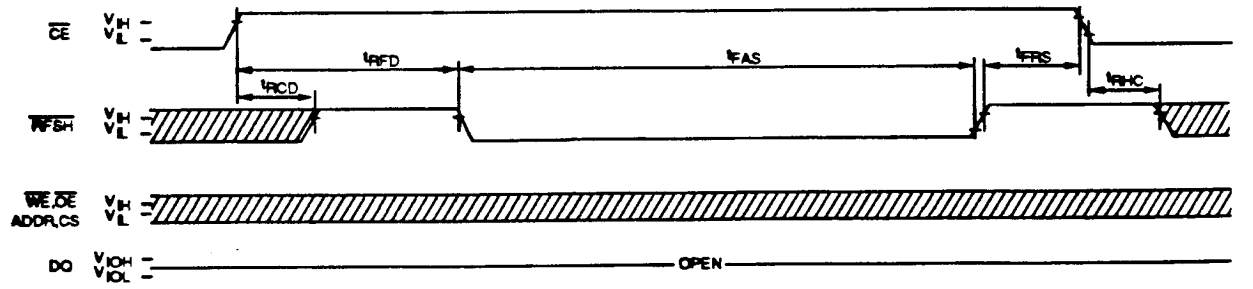
ADDRESS ($\overline{CE}$ ONLY) REFRESH CYCLE



AUTO REFRESH CYCLE



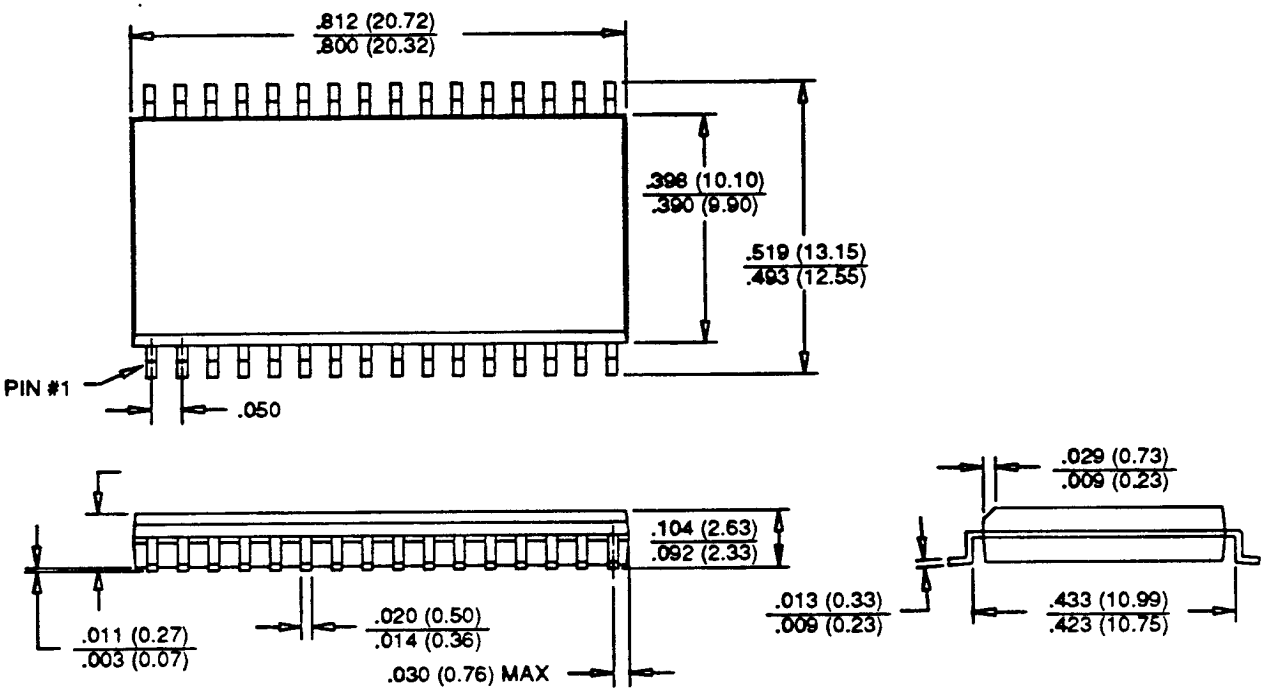
SELF REFRESH CYCLE



DON'T CARE

UNDEFINED

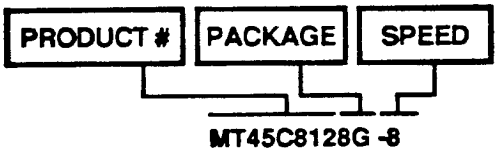
32-PIN PLASTIC SOIC
(450 mil)



Note: Consult factory for dimensions of 525 mil SOIC package

ORDER INFORMATION

Pseudo Static, 80 ns in Plastic SOIC



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. Micron DRAMs are functionally equivalent to other manufacturers' products meeting JEDEC standards. Several parameters are sampled; however, functionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives continuous AMBYX™ sytem level testing during many hours of accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.