### TOSHIBA PHOTOCOUPLER GaAlAs IRED & PHOTO-IC

# **TLP718F**

Isolated Bus Drivers

High Speed Line Receivers

Microprocessor System Interfaces

The Toshiba TLP718F consists of a GaAlAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP718F is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/µs.

The TLP718F is inverter logic type. For buffer logic type, the TLP715F is in line-up.

Absolute maximum ratings and electrical characteristics are the same as in the TLP718 technical data sheets.

- Inverter logic type (totem pole output)
- Guaranteed performance over temperature : −40 to 100°C
- Power supply voltage: 4.5 to 20 V
- Input current: I<sub>FHL</sub> = 3mA (max)
- Switching time (t<sub>pHL</sub> / t<sub>pLH</sub>): 250 ns (max)
- Common-mode transient immunity: ±10 kV/µs (min)
- Isolation voltage : 5000 Vrms (min)
- UL recognized UL1577, File No.E67349
- c-UL recognized
   CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4)

TÜV recognized / VDE under application : DIN EN60747-5-5 Maximum Operating Insulation Voltage :  $1140V_{pk}$  Highest Permissible Over Voltage :  $8000V_{pk}$  (Note) : When a EN60747-5-5 approved type is needed,

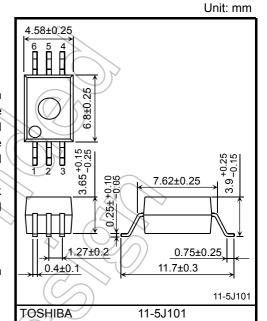
(Note) : When a EN60747-5-5 approved type is needed, Please designate "Option(D4)"

Construction Mechanical Rating

	7,62 mm pitch standard type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

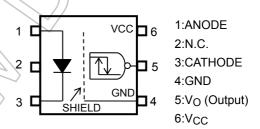
### **Truth Table**

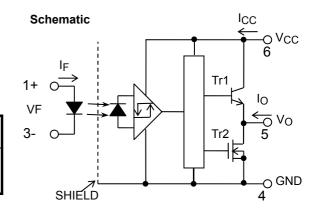
Input	LED	Tr1	Tr2	Output
Н	ON	OFF	ON	L
L	OFF	ON	OFF	Н



Weight: 0.26 g (typ.)

## Pin Configuration (Top View)





 $0.1 \, \mu F$  bypass capacitor must be connected between pins 6 and 4.

Start of commercial production 2008/12

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