







SLOS382 - SEPTEMBER 2001

LOW-NOISE, HIGH-SPEED, 450 mA CURRENT FEEDBACK AMPLIFIERS

FEATURES

- Low Noise
 - 2.9 pA/√Hz Noninverting Current Noise
 - 10.8 pA/√Hz Inverting Current Noise
 - 2.2 nV/√Hz Voltage Noise
- High Output Current, 450 mA
- High Speed
 - 128 MHz , -3 dB BW(R_L = 50 Ω , R_F = 470 Ω)
 - 1550 V/μs Slew Rate (G = 2, $R_1 = 50 Ω$)
- Wide Output Swing
 - 26 V_{PP} Output Voltage, R_L = 50 Ω
- Low Distortion
 - -80 dBc (1 MHz, 2 V_{PP}, G = 2)
- Low Power Shutdown Mode (THS3125)
 - 370-μA Shutdown Supply Current
- Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD Package

APPLICATIONS

- Video Distribution
- Instrumentation

- Line Drivers
- Motor Drivers
- Piezo Drivers

DESCRIPTION

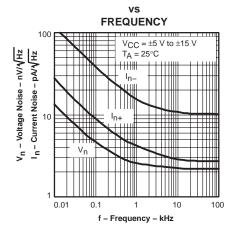
The THS3122/5 are low-noise, high-speed current feedback amplifiers, with high output current drive. This makes them ideal for any application that requires low distortion over a wide frequency with heavy loads. The THS3122/5 can drive four serially terminated video lines while maintaining a differential gain error less than 0.03%.

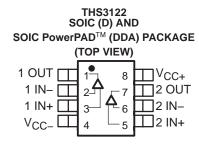
The high output drive capability of the THS3122/5 enables the devices to drive $50-\Omega$ loads with low distortion over a wide range of output voltages:

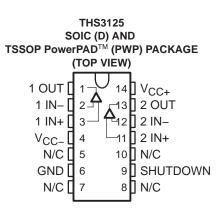
- -80 -dBc THD at 2 VPP
- -75 -dBc THD at 8 VPP

The THS3122/5 can operate from ± 5 V to ± 15 V supply voltages while drawing as little as 7.2 mA of supply current per channel. They offer a low power shutdown mode, reducing the supply current to only 370 μ A. The THS3122/5 are packaged in a standard SOIC, SOIC PowerPADTM, and TSSOP PowerPAD packages.

VOLTAGE NOISE AND CURRENT NOISE









Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



AVAILABLE OPTIONS

		EVALUATION.			
TA	SOIC-8 (D)	SOIC-8 PowerPAD SOIC-14 (DDA) (D)		TSSOP-14 (PWP)	EVALUATION MODULES
0°C to 70°C	THS3122CD	THS3122CDDA	THS3125CD	THS3125CPWP	THS3122EVM
-40°C to 85°C	THS3122ID	THS3122IDDA	THS3125ID	THS3125IPWP	THS3125EVM

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC+} to V _{CC-}	33 V
Input voltage	
Output current (see Note 1)	00
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T _A : Commercial	0°C to 70°C
Industrial	40°C to 85°C
Storage temperature, T _{stq} : Commercial	65°C to 125°C
Industrial	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS3122 and THS3125 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	AL^{θ}	T _A = 25°C POWER RATING
D-8	95°C/W [‡]	1.32 W
DDA	67°C/W	1.87 W
D-14	66.6°C/W [‡]	1.88 W
PWP	37.5°C/W	3.3 W

[‡] This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Overally and V	Dual supply	±5		±15	
Supply voltage, V _{CC+} to V _{CC-}	Single supply	10		30	V
0 1 1 1 1 1	C-suffix	0		70	20
Operating free-air temperature, T _A	I-suffix	-40		85	°C
Object description of a few days and affect to the OND of	High level (device shutdown)	2			
Shutdown pin input levels, relative to the GND pin	Low level (device active)			0.8	V



electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ± 15 V, R_F= 750 Ω , R_L = 100 Ω (unless otherwise noted)

dynamic performance

	PARAMETER		TEST CONDITI	ONS	MIN TYP MAX	UNIT
		D. 50.0	R _F = 50 Ω,	V _{CC} = ±5 V	138	
	On all along the addition (O dD)	$R_L = 50 \Omega$	G = 1	V _{CC} = ±15 V	160	
	Small-signal bandwidth (–3 dB)	D. 50.0	R _F =470 Ω,	V _{CC} = ±5 V	126	M1.1-
D\A/		$R_L = 50 \Omega$	G = 2	V _{CC} = ±15 V	128	MHz
BW	Baradaddh (0.4 dB)	•	R _F = 470 Ω,	V _{CC} = ±5 V	20	
	Bandwidth (0.1 dB)		G = 2	V _{CC} = ±15 V	30	
			V _{O(PP)} = 4 V	V _{CC} = ±5 V	47	
	Full power bandwidth	G = -1	V _{O(pp)} = 20 V	$V_{CC} = \pm 15 \text{ V}$	64	MHz
			V _O = 10 V _{PP}	$V_{CC} = \pm 15 \text{ V}$	1550	
SR	Slew rate (see Note 2), G=8	G = 2 $R_F = 680 \Omega$	V- 5.V	$V_{CC} = \pm 5 \text{ V}$	500	V/μs
		117 - 000 32	$V_O = 5 V_{PP}$	$V_{CC} = \pm 15 \text{ V}$	1000	
	Cattling time to 0.49/		V _O = 2 V _{PP}	$V_{CC} = \pm 5 \text{ V}$	53	
t _S	Settling time to 0.1%	G = -1	$V_O = 5 V_{PP}$	$V_{CC} = \pm 15 \text{ V}$	64	ns

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

	PARAMET	ER .		TEST CONDITIO	NS	MIN TYP	MAX	UNIT
				$R_{F} = 470 \Omega$,	V _{O(PP)} = 2 V	-80		
THD	Total harmonic distort	ion	$V_{CC} = \pm 15 \text{ V}$, f = 1 MHz	V _{O(PP)} = 8 V	-75		dD.
טחו	rotal narmonic distort	On		$R_{F} = 470 \Omega$,	$V_{O(PP)} = 2 V$	-77		dBc
			$V_{CC} = \pm 5 V$,	f = 1 MHz	V _{O(PP)} = 5 V	-76		
Vn	Input voltage noise		$V_{CC} = \pm 5 \text{ V}, =$	±15 V	f = 10 kHz	2.2		nV/√Hz
	lament assument mains	Noninverting Input	V 15 V	145.1/	4.0141-	2.9		pA/√Hz
In	Input current noise	Inverting Input	$V_{CC} = \pm 5 \text{ V}, $	±15 V	f = 10 kHz	10.8		pavv⊓z
	Crosstell.		G = 2,	f = 1 MHz,	$V_{CC} = \pm 5 \text{ V}$	-67		dD.
	Crosstalk		$V_O = 2 V_{PP}$		$V_{CC} = \pm 15 \text{ V}$	-67		dBc
	Differential main arms		G = 2	$R_1 = 150 \Omega$	$V_{CC} = \pm 5 \text{ V}$	0.01%		
	Differential gain error		40 IRE modu	_	$V_{CC} = \pm 15 \text{ V}$	0.01%		
	Differential phase area		±100 IRE Rai		$V_{CC} = \pm 5 \text{ V}$	0.011°		
	Differential phase erro)[NTSC and PAL		V _{CC} = ±15 V	0.011°		



electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ± 15 V, R_F = 750 Ω , R_L = 100 Ω (unless otherwise noted) (continued)

dc performance

	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
	land to the standard		T _A = 25°C		4.4	6	
	Input offset voltage	V _{IC} = 0 V,	T _A = full range			8	\
VIO	Channel offert valte as a setable a	$V_{O} = 0 V,$ $V_{CC} = \pm 5 V,$	T _A = 25°C		0.4	2	mV
	Channel offset voltage matching	V _{CC} = ±15 V	T _A = full range			3	
	Offset drift		T _A = full range		10		μV/°C
	IN Janua hisa ayyara	V _{IC} = 0 V,	T _A = 25°C		6	23	
l.	IN- Input bias current	$V_{O} = 0 V$	T _A = full range			30	
I _{IB}	INTo Lorent his a summer	$V_{CC} = \pm 5 \text{ V},$	T _A = 25°C		0.33	2	μΑ
	IN+ Input bias current	$V_{CC} = \pm 15 \text{ V}$	T _A = full range			3	
	land offer a summer	$V_{IC} = 0 V,$ $V_{O} = 0 V,$	T _A = 25°C		5.4	22	4
lio	Input offset current	$V_{CC} = \pm 5 \text{ V},$ $V_{CC} = \pm 15 \text{ V}$	T _A = full range			30	μА
Z _{OL}	Open loop transimpedance	V _{CC} = ±5 V, V _{CC} = ±15 V	R _L = 1 kΩ,		1		МΩ

input characteristics

	PARAMETER	TEST CONDI	TIONS	MIN	TYP	MAX	UNIT
V	Vice Input common mode voltage range		T full man ma	±2.5	±2.7		.,
VICR	Input common-mode voltage range	$V_{CC} = \pm 15 \text{ V}$	T _A = full range	±12.5	±12.7		V
		V _{CC} = ±5 V,		58	62		
CMRR	Common-mode rejection ratio	$V_{I} = -2.5 \text{ V to } 2.5 \text{ V}$	T _A = full range	56			dB
CIVIKK	Common-mode rejection ratio	$V_{CC} = \pm 15 \text{ V},$	T _A = 25°C	63	67		uБ
		$V_{\parallel} = -12.5 \text{ V to } 12.5 \text{ V}$	T _A = full range	60			
Б.	lanut rasistanas	IN+			1.5		MΩ
RĮ	Input resistance	IN-			15		Ω
Ci	Input capacitance		•		2		pF

output characteristics

	PARAMETER	TE	TEST CONDITIONS			TYP	MAX	UNIT
		$G = 4$, $V_I = 1.06 V$, $V_{CC} = \pm 5 V$	R _L = 1 kΩ,	T _A = 25°C		4.1		V
		G = 4, V _I = 1.025 V,	D 500	T _A = 25°C	3.8	4		
.,	Output well-and autom	$V_{CC} = \pm 5 \text{ V}$	$R_L = 50 \Omega$,	T _A = full range	3.7			V
VO	Output voltage swing	$G = 4$, $V_I = 3.6 V$, $V_{CC} = \pm 15 V$	R _L = 1 kΩ,	T _A = 25°C		14.2		V
		G = 4, V _I = 3.325 V,	D 50.0	T _A = 25°C	12	13.3		.,
		$V_{CC} = \pm 15 \text{ V}$	$R_L = 50 \Omega$,	T _A = full range	11.5			V
		$G = 4$, $V_I = 1.025 V$, $V_{CC} = \pm 5 V$	R _L = 10 Ω,	T _A = 25°C	200	280		mA
Ю	Output current drive	$G = 4$, $V_I = 3.325 V$, $V_{CC} = \pm 15 V$	$R_L = 25 \Omega$,	T _A = 25°C	360	440		mA
ro	Output resistance		open loop	T _A = 25°C		14		Ω



4

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ± 15 V, R_F = 750 Ω , R_L = 100 Ω (unless otherwise noted) (continued)

power supply

	PARAMETER	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
), IEV	T _A = 25°C		7.2	9	
l.	Outcomet surrent (non about 1)	$VCC = \pm 5V$	T _A = full range			10	
Icc	Quiescent current (per channel)	.45.4	T _A = 25°C		8.4	10.5	mA
		$V_{CC} = \pm 15 \text{ V}$	T _A = full range			11.5	
		.57.474	T _A = 25°C	53	60		
DODD	Development and a state of the	$V_{CC} = \pm 5 \text{ V} \pm 1 \text{ V}$	T _A = full range	50			JD.
PSRR	Power supply rejection ratio	.45.4.4.4	T _A = 25°C	68	73		dB
		$V_{CC} = \pm 15 \text{ V} \pm 1 \text{ V}$	T _A = full range	66			l

shutdown characteristics (THS3125 only)

	PARAMETER		TEST CONDITIONS			MAX	UNIT
ICC(SHDN)	Shutdown quiescent current (per channel)		V _(SHDN) = 3.3 V		370	500	μΑ
t _{DIS}	Disable time (see Note 3)				200		ns
tEN	Enable time (see Note 3)	GND = 0 V VCC = ±5 V to ±15 V			500		ns
IL(SHDN)	Shutdown pin low level leakage current	VCC = ±3 V t0 ±13 V	V(SHDN) = 0 V		18	25	μΑ
IH(SHDN)	Shutdown pin high level leakage current		V(SHDN) = 3.3 V		110	130	μΑ

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

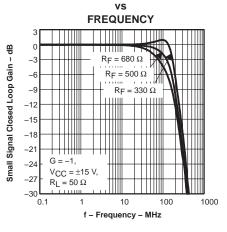
TYPICAL CHARACTERISTICS Table of Graphs

			FIGURE
	Small signal closed loop gain	vs Frequency	1 – 10
	Small and large signal output	vs Frequency	11, 12
		vs Frequency	13, 14, 15
	Harmonic distortion	vs Peak-to-peak output voltage	16, 17
V _n , I _n	Voltage noise and current noise	vs Frequency	18
CMRR	Common-mode rejection ratio	vs Frequency	19
	Crosstalk	vs Frequency	20
Z _o	Output impedance	vs Frequency	21
SR	Slew rate	vs Output voltage step	22
		vs Free-air temperature	23
VIO	Input offset voltage	vs Common-mode input voltage	24
IB	Input bias current	vs Free-air temperature	25
Vo	Output voltage	vs Load current	26
	•	vs Free-air temperature	27
	Quiescent current	vs Supply voltage	28
ICC	Shutdown supply current	vs Free-air temperature	29
	Differential gain and phase error	vs 75 Ω serially terminated loads	30, 31
	Shutdown response		32
	Small signal pulse response		33, 34
	Large signal pulse response		35, 36



SMALL SIGNAL CLOSED LOOP GAIN **FREQUENCY** $R_F = 330 \Omega$ Small Signal Closed Loop Gain - dB $R_F = 680 \Omega$ $R_F = 500 \Omega$ -12 -15 -18 -21 G = -1-24 $V_{CC} = \pm 5 V$, -27 $R_L = 50 \Omega$ -30<mark>L</mark>

SMALL SIGNAL CLOSED LOOP GAIN



SMALL SIGNAL CLOSED LOOP GAIN

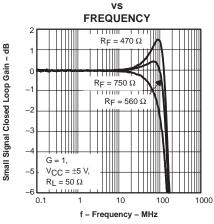


Figure 1

SMALL SIGNAL CLOSED LOOP GAIN

f - Frequency - MHz

100

1000

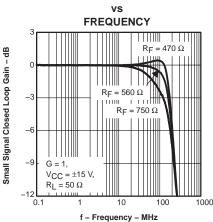


Figure 2

SMALL SIGNAL CLOSED LOOP GAIN

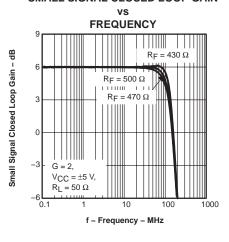


Figure 3

SMALL SIGNAL CLOSED LOOP GAIN

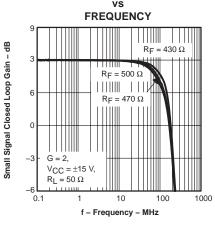


Figure 4

SMALL SIGNAL CLOSED LOOP GAIN

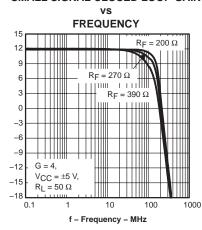


Figure 7

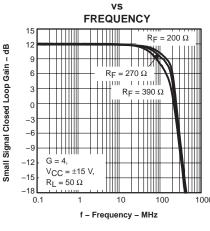


Figure 5 SMALL SIGNAL CLOSED LOOP GAIN

- dB Gain Small Signal Closed Loop 1000

Figure 6

SMALL SIGNAL CLOSED LOOP GAIN

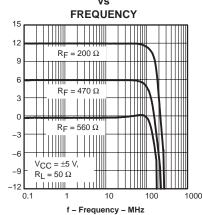


Figure 8

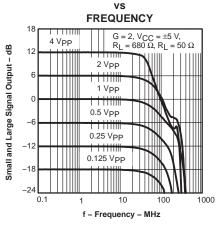
Figure 9



Small Signal Closed Loop Gain - dB

SMALL SIGNAL CLOSED LOOP GAIN FREQUENCY 15 $R_F = 200 \Omega$ 12 Small Signal Closed Loop Gain $R_F = 470 \Omega$ $R_F = 560 \Omega$ $V_{CC} = \pm 15 \text{ V},$ $R_L = 50 \Omega$ 1.1111111 -12 100 0.1 10 1000 f - Frequency - MHz

SMALL AND LARGE SIGNAL OUTPUT



SMALL AND LARGE SIGNAL OUTPUT

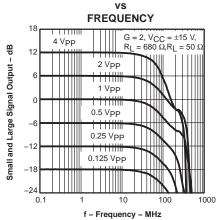


Figure 10

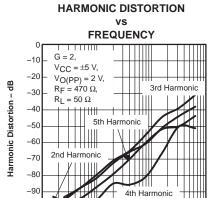


Figure 11

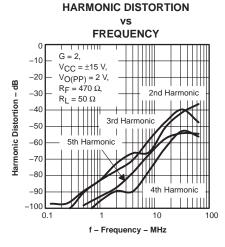


Figure 12

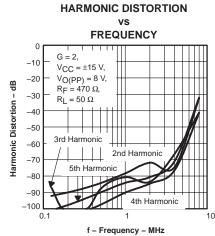
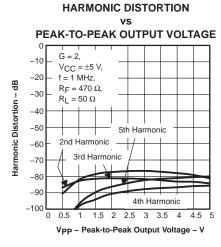


Figure 13

f - Frequency - MHz

-100

0.1



100

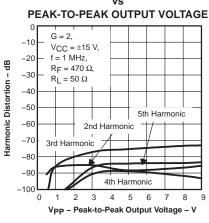


Figure 14 HARMONIC DISTORTION

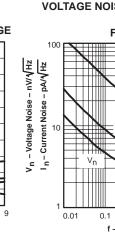


Figure 15 **VOLTAGE NOISE AND CURRENT NOISE**

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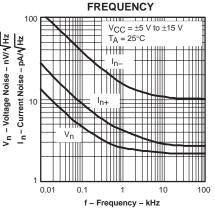


Figure 16

Figure 17

Figure 18



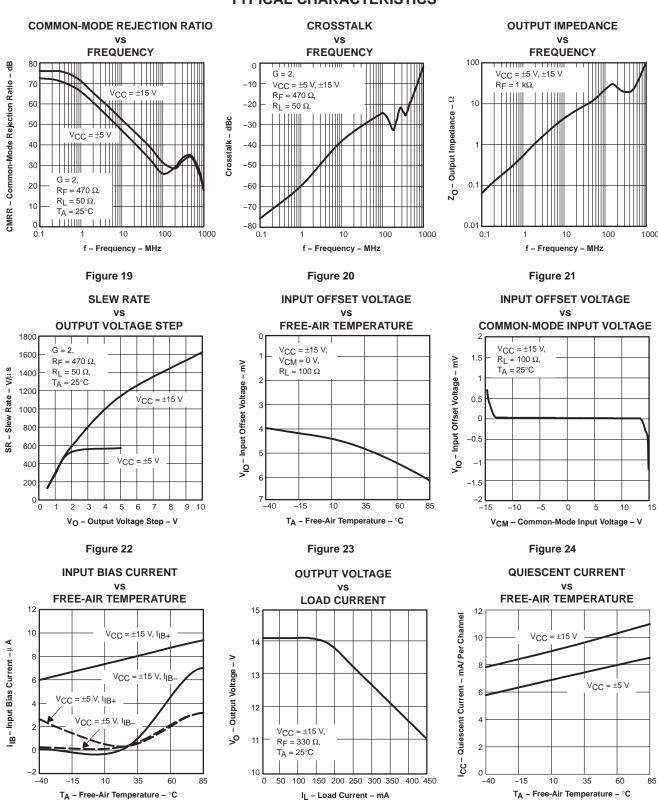




Figure 26

Figure 27

Figure 25

QUIESCENT CURRENT SUPPLY VOLTAGE 12 85 °C 10 I_{CC} - Quiescent Current - mA 8 25 °C -40 °C 6 2 0 0 2.5 7.5 10 12.5 15 V_{CC} - Supply Voltage - $\pm V$

Figure 28

DIFFERENTIAL PHASE AND GAIN ERROR

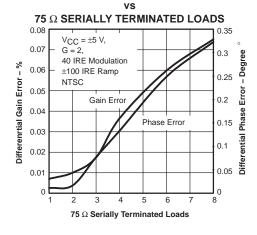


Figure 30

VS FREE-AIR TEMPERATURE 450 450 VSD = 3.3 V RF = 750 Ω VCC = ±15 V VCC = ±5 V 150 100 50

SHUTDOWN SUPPLY CURRENT

Figure 29

0

DIFFERENTIAL PHASE AND GAIN ERROR

T_A - Free-Air Temperature - °C

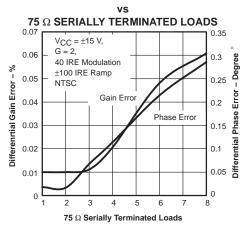
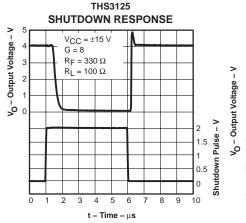
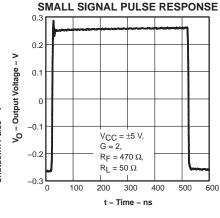


Figure 31





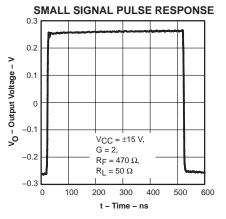


Figure 32 Figure 33 Figure 34



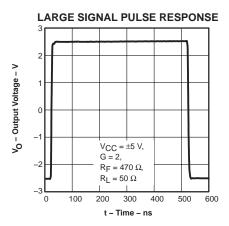


Figure 35

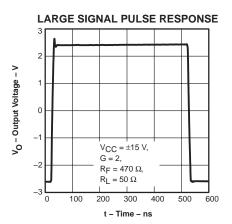


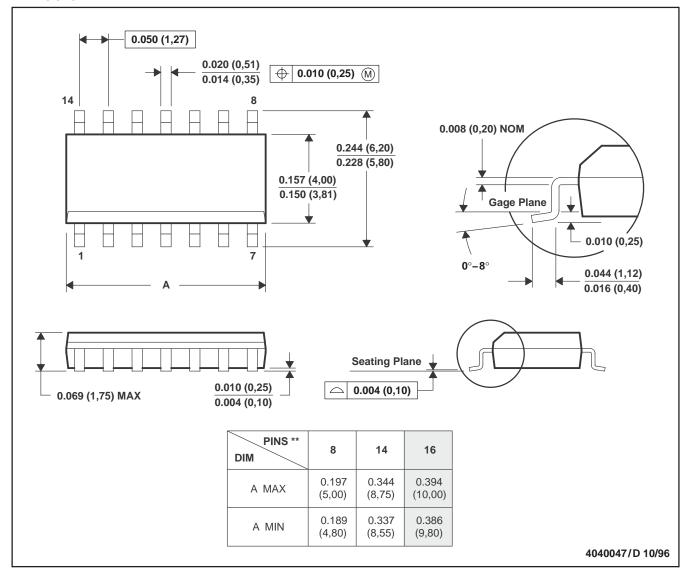
Figure 36

MECHANICAL DATA

D (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

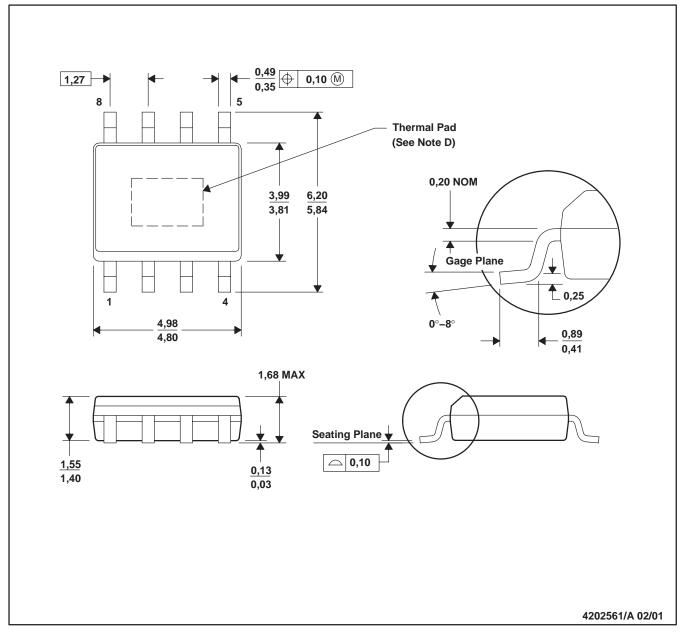
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012



MECHANICAL INFORMATION

DDA (S-PDSO-G8)

Power PAD™ PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

PowerPAD is a trademark of Texas Instruments.

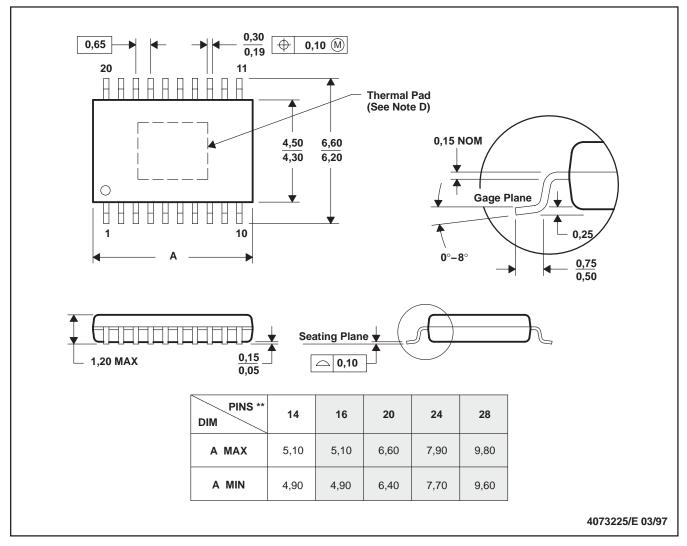


MECHANICAL INFORMATION

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusions.

D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
THS3122CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3122CDDA	ACTIVE	SO Power PAD	DDA	8	75	None	CU SNPB	Level-1-235C-UNLIM
THS3122CDDAR	ACTIVE	SO Power PAD	DDA	8	2500	None	CU SNPB	Level-1-235C-UNLIM
THS3122CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3122ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3122IDDA	ACTIVE	SO Power PAD	DDA	8	75	None	CU SNPB	Level-1-235C-UNLIM
THS3122IDDAR	ACTIVE	SO Power PAD	DDA	8	2500	None	CU SNPB	Level-1-235C-UNLIM
THS3122IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3125CD	ACTIVE	SOIC	D	14	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3125CDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3125CPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125CPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125ID	ACTIVE	SOIC	D	14	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3125IDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3125IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125IPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽²⁾ Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

8-Mar-2005

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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