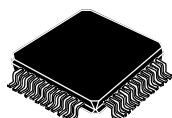


## USB 2.0 high-speed Flash drive controller

Not For New Design

### Features

- USB 2.0 interface compatible with mass storage device class
    - Integrated USB 2.0 PHY supporting USB high speed and full speed
    - Suspend and Resume operations
  - Mass storage controller interface (MSCI)
    - Supports 2 KB-page NAND Flash devices including Numonyx, Hynix, Samsung, Toshiba, Micron, Renesas
    - Reed-Solomon encoder/decoder on-the-fly correction (4 bytes of a 512-byte block)
    - Flash identification support
    - Up to 12 MB/s for read and 8 MB/s for write operations in single channel
    - Up to 4 NAND Flash supported per channel
  - Embedded ST7 8-bit MCU
  - Supply management
    - 3.3 V operation
    - Integrated 3.3-1.8 V voltage regulator
  - USB 2.0 low-power device compliant
    - Less than 100 mA during write operation with two NAND Flash devices
    - Less than 500  $\mu$ A in suspend mode
  - AutoRun CDROM partition support
  - Bootability support (HDD mode)
- 

LQFP48 7x7
- Clock management
    - Integrated PLL for generating core+USB 2.0 clocks from external 12 MHz crystal
  - Data protection
    - Write protect switch control
    - Public/private partitions support
  - Production tool device configurability:
    - USB vendor ID/product ID (VID/PID), serial number and USB strings with foreign language support
    - SCSI strings
    - One or two LED outputs
    - Adjustable NAND Flash bus frequency to reach highest performance
  - Code update in the NAND Flash memory
  - LQFP48 7x7 ECOPACK® package
  - Development support
    - Complete reference design including schematics, BOM and Gerber files
  - Supports Windows (Vista, XP, 2000, ME), Linux and MacOS. Drivers available for Windows 98 SE

**Table 1. Device summary**

| Features                                              | Orderable part numbers |                  |
|-------------------------------------------------------|------------------------|------------------|
|                                                       | ST72681/R20            | ST72681/R21      |
| USB interface                                         | USB 2.0 high speed     |                  |
| Number of NAND Flash devices supported <sup>(1)</sup> | up to 1                | up to 4          |
| R/W speed                                             | 11MB/s and 7MB/s       | 12MB/s and 8MB/s |
| Operating voltage                                     | 3.0 to 3.6 V           |                  |
| Operating temperature                                 | 0 to +70 °C            |                  |
| Package                                               | LQFP48 7x7 / Die form  |                  |

1. Number of NAND Flash devices supported in a single channel.

# Contents

|          |                                       |           |
|----------|---------------------------------------|-----------|
| <b>1</b> | <b>Introduction</b>                   | <b>4</b>  |
| <b>2</b> | <b>Pin description</b>                | <b>5</b>  |
| <b>3</b> | <b>Application schematics</b>         | <b>8</b>  |
| <b>4</b> | <b>NAND Flash interface</b>           | <b>10</b> |
| 4.1      | NAND Flash support table              | 10        |
| 4.2      | NAND error correction                 | 11        |
| 4.2.1    | Hardware error correction             | 11        |
| 4.2.2    | Firmware error management             | 11        |
| 4.3      | Management of bad NAND Flash blocks   | 11        |
| 4.3.1    | Bad block identification              | 11        |
| 4.3.2    | Bad block replacement                 | 12        |
| 4.3.3    | Late fail block                       | 12        |
| 4.4      | Wear levelling                        | 12        |
| 4.4.1    | LUT usage                             | 12        |
| 4.5      | NAND Flash interface configuration    | 13        |
| <b>5</b> | <b>Mass storage implementation</b>    | <b>14</b> |
| 5.1      | USB characteristics                   | 14        |
| 5.2      | BOT / SCSI implementation             | 14        |
| 5.2.1    | BOT specification                     | 14        |
| 5.2.2    | SCSI specification                    | 14        |
| 5.2.3    | Bootability specification             | 14        |
| 5.3      | Multi-LUN device characteristics      | 14        |
| 5.3.1    | Public drive                          | 15        |
| 5.3.2    | Private drive                         | 15        |
| 5.3.3    | Additional drive                      | 15        |
| 5.3.4    | CD-ROM considerations                 | 15        |
| 5.4      | Mass storage interface configuration  | 15        |
| <b>6</b> | <b>Human interface implementation</b> | <b>16</b> |
| 6.1      | LED behavior                          | 16        |
| 6.2      | Read only switch                      | 16        |
| <b>7</b> | <b>Electrical characteristics</b>     | <b>17</b> |

|           |                                                   |           |
|-----------|---------------------------------------------------|-----------|
| 7.1       | Parameter conditions                              | 17        |
| 7.1.1     | Minimum and maximum values                        | 17        |
| 7.1.2     | Typical values                                    | 17        |
| 7.1.3     | Typical curves                                    | 17        |
| 7.1.4     | Loading capacitor                                 | 17        |
| 7.1.5     | Pin input voltage                                 | 18        |
| 7.2       | Absolute maximum ratings                          | 18        |
| 7.2.1     | Voltage characteristics                           | 18        |
| 7.2.2     | Current characteristics                           | 19        |
| 7.2.3     | Thermal characteristics                           | 19        |
| 7.3       | Operating conditions                              | 19        |
| 7.3.1     | General operating conditions                      | 19        |
| 7.4       | Supply current characteristics                    | 20        |
| 7.4.1     | RUN and SUSPEND modes                             | 20        |
| 7.4.2     | Supply and clock managers                         | 20        |
| 7.5       | Clock and timing characteristics                  | 20        |
| 7.5.1     | General timings                                   | 20        |
| 7.5.2     | Crystal oscillator                                | 21        |
| 7.6       | EMC characteristics                               | 22        |
| 7.6.1     | Functional EMS (electromagnetic susceptibility)   | 22        |
| 7.6.2     | Electromagnetic interference (EMI)                | 23        |
| 7.6.3     | Absolute maximum ratings (electrical sensitivity) | 23        |
| 7.7       | I/O port pin characteristics                      | 24        |
| 7.7.1     | General characteristics                           | 24        |
| 7.7.2     | Output driving current                            | 25        |
| 7.8       | Control pin characteristics                       | 27        |
| 7.8.1     | Asynchronous RESET pin                            | 27        |
| 7.9       | Other communication interface characteristics     | 28        |
| 7.9.1     | MSCI parallel interface                           | 28        |
| 7.9.2     | Universal serial bus interface (USB)              | 29        |
| <b>8</b>  | <b>Package mechanical data</b>                    | <b>31</b> |
| <b>9</b>  | <b>Device ordering information</b>                | <b>32</b> |
| <b>10</b> | <b>Revision history</b>                           | <b>33</b> |

# 1 Introduction

The ST72681 is a USB 2.0 high-speed Flash drive controller. The USB 2.0 high-speed interface including PHY and function supports USB 2.0 mass storage device class.

The mass storage controller interface (MSCI) combined with the Reed-Solomon encoder/decoder on-the-fly correction (4-byte on 512-byte data blocks) provides a flexible, high transfer rate solution for interfacing a wide of range NAND Flash memory device types.

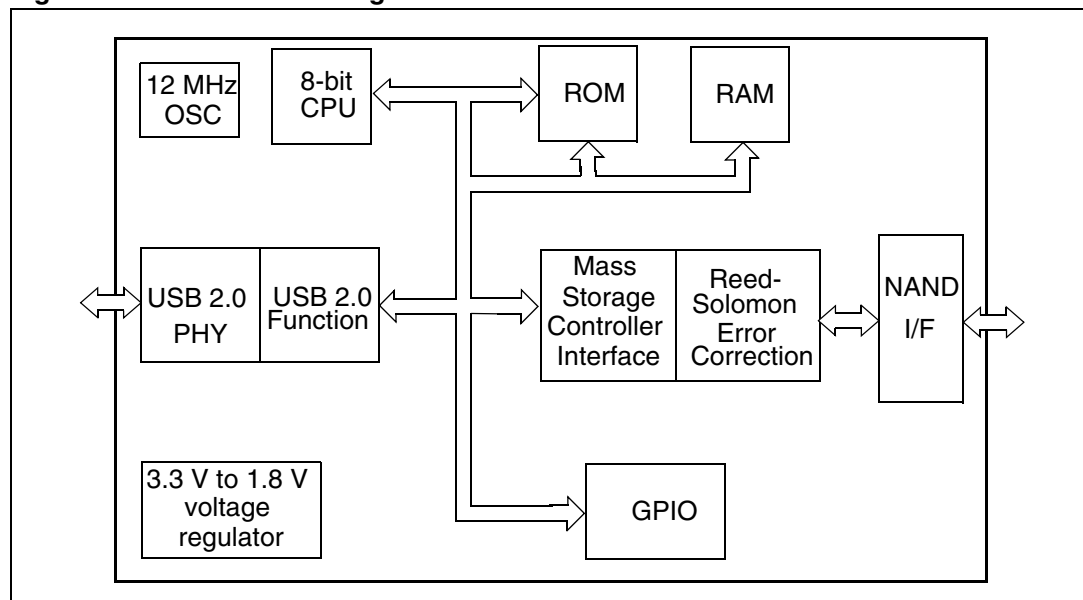
The internal 60 MHz PLL driven by the 12 MHz oscillator is used to generate the 480 MHz frequency for the USB 2.0 PHY.

The ST7 8-bit CPU runs the application program from the internal ROM and RAM. USB data and patch code are stored in internal RAM.

I/O ports provide functions for EEPROM connection, LEDs and write protect switch control.

The internal 3.3 to 1.8 V voltage regulator provides the 1.8 V supply voltage to the digital part of the circuit.

**Figure 1. Device block diagram**



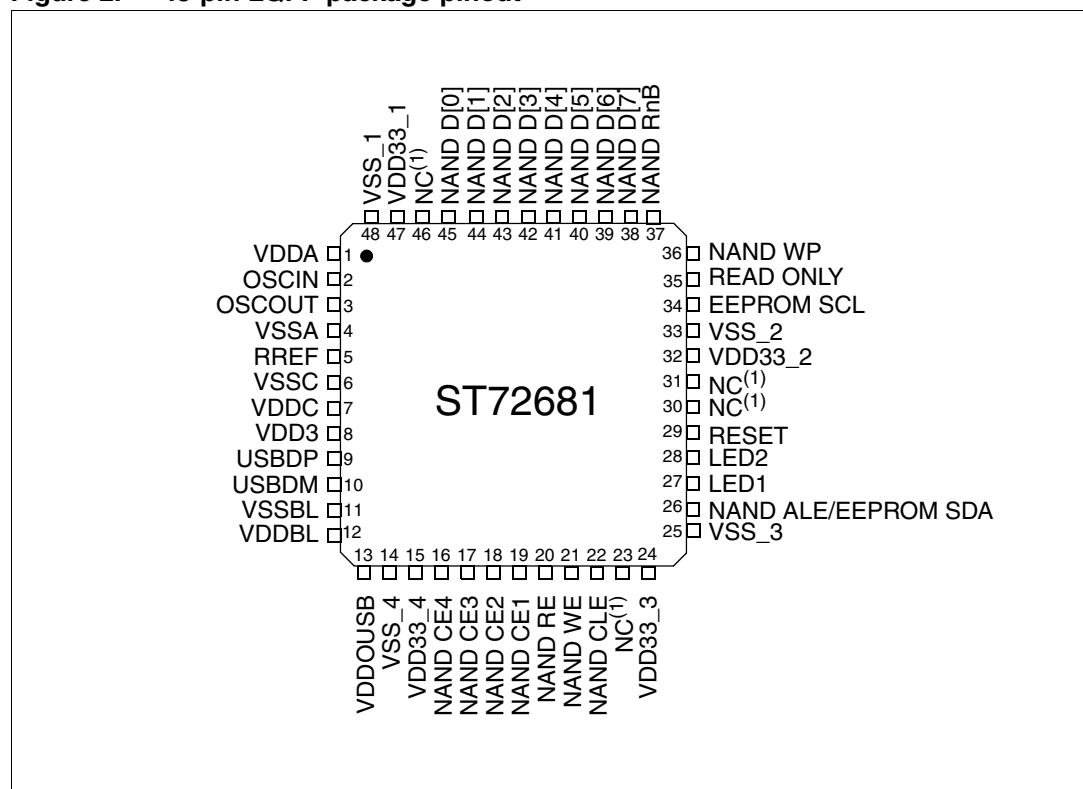
## 2 Pin description

[Figure 2](#) shows the LQFP48 package pinout, while [Table 2](#), [Table 3](#), [Table 4](#), and [Table 5](#) give the pin description.

The legend and abbreviations used in these tables are the following:

- Type
  - I = input
  - O = output
  - S = supply
- Input level: A = Dedicated analog input
- In/Output level
  - $C_T$  = CMOS  $0.3V_{DD}/0.7V_{DD}$  with input trigger
  - $T_T$  = TTL 0.8V / 2 V with Schmitt trigger
- Output level
  - D8 = 8mA drive
  - D4 = 4mA drive
  - D2 = 2mA drive

**Figure 2. 48-pin LQFP package pinout**



1. Must remain NOT connected in the application.

**Table 2. Power supply**

| Pin | Pin name | Type | Description                                       |
|-----|----------|------|---------------------------------------------------|
| 48  | VSS_1    | S    | Ground                                            |
| 47  | VDD33_1  | S    | I/Os and regulator supply voltage                 |
| 33  | VSS_2    | S    | Ground                                            |
| 32  | VDD33_2  | S    | I/Os and regulator supply voltage                 |
| 25  | VSS_3    | S    | Ground                                            |
| 24  | VDD33_3  | S    | I/Os and regulator supply voltage                 |
| 14  | VSS_4    | S    | Ground                                            |
| 15  | VDD33_4  | S    | I/Os and regulator supply voltage                 |
| 13  | VDDOUSB  | S    | USB2 PHY, OSC and PLL power supply output (1.8 V) |

**Table 3. USB 2.0 interface**

| Pin | Pin name | Type | Description                                                                         |
|-----|----------|------|-------------------------------------------------------------------------------------|
| 12  | VDDBL    | S    | Supply voltage for buffers and de-serialization flip flops (1.8 V)                  |
| 11  | VSSBL    | S    | Ground for buffers and de-serialization flip flops (1.8 V)                          |
| 10  | USBDM    | I/O  | USB2 DATA -                                                                         |
| 9   | USBDP    | I/O  | USB2 DATA +                                                                         |
| 8   | VDD3     | S    | Supply voltage for the FS compliance (3.3 V)                                        |
| 7   | VDDC     | S    | Supply voltage for DLL & XOR tree (1.8 V)                                           |
| 6   | VSSC     | S    | Ground for DLL & XOR tree (1.8 V)                                                   |
| 5   | RREF     | I/O  | Ref. resistor for integrated impedance process adaptation (11.3 kOhms 1% pull down) |

**Table 4. USB 2.0 and core clock system**

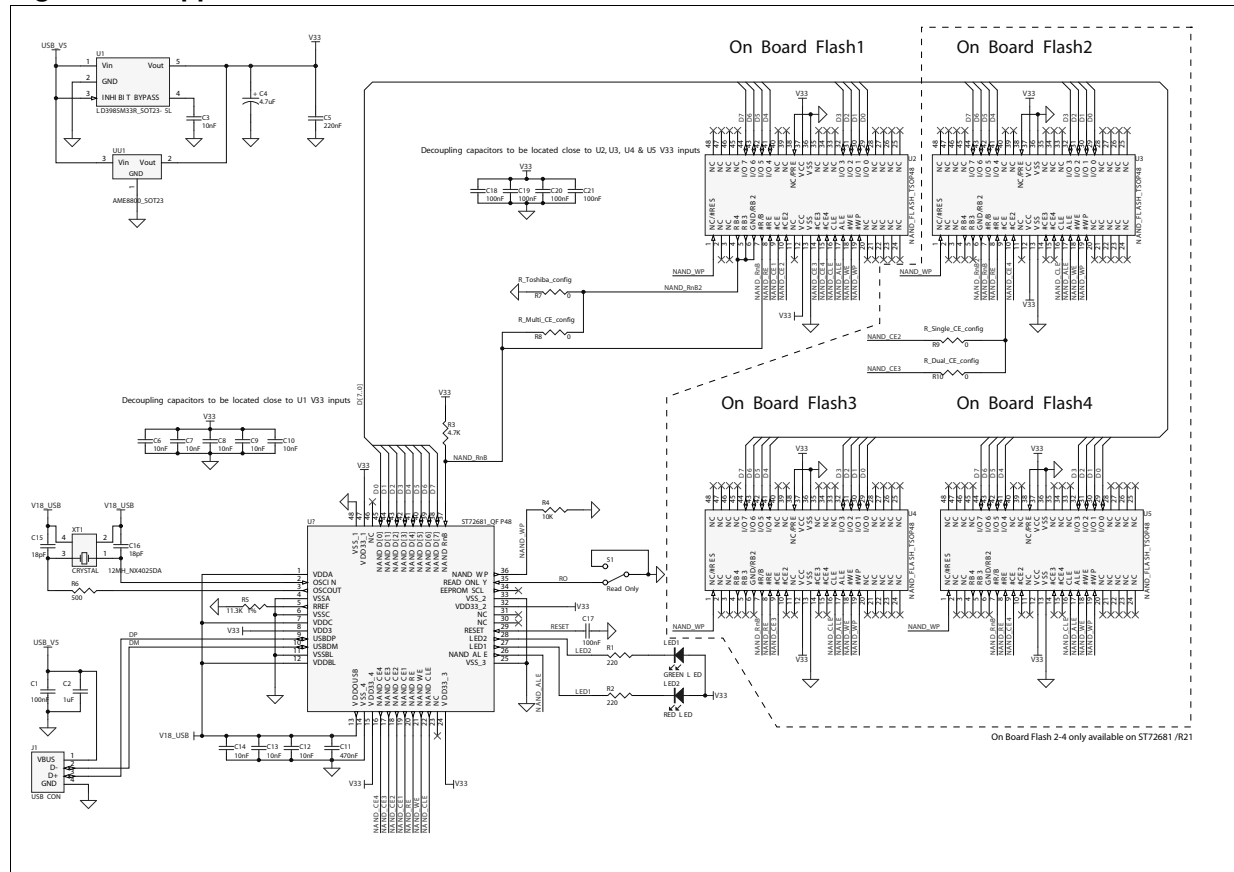
| Pin | Pin name | Type | Description                                 |
|-----|----------|------|---------------------------------------------|
| 4   | VSSA     | S    | Ground for oscillator & PLL (1.8 V)         |
| 3   | OSCOUT   | O    | 12 MHz oscillator output                    |
| 2   | OSCIN    | I    | 12 MHz oscillator input                     |
| 1   | VDDA     | S    | Supply voltage for oscillator & PLL (1.8 V) |

Table 5. General purpose I/O ports /mass storage I/Os

| Pin | Pin name   | Type | Level          |         | Main function<br>(after reset)                      |
|-----|------------|------|----------------|---------|-----------------------------------------------------|
|     |            |      | Input          | Outputs |                                                     |
| 45  | NAND D[0]  | I/O  | T <sub>T</sub> | D4      | NAND Data [0]                                       |
| 44  | NAND D[1]  | I/O  | T <sub>T</sub> | D4      | NAND Data [1]                                       |
| 43  | NAND D[2]  | I/O  | T <sub>T</sub> | D4      | NAND Data [2]                                       |
| 42  | NAND D[3]  | I/O  | T <sub>T</sub> | D4      | NAND Data [3]                                       |
| 41  | NAND D[4]  | I/O  | T <sub>T</sub> | D4      | NAND Data [4]                                       |
| 40  | NAND D[5]  | I/O  | T <sub>T</sub> | D4      | NAND Data [5]                                       |
| 39  | NAND D[6]  | I/O  | T <sub>T</sub> | D4      | NAND Data [6]                                       |
| 38  | NAND D[7]  | I/O  | T <sub>T</sub> | D4      | NAND Data [7]                                       |
| 26  | NAND ALE   | I/O  | T <sub>T</sub> | D8      | NAND Address Latch Enable                           |
| 22  | NAND CLE   | O    | T <sub>T</sub> | D8      | NAND Command Latch Enable                           |
| 21  | NAND WE    | O    | T <sub>T</sub> | D8      | NAND WRite Enable                                   |
| 20  | NAND RE    | O    | T <sub>T</sub> | D8      | NAND read enable                                    |
| 19  | NAND CE1   | O    | T <sub>T</sub> | D4      | NAND Chip Enable 1                                  |
| 18  | NAND CE2   | O    | T <sub>T</sub> | D4      | NAND Chip Enable 2                                  |
| 17  | NAND CE3   | O    | T <sub>T</sub> | D4      | NAND Chip Enable 3                                  |
| 16  | NAND CE4   | O    | T <sub>T</sub> | D4      | NAND Chip Enable 4                                  |
| 37  | NAND RnB   | I    | T <sub>T</sub> | D2      | NAND Ready/ $\overline{\text{Busy}}$                |
| 36  | NAND WP    | O    | T <sub>T</sub> | D2      | NAND Write Protect                                  |
| 35  | READ ONLY  | I    | T <sub>T</sub> | D2      | Read -only switch ("0": Read/Write; "1": Read only) |
| 34  | EEPROM SCL | O    | T <sub>T</sub> | D2      | EEPROM serial clock                                 |
| 28  | LED2       | O    | T <sub>T</sub> | D8      | Green LED (USB access)                              |
| 27  | LED1       | O    | T <sub>T</sub> | D8      | Red LED (NAND memory access)                        |

### 3 Application schematics

Figure 3. Application schematic



ST72681/R20 only supports single NAND Flash Chip Enable configuration (one NAND Flash device with one Chip Enable signal). Note that pins NAND\_RnB2, NAND\_CE2, NAND\_CE3 and NAND\_CE4 should remain unconnected.

ST72681/R21 can support up to four NAND Flash Chip Enable signals. The application can use one of the following configurations:

- One NAND Flash device with four Chip Enable signals; NAND\_CE1, NAND\_CE2, NAND\_CE3 and NAND\_CE4 are used.
- One NAND Flash device with two Chip Enable signals; NAND\_CE1 and NAND\_CE2 are used.
- One NAND Flash device with one Chip Enable signal; only NAND\_CE1 is used.
- Two NAND Flash devices with two Chip Enable signals; NAND\_CE1 and NAND\_CE2 are used to select the first NAND Flash device and NAND\_CE3 and NAND\_CE4 to select the second NAND Flash device.
- Two NAND Flash devices with one Chip Enable signal; NAND\_CE1 and NAND\_CE2 are used to select is used to select the first NAND Flash device and the 2nd NAND Flash device, respectively.
- 4 NAND Flash devices with 1Chip Enable signal; NAND\_CE1 selects the first NAND Flash device, NAND\_CE2 the 2nd NAND Flash device, NAND\_CE3 to select the third, and NAND\_CE4 to select the fourth NAND Flash device.

## 4 NAND Flash interface

### 4.1 NAND Flash support table

**Table 6. Known NAND Flash compatibility guide for R20 and R21 devices<sup>(1)(2)</sup>**

| NAND name          | NAND size (Mbytes or Gbytes) and type | Number of NAND devices supported |              |
|--------------------|---------------------------------------|----------------------------------|--------------|
|                    |                                       | R20 device                       | R21 device   |
| Samsung K9F1G08U   | 128 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Samsung K9F2G08U   | 256 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Samsung K9F4G08U   | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Samsung K9K4G08U   | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Samsung K9W4G08U   | 512 MB; SLC2K; Dual CE                | -                                | 1 or 2       |
| Samsung K9K8G08U   | 1 GB; SLC2K; Single CE                | 1                                | 1, 2, 3 or 4 |
| Samsung K9W8G08U   | 1 GB; SLC2K; Dual CE                  | -                                | 1 or 2       |
| Samsung K9WAG08U   | 2 GB; SLC2K; Dual CE                  | -                                | 1 or 2       |
| Samsung K9NBG08U   | 4 GB; SLC2K; Quad CE                  | -                                | 1            |
| Samsung K9G4G08U   | 512 MB; MLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Samsung K9L8G08U   | 1 GB; MLC2K; Single CE                | 1                                | 1, 2, 3 or 4 |
| Samsung K9HAG08U   | 2 GB; MLC2K; Dual CE                  | -                                | 1 or 2       |
| Samsung K9MBG08U   | 4 GB; MLC2K; Quad CE                  | -                                | 1            |
| Toshiba TH58NVG0S3 | 128 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Toshiba TH58NVG1S3 | 256 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Toshiba TH58NVG2S3 | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Toshiba TH58NVG1D4 | 256 MB; MLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Toshiba TH58NVG2D4 | 512 MB; MLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Toshiba TH58NVG3D4 | 1 GB; MLC2K; Single CE                | 1                                | 1, 2, 3 or 4 |
| Numonyx NAND01GW3B | 128 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Numonyx NAND02GW3B | 256 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Numonyx NAND04GW3B | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Numonyx NAND08GW3B | 1 GB; SLC2K; Single CE                | 1                                | 1, 2, 3 or 4 |
| Numonyx NAND04GW3C | 512 MB; MLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UF081G2M | 128 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UG082G2M | 256 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UG084G2M | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UH084G5M | 512 MB; SLC2K; Dual CE                | -                                | 1 or 2       |
| Hynix HY27UH088G2M | 1 GB; SLC2K; Single CE                | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UT084G2M | 512 MB; MLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Hynix HY27UU088G5M | 1 GB; MLC2K; Dual CE                  | -                                | 1 or 2       |
| Micron 29F2G08AA   | 256 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Micron 29F4G08BA   | 512 MB; SLC2K; Single CE              | 1                                | 1, 2, 3 or 4 |
| Micron 29F8G08FA   | 1 GB; SLC2K; Dual CE                  | -                                | 1 or 2       |

1. This list is provided as a guide only as it is not possible to automatically guarantee support for all the additions and updates across the listed ranges of manufacturers' devices.

2. Only NAND Flash devices with 2 Kbyte pages are supported.

## 4.2 NAND error correction

No NAND Flash memory arrays are guaranteed by manufacturers to be error-free. Error occurrence depends on the Flash cell type (MLC or SLC).

The ST72681 embeds hardware and firmware mechanisms to correct the errors.

### 4.2.1 Hardware error correction

The ST72681 embeds a Reed-Solomon algorithm-based hardware cell. This cell directly manages 512-byte data packets on the NAND Flash I/O system.

Based on a data packet contents, the cell generates an 80-bit Error Correction Code (ECC) consisting of 8 words each containing 10 bits.

During write operations to NAND memory, the 512-bytes of data and the ECC are stored together in the same page. The ECC is stored in the corresponding Redundant Area (RA), using 10 bytes.

During read operations, the 512-bytes of data and the 8 ECC words are read back and are passed through the Reed-Solomon cell for decoding. The cell allows the correction of 4 symbols in this 520-symbol packet (512 symbols from data + 8 symbols from ECC).

The hardware cell gives 3 possible results:

- No error detected: the data packet can be used as it is.
- Correctable error detected: the corrected data are available in a specific 512-byte buffer in the Reed-Solomon cell and are ready to use.
- Uncorrectable error detected: data corruption is not repairable.

### 4.2.2 Firmware error management

The firmware defines the error correction possibilities with the corrected data packet.

When data is not repairable, the block is considered as bad and replaced by another one. See below for further information.

## 4.3 Management of bad NAND Flash blocks

NAND Flash device manufacturers deliver their products with factory-marked bad blocks. This marking depends on the manufacturer and the NAND Flash type (page size, memory technology, etc.). The ST72681 supports all bad block markings currently available on the market.

### 4.3.1 Bad block identification

During firmware initialization, the MCU scans the entire NAND Flash configuration to identify bad blocks.

A bad block is defined as follows:

- 5 different Block Status bytes are considered: 4 Status bytes from page 0 and 1 from an other page (page 127 for MLC NAND Flash memory; page 1 for SLC NAND Flash memory).
- The considered block is declared bad if 1 of these 5 bytes contains 4 bits or more at 0.

### 4.3.2 Bad block replacement

The firmware works with groups of 1024 blocks, called zones. A complete NAND Flash configuration can contain several zones.

Each zone is described in a Look Up Table (LUT) containing 1024 entries. A LUT is composed of 3 parts: used blocks, free blocks and bad blocks.

- The “bad blocks” part contains as many entries as the number of bad blocks identified in that zone.
- The “used blocks” part can have a size of 1000, 900 or 500 entries. This size is configurable and also depends on the number of identified bad blocks.
- The “free blocks” part contains the remaining entries.

The used blocks part is used to do a correspondence between NAND Flash blocks and logical address ranges.

This system allows all bad blocks to be masked from the Host. As a result, bad blocks are never seen. Only a range of logical addresses are visible which correspond to the sum of the used blocks part of all zones.

### 4.3.3 Late fail block

During normal application life, defects can appear in the NAND Flash memory. Under certain conditions, these defects are not correctable and the corresponding block is declared as “bad”.

In this case, new bad blocks are identified in the bad blocks part of the LUT and replaced by new blocks from the “free blocks” part.

## 4.4 Wear levelling

During normal application life, the NAND Flash memories written and erased (by block) many times. The NAND Flash device is guaranteed for a limited number of writes (about 100 000 cycles). As a consequence, the controller must keep write/erase operations to a minimum for any individual block.

A method to limit these cycles is to use a “Wear Levelling” scheme between all NAND Flash memory blocks.

### 4.4.1 LUT usage

The LUT is used for transfers between a logical address range and a block. It contains free blocks which are used in the “wear levelling” scheme.

During write command treatment, the firmware calculates the zones, blocks and pages for data write access. In a block write operation, the firmware applies the following scheme to avoid block wearing:

- The least recently-used block is chosen from the free block part of the LUT.
- Valid data from the old block is copied to the new block.
- New data from the write command is written to the new block.
- The old block is erased.
- The LUT is updated after identifying the new block in the used block part and the old block in the free block part.

Using this scheme, a logical address range doesn't correspond to a constant block. A write command repeated several times to the same logical address writes physically into different blocks.

This method shares the wearing evenly across all blocks of the concerned zone.

## 4.5 NAND Flash interface configuration

Applications based on ST72681 can be configured through a dedicated PC software tool.

The NAND Flash RE and WE signals frequencies can be independently configured to 30 MHz, 20 MHz, 15 MHz, 12 MHz and 10 MHz.

The logical size reduction factor can be configured to 90% or 50% in the event of having too many bad blocks. this option resizes the used blocks part of the LUT to 900 or 500.

## 5 Mass storage implementation

### 5.1 USB characteristics

The ST72681 is compliant with USB 2.0 specification.

It is able to operate in both high speed and full speed modes using a bidirectional control endpoint 0 and a bidirectional bulk endpoint 2.

It automatically recognizes the speed to use on the bus by a process of negotiation with USB Host.

### 5.2 BOT / SCSI implementation

#### 5.2.1 BOT specification

The USB Mass Storage Class Bulk Only Transport (BOT) specification version 1.0 is implemented. It allows the device to be recognized by the host as a mass-storage USB device.

#### 5.2.2 SCSI specification

Moreover, inside BOT transfers, SCSI commands are encapsulated for mass storage operations.

The related specifications are SBC-2 revision 10 (SCSI Block Commands 2) and SPC-4 revision 7a (SCSI Primary Commands 4).

#### 5.2.3 Bootability specification

The USB Mass Storage Specification for Bootability revision 1.0 is implemented.

It allows the PC host to boot the operating system from the USB mass storage application. In this case, the Host uses BOT LUN 0 (logical unit number).

A specific tool must be used to format the logical drive in order to make it bootable by programming the correct information.

### 5.3 Multi-LUN device characteristics

The application can be configured with a dedicated PC software tool as a multi-LUN device.

In this case, up to 3 different drives are available: public drive, additional drive and private drive.

Public and additional drives can be configured as removable drive, hard disk drive or CD-ROM drive.

### 5.3.1 Public drive

The public drive is the default configuration in a mono-LUN mode. In this default case, it is declared as a removable drive.

The public drive is mandatory and can not be removed from the configuration. By customization (using PC software), it can be declared as a removable drive, a CD-ROM drive or a hard disk drive.

This drive is the LUN 0 in BOT commands.

### 5.3.2 Private drive

The Private drive is optional. Its type is “removable drive” and is not configurable.

This drive is protected by password and cannot be directly accessed through the PC operating system. A PC software tool is necessary to send a command with the password to unlock the device. The device is then open and accessible by the PC operating system until reset or reception of a new command to lock the drive.

This drive is the LUN 1 in BOT commands.

### 5.3.3 Additional drive

The additional drive is optional. Its type can be “removable drive”, “hard disk drive” or “CD-ROM drive”.

This drive is LUN 1 in BOT commands if the private drive option is not active, and is LUN 2 if the private drive option is active.

### 5.3.4 CD-ROM considerations

When a drive is declared as CD-ROM, the ST72681/R21 manages this drive with a logical block size of 2 Kbytes. To be correctly recognized by the host, it is preferable to build a CDFS partition on this CD-ROM. See the ‘ST7268x Production Tool User Manual’ for more information.

Note that the ST72681/R20 doesn’t consider the CD-ROM partition as a specific case. The logical block size is 512 bytes and any file system can be used.

In both cases, the CD-ROM partition allows the use of the AutoRun operating system feature. During device connection, the CD-ROM partition is recognized and the host tries to run the application corresponding to the ‘autorun.inf’ file present into this CD-ROM partition.

## 5.4 Mass storage interface configuration

In addition to the parameters already described as configurable in the previous chapters, additional customizable information includes:

- USB parameters: VID, PID, all string information
- SCSI parameters: strings for inquiry commands

## 6 Human interface implementation

### 6.1 LED behavior

The application is designed to manage 2 LEDs. This behavior is configurable through PC dedicated software: 'ST7268x Production Tool'.

By default, LED 1 responds to NAND Flash memory access activity and LED 2 responds to USB activity.

Use of LED 1 is optional. When this option is not active, LED 2 reacts to both USB and NAND Flash activity.

### 6.2 Read only switch

The READ ONLY pin of the ST72681 is an input pin to be connected to VDD or GND depending on the behavior of the device.

- When this pin is connected to GND, no limitations are applied on the PC command received.
- When this pin is connected to VDD or unconnected, the firmware filters all accesses to the NAND Flash which modify the NAND Flash state (write, erase, etc.) and returns an error to the PC.

## 7 Electrical characteristics

### 7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to  $V_{SS}$ .

#### 7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the Devices with an ambient temperature at  $T_A = 25\text{ °C}$  and  $T_A = T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean  $\pm 3\Sigma$ ).

#### 7.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$  and  $V_{DD33} = 3.3\text{ V}$ . They are given only as design guidelines and are not tested.

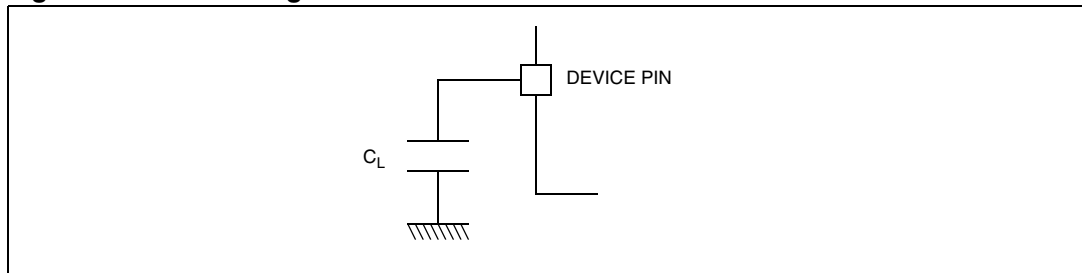
#### 7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 4](#).

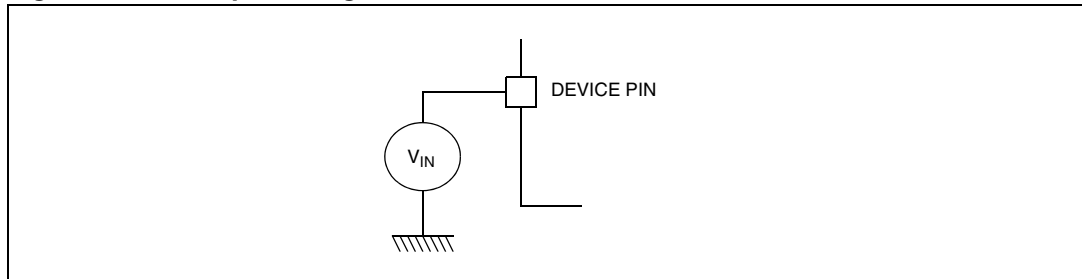
**Figure 4. Pin loading conditions**



### 7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 5](#).

**Figure 5. Pin input voltage**



## 7.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the Device. This is a stress rating only and functional operation of the Device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 7.2.1 Voltage characteristics

**Table 7. Voltage characteristics**

| Symbol              | Ratings                                            | Maximum value                                | Unit |
|---------------------|----------------------------------------------------|----------------------------------------------|------|
| $V_{DD33} - V_{SS}$ | Supply voltage                                     | 4.0                                          | V    |
| $V_{IN}^{(1)(2)}$   | Input voltage on any other pin                     | $V_{SS} - 0.3$ to $V_{DD33} + 0.3$           | V    |
| $V_{ESD(HBM)}$      | Electrostatic discharge voltage (Human Body Model) | See <a href="#">Section 7.6.3 on page 23</a> |      |
| $V_{ESD(MM)}$       | Electrostatic discharge voltage (Machine Model)    |                                              |      |

1. Directly connecting the  $\overline{RESET}$  and I/O pins to  $V_{DD33}$  or  $V_{SS}$  could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7k $\Omega$  for  $\overline{RESET}$ , 10k $\Omega$  for I/Os). For the same reason, unused I/O pins must not be directly tied to  $V_{DD33}$  or  $V_{SS}$ .
2. When the current limitation is not possible, the  $V_{IN}$  absolute maximum rating must be respected, otherwise refer to  $I_{INJ(PIN)}$  specification. A positive injection is induced by  $V_{IN} > V_{DD33}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .

## 7.2.2 Current characteristics

**Table 8. Current characteristics**

| Symbol                  | Ratings                                                           | Maximum value | Unit |
|-------------------------|-------------------------------------------------------------------|---------------|------|
| $I_{VDD33}$             | Total current into $V_{DD33}$ power lines (source) <sup>(1)</sup> | 200           | mA   |
| $I_{VSS}$               | Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>  | 200           |      |
| $I_{IO}$ <sup>(2)</sup> | Output current sunk by any I/O (type D2)                          | 25            |      |
|                         | Output current sunk by any I/O (type D4)                          | 35            |      |
|                         | Output current sunk by any I/O (type D8)                          | 50            |      |
|                         | Output current source by any I/Os and control pin                 | -25           |      |

1. All power supply ( $V_{DD33}$ ) and ground ( $V_{SS}$ ) lines must always be connected to the external supply.
2. Refer to [Table 5: General purpose I/O ports /mass storage I/Os](#) for the output drive capability of each of the I/Os.

## 7.2.3 Thermal characteristics

**Table 9. Thermal characteristics**

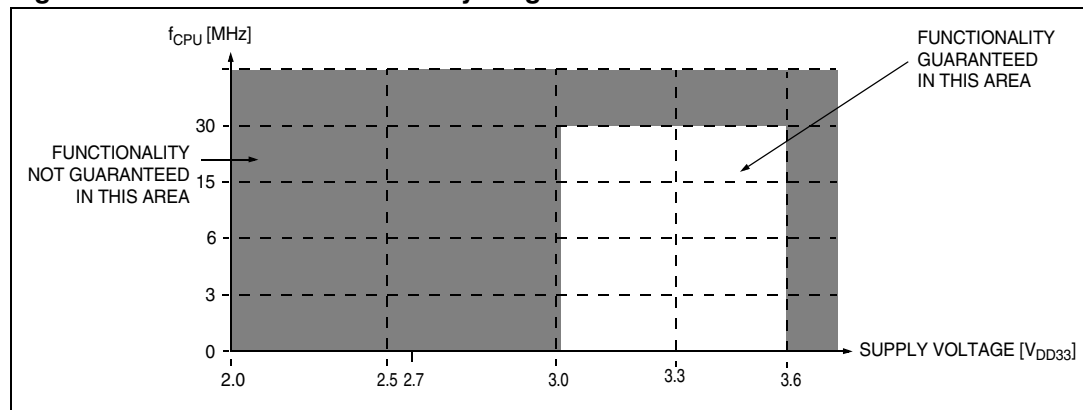
| Symbol     | Ratings                      | Value       | Unit |
|------------|------------------------------|-------------|------|
| $T_{STG}$  | Storage temperature range    | -65 to +150 | °C   |
| $T_{JMAX}$ | Maximum junction temperature | 120         | °C   |

## 7.3 Operating conditions

### 7.3.1 General operating conditions

**Table 10. General operating conditions**

| Symbol     | Parameter                 | Conditions | Min | Max | Unit |
|------------|---------------------------|------------|-----|-----|------|
| $f_{CPU}$  | Internal clock frequency  |            | 0   | 30  | MHz  |
| $V_{DD33}$ | Power supply              |            | 3.0 | 3.6 | V    |
| $T_A$      | Ambient temperature range |            | 0   | 70  | °C   |

**Figure 6. Guaranteed functionality range**

## 7.4 Supply current characteristics

### 7.4.1 RUN and SUSPEND modes

**Table 11. RUN and SUSPEND modes**

| Symbol   | Parameter                      | Conditions                                             | Min. | Typ. | Max. | Unit          |
|----------|--------------------------------|--------------------------------------------------------|------|------|------|---------------|
| $I_{DD}$ | Supply current in RUN mode     | $f_{OSC} = 12 \text{ MHz}$                             | 15   | 25   | 35   | mA            |
|          | Supply current in SUSPEND mode | $V_{DD33} = 3.3 \text{ V}$ , $T_A = +25^\circ\text{C}$ | 60   | 90   | 190  | $\mu\text{A}$ |

### 7.4.2 Supply and clock managers

**Table 12. Supply and clock managers**

| Symbol       | Parameter                                           | Conditions | Typ. <sup>(1)</sup> | Max. <sup>(2)</sup> | Unit          |
|--------------|-----------------------------------------------------|------------|---------------------|---------------------|---------------|
| $I_{DD(CK)}$ | Supply current of crystal oscillator <sup>(3)</sup> |            | 1000                | 2000                | $\mu\text{A}$ |

1. Typical data are based on  $T_A = 25^\circ\text{C}$  and  $f_{CPU} = 12 \text{ MHz}$ .

2. Not tested in production, guaranteed by characterization.

3. Data based on characterization results done with the external components specified in [Section 7.5.2: Crystal oscillator](#), not tested in production.

## 7.5 Clock and timing characteristics

Subject to general operating conditions for  $V_{DD33}$ ,  $f_{OSC}$ , and  $T_A$ .

### 7.5.1 General timings

**Table 13. General timing characteristics**

| Symbol        | Parameter              | Conditions                 | Min. | Typ. <sup>(1)</sup> | Max. | Unit      |
|---------------|------------------------|----------------------------|------|---------------------|------|-----------|
| $t_{C(INST)}$ | Instruction cycle time |                            | 2    | 3                   | 12   | $t_{CPU}$ |
|               |                        | $f_{CPU} = 15 \text{ MHz}$ | 133  | 200                 | 800  | ns        |

**Table 13. General timing characteristics (continued)**

| Symbol      | Parameter                                                                       | Conditions                 | Min.  | Typ. <sup>(1)</sup> | Max.  | Unit          |
|-------------|---------------------------------------------------------------------------------|----------------------------|-------|---------------------|-------|---------------|
| $t_{V(IT)}$ | Interrupt reaction time <sup>(2)</sup><br>$t_{V(IT)} = \Delta t_{c(INST)} + 10$ |                            | 10    |                     | 22    | $t_{CPU}$     |
|             |                                                                                 | $f_{CPU} = 12 \text{ MHz}$ | 0.666 |                     | 1.466 | $\mu\text{s}$ |

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch.  $\Delta t_{c(INST)}$  is the number of  $t_{CPU}$  cycles required to finish executing the current instruction.

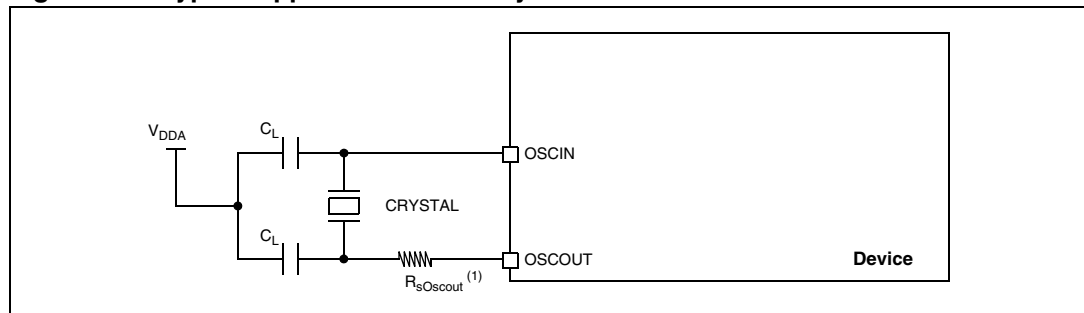
## 7.5.2 Crystal oscillator

The ST72681 internal clock is supplied from a crystal oscillator. All the information given in this paragraph are based on characterization results with specified typical external components. In the application the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal manufacturer for more details (frequency, package, accuracy...).

**Table 14. Crystal oscillator characteristics**

| Symbol         | Parameter                                    | Conditions                | Min. | Typ. | Max.     | Unit |
|----------------|----------------------------------------------|---------------------------|------|------|----------|------|
| $f_{OSC}$      | Oscillator frequency                         |                           |      | 12   |          | MHz  |
| $CK_{ACC}$     | Total crystal oscillator accuracy            | abs. value + temp + aging |      |      | $\pm 60$ | ppm  |
| $\alpha_{OSC}$ | Crystal oscillator duty cycle <sup>(1)</sup> |                           | 45   | 50   | 55       | %    |

1. The crystal oscillator duty cycle has to be adjusted through the two  $C_L$  capacitors. Refer to the crystal manufacturer for more details.

**Figure 7. Typical application with a crystal oscillator**

1. Depending on the crystal oscillator power dissipation, a serial resistor  $R_{sOscout}$  may be added. Refer to the crystal oscillator manufacturer for more details.

**Table 15. Typical  $C_L$  and  $R_S$  values by crystal oscillator**

| Supplier | Typical crystal oscillator | $C_L$ (pF) | $R_{sOscout}(\Omega)$ |
|----------|----------------------------|------------|-----------------------|
| NDK      | AT51 or AT41               | 16         | 560                   |

## 7.6 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### 7.6.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD33}$  and  $V_{SS33}$  through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the  $\overline{\text{RESET}}$  pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Table 16. EMC characterization and optimization values**

| Symbol            | Parameter                                                                                                                                          | Conditions                                                                                                                                              | Level/Class |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| $V_{\text{FESD}}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance                                                                     | $V_{\text{DD33}} = 3.3 \text{ V}$ , $T_A = +25 \text{ }^\circ\text{C}$ , $f_{\text{OSC}} = 12 \text{ MHz}$<br>complies with IEC 1000-4-2 specifications | 4B          |
| $V_{\text{FFTB}}$ | Fast transient voltage burst limits to be applied through 100pF on $V_{\text{DD33}}$ and $V_{\text{SS33}}$ pins to induce a functional disturbance | $V_{\text{DD33}} = 3.3 \text{ V}$ , $T_A = +25 \text{ }^\circ\text{C}$ , $f_{\text{OSC}} = 12 \text{ MHz}$<br>complies with IEC 1000-4-4 specifications | 4A          |

## 7.6.2 Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

**Table 17. Electromagnetic interference**

| Symbol           | Parameter  | Conditions <sup>(1)</sup>                                                                     | Monitored Frequency Band | Max vs. [f <sub>OSC</sub> @12 MHz] | Unit |
|------------------|------------|-----------------------------------------------------------------------------------------------|--------------------------|------------------------------------|------|
| S <sub>EMI</sub> | Peak level | V <sub>DD33</sub> = 3.3 V, T <sub>A</sub> = +25 °C, complies with SAE J 1752/3 specifications | 0.1 MHz to 30 MHz        | 20                                 | dBμV |
|                  |            |                                                                                               | 30 MHz to 130 MHz        | 25                                 |      |
|                  |            |                                                                                               | 130 MHz to 1 GHz         | 25                                 |      |
|                  |            |                                                                                               | SAE EMI Level            | 4                                  | -    |

1. Refer to Application Note AN1709 for data on other package types.

## 7.6.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts\*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

**Table 18. Absolute Maximum Ratings**

| Symbol                | Ratings                                            | Conditions              | Max. <sup>(1)</sup> | Unit |
|-----------------------|----------------------------------------------------|-------------------------|---------------------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (Human Body Model) | T <sub>A</sub> = +25 °C | 2000                | V    |

1. Data based on characterization results, not tested in production.

### Static latch-up (LU)

3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test complies with EIA/JESD 78 IC latch-up specifications.

**Table 19. Electrical sensitivity values**

| Symbol | Parameter             | Conditions              | Class <sup>(1)</sup> |
|--------|-----------------------|-------------------------|----------------------|
| LU     | Static latch-up class | T <sub>A</sub> = +25 °C | A                    |

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

## 7.7 I/O port pin characteristics

### 7.7.1 General characteristics

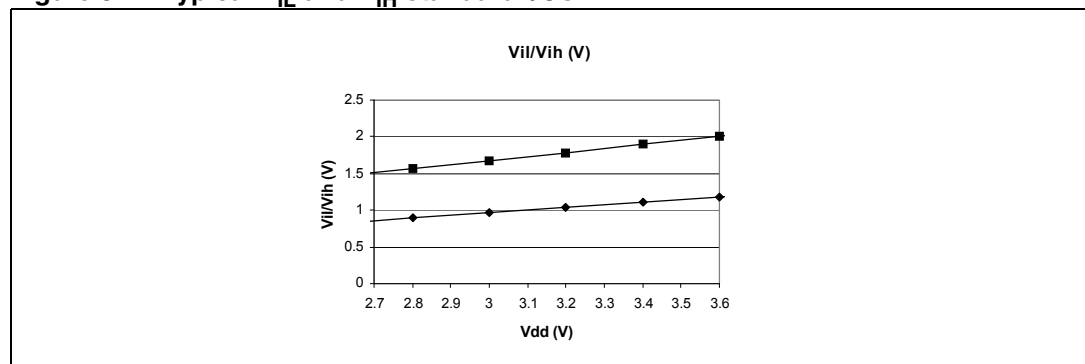
Subject to general operating conditions for  $V_{DD33}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

**Table 20. General I/O port pin characteristics**

| Symbol    | Parameter                                         | Conditions                                            | Min.                   | Typ. | Max.                   | Unit      |
|-----------|---------------------------------------------------|-------------------------------------------------------|------------------------|------|------------------------|-----------|
| $V_{IL}$  | Input low level voltage                           | TTL ports                                             |                        |      | $0.16 \times V_{DD33}$ | V         |
| $V_{IH}$  | Input high level voltage                          |                                                       | $0.85 \times V_{DD33}$ |      |                        |           |
| $V_{hys}$ | Schmitt trigger voltage hysteresis <sup>(1)</sup> |                                                       | 400                    |      |                        | mV        |
| $I_L$     | Input leakage current                             | $V_{SS} \leq V_{IN} \leq V_{DD33}$ ,<br>standard I/Os |                        |      | 1                      | $\mu A$   |
| $I_{L5V}$ | 5V tolerant input leakage current                 | $V_{SS} \leq V_{IN} \leq V_{DD33}$                    |                        |      | 10                     |           |
|           |                                                   | $V_{IN} = 5V$ , 25 °C                                 |                        | 30   |                        |           |
| $R_{PU}$  | Weak pull-up equivalent resistor <sup>(2)</sup>   | $V_{IN} = V_{SS}$ $V_{DD33} = 3.3 V$                  | 32                     | 50   | 75                     | $k\Omega$ |

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. The  $R_{PU}$  pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, tested in production at  $V_{DD33}$  max.

**Figure 8. Typical  $V_{IL}$  and  $V_{IH}$  standard I/Os**



**Figure 9. Typical  $R_{PU}$  vs.  $V_{DD33}$  with  $V_{IN}=V_{SS}$**

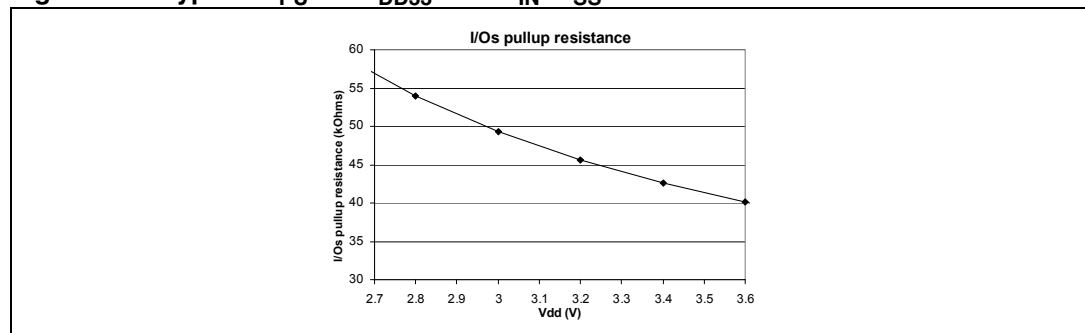
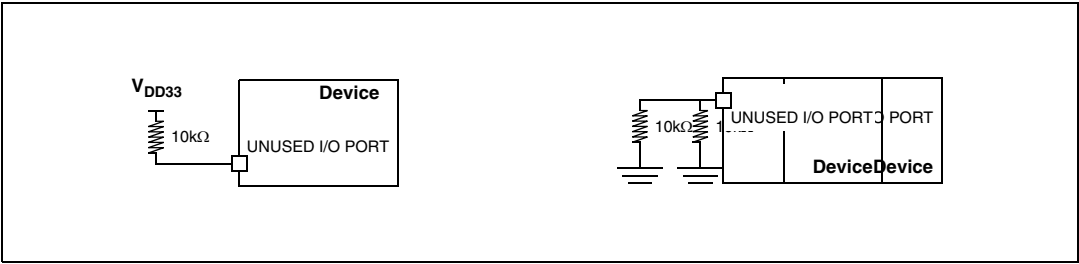


Figure 10. Two typical Applications with unused I/O Pin



### 7.7.2 Output driving current

Subject to general operating conditions for  $V_{DD33}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Table 21. Output driving current

| Symbol                       | Parameter                                                                                                        | Conditions              | Min. | Max. | Unit |
|------------------------------|------------------------------------------------------------------------------------------------------------------|-------------------------|------|------|------|
| $V_{OL}^{(1)}$               | Output low level voltage for a D2 I/O pin when 8 pins are sunk at same time (see <a href="#">Figure 11</a> )     | $I_{IO} = 2 \text{ mA}$ |      | 300  | mV   |
|                              | Output low level voltage for a D4 I/O pin when 8 pins are sunk at same time (see <a href="#">Figure 12</a> )     | $I_{IO} = 4 \text{ mA}$ |      | 400  |      |
|                              | Output low level voltage for a D8 I/O pin when 8 pins are sunk at same time (see <a href="#">Figure 13</a> )     | $I_{IO} = 8 \text{ mA}$ |      | 500  |      |
| $V_{DD33}$<br>$V_{OH}^{(2)}$ | Output high level voltage for a D2 I/O pin when 8 pins are sourced at same time (see <a href="#">Figure 14</a> ) | $I_{IO} = 2 \text{ mA}$ |      | 600  | mV   |
|                              | Output high level voltage for a D4 I/O pin when 8 pins are sourced at same time (see <a href="#">Figure 15</a> ) | $I_{IO} = 4 \text{ mA}$ |      | 600  |      |
|                              | Output high level voltage for a D8 I/O pin when 8 pins are sourced at same time (see <a href="#">Figure 16</a> ) | $I_{IO} = 8 \text{ mA}$ |      | 600  |      |

- The  $I_{IO}$  current sunk must always respect the absolute maximum rating specified in [Section 7.2.2: Current characteristics](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
- The  $I_{IO}$  current sourced must always respect the absolute maximum rating specified in [Section 7.2.2: Current characteristics](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD33}$ . True open drain I/O pins do not have  $V_{OH}$ .

Figure 11. Typical  $V_{OL}$  at  $V_{DD33} = 3.3 \text{ V}$  (I/O D2)

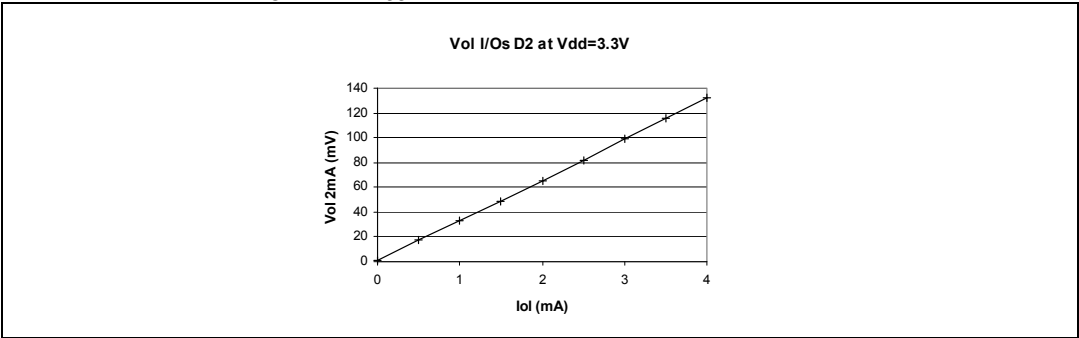


Figure 12. Typical  $V_{OL}$  at  $V_{DD33} = 3.3\text{ V}$  (I/O D4)

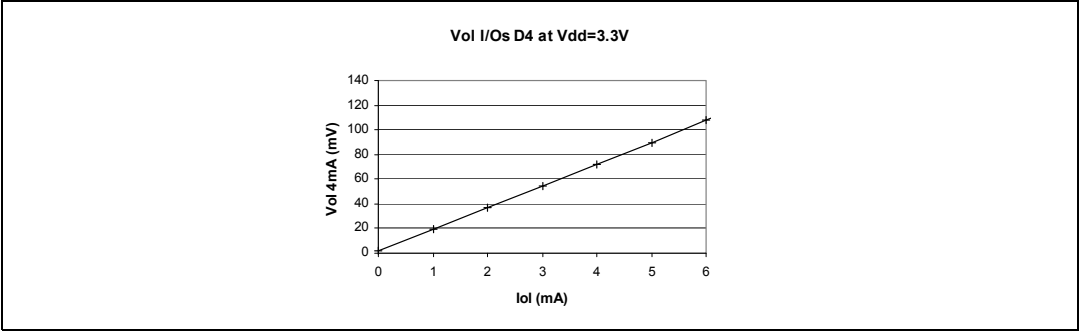


Figure 13. Typical  $V_{OL}$  at  $V_{DD33} = 3.3\text{ V}$  (I/O D8)

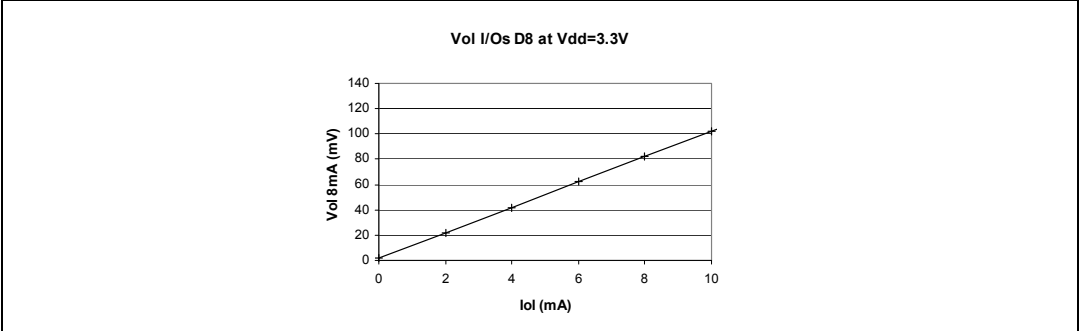


Figure 14. Typical  $V_{DD33}-V_{OH}$  vs.  $V_{DD33}$  (I/O D2)

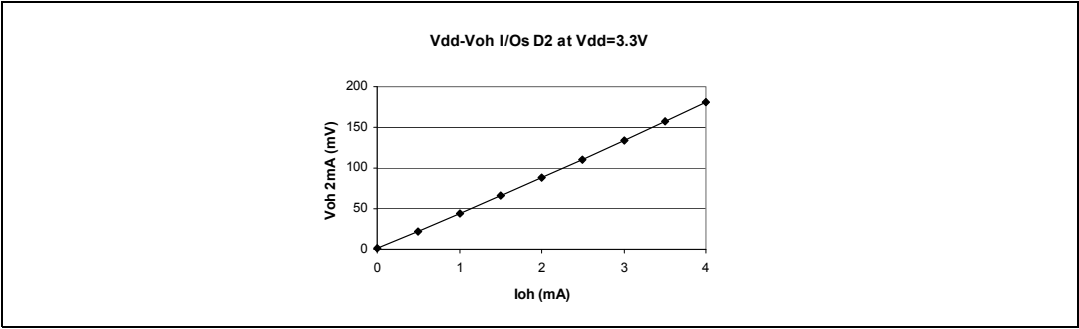


Figure 15. Typical  $V_{DD33}-V_{OH}$  vs.  $V_{DD33}$  (I/O D4)

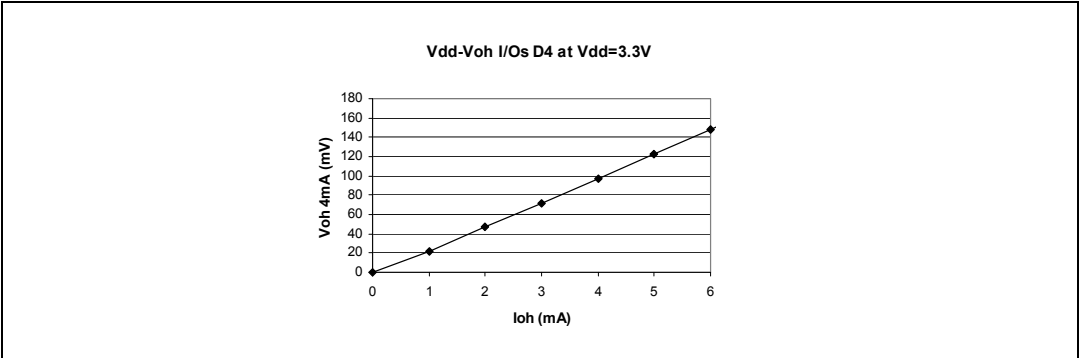
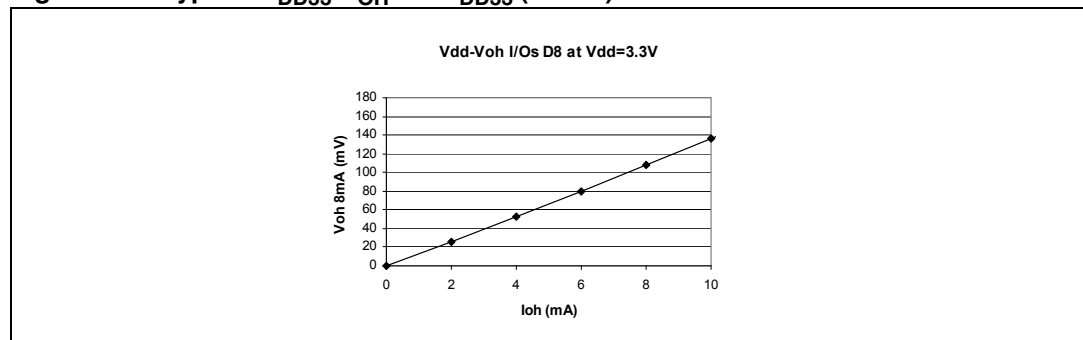


Figure 16. Typical  $V_{DD33}-V_{OH}$  vs.  $V_{DD33}$  (I/O D8)

## 7.8 Control pin characteristics

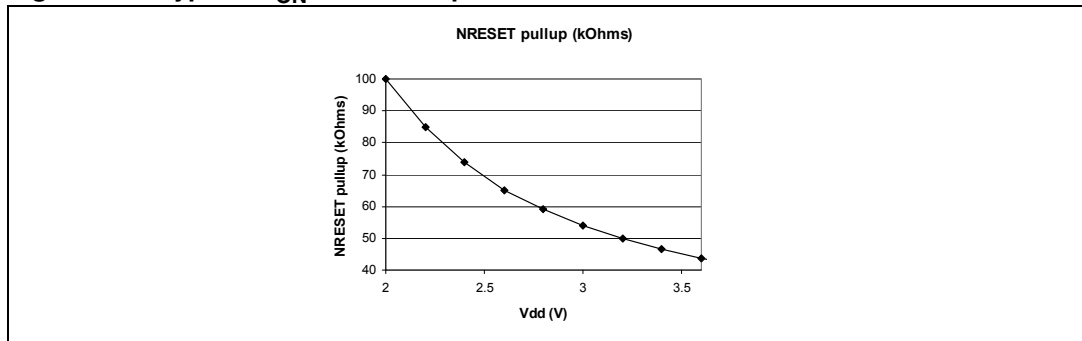
### 7.8.1 Asynchronous $\overline{\text{RESET}}$ pin

$T_A = 0$  to  $+55$  °C unless otherwise specified.

Table 22.  $\overline{\text{RESET}}$  pin characteristics

| Symbol                | Parameter                                     | Conditions                 | Min.                   | Typ. | Max.                   | Unit          |
|-----------------------|-----------------------------------------------|----------------------------|------------------------|------|------------------------|---------------|
| $V_{IL}$              | Input low level voltage <sup>(1)</sup>        |                            |                        |      | $0.16 \times V_{DD33}$ | V             |
| $V_{IH}$              | Input high level voltage                      |                            | $0.85 \times V_{DD33}$ |      |                        |               |
| $V_{hys}$             | Schmitt trigger voltage hysteresis            |                            |                        | 450  |                        | mV            |
| $R_{ON}$              | Pull-up equivalent resistor                   | $V_{DD33} = 3.3 \text{ V}$ | 20                     | 40   | 80                     | $k\Omega$     |
|                       |                                               | $V_{DD33} = 2 \text{ V}$   |                        | 100  |                        |               |
| $t_{eh}(\text{RSTL})$ | External reset pulse hold time <sup>(2)</sup> |                            | 2.5                    |      |                        | $\mu\text{s}$ |
| $t_g(\text{RSTL})$    | Filtered glitch duration <sup>(3)</sup>       |                            |                        | 200  |                        | ns            |
| $t_{ew}(\text{RSTL})$ | External reset pulse duration <sup>(4)</sup>  |                            | 500                    |      |                        | $\mu\text{s}$ |
| $t_{iw}(\text{RSTL})$ | Internal reset pulse duration                 |                            |                        | 2    |                        | $t_{CPU}$     |

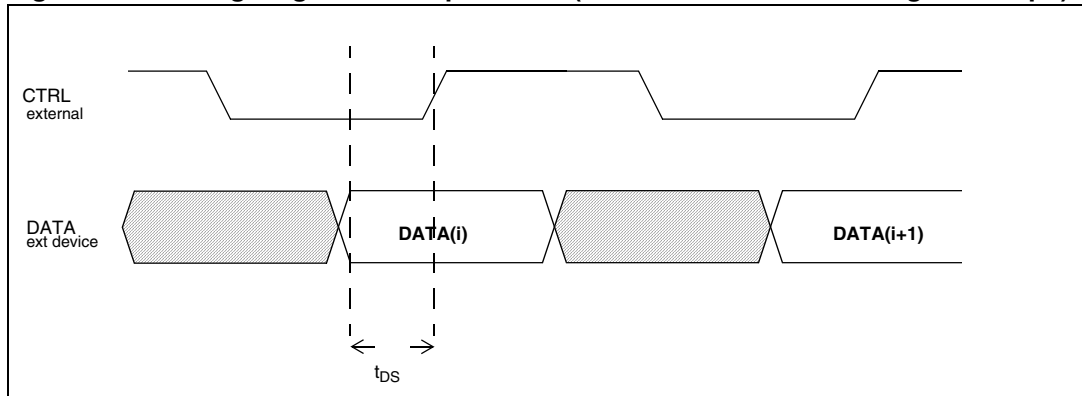
1. The level on the  $\overline{\text{RESET}}$  pin must be free to go below the  $V_{IL}$  max. level specified in [Section 7.8.1: Asynchronous  \$\overline{\text{RESET}}\$  pin](#). Otherwise the reset will not be taken into account internally.
2. To guarantee the reset of the Device, a minimum pulse has to be applied to the  $\overline{\text{RESET}}$  pin. All short pulses applied on  $\overline{\text{RESET}}$  pin with a duration below  $t_{eh}(\text{RSTL})$  can be ignored. Not tested in production, guaranteed by design.
3. The reset network protects the device against parasitic resets.
4. The external reset duration must respect this timing to guarantee a correct start-up of the internal regulator at power-up. Not tested in production, guaranteed by design.

Figure 17. Typical  $R_{ON}$  on  $\overline{RESET}$  pin

## 7.9 Other communication interface characteristics

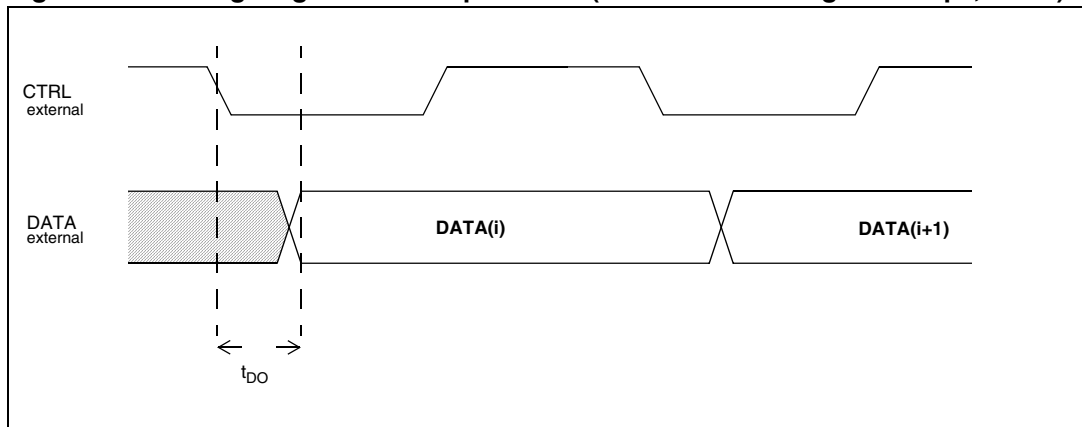
### 7.9.1 MSCI parallel interface

Figure 18. Timing diagrams for input mode (with max load on CTRL signal = 50 pF)



1.  $t_{DS}$  is the setup time for data sampling.

Figure 19. Timing diagrams for output mode (with max CTRL signal = 50 pF, DATA)



1.  $t_{DO}$  is the data output time for data sampling.

**Table 23. MSCI Parallel Interface: DC Characteristics**

| Symbol     | Parameter             | Conditions | Min. | Typ. <sup>(1)</sup> | Max. | Unit |
|------------|-----------------------|------------|------|---------------------|------|------|
| $t_{DS}$   | Data Setup Time       |            |      | 11                  |      | ns   |
| $t_{DO}$   | Data Output time      |            |      | 6                   |      | ns   |
| $C_{CTRL}$ | CTRL line capacitance |            |      | 50                  |      | pF   |
| $C_{DATA}$ | Data line capacitance |            |      | 50                  |      | pF   |

1. Data based on design simulation and not tested in production.

## 7.9.2 Universal serial bus interface (USB)

**Table 24. DC characteristics**

| Symbol                 | Parameter                       | Conditions                                                        | Min. | Typ. | Max. | Unit |
|------------------------|---------------------------------|-------------------------------------------------------------------|------|------|------|------|
| $I_{DDsuspnd}$         | Suspend current                 | $V_{DD33} = 3.3\text{ V}$ , Power-down mode, 25 °C <sup>(1)</sup> | 60   | 90   | 190  | μA   |
| $R_{PU}$               | Pull-up resistor <sup>(2)</sup> |                                                                   |      | 1.5  |      | kΩ   |
| <b>Full speed mode</b> |                                 |                                                                   |      |      |      |      |
| $V_{TERM}$             | Termination voltage             |                                                                   | 0.8  |      | 2.0  | V    |
| $V_{OH}$               | High level output voltage       |                                                                   | 2.8  |      | 3.6  | V    |
| $V_{OL}$               | Low level output voltage        |                                                                   |      |      | 0.8  | V    |
| $V_{CRS}$              | Crossover voltage               |                                                                   | 1.3  |      | 2.0  | V    |
| <b>High speed mode</b> |                                 |                                                                   |      |      |      |      |
| $V_{HSOH}$             | HS data signalling high         |                                                                   |      | 400  |      | mV   |
| $V_{HSOL}$             | HS data signalling low          |                                                                   |      | 5    |      | mV   |

1. The values provided do not take into account the current through both the 1.5kΩ pull-up resistor (on the device-side) and the 15kΩ pull-down resistor (on the host-side).

2. Not tested in production, guaranteed by characterization.

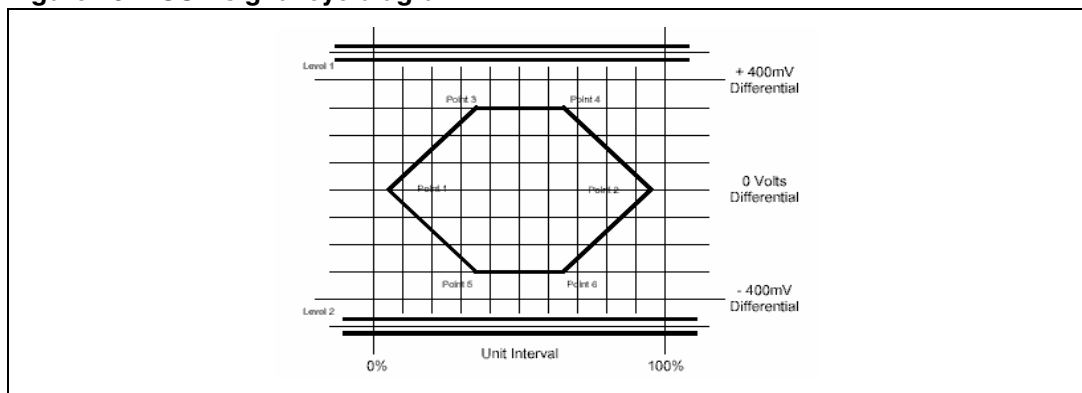
**Table 25. Timing characteristics**

| Symbol                 | Parameter    | Conditions           | Min.   | Max.               | Unit |
|------------------------|--------------|----------------------|--------|--------------------|------|
| <b>Full speed mode</b> |              |                      |        |                    |      |
| $t_{FR}$               | Rise time    | $C_L = 50\text{ pF}$ | 4      | 20                 | ns   |
| $t_{FF}$               | Fall time    | $C_L = 50\text{ pF}$ | 4      | 20                 | ns   |
| <b>High speed mode</b> |              |                      |        |                    |      |
| $t_{HSR}$              | Rise time    |                      |        | 500 <sup>(1)</sup> | ps   |
| $t_{HSF}$              | Fall time    |                      |        | 500 <sup>(1)</sup> | ps   |
| $t_{HSDRAT}$           | HS data rate |                      | 479.76 | 480.24             | Mb/s |

1. Not tested in production, guaranteed by characterization.

**Table 26. USB High Speed Transmit Waveform requirements**

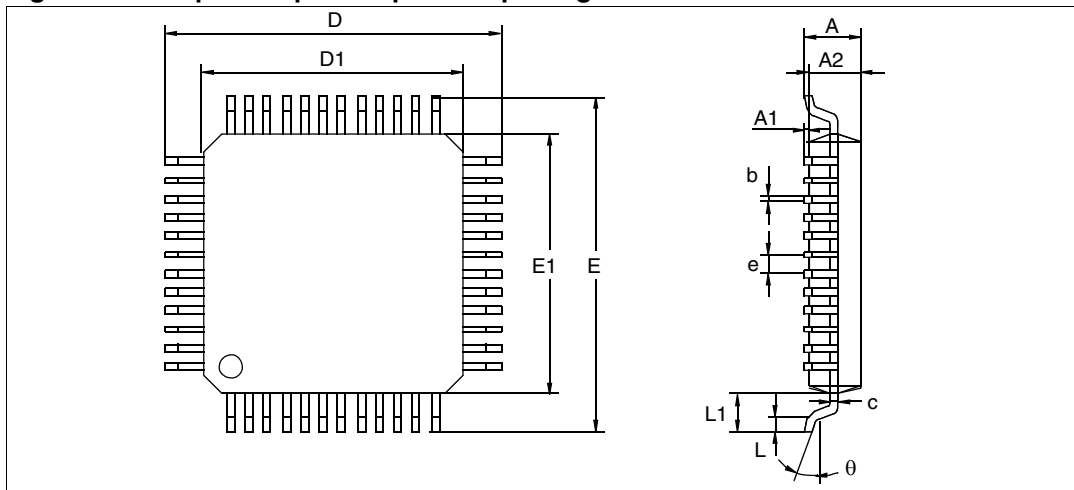
|                    | Voltage Level (DP - DN) | Time              |
|--------------------|-------------------------|-------------------|
| Unit Interval (UI) | -                       | 2.082 to 2.084 ns |
| Level 1            | 475 mV                  | -                 |
| Level 2            | -475 mV                 | -                 |
| Point 1            | 0V                      | 5% UI             |
| Point 2            | 0V                      | 95% UI            |
| Point 3            | 300 mV                  | 35% UI            |
| Point 4            | 300 mV                  | 65% UI            |
| Point 5            | -300 mV                 | 35% UI            |
| Point 6            | -300 mV                 | 65% UI            |

**Figure 20. USB signal eye diagram**

## 8 Package mechanical data

In order to meet environmental requirements, ST offers this device in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 21. 48-pin low profile quad flat package outline**



**Table 27. 48-pin low profile quad flat package dimensions**

| Dim. | mm             |      |      | inches <sup>(1)</sup> |        |        |
|------|----------------|------|------|-----------------------|--------|--------|
|      | Min.           | Typ. | Max. | Min.                  | Typ.   | Max.   |
| A    |                |      | 1.60 |                       |        | 0.0630 |
| A1   | 0.05           |      | 0.15 | 0.0020                |        | 0.0060 |
| A2   | 1.35           | 1.40 | 1.45 | 0.0530                | 0.0550 | 0.0570 |
| b    | 0.17           | 0.22 | 0.27 | 0.0070                | 0.0090 | 0.0110 |
| C    | 0.09           |      | 0.20 | 0.0040                |        | 0.0080 |
| D    |                | 9.00 |      |                       | 0.3540 |        |
| D1   |                | 7.00 |      |                       | 0.2760 |        |
| E    |                | 9.00 |      |                       | 0.3540 |        |
| E1   |                | 7.00 |      |                       | 0.2760 |        |
| e    |                | 0.50 |      |                       | 0.0200 |        |
| θ    | 0°             | 3.5° | 7°   | 0°                    | 3.5°   | 7°     |
| L    | 0.45           | 0.60 | 0.75 | 0.0180                | 0.0240 | 0.0300 |
| L1   |                | 1.00 |      |                       | 0.0390 |        |
|      | Number of Pins |      |      |                       |        |        |
| N    | 48             |      |      |                       |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 9 Device ordering information

**Table 28. Feature comparison table**

| Features added in the ST72681/R21 versus ST72681/R20 | Description                                                                                                |
|------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| Support for up to 4 NAND Flash devices               | Firmware revision R21 upgrades the number of supported NAND Flash devices from 1 to 4 in a single channel. |
| Continued AutoRun CDROM partition support            | AutoRun runs a program when the USB Flash Drive is inserted into a computer.                               |

**Table 29. Ordering information**

| Part number                            | Package      | Operating voltage | Temperature range |
|----------------------------------------|--------------|-------------------|-------------------|
| ST72681/R20                            | LQFP48 7x7mm | 3.0 to 3.6 V      | 0 to +70 °C       |
| ST72681/R21 (latest firmware revision) | LQFP48 7x7mm | 3.0 to 3.6 V      | 0 to +70 °C       |

## 10 Revision history

**Table 30. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27-May-2005 | 1.0      | <p>Changed status of the document</p> <p>Changed description on 1st page</p> <p>Removed unconnected pins in <a href="#">Table 5 on page 7</a></p> <p>Changed <a href="#">Table 4 on page 6</a></p> <p>Changed pin 5 description in <a href="#">Table 3 on page 6</a></p> <p>Changed section 3 on page 7</p> <p>Changed <a href="#">Figure 3 on page 8</a> and <a href="#">Figure 4</a></p>                                                                                                                                                                                                                                                                                                                                   |
| 18-Nov-2005 | 2.0      | <p>Electrical Characteristics section added, <a href="#">Section 4 on page 10</a></p> <p>Additional features listed on front page</p> <p>Status of document changed to Datasheet</p> <p>Application schematics modified, Figure 4 removed</p> <p>Section 4.6 (Memory Characteristics) removed</p> <p>VDDOUSB marked as O (output) in <a href="#">Table 2 on page 6</a></p>                                                                                                                                                                                                                                                                                                                                                   |
| 06-Feb-2006 | 3.0      | <p>Additional features listed on front page</p> <p>Application schematics modified, <a href="#">Figure 3 on page 8</a></p> <p>Feature comparison table added for R20 firmware update, <a href="#">Table 28</a></p> <p><a href="#">Figure 3 on page 8</a> updated, with note added</p>                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 09-Jan-2007 | 4.0      | <p>Additional features listed on front page related to firmware release R21. Application schematics updated for R21, <a href="#">Figure 3 on page 8</a></p> <p>Feature comparison table added for R21 firmware update, <a href="#">Table 28</a></p> <p>I<sub>DDsuspend</sub> values and note updated, <a href="#">Table 24</a></p>                                                                                                                                                                                                                                                                                                                                                                                           |
| 30-Aug-2007 | 5.0      | <p>Updated information in <a href="#">Table 6: Known NAND Flash compatibility guide for R20 and R21 devices on page 10</a>.</p> <p>Added <a href="#">Section 4.2: NAND error correction on page 11</a>, <a href="#">Section 4.3: Management of bad NAND Flash blocks on page 11</a>, <a href="#">Section 4.4: Wear levelling on page 12</a> and <a href="#">Section 4.5: NAND Flash interface configuration on page 13</a>.</p> <p>Added <a href="#">Section 5: Mass storage implementation on page 14</a> and <a href="#">Section 6: Human interface implementation on page 16</a>.</p> <p>Added internal clock frequency (f<sub>CPU</sub>) value in <a href="#">Table 10: General operating conditions on page 19</a>.</p> |
| 22-Jan-2009 | 6        | <p>Updated datasheet status to "not recommended for new design".</p> <p>Replaced ST by Numonyx for NAND Flash memories. Updated mass storage in <a href="#">Section : Features</a>. Added <a href="#">Note 2</a> below <a href="#">Table 6</a>.</p> <p>Removed dynamic latch-up in <a href="#">Section 7.6.3: Absolute maximum ratings (electrical sensitivity)</a>.</p> <p>Changed TQFP48 to LQFP48.</p> <p>Updated ECOPACK text in <a href="#">Section 8: Package mechanical data</a>.</p>                                                                                                                                                                                                                                 |

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