REALTEK SEMICONDUCTOR INC.
ALC203 APPLICATION NOTES

0. Revision History

Version 0.2:
(1) Add Jack Sense circuit

(2) Add Universal Audio Jack ® circuit

(3) Add Smart GPIO Volume Control ® circuit

(4) Add application circuit for motherboard

1. Introduction

The ALC203 has a 20-bit stereo DAC and 18-bit stereo ADC, full duplex AC'97 2.3 compatible audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC203 incorporates proprietary converter technology to achieve a high SNR, greater than 95 dB. The ALC203 AC'97 CODEC supports independent variable sampling rates and built-in 3D effects.

This document contains some notes on application circuits for the ALC203.

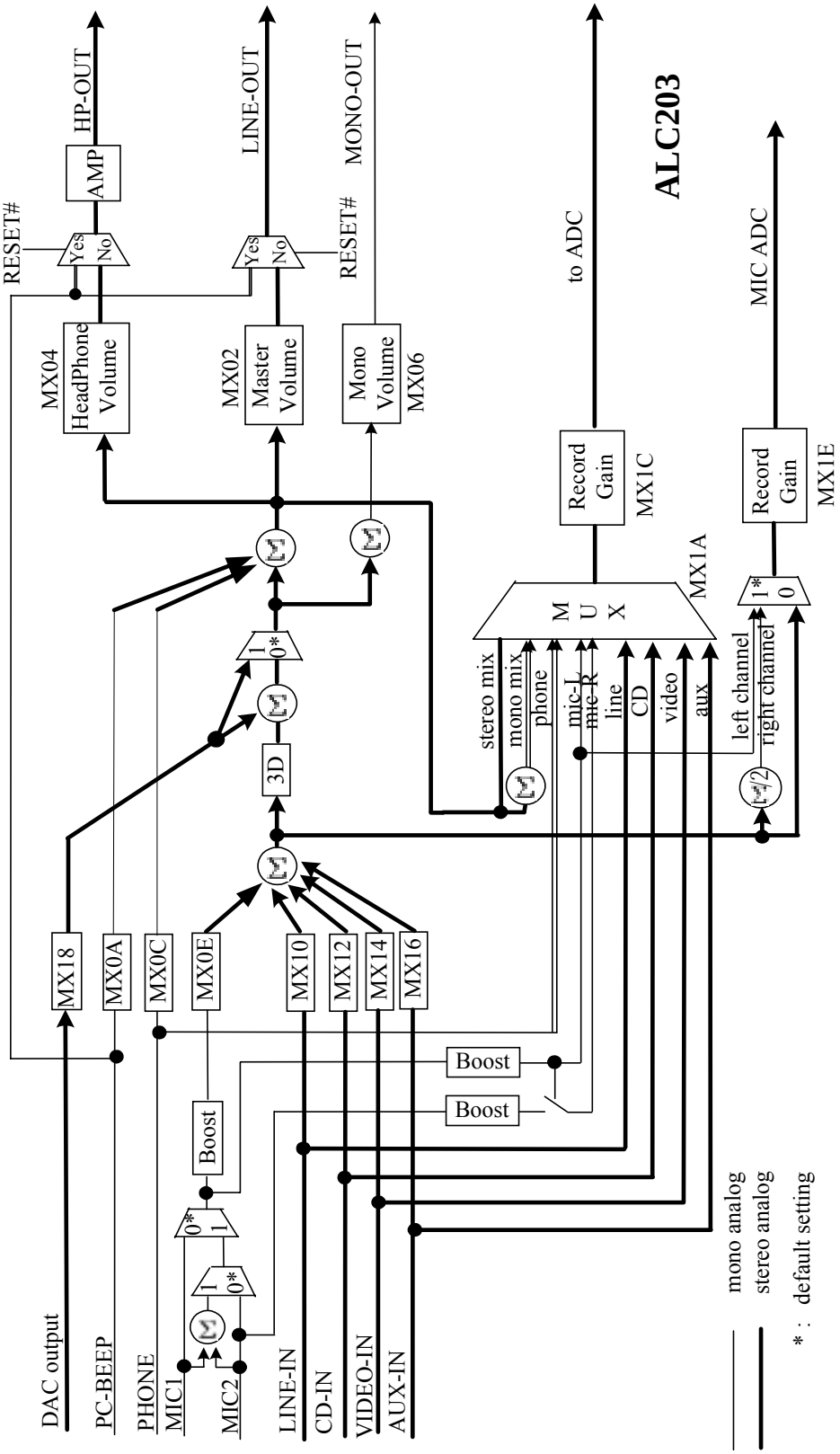
This guide is intended for the Realtek customer who will be designing a hardware system around the Realtek ALC203 chip. Using this guide, the following goals can be achieved:

(1) Create a noise-free, power stable environment that is suitable for the ALC203.
(2) Reduce the possibility of EMI and EMC and their influence to the chip.
(3) Simplify the task of routing signal traces, so as to make a better circuit for the ALC203.

All information provided in this guide has been tested by Realtek systems engineers to be accurate and directly applicable to proper system designs using ALC203.

2. Mixer Block Diagram

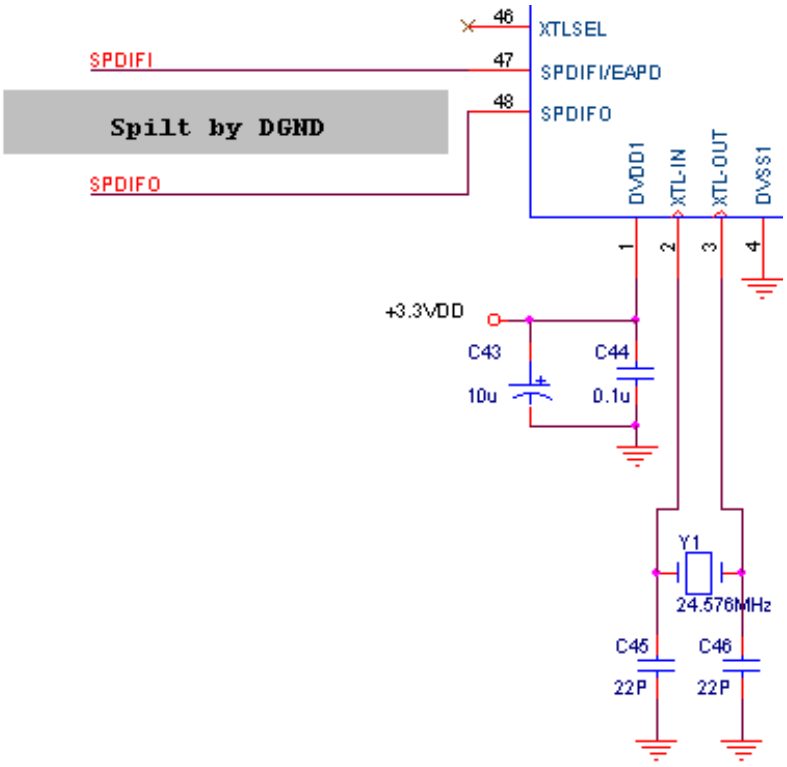
The Mixer Block Diagram shows the analog data path, and its control mixers. The ALC203 supports flexible analog paths to fit different applications.



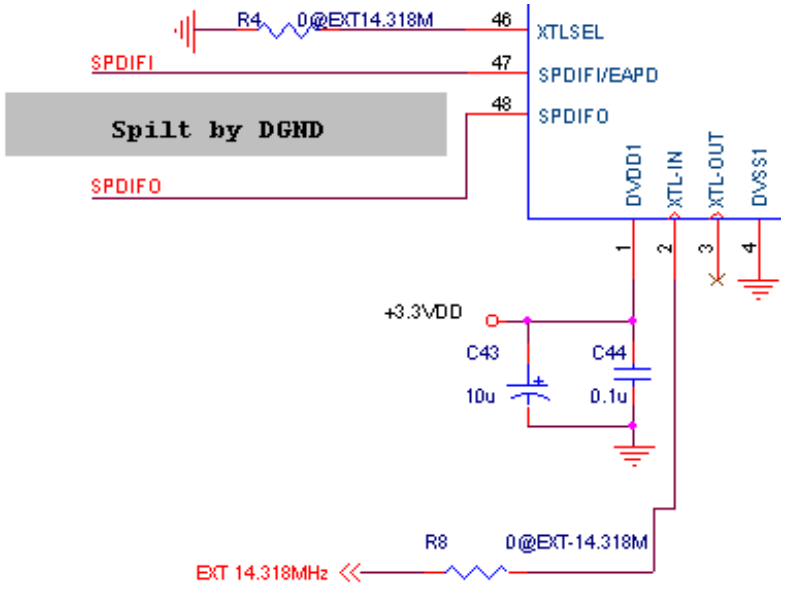
Analog data path

3. Saving 24.576MHz Crystal

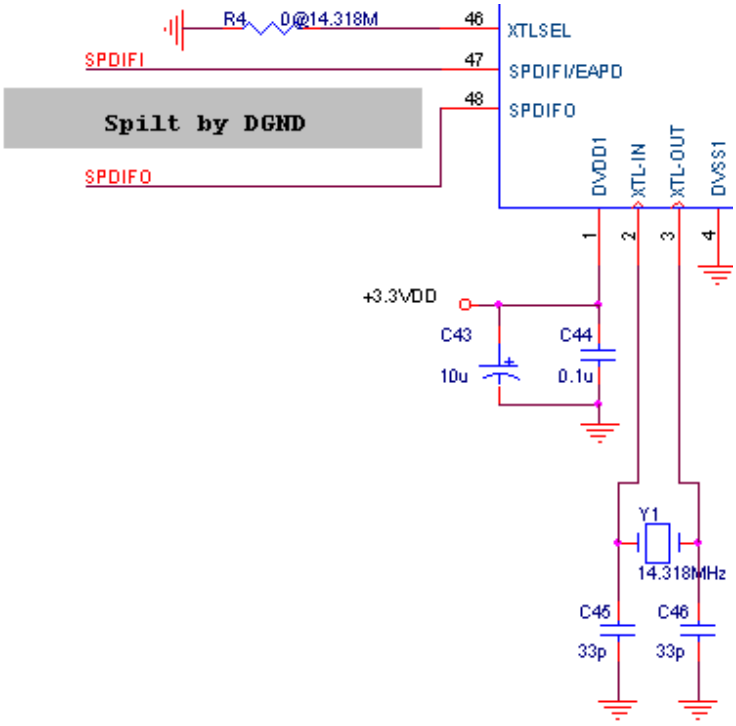
The ALC203 has a built in 14.318MHz to 24.576MHz phase-lock-loop clock generator. The 14.318MHz frequency from the clock generator can be used as the clock source for the ALC203 by pulling XTLSEL (pin-46) low.



Float XTLSEL when 24.576MHz crystal is used



Pull-low XTLSEL if External 14.318MHz is used



Pull-low XTLSEL if External 14.318MHz crystal is used

4. Output Amplifier at HP-OUT

The ALC203 embeds 50mW@20Ω amplifiers @ HP-out and Aux-in as HP-out to drive the headphones, saving external earphone driving circuitry.

Standard AC97 Requires External Amplifier

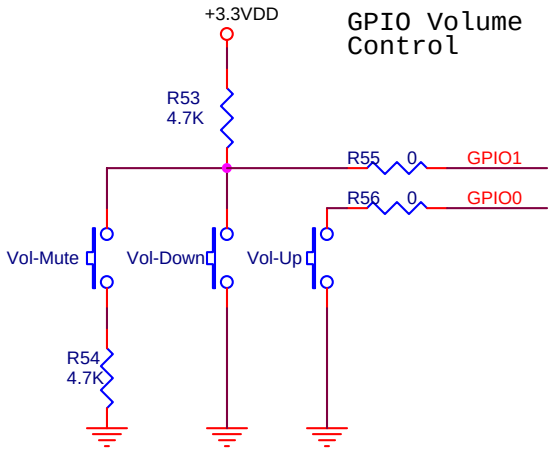
ALC203 Has Embedded Headphone Amplifier

5. General Purpose I/O (GPIO)

ALC203 supports 2 GPIO pins for general input-output applications. GPIO0 is at pin43 and GPIO1 is at pin44. Both GPIO0 and GPIO1 can be separately programmed as input or output.

6. Smart GPIO Volume Control®

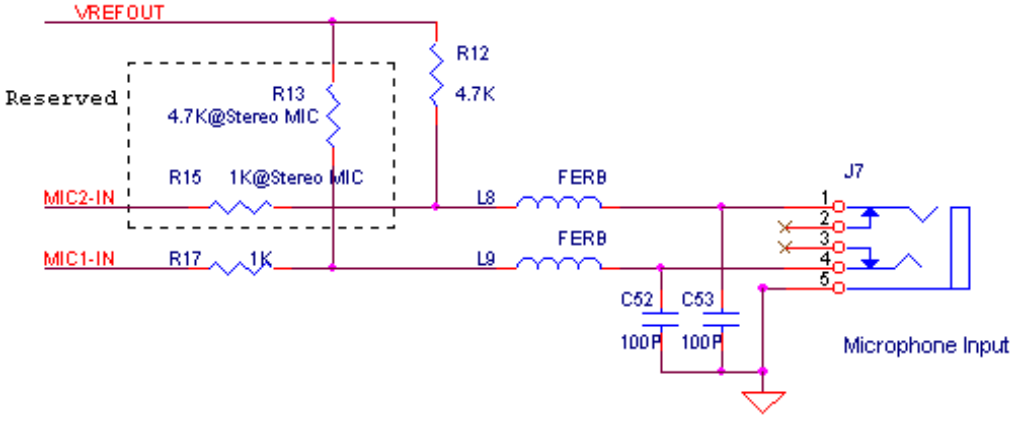
ALC203 supports Smart GPIO Volume Control ® which is designed for NB manufacturer. With this circuit, manufacturers can implement volume control by button, and end users can experience one-shot volume up/down or continuously pressing volume up/down



Smart GPIO Volume Control

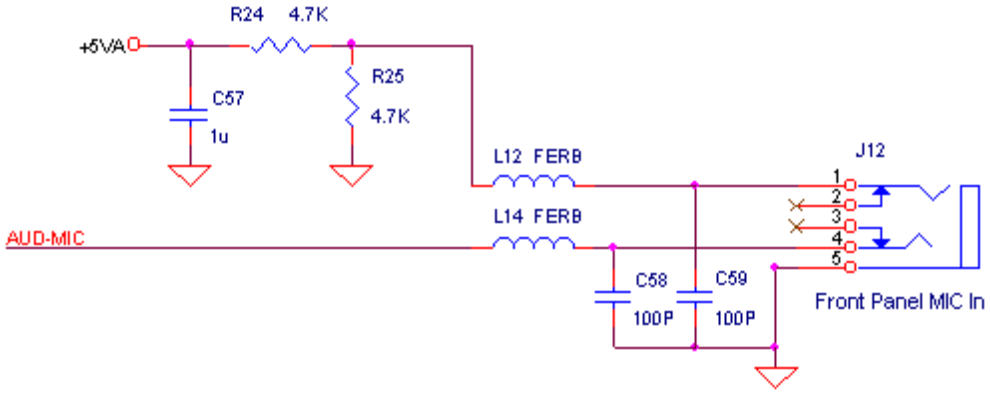
7. Stereo MIC Input

ALC203 supports 2 microphone inputs, MIC1 (pin21) and MIC2 (pin22). MIC1 and MIC2 can be implemented as stereo microphone input. Or either microphone input can also be implemented individually.

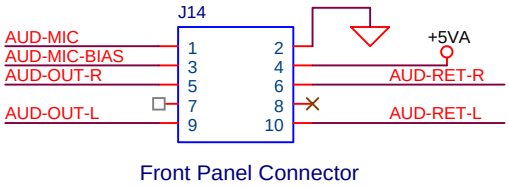


Implementation of Stereo MIC-in

For the phone jack in the front panel, following INTEL's "Front Panel IO Connectivity Design Guide V1.0" specifications, MIC-in phone jack in the front panel is implemented as in the diagram below.



Implementation of MIC-in in front panel

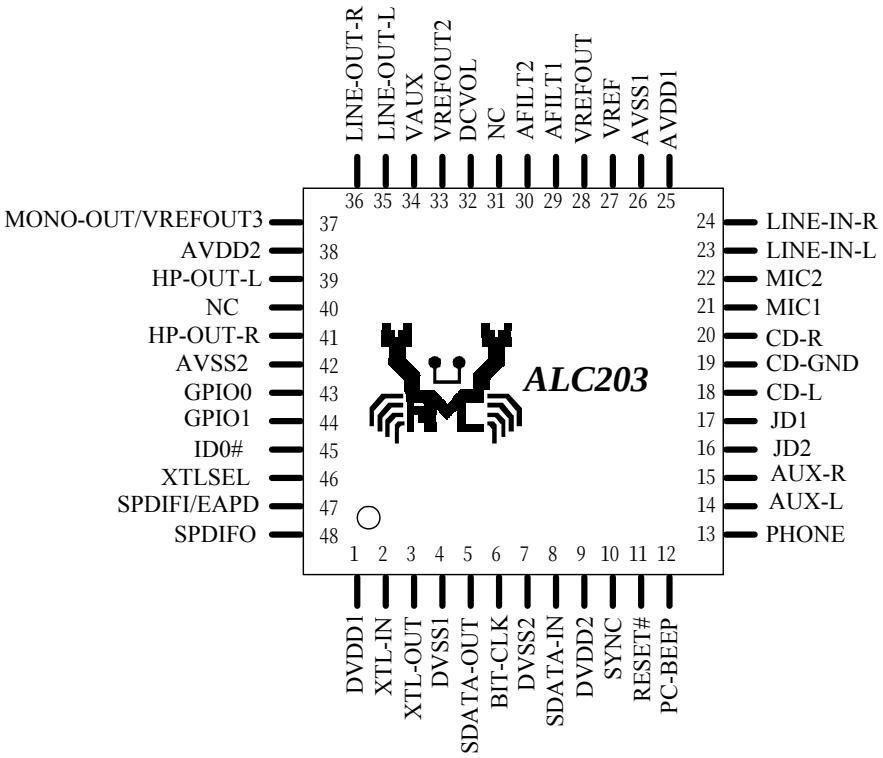


Implementation of MIC-in in front panel connector

8. S/PDIF-In Function

ALC203 support the S/PDIF-In function. The frequency of the S/PDIF signal is about 1.5MHz~6MHz. Therefore, to prevent cross-talk interference from S/PDIF output, *do not* layout S/PDIF input and S/PDIF output traces in a parallel configuration. It is recommended to maintain double width or ground between S/PDIF input and S/PDIF output traces.

9. Pin Assignments



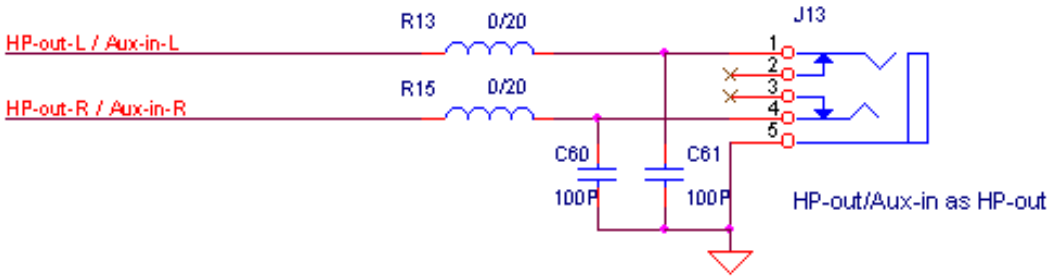
10. Complete Application Circuits

The application circuits are contained in a separate file. Please refer to the file titled “ALC203_Demo_Circuit_Ver_xx.PDF” for the schematics for those circuits.

11. Regulator Selection

The ALC203 has built in amplifiers. It normally consumes 60mA from +5V AVDD when driving active powered speakers. If the ALC203 drives earphones with 16ohm load on both amplifiers, ALC203 will consume more than 100mA power from the +5V regulator when playing a testing full swing sine wave. To prevent the power regulator from overheating, it is recommended to use a +5V regulator with internal thermal overload protection and at least 200mA output current capability. For example the LM7805CT can be used.

If only a 78L05 is used to supply 100mA output current, a 20Ω resister should be placed in the path of HP-out or Aux-in as HP-out to limit current consumption. This will protect the 78L05 from damage.



Serial resistor on output path to limit current

The following table shows the maximum current consumed from AVDD under various loads. These test values are measured by a 2-channel DAC playing a full-scale sinusoidal wave (1KHz, 44.1KHz sampling rate) on HP-out.

	Powered Speaker	20 Ω Earphone	16 Ω Earphone	8 Ω passive speaker
R13, R15 = 0 ohm	58 mA	97 mA	110 mA	141 mA
R13, R15 = 20 ohm	58 mA	81 mA	88 mA	94 mA

Playing a full scale sinusoidal wave, power consumed from +5V AVDD

12. S/PDIF IO Layout Guide

Crosstalk is an undesirable feature with S/PDIF signals. It causes a disturbance between S/PDIF-IN and S/PDIF-OUT signals. Mutual coupling mechanisms will be formed if S/PDIF-IN and S/PDIF-OUT are parallel, the mutual capacitance and mutual inductance between traces have capacitive and inductive coupling of electromagnetic field generated by S/PDIF-OUT. Figure 12-1 indicates the coupling energy from S/PDIF-OUT may interfere S/PDIF-IN operation.

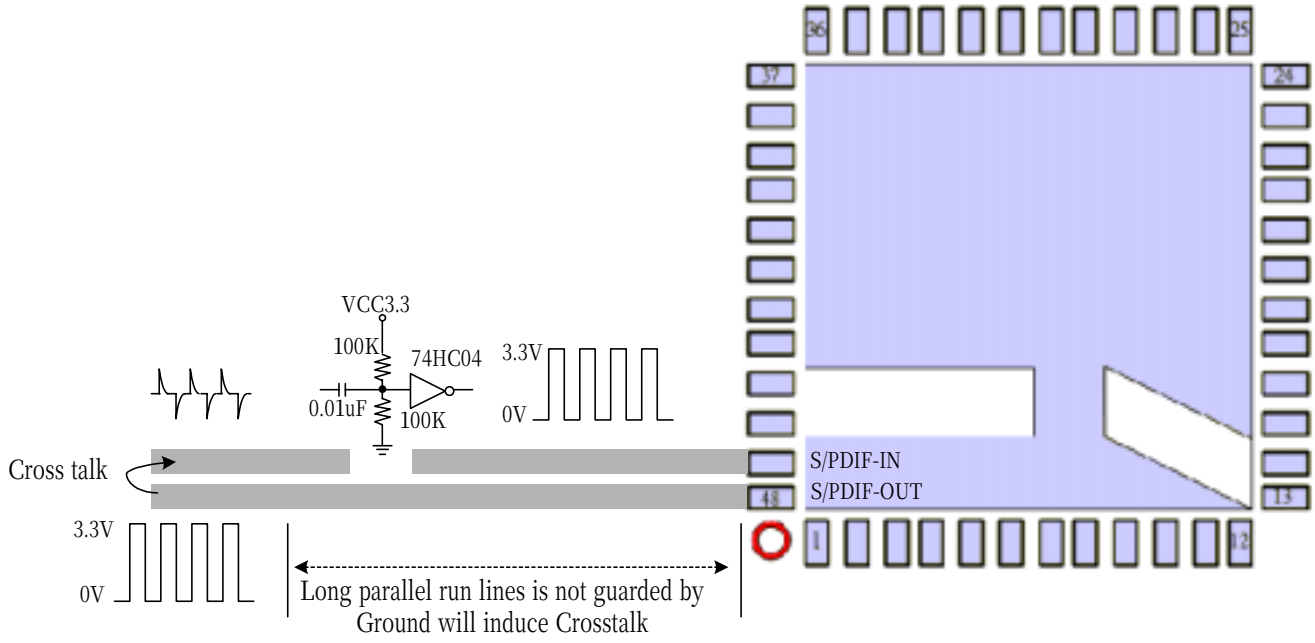


Figure 12-1 Crosstalk between S/PDIF-IN and S/PDIF-OUT traces

Design and layout rules listed here are useful to prevent crosstalk.

1.Minimize physical distance between IO connector (or header) and ALC203.

2.Avoid routing of S/PDIF-IN trace parallel to S/PDIF-OUT. Figure 12-2 shows an approximate equation to minimize crosstalk, distance (H) with reference plane must be minimized, and distance (D) between traces must be maximized. (Refer to "High Speed Digital Design". Johnson, H. W., and M. Graham. 1993. Englewood Cliffs, NJ: Prentice Hall)

3.S/PDIF-IN and S/PDIF-OUT signals are separated by ground traces will reduce crosstalk. (Figure 12-3)

4.A simple rule to minimize coupling between traces is the 3-W rule. The distance separation between centerline of traces must be three times the width of a single trace. (Figure 12-4)

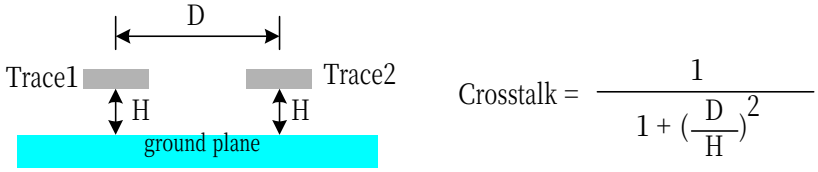


Figure 12-2 Approximate equation to estimate crosstalk

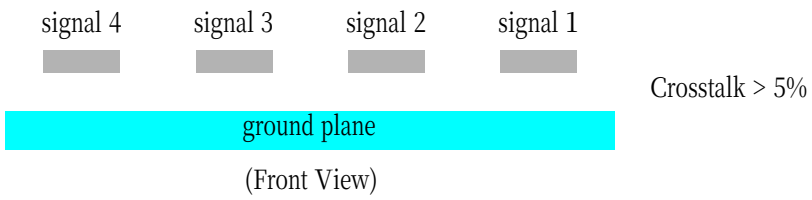


Figure 12-3a Traces without separation have significant crosstalk

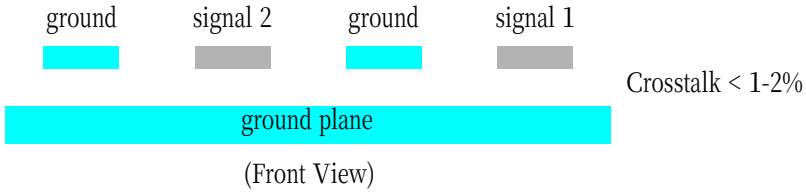


Figure 12-3b Traces separated by ground can reduce crosstalk

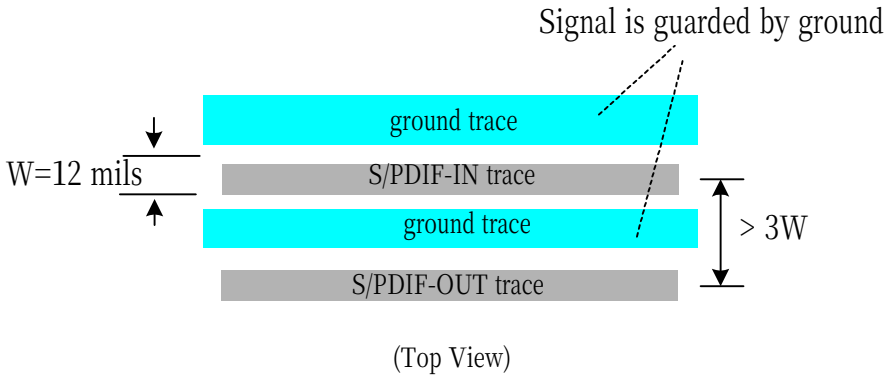


Figure 12-4 The 3-W rule to minimize coupling

Additional to above layout rules, the 3-W rule represents the approximate only 70% flux boundary, 10-W should be used to get approximate 98% boundary. (Refer to "EMC and the Printed Circuit Board", Mark I. MONTROSE) However, it may be not easy to separate traces with 10-W distance, Figure 12-5 is 5-W (W=12 mils) separations adapted on Realtek's demo board.

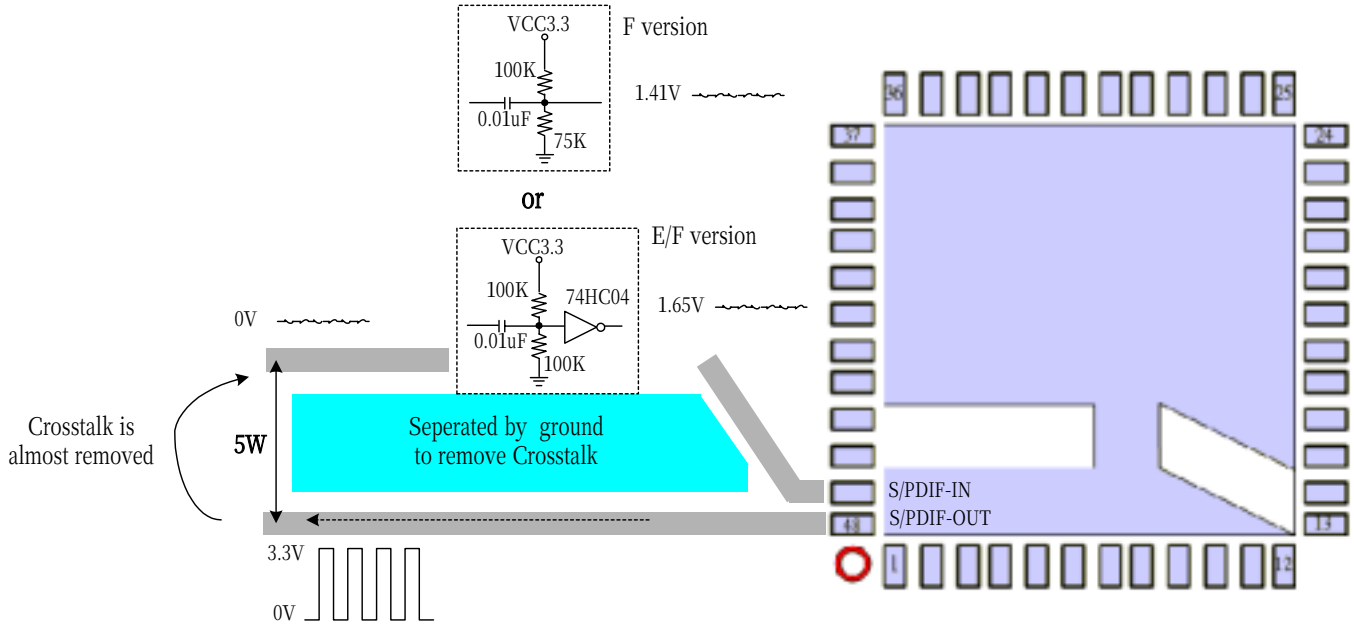
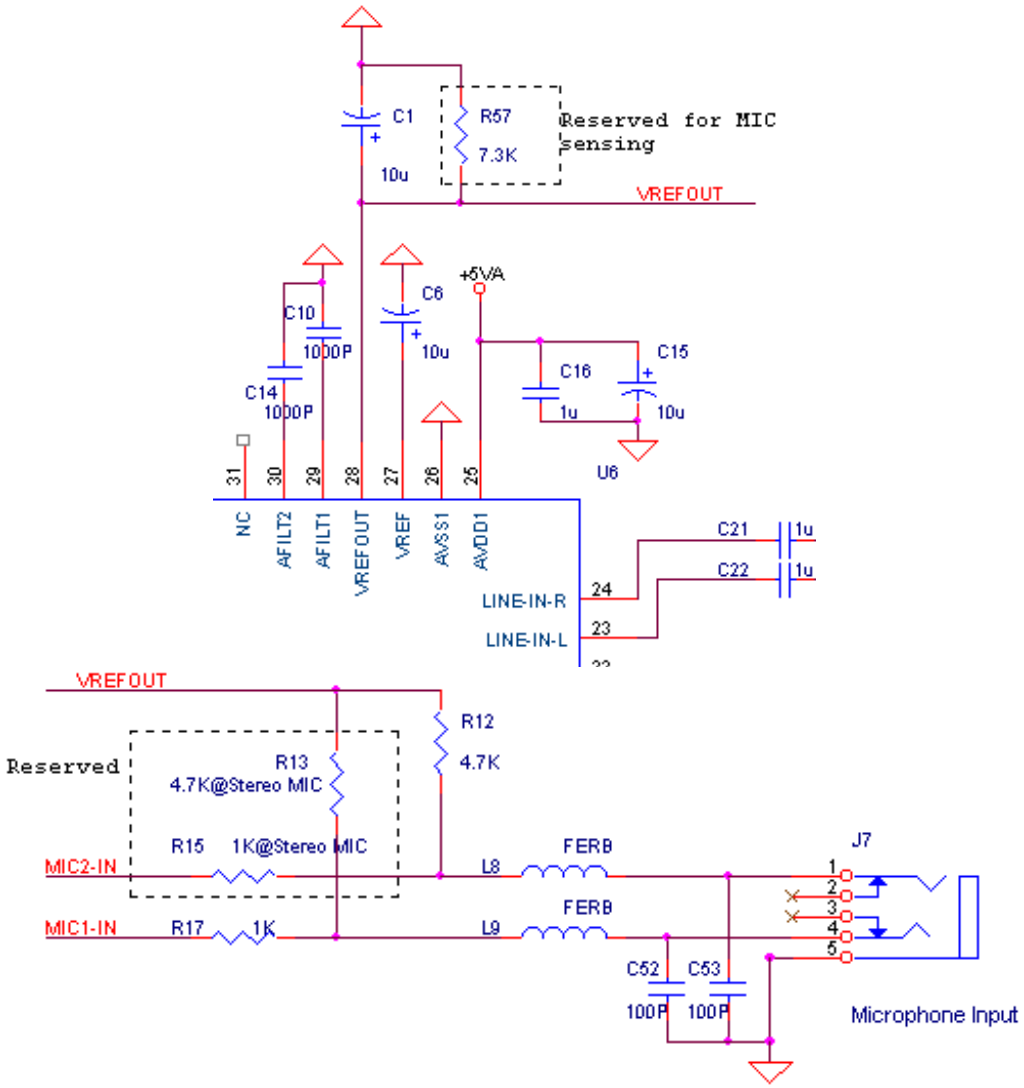


Figure 12-5 The suggested layout on Realtek's demo board

13. Jack Sense

ALC203 supports AC'97 2.3 "Jack Sensing and reporting of connected devices" features on Line-out, Line-in and Mic-in. With this feature, end users could easily get the phone jacks' status when plugging devices into. However, motherboard manufactures don't need to change too much in the circuit design. Only need to attach one resistor parallel with filter capacitor on Vrefout, shown as below. And do nothing to Line-out and Line-in for jack sensing.

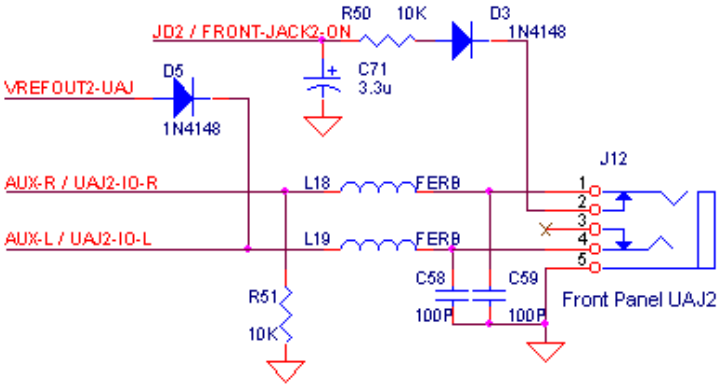


Circuit modification of Mic-in Jack Sensing implementation

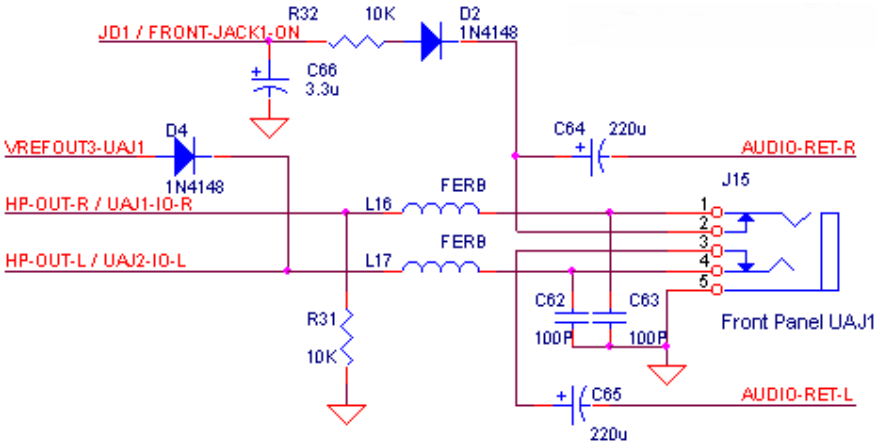
Notice: the resistor R57 is used to fine tune jack sense, so the value may range from 6.8k to 8.2k

14. Universal Audio Jack®

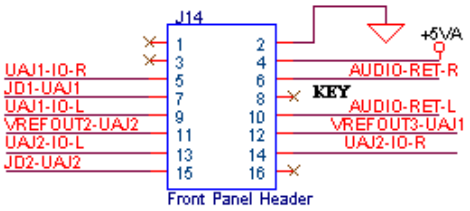
ALC203 supports a proprietary technology "Universal Audio Jack" which bases on AC'97 2.3 "Jack Sensing and reporting connected device" concepts and provides more intelligent way to sense the devices plugged into phone jack. ALC203 has 2 sets of UAJ, which are UAJ1 on 39/41 (HP-out) accompanied with JD1 (pin17) and Vrefout3 (pin13), and UAJ2 on 14/15 (Aux-in) accompanied with JD2 (pin16) and Vrefout2 (pin32). Those JDs and Vrefout2/3 are dedicated to each UAJ set, so be careful not to erroneously connect. To implement UAJ, motherboard manufactures need do some modifications on the circuit design. Illustrations of UAJ implemented on the front panel and pin assignment modification of front panel header are shown below.



UAJ2 on front panel



UAJ1 on front panel



Front panel header pin assignment

Notice:
**UAJ1: pin39,41 (HP-out), pin13 (Vrefout3/Mono-out) and pin17 (JD1) are used*
**UAJ2: pin14,15 (Aux-in), pin32 (Vrefout2) and pin16 (JD2) are used*

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