

High Performance Regulators for PCs

Nch FET Ultra LDO

for PC Chipsets



BD3506F, BD3506EFV

No.10030EAT30

Description

The BD3506F/EFV is an ultra-low dropout linear regulator for chipset that can achieve ultra-low voltage input to ultra-low voltage output. By using N-MOS FET for built-in power transistor, the regulator can be used at ultra-low I/O voltage difference up to voltage difference generated by ON resistor ($R_{on} = 120\text{ m}\Omega/100\text{ m}\Omega$). Because by reducing the I/O voltage difference, large current ($I_{omax} = 2.5\text{ A}$) output is achieved and conversion loss can be reduced, switching power supply can be replaced. BD3506F/EFV does not need any choke coil, diode for rectification and power transistors which are required for switching power supply, total cost of the set can be reduced and compact size can be achieved for the set. Using external resistors, optional output from 0.65V to 2.5V can be set. In addition, since voltage output start-up time can be adjusted by using the NRCS terminal, it is possible to meet the power supply sequence of the set.

Features

- 1) Built-in high-accuracy reference voltage circuit ($0.65\text{ V} \pm 1\%$)
- 2) Built-in VCC low input maloperation prevention circuit ($V_{cc} = 4.15\text{ V}$)
- 3) Reduced rush current by NRCS
- 4) Built-in ultra-low on-resistor ($120/100\text{ m}\Omega$ typ) Nch Power MOSFET (BD3506F/BD3506EFV)
- 5) Built-in current limiting circuit (2.5 A min)
- 6) Built-in thermal shutdown circuit
- 7) Output variable type ($0.65\text{--}2.5\text{ V}$)
- 8) Adoption of SOP8 package (BD3506F): $5.0 \times 6.2 \times 1.5\text{ (mm)}$
- 9) Adoption of high power HTSSOP-B20 package (BD3506EFV): $5.0 \times 6.4 \times 1.0\text{ (mm)}$

Applications

Mobile PC, desktop PC, LCD-TV, DVD, digital home appliances

Line up

Parameter	BD3506F	BD3506EFV
R_{on}	120m Ω	100m Ω
Output Current	2.5A	2.5A
Package	SOP8	HTSSOP-B20

Absolute Maximum Ratings($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Ratings		Unit
		BD3506F	BD3506EFV	
Input Voltage1	VCC	7 * ¹	7 * ¹	V
Input Voltage2	VIN	7 * ¹	7 * ¹	V
Enable Input Voltage	Ven	7	7	V
Power Dissipation1	Pd1	560 * ²	-	mW
Power Dissipation2	Pd2	690 * ³	1000 * ⁴	mW
Operating Temperature Range	Topr	-10~+100	-10~+100	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55~+125	-55~+125	$^\circ\text{C}$
Maximum Junction Temperature	Tjmax	+150	+150	$^\circ\text{C}$

*¹ However, not exceeding Pd.

*² In the case of $T_a \geq 25^\circ\text{C}$ (no heat radiation board), derated at $4.48\text{ mW}/^\circ\text{C}$.

*³ In the case of $T_a \geq 25^\circ\text{C}$ (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at $5.52\text{ mW}/^\circ\text{C}$.

*⁴ In the case of $T_a \geq 25^\circ\text{C}$ (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at $8.00\text{ mW}/^\circ\text{C}$.

●Recommended Operating Conditions(Ta=25°C)

Parameter	Symbol	Ratings		Unit
		MIN	MAX	
Input Voltage1	VCC	4.3	5.5	V
Input Voltage2	VIN	1.2	VCC-1 * ⁵	V
Output Voltage	Vo	VFB	2.5	V
Enable Input Voltage	Ven	-0.3	5.5	V
Capacitor in NRCS pin	CNRCS	0.001	1	μF

*⁵ However, irrespective of charging order of VCC and VIN.

* No radiation-resistant design is adopted for the present product.

●Electrical Characteristics (unless otherwise noted, Ta=25 VCC=5V Ven=3V VIN=1.8V R1=3.9KΩ R2=3.3KΩ)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Bias Current	I _{CC}	-	0.7	1.4	mA	
Bias current	I _{ST}	-	0	10	μA	Ven=0V
Shut-Down Mode Current	V _{OUT}	-	1.200	-	V	I _o =50mA
Output Voltage	I _o	2.5	-	-	A	
Maximum Output Current	I _{ost}	-	2.0	-	A	Vo=0V
Maximum Short Current	T _{cvo}	-	0.01	-	%/°C	
Temperature coefficient of Output Voltage	V _{FB1}	0.643	0.650	0.657	V	I _o =50mA
Feed Back Voltage 1	V _{FB2}	0.630	0.650	0.670	V	I _o =0 to 2A, Ta=-10 to 100°C* ⁵
Feed Back Voltage 2	Reg.I1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 1	Reg.I2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Line Regulation 2	Reg.L	-	0.5	10	mV	I _o =0 to 2A
Dropout Voltage (BD3506F)	dVo	-	120	200	mV	I _o =1A, VIN=1.2V, Ta=-10 to 100°C* ⁵
Dropout Voltage (BD3506EFV)	dVo	-	100	160	mV	I _o =1A, VIN=1.2V, Ta=-10 to 100°C* ⁵
Standby Discharge Current	I _{den}	150	-	-	mA	Ven=0V, Vo=1V
[Enable]						
High level Enable Input Voltage	Enhi	2	-	5.5	V	
Low level Enable Input Voltage	Enlow	-0.3	-	0.8	V	
Enable pin Input Current	I _{en}	-	7	10	μA	Ven=3V
[Voltage Feed Back]						
Feed Back terminal Bias Current	I _{FB}	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	I _{nrCS}	14	20	26	μA	V _{nrCS} =0.5V
NRCS Standby Voltage	V _{STB}	-	0	50	mV	Ven=0V
[UVLO]						
VCC UVLO	V _{CCUVLO}	4.00	4.15	4.30	V	V _{CC} :Sweep-up
VCC UVLO Hysteresis	V _{CCHYS}	100	160	220	mV	V _{CC} :Sweep-down

*⁵ Design Guarantee

●Reference Data

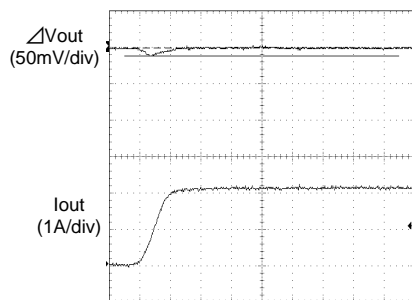


Fig.1 Transient Response

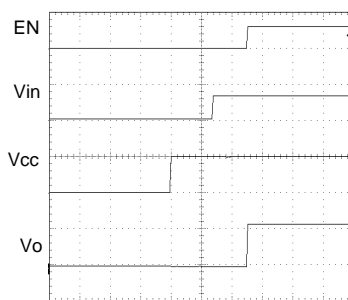
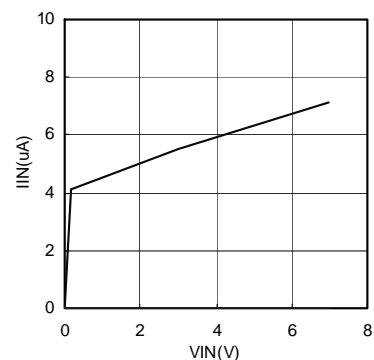
Fig.2 Input Voltage Sequence
Final Input Voltage
EN

Fig.3 VIN-IIN(Ta=25°C)

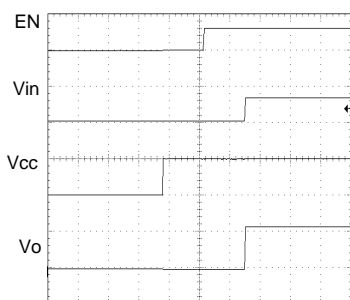
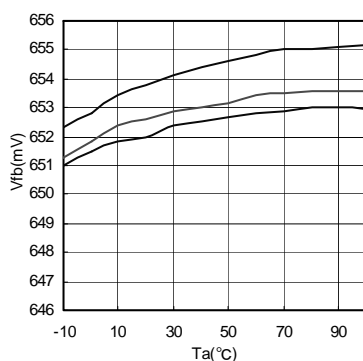
Fig.4 Input Voltage Sequence
Final Input Voltage
VIN

Fig.5 Ta-Vfb

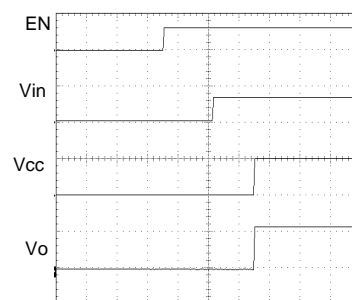
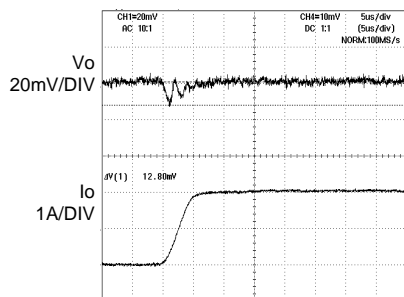
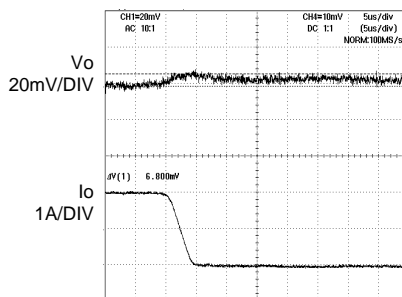
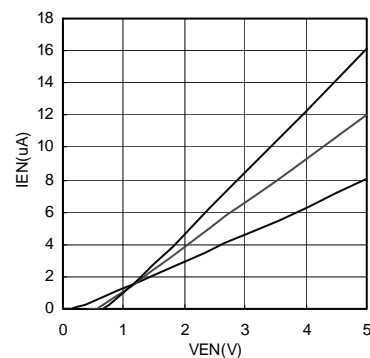
Fig.6 Input Voltage Sequence
Final Input Voltage
VCCFig.7 Transient Response (rise)
Cout=100uFFig.8 Transient Response (fall)
Cout=100uF

Fig.9 VEN-IEN

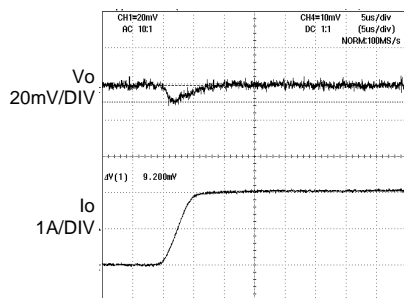
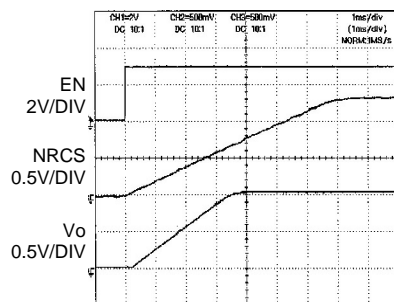
Fig.10 Transient Response (rise)
Cout=220uF

Fig.11 Start up Wave Form

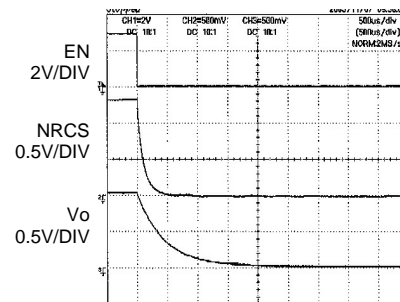
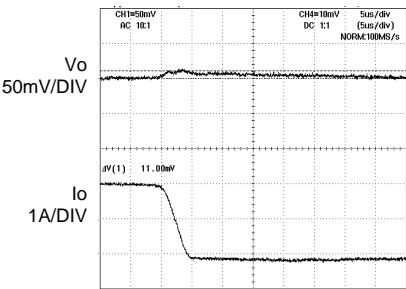
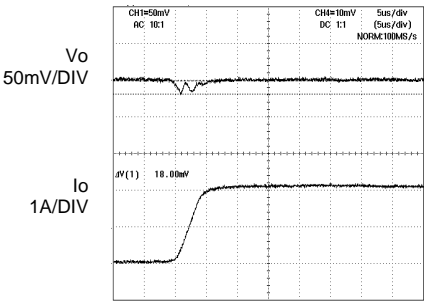
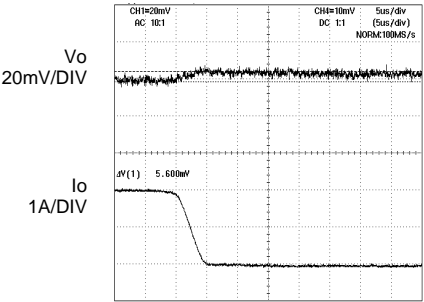
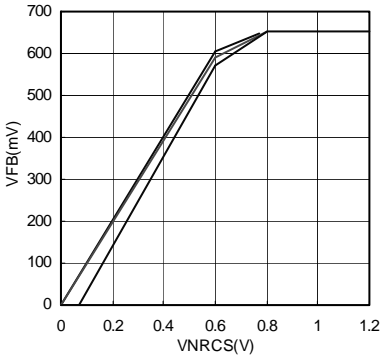
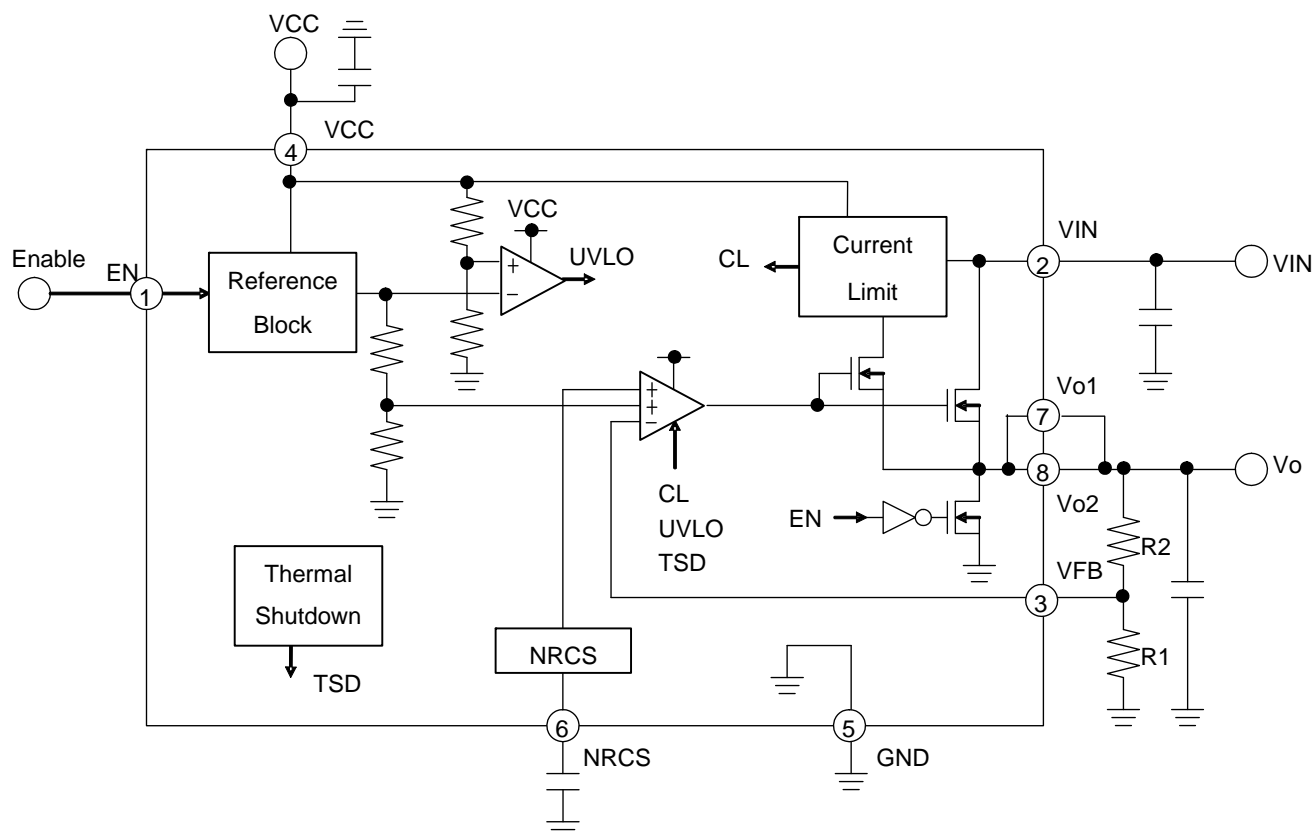


Fig.12 Shut down Wave Form

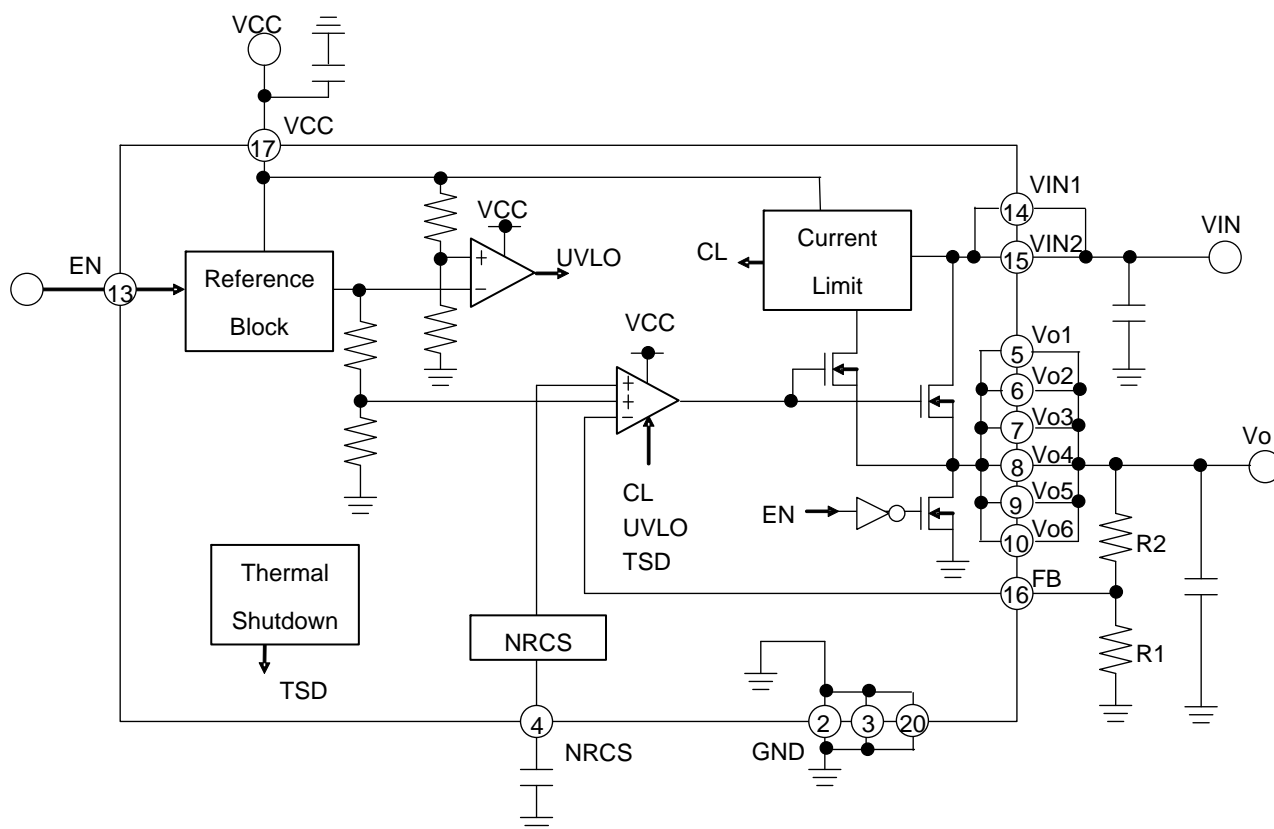


●Block Diagram

©BD3506F



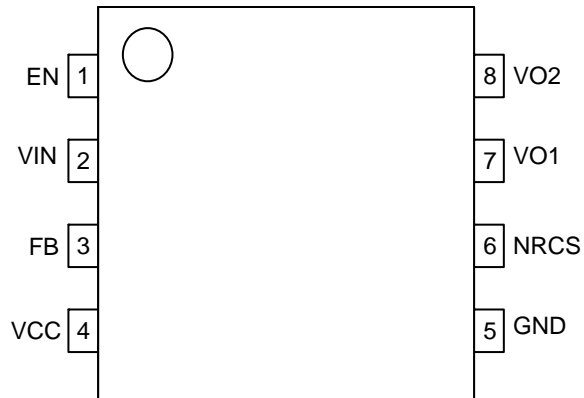
©BD3506EFV



●Pin Configuration and Pin Function

◎BD3506F

○Pin Configuration

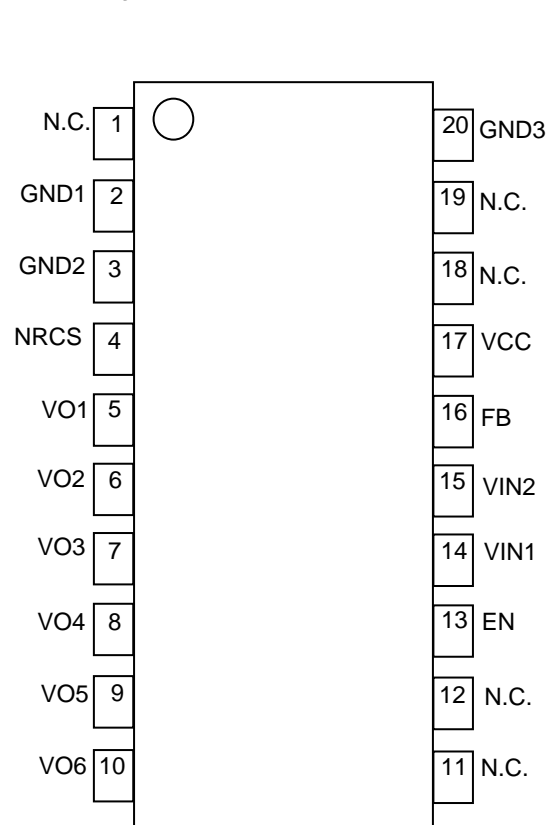


○Pin Function

Pin No.	Pin Name	PIN FUNCTION
1	EN	Enable Pin
2	VIN	Input Voltage Pin
3	FB	Output Voltage Feedback
4	VCC	Power Source
5	GND	Ground Pin
6	NRCS	NRCS(Non Rush Current on Start Up) time setup
7	VO1	VO1 Pin
8	VO2	VO2 Pin

◎BD3506EFV

○Pin Configuration



○Pin Function

PIN No.	PIN Name	PIN FUNCTION
1	N.C.	Non connection
2	GND1	Ground1 Pin
3	GND2	Ground2 Pin
4	NRCS	NRCS(Non Rush Current on Start Up) time setup
5	VO1	VO1 Pin
6	VO2	VO2 Pin
7	VO3	VO3 Pin
8	VO4	VO4 Pin
9	VO5	VO5 Pin
10	VO6	VO6 Pin
11	N.C.	Non connection
12	N.C.	Non connection
13	EN	Enable Pin
14	VIN1	Input Voltage1 Pin
15	VIN2	Input Voltage2 Pin
16	FB	Output Voltage Feedback
17	VCC	Power Source
18	N.C.	Non connection
19	N.C.	Non connection
20	GND3	Ground3 Pin

●Block Function**•AMP**

An error amplifier that compares reference voltage (VREF) to Vo and drives Nch FET (Ron = 120/100 mΩ) of output. The frequency characteristics are optimized so that low ESR functional polymer capacitor can be used for the output capacitor and high-speed transient response can be achieved. The input voltage range at the AMP section is GND-2.5V and the output voltage range of the AMP section is GND-VCC. At the time of EN OFF or UVLO, the output is brought to the LOW level and the output NchFET is turned OFF.

•EN

By the logic input pin, regulator ON/OFF is controlled. At the time of OFF, the circuit current is controlled to be 0 μA to reduce the standby current consumption of the apparatus. In addition, EN turns ON FET that can discharge NRCS terminal Vo and removes excess electric charge to prevent maloperation of IC on the load side. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence.

•UVLO

UVLO turned OFF output to prevent output voltage from making maloperation at the time of Vcc reduced voltage. Same as EN, UVLO discharges NRCS Vo. When voltage exceeds the threshold voltage (TYP 4.15V), UVLO starts output.

•CURRENT LIMIT

In the event the output current that exceeds the current (2.5A or more) set inside the IC flows when output is turned ON, output voltage is attenuated to protect the IC on the load side. When current reduces, output voltage returns to the set voltage.

•NRCS

Connecting an external capacitor to the counter-GND of NRCS pin can achieve soft start. The output voltage startup time is determined by the time when the NRCS terminal reaches VFB (0.65V). During start-up, the NRCS terminal serves as a constant current source of 20 μA (Typ.) output, and charges the capacitor externally connected.

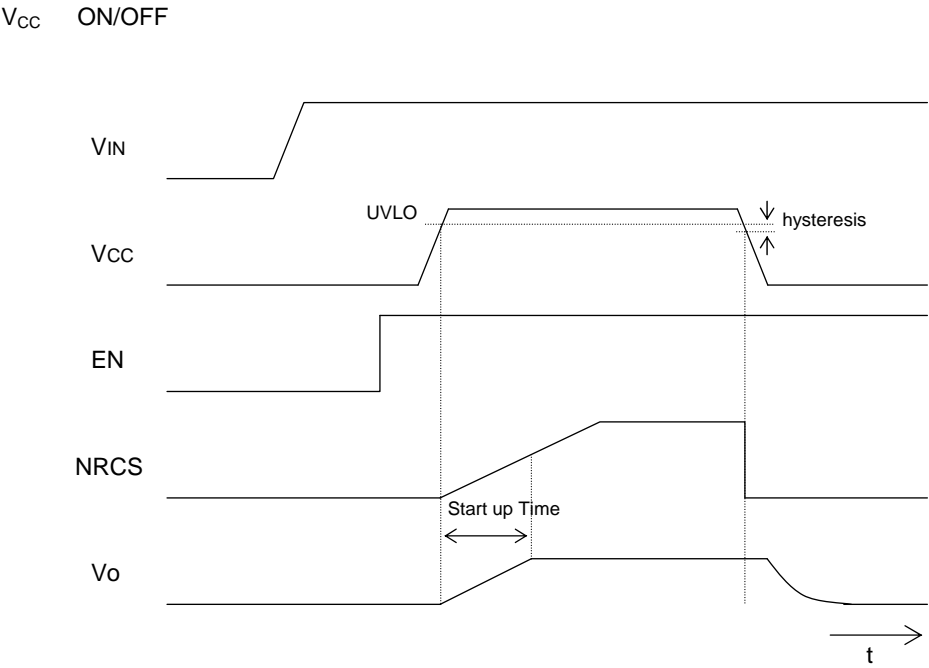
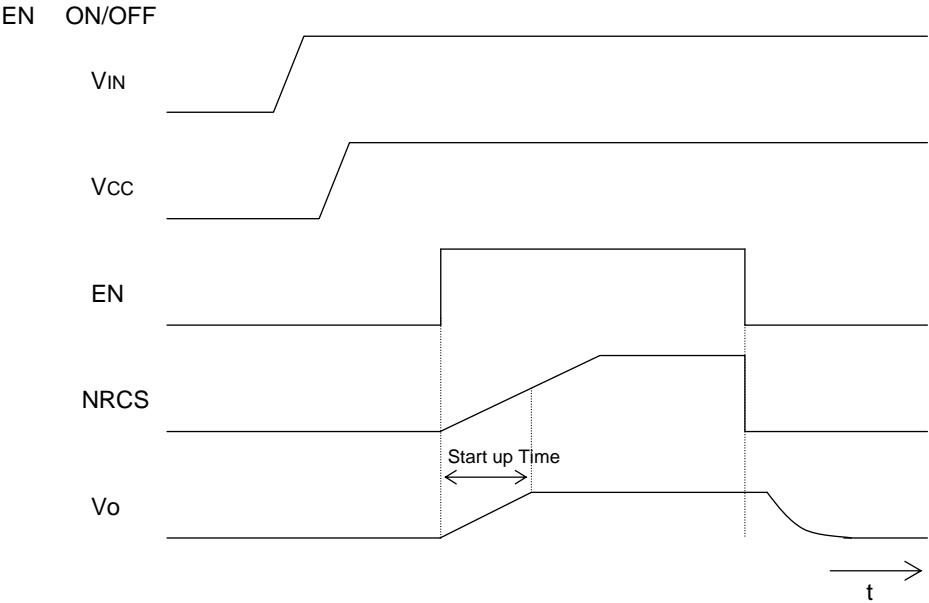
•TSD (Thermal Shut down)

In order to prevent thermal breakdown and thermal runaway of the IC, the output is turned OFF when chip temperature becomes high. In addition, when temperature returns to the specified temperature, the output is recovered. However, since the temperature protection circuit is originally built in to protect the IC itself, thermal design within Tj(max) is requested.

•VIN

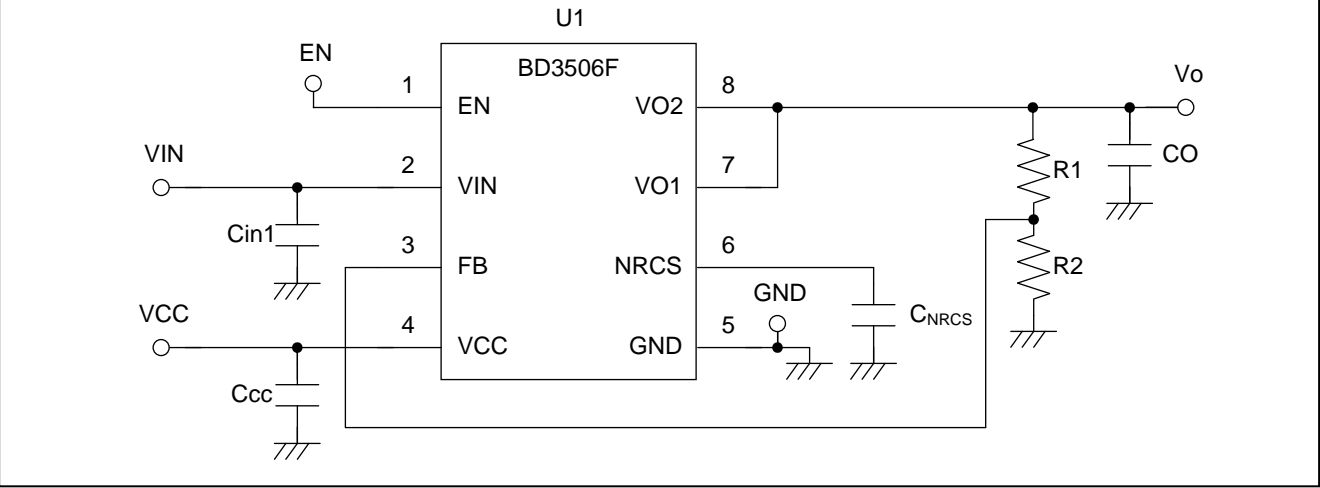
This is a large-current supply line. The VIN terminal is connected to the drain of output NchFET. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence. However, because there is body Di of output NchFET between VIN and Vo, there is electrical connection (Di-connection) between VIN and Vo. Consequently, when the output is turned ON/OFF by VIN, reverse current flows from Vo to VIN, to which care must be taken.

●Timing Chart



●Evaluation Board

■BD3506F Evaluation Board Circuit

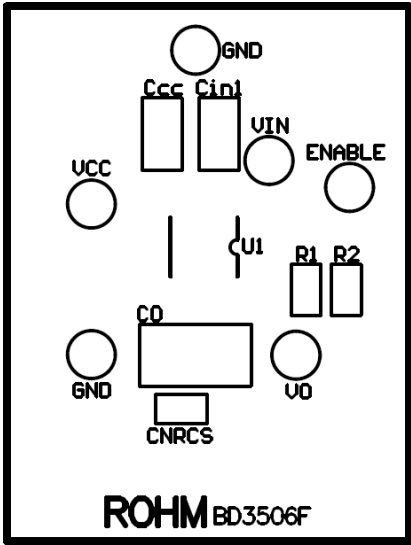


■BD3506F Evaluation Board Application Components

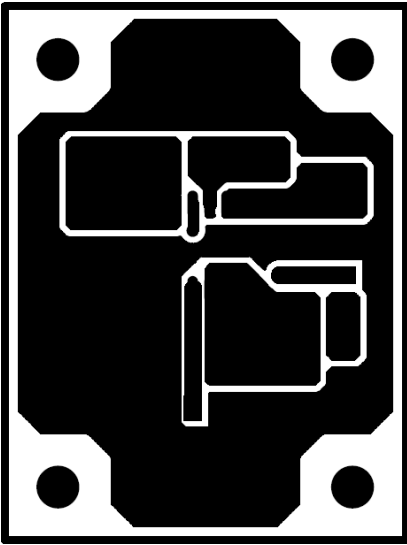
Part No	Value	Company	Parts Name
U1	-	ROHM	BD3506F
R1	3.3k	ROHM	MCR03Series
R2	3.9k	ROHM	MCR03Series

Part No	Value	Company	Parts Name
Ccc	1μF	MURATA	GRM18 Series
Cin1	10μF	MURATA	GRM21 Series
Co	220μF	SANYO,etc	2R5TPE220MF
C6	0.01μF	MURATA	GRM18 Series

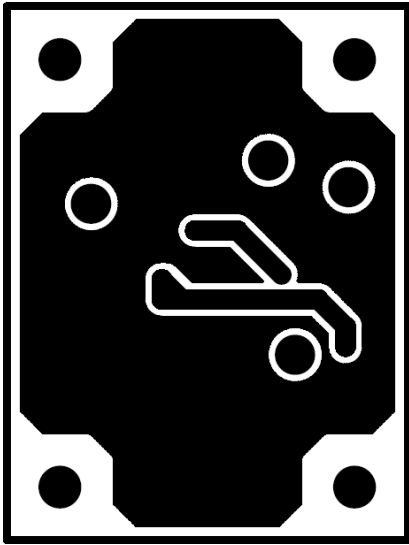
■BD3506F Evaluation Board Layout
Silk Screen



TOP Layer

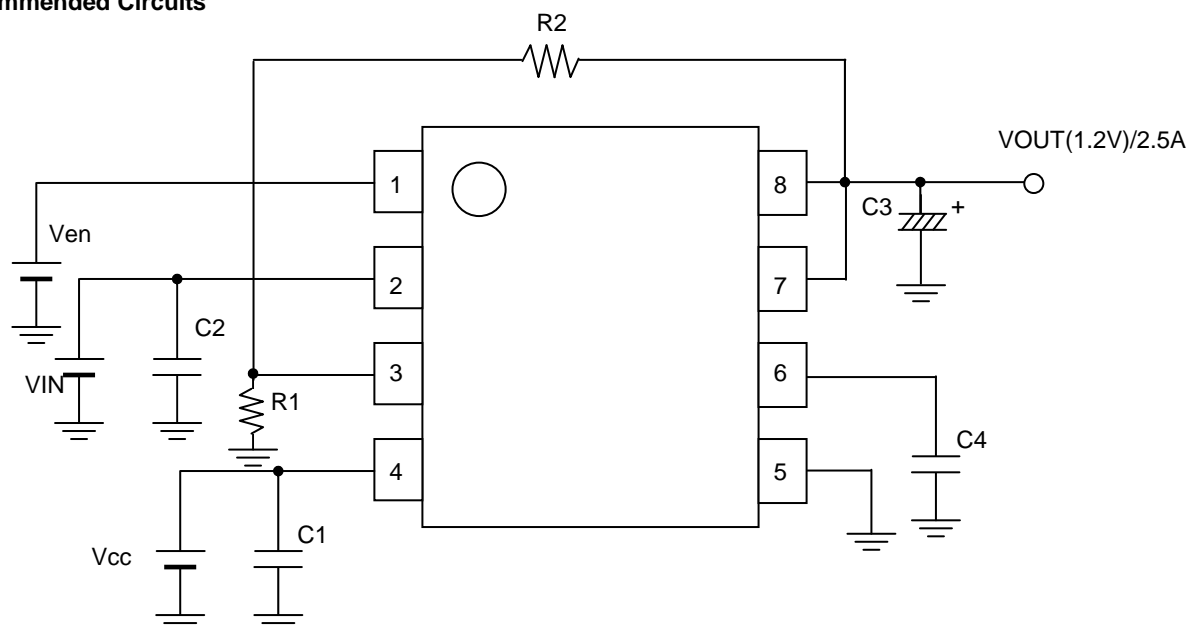


Bottom Layer



For Evaluation Board, BD3506EFV is available.

●Recommended Circuits



Part No	Value	Notes for use
R1/R2	6.5k/5.5k	The present IC can set output voltage by external reference voltage (VR) and value of output voltage setting resistors (R1, R2). Output voltage can be set by $VR \times R2 / (R1 + R2)$ but it is recommended to use at the resistance value (total: about 10 kΩ) which is not susceptible to VREF bias current (± 100 nA).
C3	100μF	Connect the output capacitor between Vo1, Vo2 terminals and GND terminal without fail in order to stabilize output voltage. The output capacitor has a role to compensate for the phase of loop gain and to reduce output voltage fluctuation when load is rapidly changed. When there is an insufficient capacity value, there is a possibility to cause oscillation, and when the equivalent serial resistance (ESR) of the capacitors is large, output voltage fluctuation is increased when load is rapidly changed. About 100-μF high-performance electrolytic capacitors are recommended but output capacitor greatly depends on temperature and load conditions. In addition, when only ceramic capacitors with low ESR are used, or various capacitors are connected in series, the total phase allowance of loop gain becomes not sufficient, and oscillation may result. Thoroughgoing confirmation at application temperature and under load range conditions is requested.
C1	0.1μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (Vcc). When output impedance of this power supply increases, the input voltages (Vcc,) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 0.1 μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C2	10μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (VIN). When output impedance of this power supply increases, the input voltages (VIN) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10 μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C4	1μF	To the present IC, there mounted is a function (Non Rush Current on Start-up: NRCS) to prevent rush current from VIN to load and output capacitor via Vo at the output voltage start-up. When the EN terminal is reset from High or UVLO, constant current is allowed to flow from the NRCS terminal. By this current, voltage generated at the NRCS terminal becomes the reference voltage and output voltage is started. In order to stabilize the NRCS set time, it is recommended to use a capacitor (B special) with less capacity value change caused by temperature change.

●About heat loss

In designing heat, operate the apparatus within the following conditions.
(Because the following temperatures are warranted temperature, be sure to take margin, etc. into account.)

1. Ambient temperature T_a shall be not more than 100°C.
2. Chip junction temperature T_j shall be not more than 150°C.

Chip junction temperature T_j can be considered under the following two cases.

- ① Chip junction temperature T_j is found from IC surface temperature T_C under actual application conditions:

$$T_j = T_C + \theta_{j-c} \times W$$

<Reference value>

θ_{j-c} : SOP8 41.0°C/W

HTSSOP-B20 45.0°C/W

Substrate size: 70 × 70 × 1.6mm
(Substrate surface copper foil area: less 3%)

θ_{j-a} : HTSSOP-B20 125.0°C/W

86.2°C/W

54.3°C/W

39.1°C/W

- ② Chip junction temperature T_j is found from ambient temperature T_a :

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference value>

θ_{j-a} : SOP8 222.0°C/W (IC only)

181.0°C/W Single-layer substrate

(substrate surface copper foil area: less 3%)

Single-layer substrate

(substrate surface copper foil area: less 3%)

2nd-layer

86.2°C/W (substrate surface copper foil area: 15 × 15mm²)

2nd-layer

54.3°C/W (substrate surface copper foil area: 70 × 70mm²)

4th-layer

39.1°C/W (substrate surface copper foil area: 70 × 70mm²)

Substrate size 70 × 70 × 1.6mm³ (thermal vias in the board.)

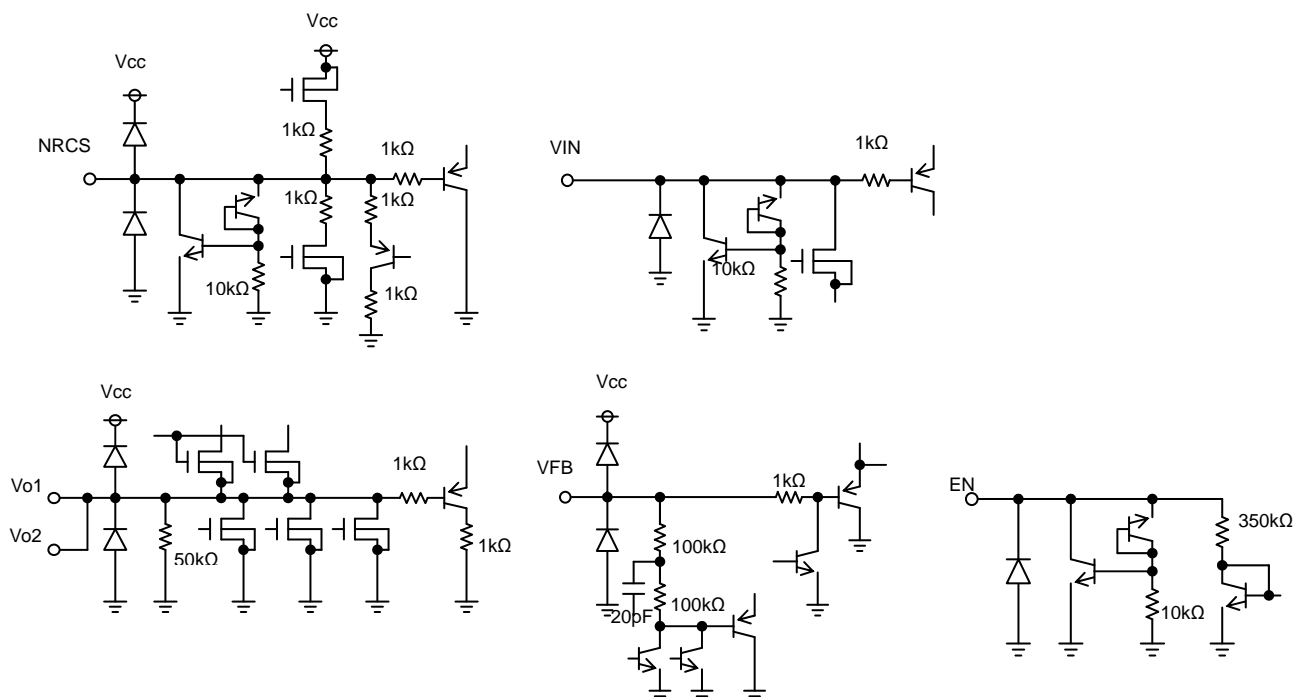
Most of heat loss in BD3506F/EFV occurs at the output Nch FET. The power lost is determined by multiplying the voltage between V_{IN} and V_o by the output current. Confirm voltage and output current conditions of V_{IN} and V_o used, and collate them with the thermal derating characteristics. Because BD3506EFV employs the power PKG, the thermal derating characteristics significantly vary in accord with the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power dissipation (W) = {Input voltage (V_{IN}) – Output voltage ($V_o \doteq V_{REF}$)} × I_o (averaged)

Ex.) If V_{IN} = 1.8 volts, V_o = 1.2 volts, and I_o (averaged) = 1.5 A, the power dissipation is given by the following:

$$\begin{aligned} \text{Power dissipation (W)} &= (1.8 \text{ volts} - 1.2 \text{ volts}) \times 1.5 \text{ (A)} \\ &= 0.9 \text{ W} \end{aligned}$$

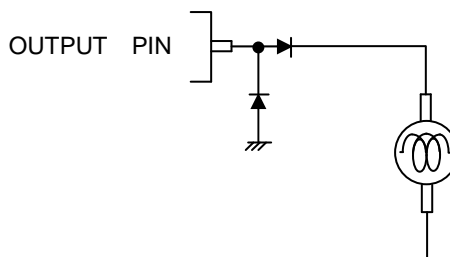
●Equivalent Circuit



●Notes for use

1. Input terminals (VCC,VIN,EN)
In the present IC, EN terminal, VIN terminal, and VCC terminal have an independent construction. In addition, in order to prevent malfunction at the time of low input, the UVLO function is equipped with the VCC terminal. They begin to start output voltage when all the terminals reach threshold voltage without depending on the input order of input terminals.
2. Operating range
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.
3. Permissible dissipation
With respect to the permissible dissipation, the thermal derating characteristics are shown in the Exhibit, which we hope would be used as a good-rule-of-thumb. Should the IC be used in such a manner to exceed the permissible dissipation, reduction of current capacity due to chip temperature rise, and other degraded properties inherent to the IC would result. You are strongly urged to use the IC within the permissible dissipation.
4. Built-in thermal shutdown protection circuit
The thermal shutdown circuit is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.
5. Inspection by set substrate
In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.
6. For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc..
7. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.
8. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)



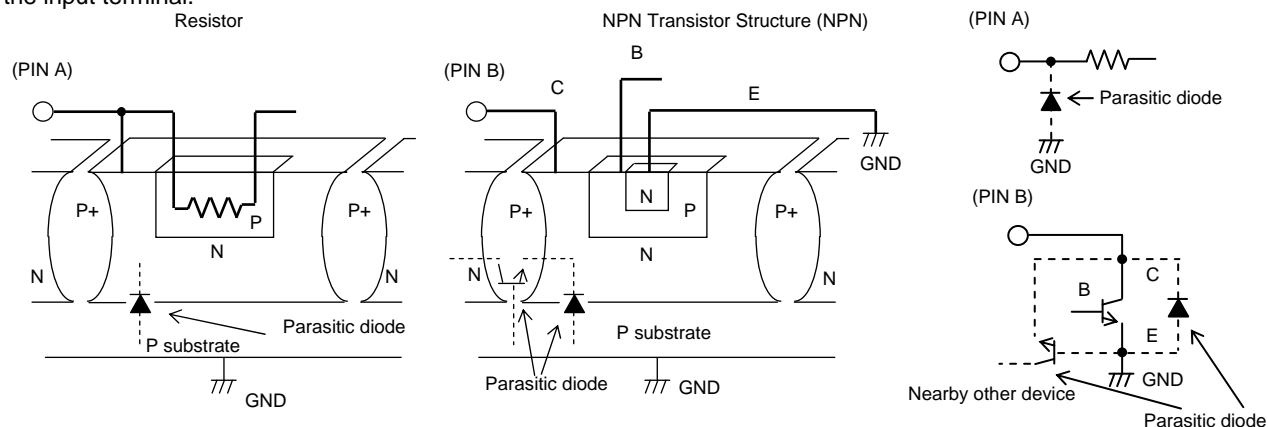
9. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC. In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.

10. The present IC is a monolithic IC and has P⁺ isolation between elements to separate elements and a P substrate. With this P layer and N layer of each element, PN junction is formed, and various parasitic elements are formed. For example, when resistors and transistors are connected to terminals as illustrated below,

Oat the resistor, when GND>terminal A, and at transistor (NPN), when GND>terminal B,PN junction works as a parasitic diode.

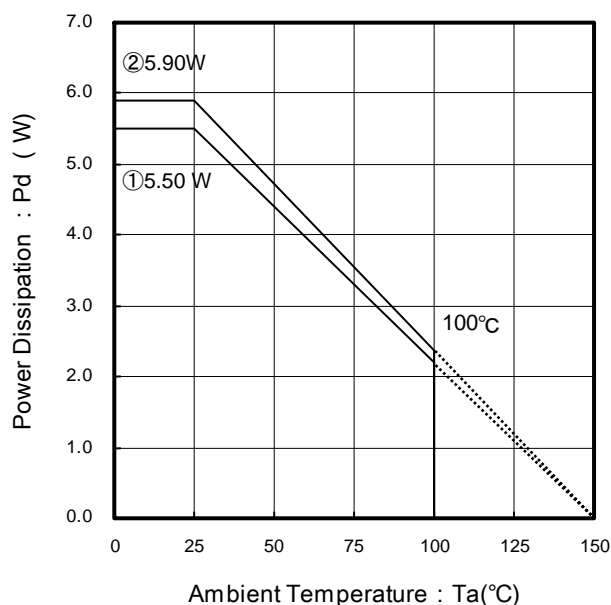
Oat the transistor (NPN), when GND>terminal B,the parasitic NPN transistor is operated by the N-layer of other element adjacent to the parasitic diode.

The parasitic element is inevitably formed because of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC to operate the parasitic element such as applying voltage lower than GND (P substrate) to the input terminal.



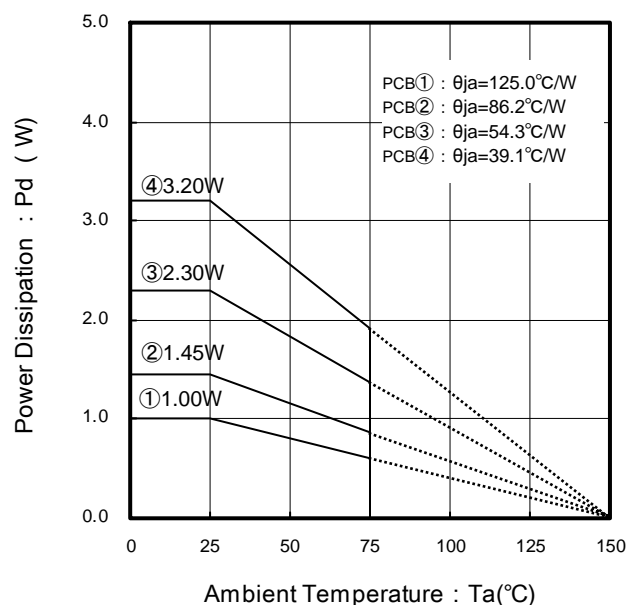
●Power Dissipation

SOP8



- ① Without heat sink
 $\theta_{j-a}=222^{\circ}\text{C/W}$
 ② Mounted on board
 70mm×70mm×1.6mm Glass-epoxy PCB
 $\theta_{j-a}=181^{\circ}\text{C/W}$

HTSSOPB-20



measure : TH-156(Kuwano-Denki)
measure condition : Rohm Standard Board
PCB size : 70mm×70mm×1.6mm(PCB with Thermal Via)
PCB① : Single-layer substrate
PCB② : Double-layer substrate
(substrate surface copper foil area 15mm × 15mm)
PCB③ : Double-layer substrate
(substrate surface copper foil area 70mm × 70mm)
PCB④ : Fourth-layer substrate
(substrate surface copper foil area 70mm × 70mm)

B	D	3	5	0	6	E	F	V	-	E	2
Part No.		Part No.				Package F : SOP8 EFV : HTSSOPB-20			Packaging and forming specification E2: Embossed tape and reel		

Technical drawing of the 1000 Series PCB Mounting Dimensions. The drawing shows a top view and a side view of a component.

Top View Dimensions:

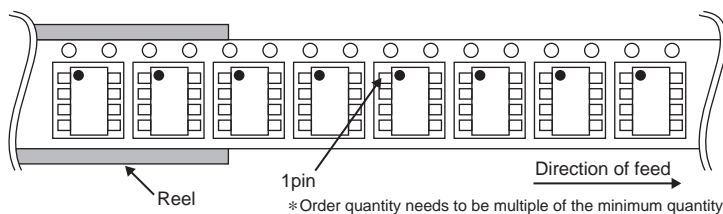
- Overall width: 6.2 ± 0.3
- Mounting hole diameter: 4.4 ± 0.2
- Pin pitch: 5.0 ± 0.2 (MAX 5.35 include BURR)
- Pin numbers: 1, 2, 3, 4, 5, 6, 7, 8
- Mounting hole diameter: $0.17 \begin{smallmatrix} +0.1 \\ -0.05 \end{smallmatrix}$
- Pin diameter: 0.42 ± 0.1
- Mounting hole depth: 0.3 MIN
- Angle: $4^\circ \begin{smallmatrix} +6^\circ \\ -4^\circ \end{smallmatrix}$

Side View Dimensions:

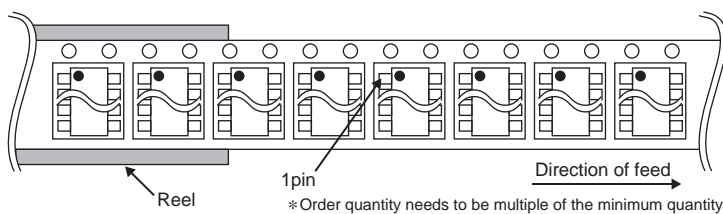
- Overall height: 1.5 ± 0.1
- Mounting hole diameter: $0.17 \begin{smallmatrix} +0.1 \\ -0.05 \end{smallmatrix}$
- Pin diameter: 0.42 ± 0.1

(Unit : mm)

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

[illegible]

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

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