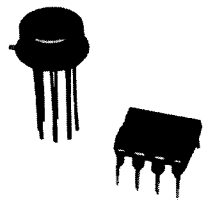
BURR-BROWN®



OPA2111

MILITARY & DIE VERSIONS AVAILABLE

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested: 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

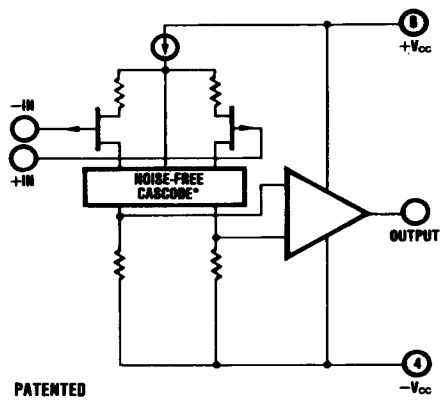
The OPA2111 is a high precision monolithic *Difet* (dielectrically isolated FET) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op-amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 SIMPLIFIED CIRCUIT (EACH AMPLIFIER)

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-540C

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
NOISE														
Voltage, f_O = 10Hz	Max: 100% tested		40	80		30	60		40	80		40		nV/√Hz
f_O = 100Hz	Max: 100% tested		15	40		11	30		15	40		15		nV/√Hz
f_O = 1kHz	Max: 100% tested		8	15		7	12		8	15		8		nV/√Hz
f_O = 10kHz	(1)		6	8		6	8		6	8		6		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7	1.2		0.6	1.0		0.7	1.2		0.7		µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24		15		fA, p-p
f_O = 0.1Hz to 20kHz	(1)		0.8	1.3		0.6	1.0		0.8	1.0		0.8		fA/√Hz
OFFSET VOLTAGE[2]														
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75		±0.3	±2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			±1			±0.5			2			2		µV/°C
Supply Rejection		90	110		96	110		90	110		86	110		dB
			±3	±31		±3	±16		±3	±31		±3	±50	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136			136		dB
BIAS CURRENT[2]														
Initial Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8		±3	±15	pA
Match			±1			±0.5			±1			2		pA
OFFSET CURRENT[2]														
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6		±3	±12	pA
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11	±10	±11		±10	±11			±10	±11	V	
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ	16	32		16	32		16	32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2			2		V/µs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6			6		µs
0.01%	10V step		10			10			10			10		µs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7		5	9	mA
TEMPERATURE RANGE														
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	0		+70	°C
Operating "M" Package	Ambient temp.	−55		+125	−55		+125	−55		+125	−55		+125	°C
"P" Package											−40		+85	°C
Storage "M" Package	Ambient temp.	−65		+150	−65		+150	−65		+150	−65		+150	°C
"P" Package											−40		+85	°C
θ Junction-Ambient			200			200			200			200[4]		°C/W

NOTES: (1) Sample tested—maximum parameters are guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical θ_{J-A} = 150°C/W for plastic DIP.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

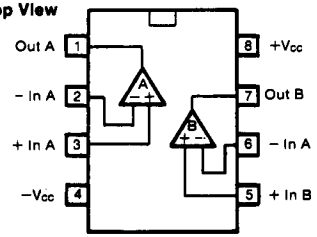
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	0		+70	°C
INPUT														
OFFSET VOLTAGE(1)	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5		±0.9	±5	mV
Input Offset Voltage			±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Average Drift			1			0.5			2			2		µV/°C
Match			100			100			100			100		dB
Supply Rejection		86	±10	±50	90	±10	±32	86	±10	±50	82	±10	±80	µV/V
BIAS CURRENT(1)	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2.0nA	±16.3nA		±125	±500	pA
Initial Bias Current			60			30			1nA					pA
Match														
OFFSET CURRENT(1)	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
Input Offset Current														
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		80	100		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		100	120		dB
Match			5			3			5			5		dB
RATED OUTPUT														
Voltage Output	$R_L = 2k\Omega$	±10.5	±11		±10.5	±11		±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8		5	10	mA

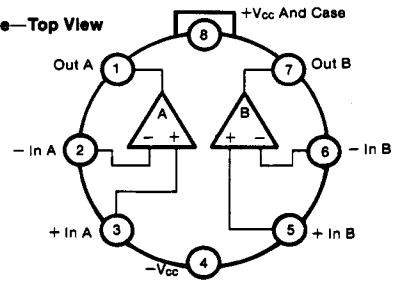
NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAMS

'P' Package—Top View



'M' Package—Top View



ORDERING INFORMATION

Model	Package	Temperature Range	Offset Voltage, max (mV)
OPA2111AM	TO-99	−25°C to +85°C	±0.75
OPA2111BM	TO-99	−25°C to +85°C	±0.5
OPA2111KM	TO-99	0°C to +70°C	±2.0
OPA2111SM	TO-99	−55°C to +125°C	±0.75
OPA2111KP	Plastic	0°C to +70°C	±2.0

BURN-IN SCREENING OPTION

Model	Package	Temperature Range	Burn-in Temp. (160h)(1)
OPA2111AM-BI	TO-99	−25°C to +85°C	+125°C
OPA2111BM-BI	TO-99	−25°C to +85°C	+125°C
OPA2111KM-BI	TO-99	0°C to +70°C	+125°C
OPA2111SM-BI	TO-99	−55°C to +125°C	+125°C
OPA2111KP-BI	Plastic	0°C to +70°C	+85°C

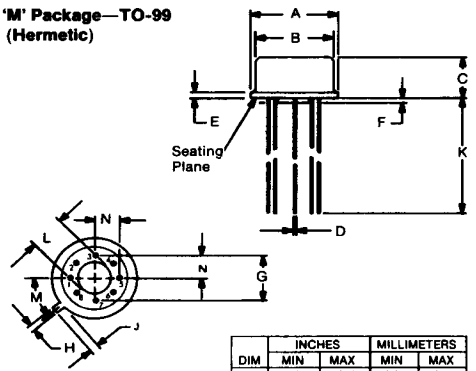
NOTE: (1) Or equivalent combination of time and temperature.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	−65°C to +150°C
"P" Package	−40°C to +85°C
Operating Temperature Range: "M" Package	−55°C to +125°C
"P" Package	−40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to ground (+25°C)	Continuous
Junction Temperature	+175°C

MECHANICAL

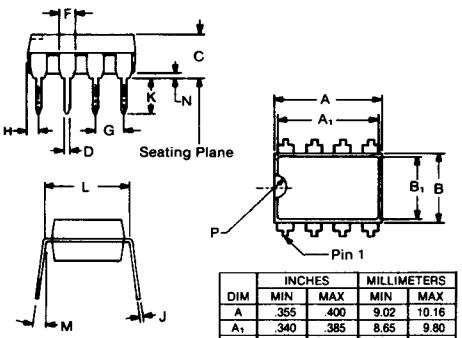
'M' Package—TO-99 (Hermetic)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

'P' Package—Plastic DIP



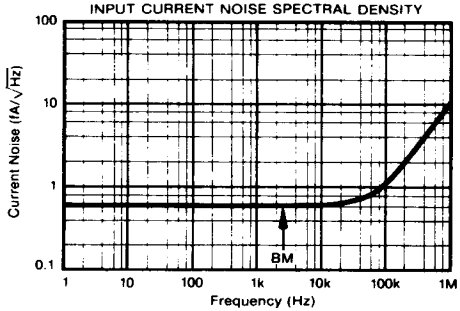
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.02	10.16
A_1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	.0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

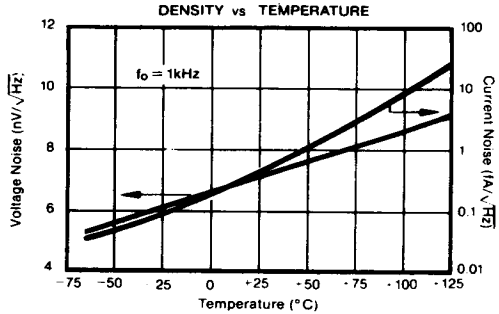
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm 15VDC$ unless otherwise noted.

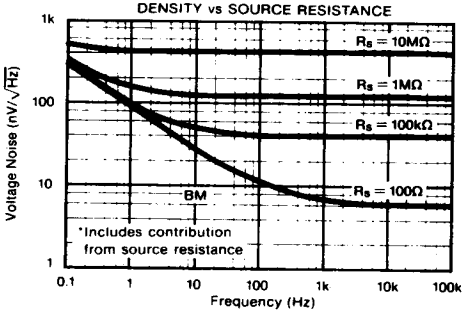
INPUT CURRENT NOISE SPECTRAL DENSITY



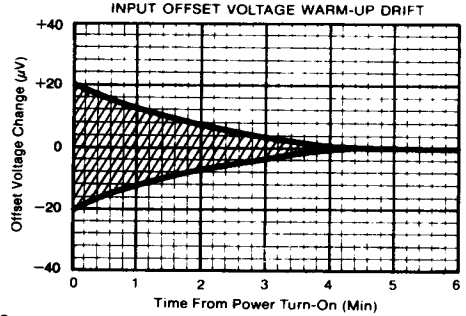
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



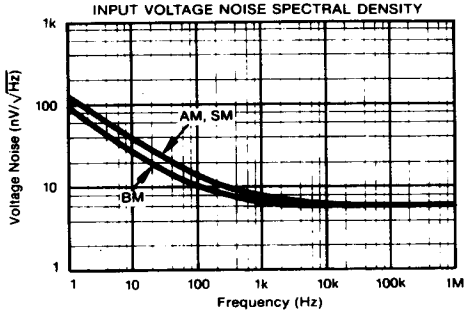
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



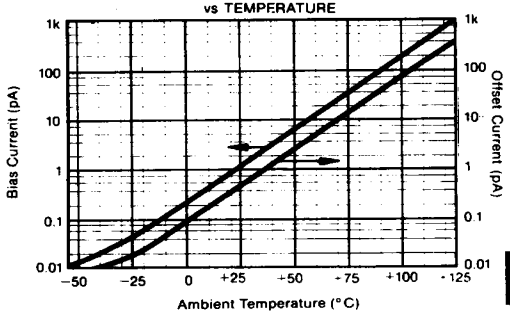
INPUT OFFSET VOLTAGE WARM-UP DRIFT



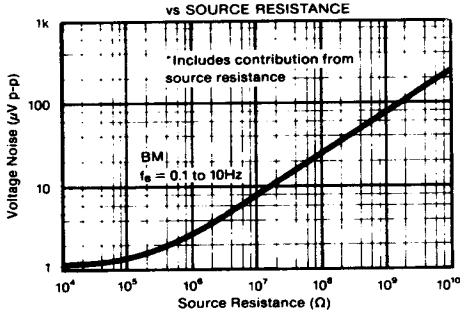
INPUT VOLTAGE NOISE SPECTRAL DENSITY



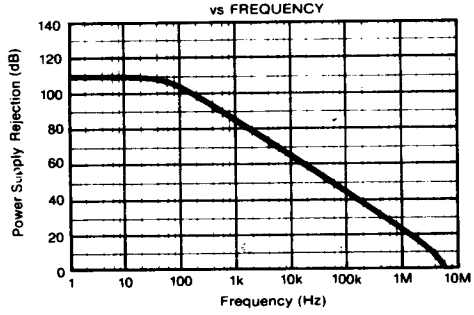
BIAS AND OFFSET CURRENT vs TEMPERATURE



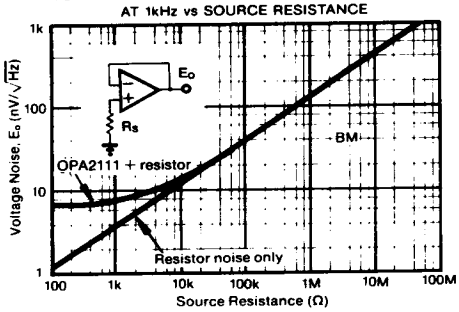
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



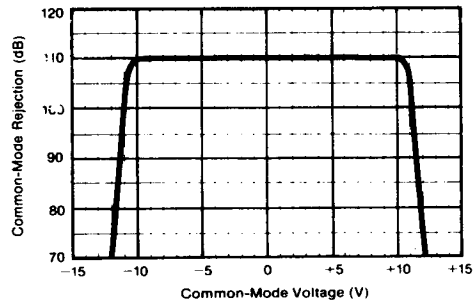
POWER SUPPLY REJECTION vs FREQUENCY



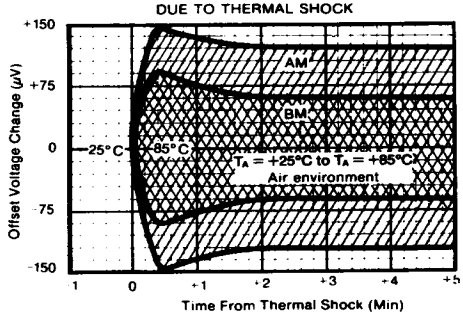
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



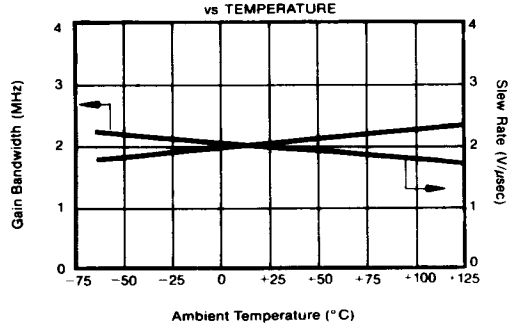
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



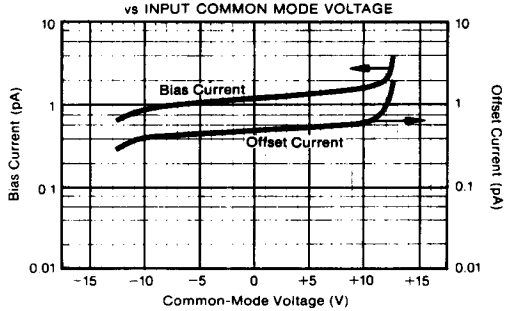
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



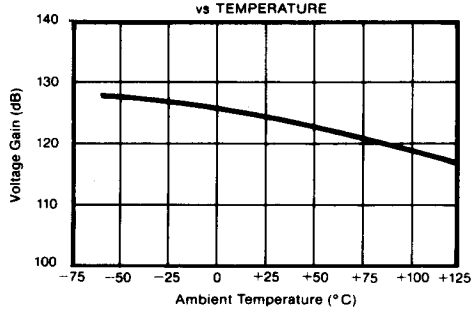
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



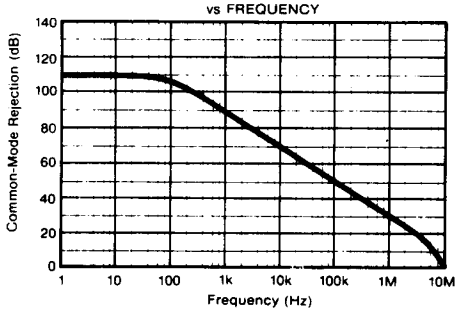
BIAS AND OFFSET CURRENT
vs INPUT COMMON MODE VOLTAGE



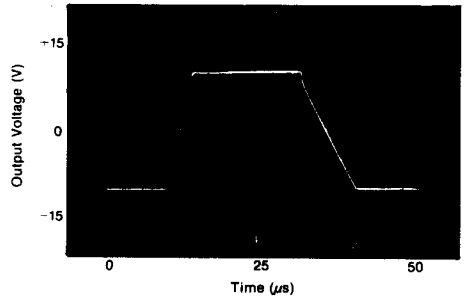
OPEN-LOOP GAIN
vs TEMPERATURE



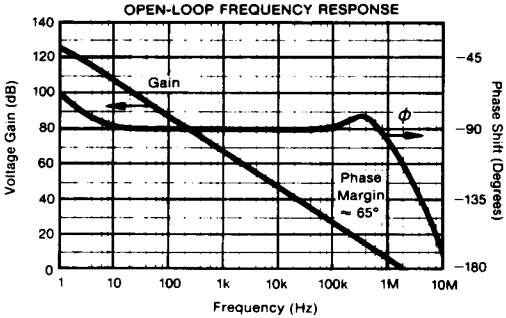
COMMON-MODE REJECTION
vs FREQUENCY



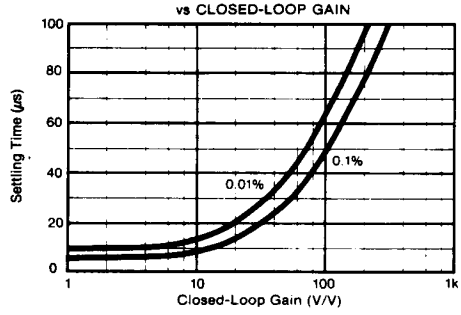
LARGE SIGNAL TRANSIENT RESPONSE



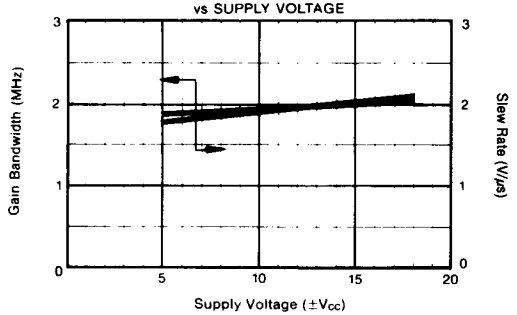
OPEN-LOOP FREQUENCY RESPONSE



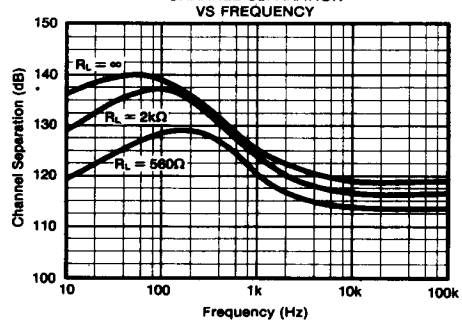
SETTLING TIME
vs CLOSED-LOOP GAIN

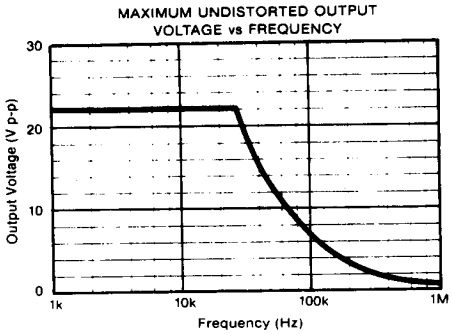


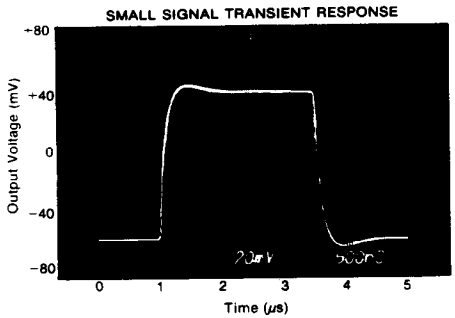
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE

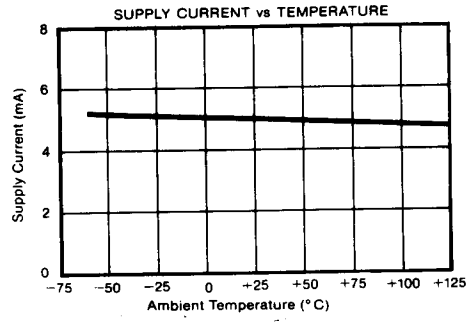


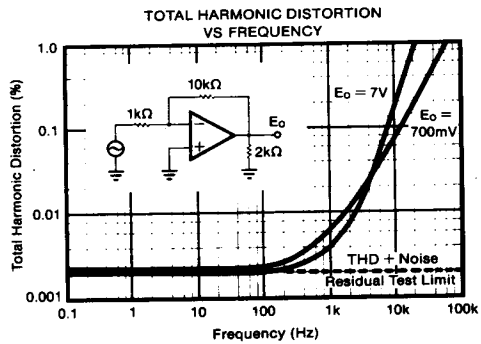
CHANNEL SEPARATION
VS FREQUENCY











APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

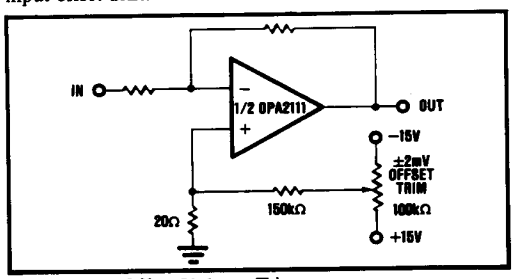


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances

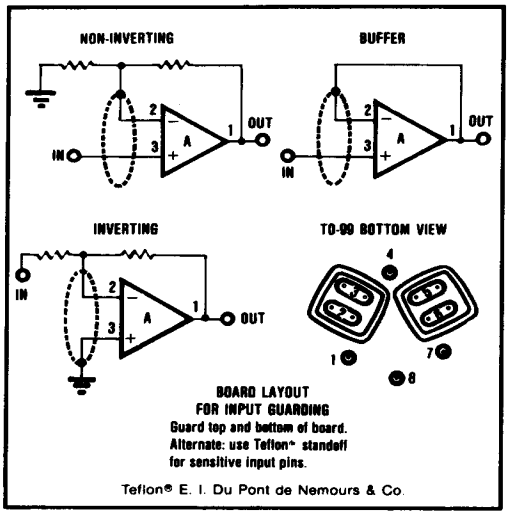


FIGURE 2. Connection of Input Guard.

the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

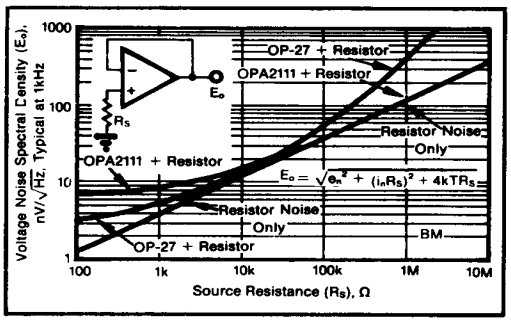


FIGURE 3. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA2111 is not compromised by common-mode voltage.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

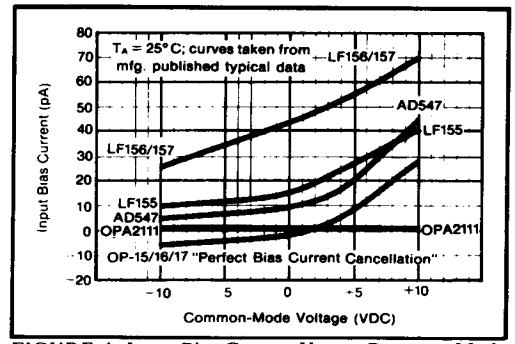


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

Figures 5 through 13 are circuit diagrams of various applications for the OPA2111.

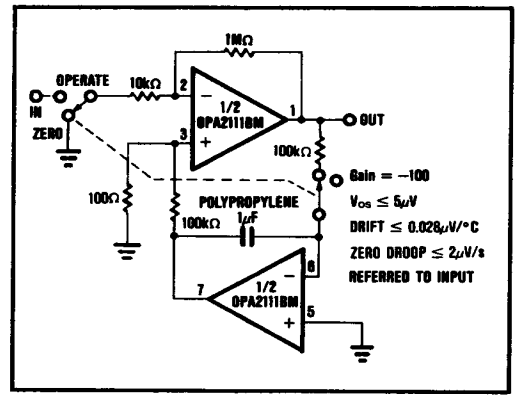


FIGURE 5. Auto-Zero Amplifier.

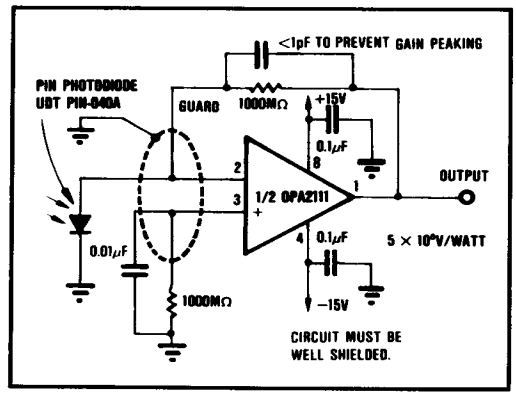


FIGURE 6. Sensitive Photodiode Amplifier.

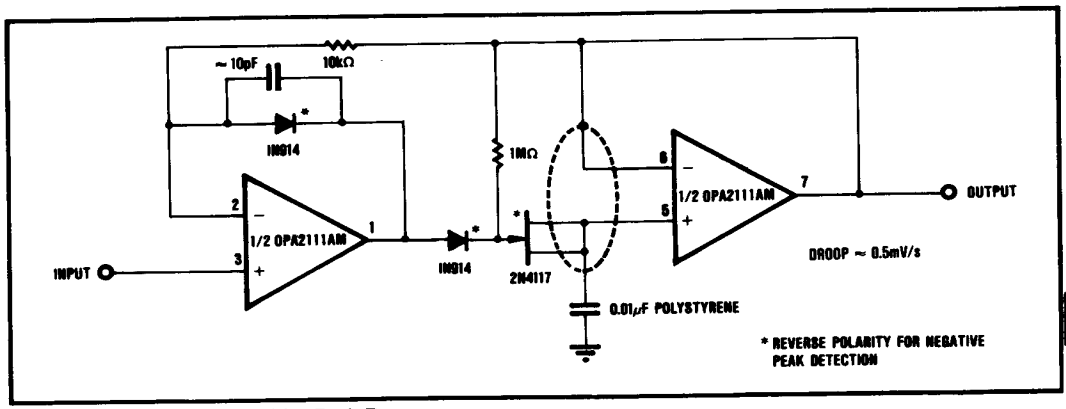


FIGURE 7. Low-Droop Positive Peak Detector.

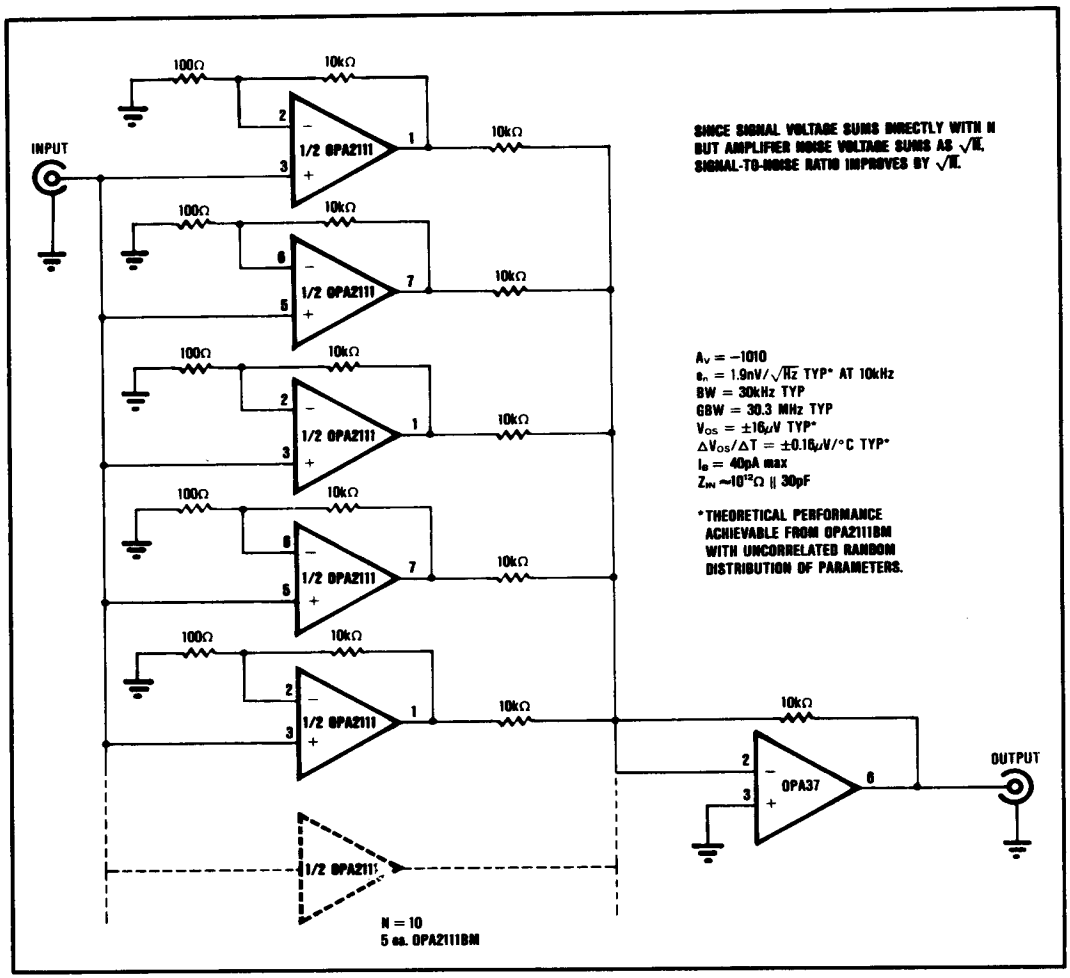


FIGURE 8. 'N' Stage Parallel-Input Amplifier.

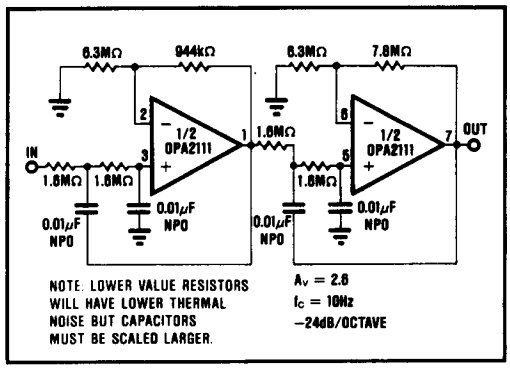


FIGURE 9. 10Hz Fourth-Order Butterworth Low-Pass Filter.

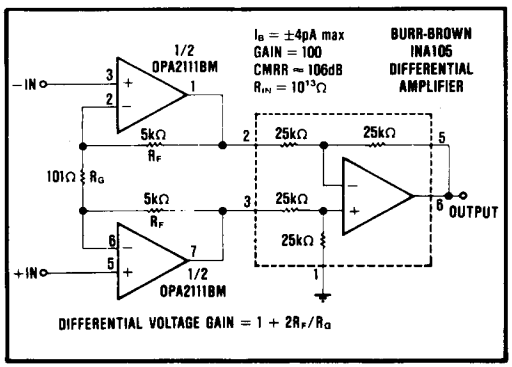


FIGURE 10. FET Input Instrumentation Amplifier.

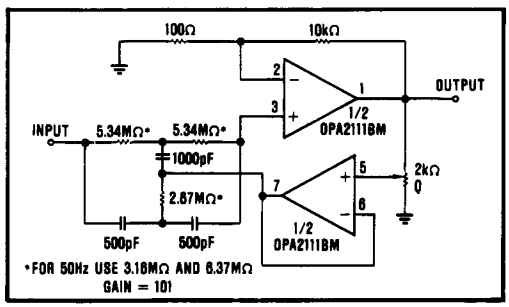


FIGURE 11. High-Impedance 60Hz Reject Filter with Gain.

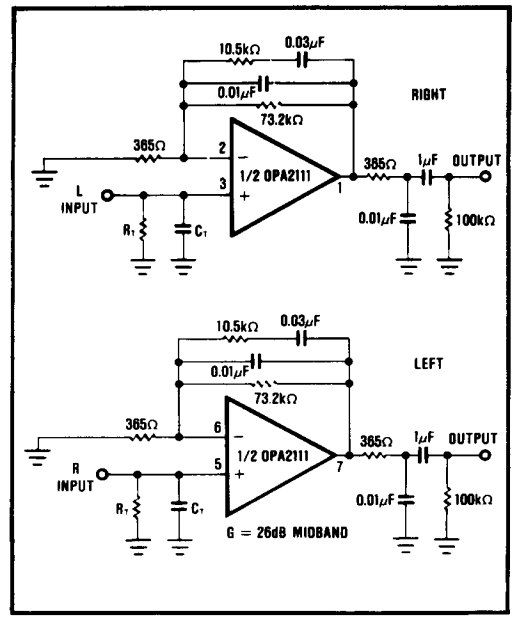


FIGURE 12. RIAA Equalized Stereo Preamplifier.

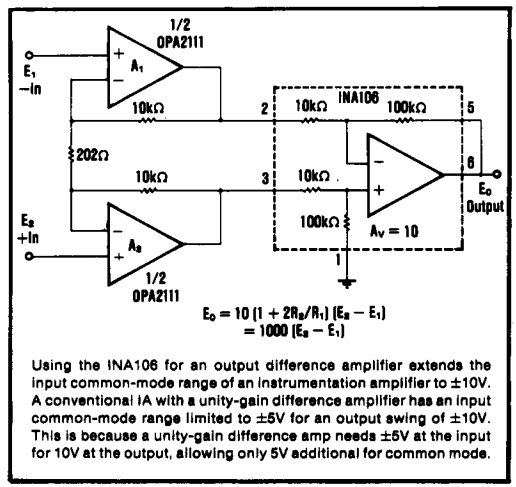


FIGURE 13. Precision Instrumentation Amplifier.