Low-voltage low-power stereo audio CODEC with DSP features

UDA1344TS

FEATURES

General

- Low power consumption
- 3.0 V power supply
- System clock of $256f_s$, $384f_s$ and $512f_s$
- Supports sampling frequencies from 8 to 55 kHz
- Non-inverting ADC plus integrated high-pass filter to cancel DC offset
- ADC supports 2 V (RMS) input signals
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- Integrated digital interpolation filter plus non-inverting DAC
- Functions controllable either via L3 microcontroller interface or via static pins
- UDA1344TS is pin and function compatible with UDA1340M
- Small package size (SSOP28)
- Easy application.

Multiple format input interface

- I^2S-bus, MSB-justified or LSB-justified 16, 18 and 20 bits format compatible
- Three combined data formats with MSB-justified output and LSB-justified 16, 18 and 20 bits input
- $1f_s$ input and output format data rate.

DAC digital sound processing

The sound processing features of the UDA1344TS can be used in the L3 mode only:

- Digital tone control, bass boost and treble
- Digital dB-linear volume control (low microcontroller load) via L3 microcontroller
- Digital de-emphasis for 32, 44.1 and 48 kHz
- Soft mute.

BITSTREAM CONVERSION

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control), no post filter required
- High linearity, dynamic range and low distortion.

GENERAL DESCRIPTION

The UDA1344TS is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1344TS supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB-justified data format with word lengths of 16, 18 and 20 bits. The UDA1344TS also supports three combined data formats with MSB-justified data output and LSB-justified 16, 18 and 20 bits data input.

The UDA1344TS can be controlled either via static pins or via the L3 interface. In the L3 mode the UDA1344TS has special Digital Sound Processing (DSP) features in playback mode such as de-emphasis, volume control, bass boost, treble and soft mute.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1344TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifier supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating	–	9.0	11.0	mA
		ADC power-down	–	3.5	5.0	mA
$I_{DDA(DAC)}$	DAC analog supply current	operating	–	4.0	6.0	mA
		DAC power-down	–	25	75	μA
I_{DDO}	operational amplifier supply current	operating	–	4.0	6.0	mA
		DAC power-down	–	250	350	μA
I_{DDD}	digital supply current	operating	–	6.0	9.0	mA
		DAC power-down	–	2.5	4.0	mA
		ADC power-down	–	3.5	5.0	mA
T_{amb}	ambient temperature		−40	–	+85	°C
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	–	−85	−80	dB
		at −60 dB; A-weighted	–	−35	−30	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	notes 3 and 4	–	900	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	–	−90	−85	dB
		at −60 dB; A-weighted	–	−37	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	69	–	mW
P_{DA}	power consumption in playback mode		–	42	–	mW
P_{AD}	power consumption in record mode		–	37.5	–	mW
P_{PD}	power consumption in power-down mode		–	17	–	mW

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.
2. The input voltage to the ADC is inversely proportional to the supply voltage.
3. The output voltage of the UDA1344TS differs from the output voltage of the UDA1340M.
4. The output of the DAC scales proportionally with the supply voltage.

BLOCK DIAGRAM

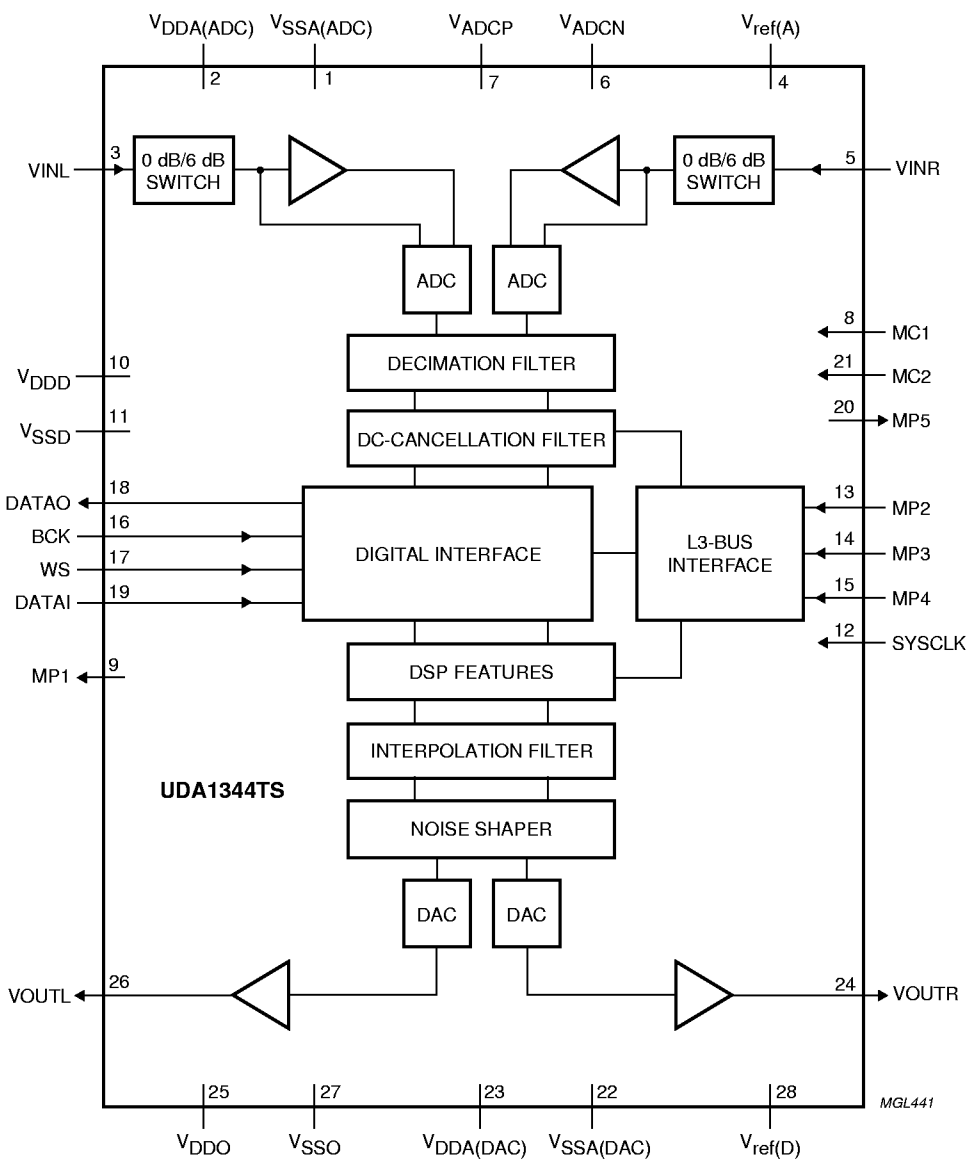


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{SSA(ADC)}$	1	ADC analog ground
$V_{DDA(ADC)}$	2	ADC analog supply voltage
VINL	3	ADC input left
$V_{ref(A)}$	4	ADC reference voltage
VINR	5	ADC input right
V_{ADCN}	6	ADC negative reference voltage
V_{ADCP}	7	ADC positive reference voltage
MC1	8	mode control 1 input (pull-down)
MP1	9	multi purpose pin 1 output
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock input: $256f_s$, $384f_s$ or $512f_s$
MP2	13	multi purpose pin 2 input
MP3	14	multi purpose pin 3 input
MP4	15	multi purpose pin 4 input
BCK	16	bit clock input
WS	17	word select input
DATAO	18	data output
DATAI	19	data input
MP5	20	multi purpose pin 5 output (pull-down)
MC2	21	mode control 2 input (pull-down)
$V_{SSA(DAC)}$	22	DAC analog ground
$V_{DDA(DAC)}$	23	DAC analog supply voltage
VOUTR	24	DAC output right
V_{DDO}	25	operational amplifier supply voltage
VOUTL	26	DAC output left
V_{SSO}	27	operational amplifier ground
$V_{ref(D)}$	28	DAC reference voltage

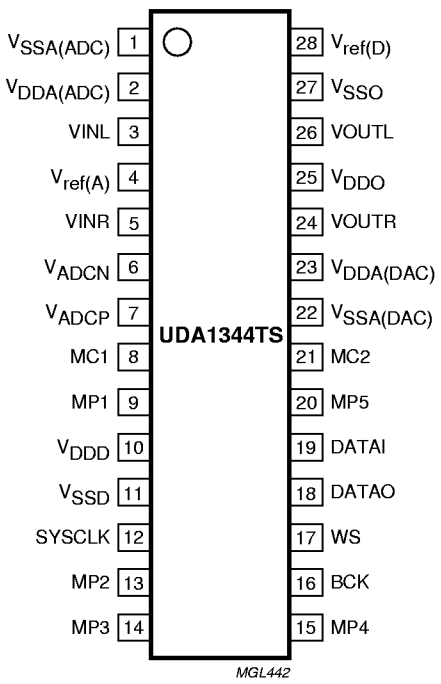


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UDA1344TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system clock must be locked in frequency to the digital interface input signals.

The BCK clock can be up to $128f_s$, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} = < 128 \times f_{WS}$.

Remarks:

1. The WS edge MUST fall on the negative edge of the BCK clock at all times for proper operation of the digital I/O data interface
2. The sampling frequency range is from 5 to 55 kHz
3. For MSB- and LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1344TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The oversampling ratio is 128.

In contrast to the UDA1340M, the UDA1344TS supports 1 V (RMS) input signals and can be set, via an external resistor, to support 2 V (RMS) input signals.

Analog front-end

The analog front-end is equipped with a selectable 0 dB or 6 dB gain block. The pin to select the gain switch is given in Section “L3 mode”. This block can be used in applications in which both 1 V (RMS) and 2 V (RMS) input signals are available.

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be connected in series with the input of the ADC. This makes a voltage divider with the internal ADC resistor and makes sure only 1 V (RMS) maximum is input to the IC. Using this application for a 2 V (RMS) input signal, the gain switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 1.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Decimation filter (ADC)

The decimation from $128f_s$ to $1f_s$ is performed in 2 stages.

The first stage realizes 3rd-order $\frac{\sin x}{x}$ characteristic. This filter decreases the sample rate by 16.

The second stage, a Finite Impulse Response (FIR) filter, consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 Decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	$0 - 0.45f_s$	±0.05
Stop band	$>0.55f_s$	−60
Dynamic range	$0 - 0.45f_s$	108
Overall gain with 0 dB input to the ADC	DC	−1.16

DC-cancellation filter (ADC)

An optional Infinite Impulse-Response (IIR) high-pass filter is provided to remove unwanted DC components. The operation is selected by the microcontroller via the L3 interface. The filter characteristics are given in Table 3.

Table 3 DC-cancellation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	–	none
Pass-band gain	–	0
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	$0 - 0.45f_s$	>110

Mute (ADC)

On recovery from power-down or switching on of the system clock, the serial data output on pin DATAO is held at LOW level until valid data is available from the decimation filter. This time depends on whether the DC-cancellation filter is selected:

- DC cancel off:

  $t = \frac{1024}{f_s}$; t = 23.2 ms at f_s = 44.1 kHz

- DC cancel on:

  $t = \frac{12288}{f_s}$; t = 279 ms at f_s = 44.1 kHz.

Interpolation filter (DAC)

The digital filter interpolates from $1f_s$ to $128f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 4 Interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	−50
Dynamic range	$0 - 0.45f_s$	108
Gain	DC	−3.5

Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

Multiple format input/output interface

The UDA1344TS supports the following data input/output formats:

- I^2S-bus format with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits
- LSB-justified serial format with data word lengths of 16, 18 or 20 bits (in L3 mode only)
- Combined data formats:
  - L3 mode: MSB-justified data output and LSB-justified 16, 18 and 20 bits data input
  - Static pin mode: MSB-justified data output and LSB-justified 16 and 20 bits data input.

The formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed.

Control mode selection

The UDA1344TS can be used under L3 microcontroller interface control or static pin control. The mode can be set via the mode control pins MC1 and MC2 (see Table 5).

Table 5 Mode control pins

PIN MC2	PIN MC1	MODE
LOW	LOW	L3 mode
LOW	HIGH	Test mode
HIGH	LOW	
HIGH	HIGH	Static pin mode

Important: in the L3 mode the UDA1344TS is completely pin and function compatible with the UDA1340M.

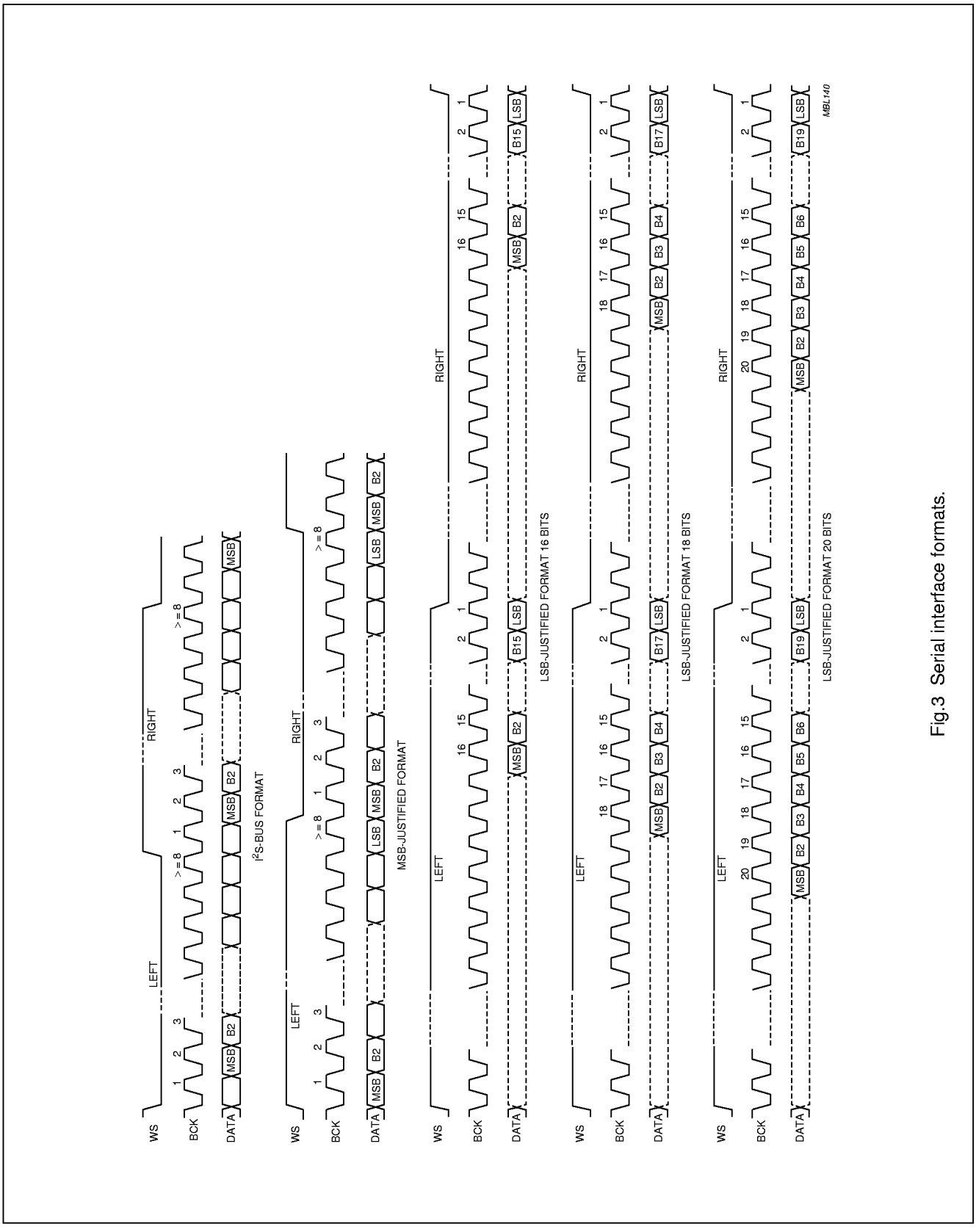


Fig.3 Serial interface formats.

Static pin mode

The UDA1344TS is set to static pin mode by setting both pins MC1 and MC2 to HIGH level.

The controllable features in this mode are:

- System clock frequency selection
- Data input/output format selection
- De-emphasis and mute control
- Power-down and ADC input level selection.

PINNING DEFINITION

The pinning definition in the static pin mode is given in Table 6.

Table 6 Pinning definition in static pin model

PIN	DESCRIPTION
MP1	data input/output setting
MP2	three-level pin to select no de-emphasis, de-emphasis or mute
MP3	$256f_s$ or $384f_s$ system clock selection
MP4	three-level pin to select ADC power-down, ADC input 1 V (RMS) or ADC input 2 V (RMS)
MP5	data input/output setting

SYSTEM CLOCK

In the static pin mode the options are $256f_s$ and $384f_s$ as given in Table 7.

Table 7 System clock selection

PIN MP3	SELECTION
LOW	$256f_s$ clock frequency
HIGH	$384f_s$ clock frequency

MUTE AND DE-EMPHASIS

The level definition of pin MP2 pin is given in Table 8.

Table 8 Levels for pin MP2

PIN MP2	SELECTION
LOW	no de-emphasis and mute
$0.5V_{DDD}$	de-emphasis 44.1 kHz
HIGH	mute

INPUT/OUTPUT DATA FORMAT SELECTION

The input/output data format can be selected using pins MP1 and MP5 as given in Table 9.

Table 9 Data format selection

PIN MP1	PIN MP5	SELECTION
LOW	LOW	input: MSB-justified
LOW	HIGH	input: I^2S-bus
HIGH	LOW	input: LSB-justified 20 bits; output: MSB-justified
HIGH	HIGH	input: LSB-justified 16 bits; output: MSB-justified

ADC INPUT VOLTAGE SELECTION AND POWER-DOWN

In the static pin mode the three-level pin MP4 is used to select 0 or 6 dB gain and power-down.

Table 10 Levels for pin MP4

PIN MP4	SELECTION
LOW	ADC power-down
$0.5V_{DDD}$	6 dB gain
HIGH	0 dB gain

L3 mode

The UDA1344TS is set to the L3 mode by setting both pins MC1 and MC2 to LOW level.

The static pins in this mode are used for:

- ADC output overload detection
- L3 interface signal input
- ADC input voltage selection.

The controllable features via the L3 interface and the definition of the control registers are given in Section “L3 interface”.

PINNING DEFINITION

The pinning definition in the L3 mode is given in Table 11.

Table 11 Pinning definition in L3 mode

PIN	FUNCTION
MP1	ADC output overload detection
MP2	L3MODE input
MP3	L3CLOCK input
MP4	L3DATA input
MP5	ADC input voltage selection: 1 V (RMS) or 2 V (RMS)

ADC OUTPUT OVERLOAD DETECTION

In practice the output is used to indicate whenever the output data, in either the left or right channel, is greater than −1 dB (actual figure is −1.16 dB) of the maximum possible digital swing. When this condition is detected pin MP1 is forced to HIGH level for at least $512f_s$ cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

ADC INPUT VOLTAGE SELECTION

In the L3 mode pin MP5 is used to select 0 or 6 dB gain.

Table 12 Levels for pin MP5

PIN MP4	SELECTION
LOW	0 dB gain
HIGH	6 dB gain

L3 INTERFACE

The UDA1344TS has a microcontroller input mode. In the microcontroller control mode, all the digital sound processing features and the system controlling features can be controlled by the microcontroller. The controllable features are:

- System clock frequency
- Data input format
- Power control
- DC filtering
- De-emphasis
- Volume
- Flat/min./max. switch
- Bass boost
- Treble
- Mute.

The exchange of data and control information between the microcontroller and the UDA1344TS is accomplished through a serial hardware interface comprising the following lines:

L3DATA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is LSB first and is organized in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

The address mode is required to select a device communicating via the L3 interface and to define the destination registers for the data transfer mode. Data transfer for the UDA1344TS can only be in one direction: input to the UDA1344TS to program its sound processing and other functional features.

Address mode

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits.

The fundamental timing is shown in Fig.4.

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1344TS is 000101 (bits 7 to 2).

Data bits 1 and 0 indicate the type of subsequent data transfer as given in Table 13.

Table 13 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	data (volume, bass boost, treble, de-emphasis, mute, mode and power control)
0	1	not used
1	0	status (system clock frequency, data input/output format and DC filter)
1	1	not used

In the event that the UDA1344TS receives a different address, it will deselect its microcontroller interface logic.

Data transfer mode

The selection preformed in the address mode remains active during subsequent data transfers, until the UDA1344TS receives a new address command.

The fundamental timing of data transfers is essentially the same as in the address mode and is shown in Fig.5.

The maximum input clock and data rate is $64f_s$.
All transfers are byte wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1344TS after the eighth bit of a byte has been received.

A multibyte data transfer is illustrated in Fig.6.

Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers.

The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode by bit 1 and bit 0 (see Table 13).

The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6).

The other bits in the data byte (bits 5 to 0) is the value that is placed in the selected registers.

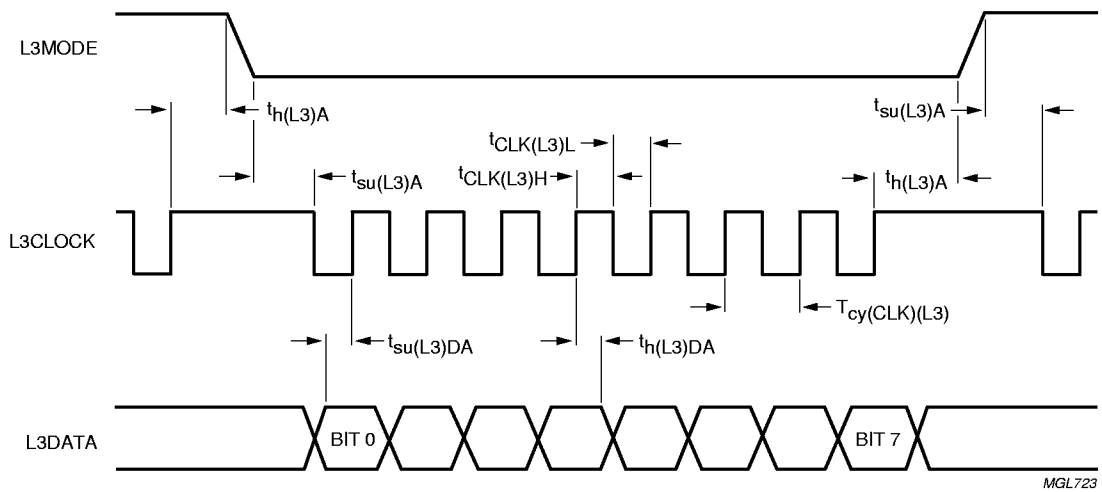


Fig.4 Timing in address mode.

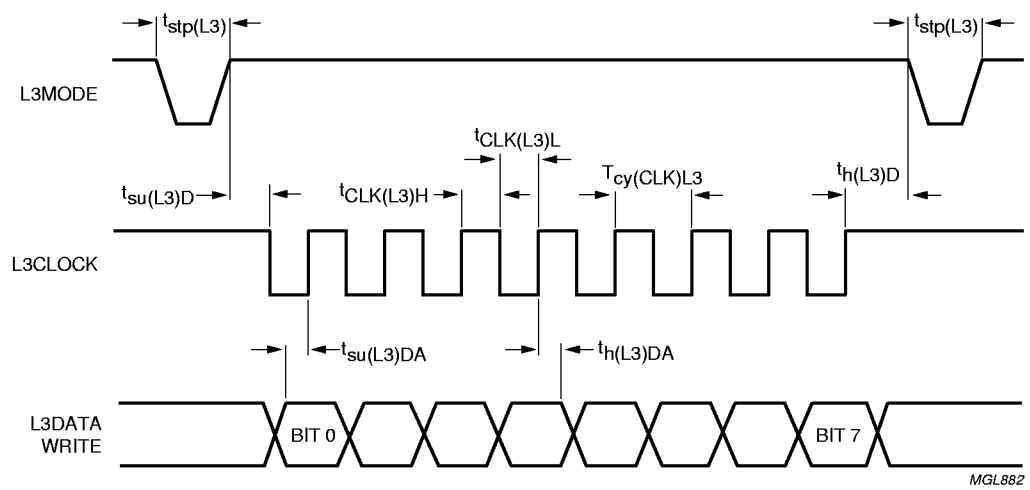


Fig.5 Timing in data transfer mode.

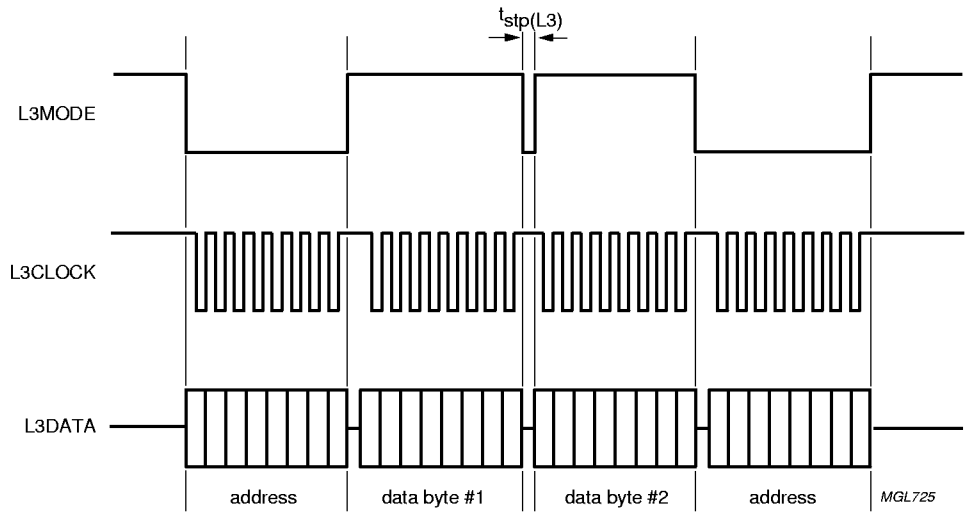


Fig.6 Multibyte data transfer.

L3 interface registers

When the data transfer of type 'status' is selected, the features system clock frequency, data input format and DC filter can be controlled.

Table 14 Data transfer of type 'status'

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	SC1	SC0	IF2	IF1	IF0	DC	SC = system clock frequency (2 bits); see Table 16
								IF = data input format (3 bits); see Table 17
								DC = DC filter (1 bit); see Table 18

When the data transfer of type 'data' is selected, the features volume, bass boost, treble, de-emphasis, mute, mode and power control can be controlled.

Table 15 Data transfer of type 'data'

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	VC = volume control (6 bits); see Table 19
0	1	BB3	BB2	BB1	BB0	TR1	TR0	BB = bass boost (4 bits); see Table 20
								TR = treble (2 bits); see Table 21
1	0	0	DE1	DE0	MT	M1	M0	DE = de-emphasis (2 bits); see Table 22
								MT = mute (1 bit); see Table 23
								M = filter mode (2 bits); see Table 24
1	1	0	0	0	0	PC1	PC0	PC = power control (2 bits); see Table 25

SYSTEM CLOCK FREQUENCY

A 2-bit value to select the used external clock frequency.

Table 16 System clock frequency settings

SC1	SC0	SELECTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

DATA INPUT FORMAT

A 3-bit value to select the used data format.

Table 17 Data format settings

IF2	IF1	IF0	FORMAT
0	0	0	I^2S-bus
0	0	1	LSB-justified 16 bits
0	1	0	LSB-justified 18 bits
0	1	1	LSB-justified 20 bits
1	0	0	MSB-justified
1	0	1	input: LSB-justified 16 bits; output: MSB-justified
1	1	0	input: LSB-justified 18 bits; output: MSB-justified
1	1	1	input: LSB-justified 20 bits; output: MSB-justified

DC FILTER

A 1-bit value to enable the digital DC filter.

Table 18 DC filtering

DC	SELECTION
0	no DC filtering
1	DC filtering

VOLUME CONTROL

A 6-bit value to program the left and right channel volume attenuation. The range is from 0 to −∞ dB in steps of 1 dB.

Table 19 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	−1
0	0	0	0	1	1	−2
:	:	:	:	:	:	:
1	1	1	0	1	1	−58
1	1	1	1	0	0	−59
1	1	1	1	0	1	−60
1	1	1	1	1	0	−∞
1	1	1	1	1	1	−∞

BASS BOOST

A 4-bit value to program the bass boost setting. The used set depends on the mode bits M1 and M0.

Table 20 Bass boost settings

BB3	BB2	BB1	BB0	BASS BOOST SETTING		
				FLAT (dB)	MIN. (dB)	MAX. (dB)
0	0	0	0	0	0	0
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24
1	1	1	1	0	18	24

TREBLE

A 2-bit value to program the treble setting. The used set depends on the mode bits M1 and M0.

Table 21 Treble settings

TR1	TR0	TREBLE SETTING		
		FLAT (dB)	MIN. (dB)	MAX. (dB)
0	0	0	0	0
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

DE-EMPHASIS

A 2-bit value to enable the digital de-emphasis filter.

Table 22 De-emphasis settings

DE1	DE0	SELECTION
0	0	no de-emphasis
0	1	de-emphasis 32 kHz
1	0	de-emphasis 44.1 kHz
1	1	de-emphasis 48 kHz

MUTE

A 1-bit value to enable the digital mute.

Table 23 Mute

MT	SELECTION
0	no muting
1	muting

MODE

A 2-bit value to program the mode of the sound processing filters of bass boost and treble.

Table 24 Flat/min./max. switch

M1	M0	SELECTION
0	0	flat
0	1	min.
1	0	min.
1	1	max.

POWER CONTROL

A 2-bit value to disable the ADC and/or DAC to reduce power consumption.

Table 25 Power control settings

PC1	PC0	SELECTION	
		ADC	DAC
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	note 1	–3000	+3000	V
		note 2	–300	+300	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	90	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; note 1						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifier supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating	–	9.0	11.0	mA
		ADC power-down	–	3.5	5.0	mA
$I_{DDA(DAC)}$	DAC analog supply current	operating	–	4.0	6.0	mA
		DAC power-down	–	25	75	μA
I_{DDO}	operational amplifier supply current	operating	–	4.0	6.0	mA
		DAC power-down	–	250	300	μA
I_{DDD}	digital supply current	operating	–	6.0	9.0	mA
		DAC power-down	–	2.5	4.0	mA
		ADC power-down	–	3.5	5.0	mA
Digital inputs						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs						
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
Three-level inputs: pins MP2 and MP4						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IM}	MIDDLE-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		−0.5	–	$0.1V_{DDD}$	V
Analog-to-digital converter						
$V_{ref(A)}$	reference voltage	referenced to $V_{SSA(ADC)}$	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(refA)}$	output resistance on pin $V_{ref(A)}$		–	24	–	kΩ
R_i	input resistance	f_i = 1 kHz	–	9.8	–	kΩ
C_i	input capacitance		–	20	–	pF
Digital-to-analog converter						
$V_{ref(D)}$	reference voltage	referenced to $V_{SSA(DAC)}$	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(refD)}$	output resistance on pin $V_{ref(D)}$		–	28	–	kΩ
R_o	output resistance of DAC		–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1 %; R_L = 5 kΩ	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	200	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads must be driven, a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
Analog-to-digital converter					
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	1.0	–	V
ΔV_i	unbalance between channels		0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	−85	−80	dB
		at −60 dB; A-weighted	−35	−30	dB
S/N	signal-to-noise ratio	$V_i = 0$ V; A-weighted	95	–	dB
α_{cs}	channel separation		100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple} = 300$ mV (p-p)	30	–	dB
Digital-to-analog converter					
$V_{o(rms)}$	output voltage (RMS value)	notes 3 and 4	900	–	mV
ΔV_o	unbalance between channels		0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	−90	−85	dB
		at −60 dB; A-weighted	−37	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	100	–	dB
α_{cs}	channel separation		100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple} = 300$ mV (p-p)	50	–	dB

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.
2. The input voltage to the ADC is inversely proportional with the supply voltage.
3. The output voltage of the UDA1344TS differs from the output voltage of the UDA1340M.
4. The output of the DAC scales proportionally with the supply voltage.

TIMING

V_{DDD} = V_{DDA} = V_{DDO} = 2.7 to 3.6 V; T_{amb} = −40 to +85 °C; R_L = 5 kΩ; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock input (see Fig.7)						
T_{sys}	system clock cycle time	$f_{sys} = 256f_s$	78	88	262	ns
		$f_{sys} = 384f_s$	52	59	174	ns
		$f_{sys} = 512f_s$	39	44	132	ns
t_{CWH}	system clock HIGH time	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWL}	system clock LOW time	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
Serial interface input/output data (see Fig.8)						
f_{BCK}	bit clock frequency		–	–	$64f_s$	Hz
$T_{cy(BCK)}$	bit clock cycle time	$T_{cy(s)}$ = cycle time of sample frequency	$\frac{T_{cy(s)}}{64}$	–	–	ns
t_{BCKH}	bit clock HIGH time		100	–	–	ns
t_{BCKL}	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(WS)}$	word select set-up time		20	–	–	ns
$t_{h(WS)}$	word select hold time		10	–	–	ns
$t_{su(DATAI)}$	data input set-up time		20	–	–	ns
$t_{h(DATAI)}$	data input hold time		0	–	–	ns
$t_{h(DATAO)}$	data output hold time		0	–	–	ns
$t_{d(DATAO–BCK)}$	data output to bit clock delay	from BCK falling edge	–	–	80	ns
$t_{d(DATAO–WS)}$	data output to word select delay	from WS edge for MSB-justified format	–	–	80	ns
L3 interface input (see Figs 4 and 5)						
$T_{cy(CLK)L3}$	L3CLOCK cycle time		500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time for address mode		190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time for address mode		190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time for data transfer mode		190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time for data transfer mode		190	–	–	ns
$t_{stp(L3)}$	L3MODE stop time		190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time in data transfer and address mode		190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time in data transfer and address mode		30	–	–	ns

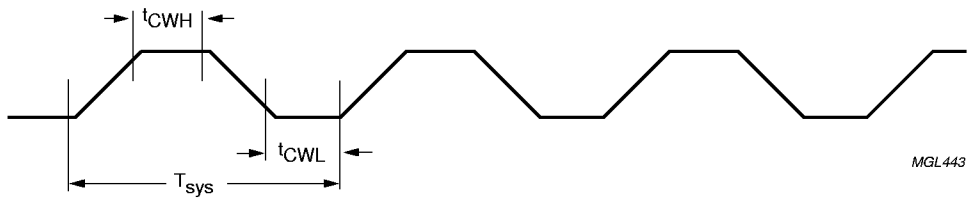


Fig.7 System clock timing.

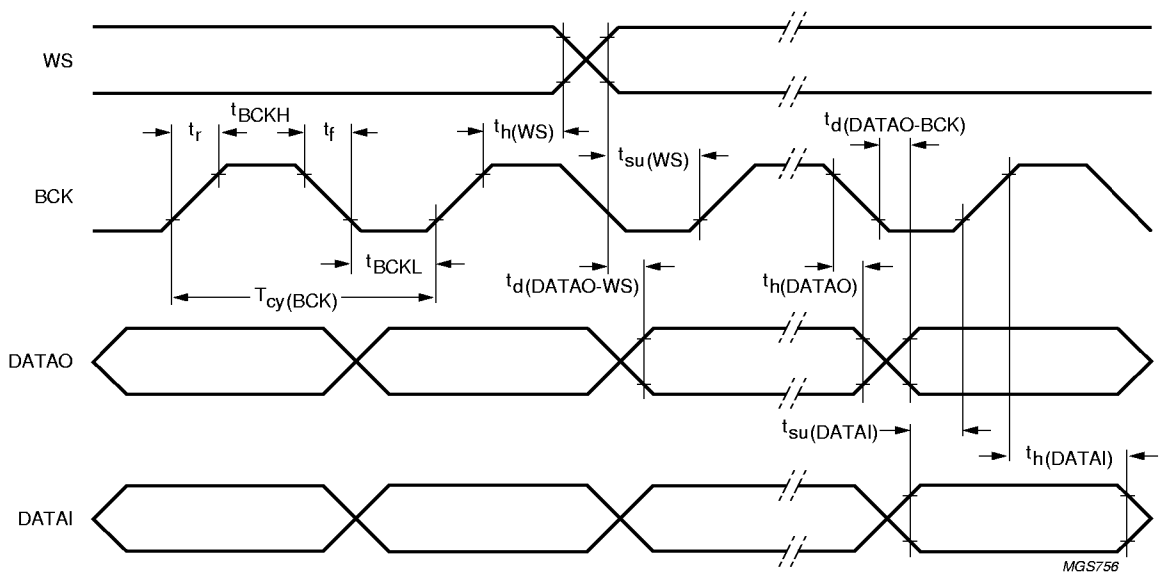


Fig.8 Serial interface timing.

APPLICATION INFORMATION

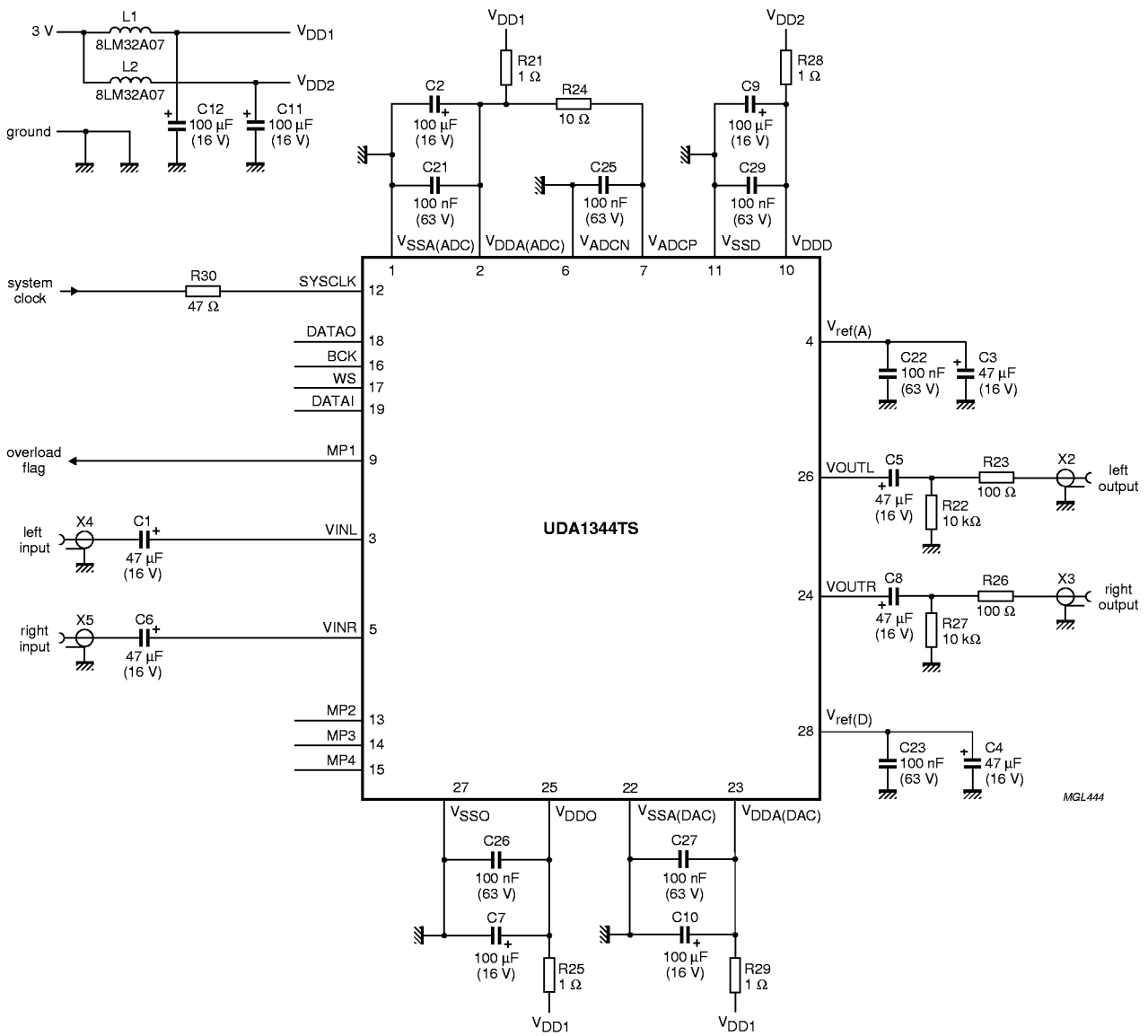
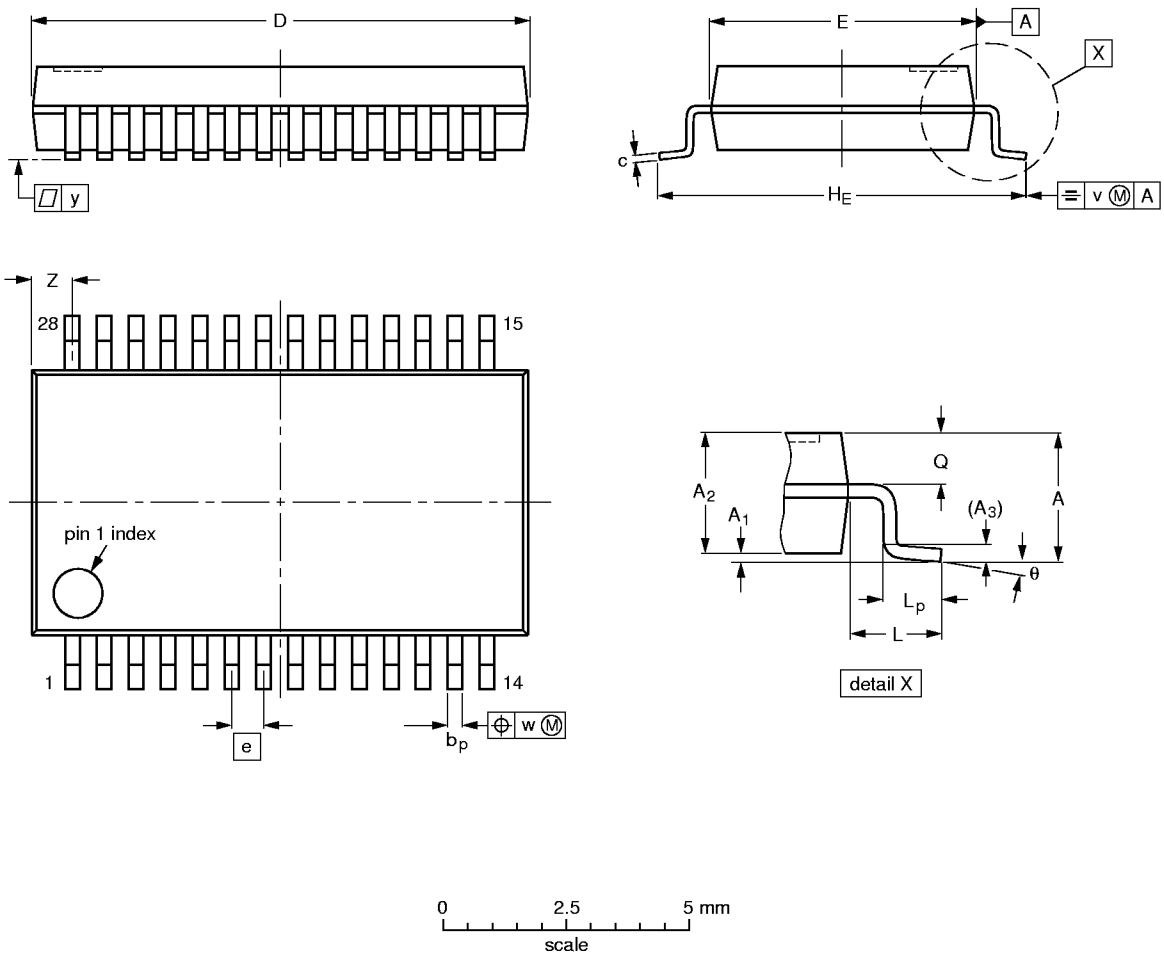


Fig.9 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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