NFC frontend CLRC663 *plus*
push your design further – best performance at lowest power consumption

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NEXT GENERATION HIGH-PERFORMANCE
MULTI-PROTOCOL NFC FRONTEND

SECURE CONNECTIONS
FOR A SMARTER WORLD

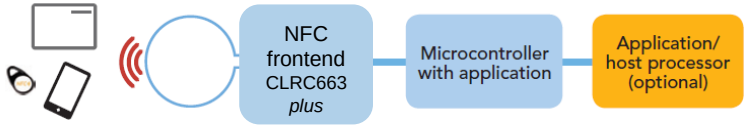
NFC product portfolio

Connected NFC tag solutions

Our connected NFC tag solutions include a NFC Forum RF interface, an EEPROM, and a field-detection function (NTAG F) or a field- detection function with an I²C interface (NTAG I²C *plus*).

NFC frontend solutions

Our standalone frontends, which work seamlessly with the NFC Reader Library, are the most flexible way to add NFC to a system.

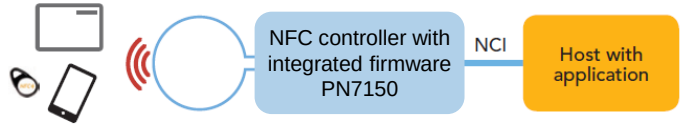


NFC controller solutions

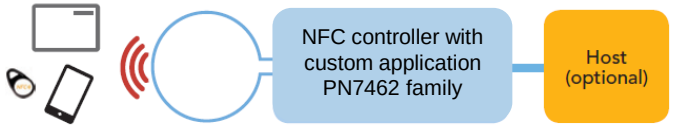
Our NFC controller solutions enable higher integration with fewer components combining an NFC frontend with an advanced 32-bit microcontroller.

Options include integrated firmware, for an easy, standardized interface, or a freely programmable microcontroller with the ability to load fully-custom applications.

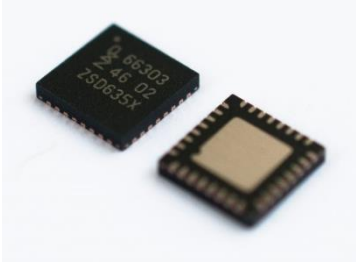
Integrated Firmware



Customizable Firmware



CLRC663 *plus* – push your design further



best performance at lowest power consumption

extended Low Power Card Detection range with new configuration options
low supply voltage for battery support down to 2.5V

design flexibility

max. operating transmitter current of 350mA with limiting value of 500mA
broad temperature range from -40°C to +105°C

backward compatibility

pin-to-pin and software compatible to CLRC663

faster time-to-market

complete support package including EMVCo compliant NFC SW library and NFC Cockpit with VCOM interface and easy antenna configuration

CLRC663 *plus* – product features

Characteristics

- 350mA maximum operating transmitter current with limiting value of 500mA
- Power supply voltage: 2.5 to 5.5V
- Extended operating temperature range: -40 to +105°C
- 512byte FIFO buffer for highest transaction performance
- Flexible and efficient power saving modes including hard power down, standby and low-power card detection
- Integrated PLL provides external system clock from 27.12MHz RF crystal

Licenses and supported standards

- Includes NXP ISO/IEC14443-A, NXP MIFARE® and Innovatron ISO/IEC14443-B licenses
- Crypto 1 intellectual property licensing rights
- Hardware supports for MIFARE Classic encryption
- EMVCo 2.6 L1 analog compliancy on RF level and digital compliancy with NXP NFC reader library

Supported RF protocols

Reader and Writer mode

- ISO/IEC 14443A/MIFARE
- ISO/IEC 14443B
- JIS X 6319-4 (comparable with FeliCa1 scheme)
- ISO/IEC 15693 (ICODE-SLIX, ICODE-DNA)
- ISO/IEC 18000-3 mode 3/ EPC Class-1 HF (ICODE-ILT)

Peer to Peer mode

- Passive-Initiator according to ISO/IEC 14443A (106kbit/s) and FeliCa (212 and 424kbit/s)

Allows to read and write

- All MIFARE® family: Ultralight, Classic 1K & 4K, DESFire EV1 & EV2 and Plus EV1
- All NTAG® family incl. NTAG I²C *plus*
- All SmartMX® family incl. SmartMX2 P40 & P60

Interfaces

- Host interfaces: SPI (10Mbit/s), I²C (1000kbit/s) and UART (1228.8kbit/s)
- SAM interface in X-mode
- Up-to 8 general purpose inputs/outputs

Packages

- HVQFN32
- Wettable flanks

CLRC663 *plus* – target markets

ACCESS CONTROL

- broad temperature range from -40°C to +105°C
- pin-to-pin and software compatible to CLRC663

GAMING

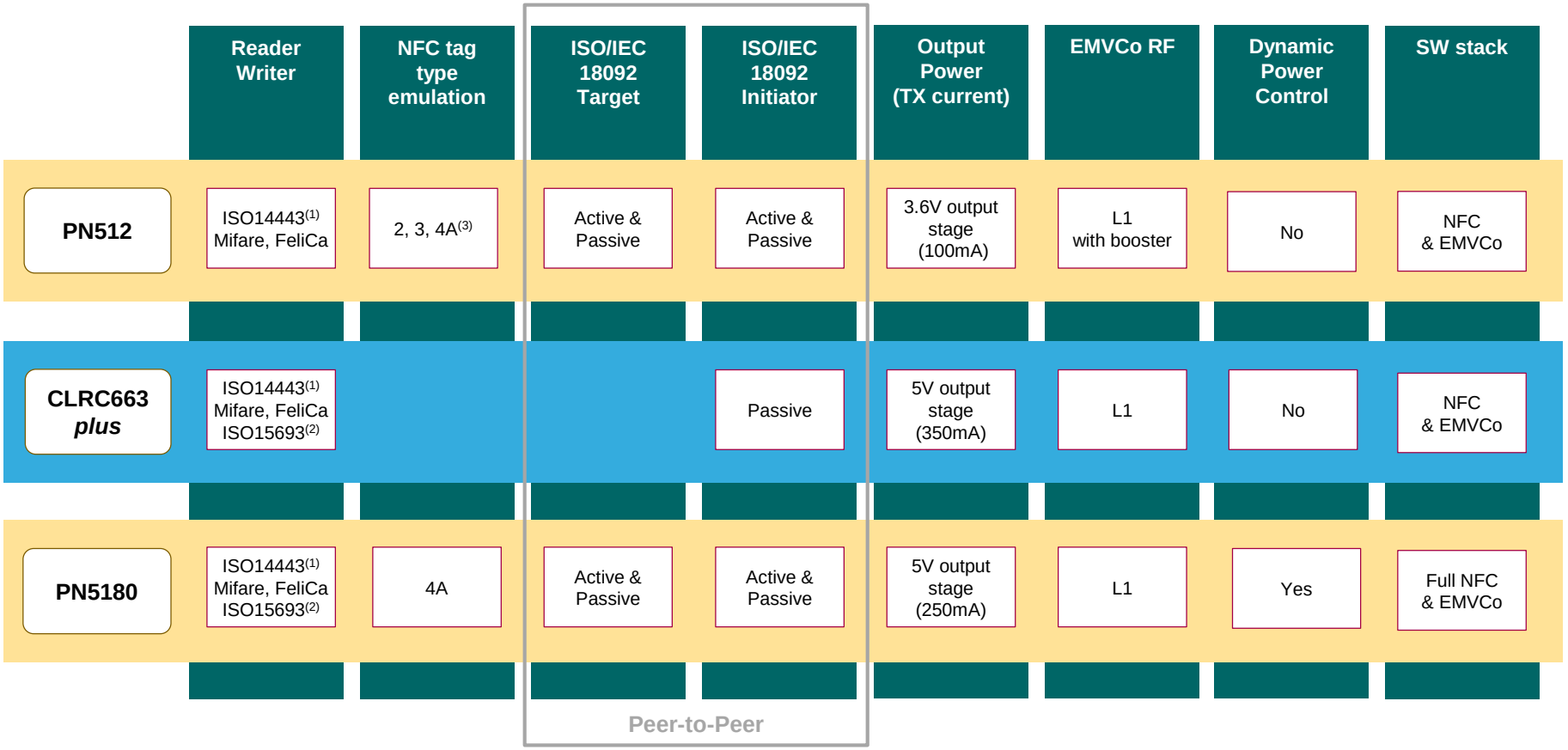
- extended Low Power Card Detection range with new configuration options
- low supply voltage for battery support down to 2.5V

PAYMENT TERMINAL

- highest transmitter current
- EMVCo 2.6 L1 analog and digital compliant

POSITIONING

CLRC663 *plus* vs. other NXP NFC frontends



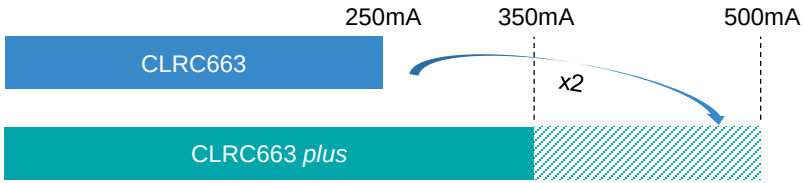
1. ISO/IEC14443
2. ISO/IEC15693
3. No software available for NFC tag type 2 and 3 emulation

CLRC663 *plus* vs. PN5180 and PN7462

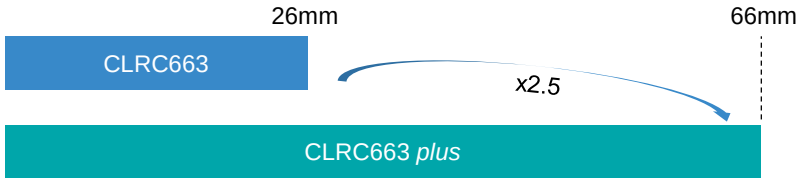
Feature	CLRC663 *plus*	PN5180	PN7462	Comment
Package	HVQFN32	HVQFN40 TFBGA64	HVQFN64	CLRC663 *plus* is pin-to-pin compatible with CLRC663
RF transmitter supply voltage	2.5 to 5.5V	2.7 to 5.5V	3 to 5.5V	CLRC663 *plus* enables better support for battery powered systems
General Purpose Input/Output pins (e.g. to drive LEDs)	4 up-to 8	up-to 7 outputs only	12 up-to 21	PN5180 has up-to 7 general purpose outputs on TFBGA64 package only
Max. operating transmitter current	350mA (lim. 500mA)	250mA with DPC	250mA with DPC	CLRC663 *plus* enables more flexibility in the antenna design
Temperature range	-40 to +105°C	-30 to +85°C	-40 to +85°C	CLRC663 *plus* has an automotive or industrial temperature range
Low power card detection	range: very good power: best	range: best power: good	range: best power: good	CLRC663 *plus* offers the lowest power consumption
Complete set of field proven software libraries	NFC & EMVCo	Full NFC & EMVCo	Full NFC & EMVCo	Full NFC forum certified library; EMVCo 2.6
Waveform Control	Yes	Yes (adaptive)	Yes (adaptive)	Adaptive Waveform Control improves wave shape stability under detuned conditions
Adaptive Range Control	No	Yes	Yes	Adaptive Range Control increases sensibility and robustness under detuned conditions
Freely programmable MCU (flash)	No	No	Cortex M0 (160kB)	PN7462 enables an 1-chip reader solution
Host interfaces	SPI, I²C, UART	SPI	USB, HSUART, SPI, I²C	PN7462 has also two master interfaces (SPI, I²C) and one contact reader interface
SAM Interface	Yes with X-mode	No	Yes	The SAM interface allows to store keys in a secure container

CLRC663 *plus* vs. CLRC663

CLRC663 *plus* vs. CLRC663



Maximum operating transmitter current increases by 40% for CLRC663 *plus* with 2x the limiting value of the CLRC663



CLRC663 *plus* has new configuration options(2) enabling up-to 2.5x the detection range in LPCD(1) mode

CLRC663 *plus* has an automotive or industrial operating temperature range: -40 to +105°C

CLRC663 *plus* enables better support for battery powered systems

1. Low Power Card Detection
2. New LPCD configuration options are Charge Pump (enabled/disabled) and LPCD Filter (enabled/disabled)

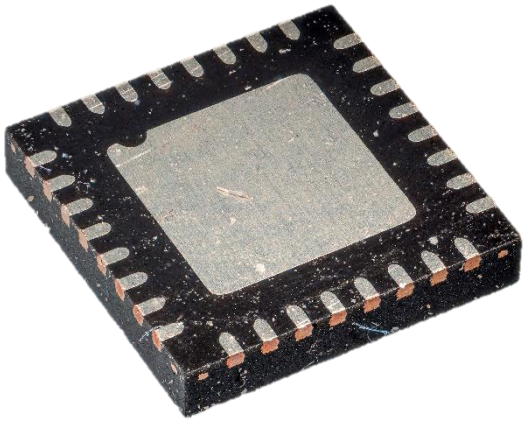
CLRC663 *plus* – LPCD in details

Card type	Standard (CLRC663)	Charge pump enabled	LPCD_FILTER enabled	Charge pump + LPCD_FILTER enabled
MIFARE® Ultralight	11 mm(2)	16 mm	29 mm	25 mm
NTAG	19 mm	24 mm	37 mm	33 mm
MIFARE DESFire® EV2	19 mm	24 mm	39 mm	35 mm
JCOP DIF	12 mm	17 mm	30 mm	27 mm
ISO RefPICC Class 6	4 mm	7 mm	18 mm	23 mm
EMVCo RefPICC	26 mm	29 mm	57 mm	66 mm

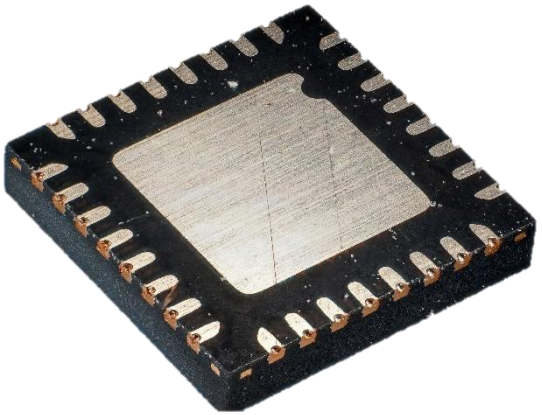
- The basic idea of the LPCD(1) is to provide a function that turns off the RF field when no card is used. This saves energy and allows battery powered NFC Reader designs
- The CLRC663 and CLRC663 *plus* offer a standalone LPCD function, which replaces the normal active card polling that is triggered by the host µController
- CLRC663 *plus* offers additional features to extend the LPCD performance
  - **Charge Pump** increases the RF field strength during the RF-on time
  - **LPCD Filter** reduces the risk of fail detections especially in case of spike noise

1. Low Power Card Detection
2. All detection ranges measured using the standard CLRC663 *plus* development board (CLEV6630B) operated with external power supply at room temperature

CLRC663 *plus* – wettable flank package



CLRC663

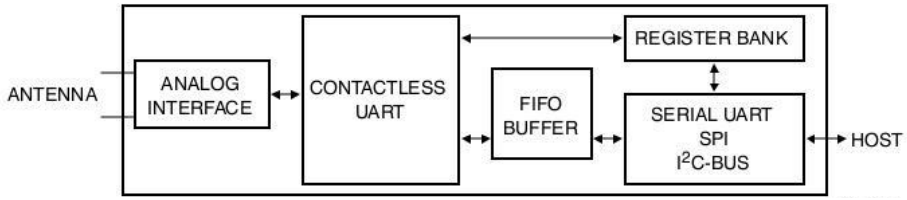


CLRC663 *plus*

- In the case of standard HVQFN packages (e.g. CLRC663 family), there is no exposed pin to visually determine whether or not the package is successfully soldered onto the PCB. The package edge has exposed copper for the terminals, these are prone to oxidation, making sidewall solder wetting difficult
- The CLRC663 *plus,* with wettable flank HVQFN package, enables 100% automatic visual inspection post-assembly ensuring higher quality of assembly

TECHNICAL OVERVIEW

CLRC663 *plus* – quick references

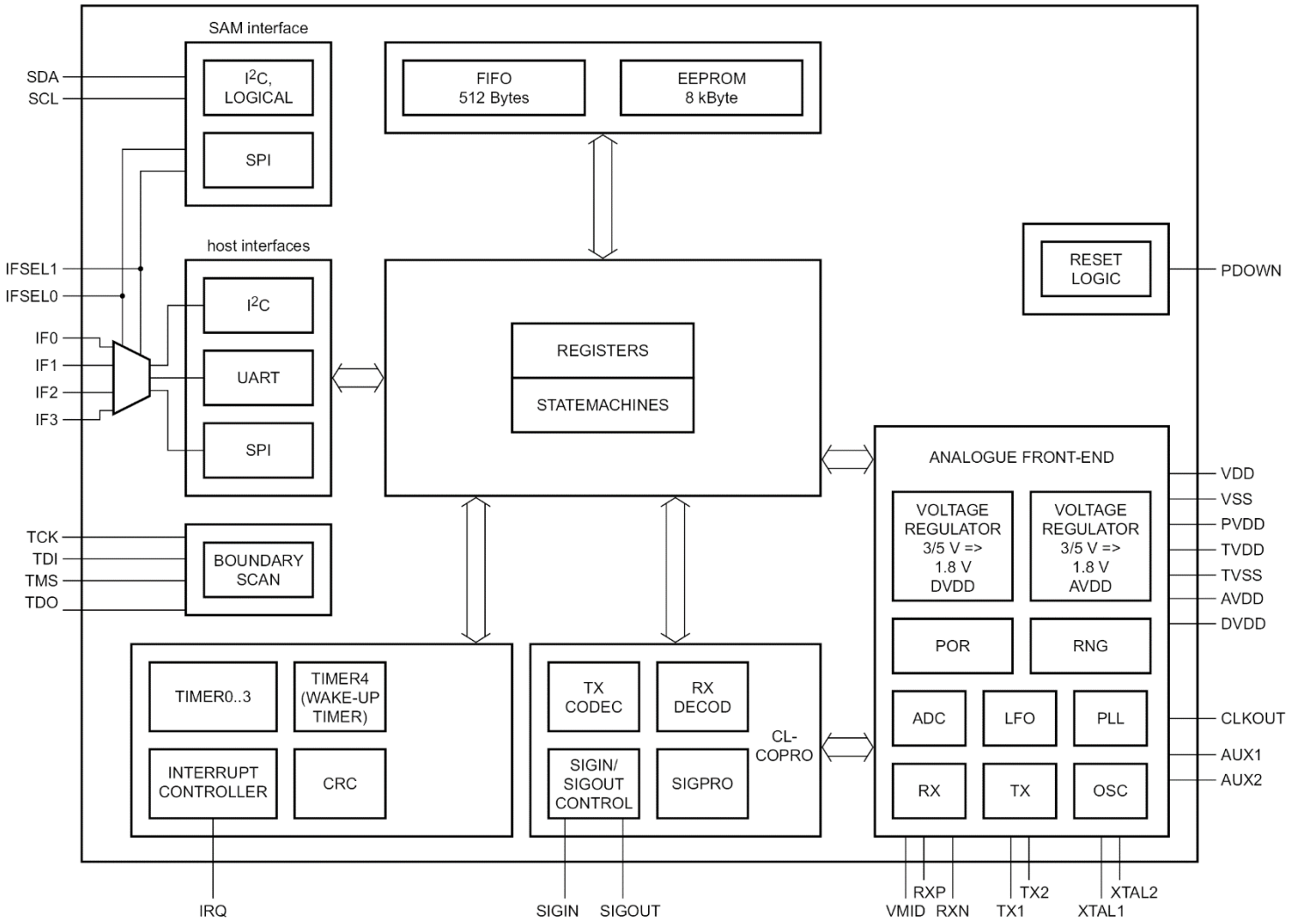


- The **analog interface** handles the modulation and demodulation of the antenna signals for the contactless interface.
- The **contactless UART** manages the protocol dependency of the contactless interface settings managed by the host
- The **FIFO buffer** ensures fast and convenient data transfer between host and the contactless UART
- The **register bank** contains the settings for the analog and digital functionality

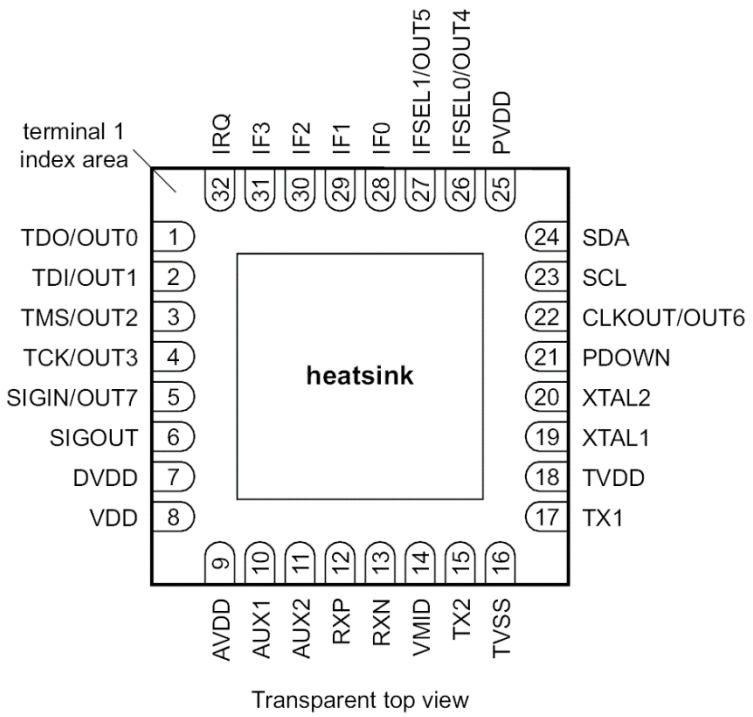
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.5	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	[1]	2.5	5.0	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage		2.5	5.0	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH [2]	-	8	40	nA
I_{DD}	supply current		-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current	transmitter permanent active	-	180	350	mA
		short term transmitter current	-	-	500	mA
T_{amb}	ambient temperature	device mounted on PCB which allows sufficient heat dissipation	–40	+25	+105	°C
T_{stg}	storage temperature	no supply voltage applied	–55	+25	+150	°C

[1] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DD}
[2] I_{pd} is the sum of all supply currents

CLRC663 *plus* – block diagram



CLRC663 *plus* – pinning



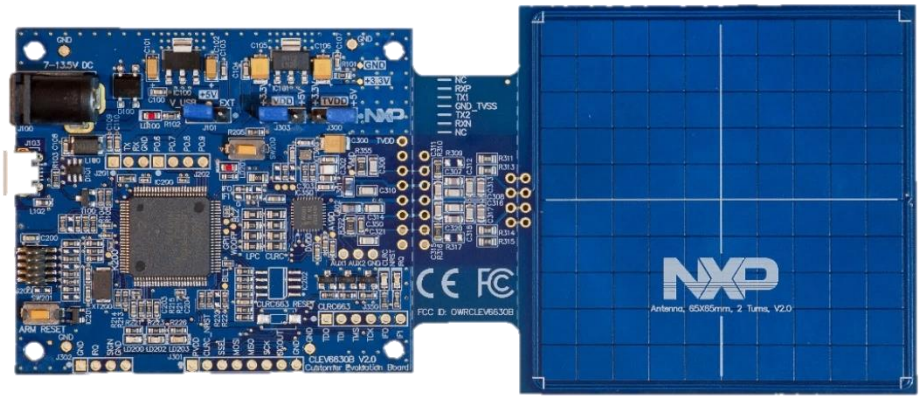
Transparent top view

Pin	Symbol	Type	Description
1	TDO / OUT0	O	test data output for boundary scan interface / general purpose output 0
2	TDI / OUT1	I	test data input boundary scan interface / general purpose output 1
3	TMS / OUT2	I	test mode select boundary scan interface / general purpose output 2
4	TCK / OUT3	I	test clock boundary scan interface / general purpose output 3
5	SIGIN /OUT7	I	Contactless communication interface output. / general purpose output 7
6	SIGOUT	O	Contactless communication interface input.
7	DVDD	PWR	digital power supply buffer [1]
8	VDD	PWR	power supply
9	AVDD	PWR	analog power supply buffer [1]
10	AUX1	O	auxiliary outputs: Pin is used for analog test signal
11	AUX2	O	auxiliary outputs: Pin is used for analog test signal
12	RXP	I	receiver input pin for the received RF signal.
13	RXN	I	receiver input pin for the received RF signal.
14	VMID	PWR	internal receiver reference voltage [1]
15	TX2	O	transmitter 2: delivers the modulated 13.56 MHz carrier
16	TVSS	PWR	transmitter ground, supplies the output stage of TX1, TX2
17	TX1	O	transmitter 1: delivers the modulated 13.56 MHz carrier
18	TVDD	PWR	transmitter voltage supply
19	XTAL1	I	crystal oscillator input: Input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz)
20	XTAL2	O	crystal oscillator output: output of the inverting amplifier of the oscillator
21	PDOWN	I	Power Down (RESET)
22	CLKOUT / OUT6	O	clock output / general purpose output 6
23	SCL	O	Serial Clock line
24	SDA	I/O	Serial Data Line
25	PVDD	PWR	pad power supply
26	IFSEL0 / OUT4	I	host interface selection 0 / general purpose output 4
27	IFSEL1 / OUT5	I	host interface selection 1 / general purpose output 5
28	IF0	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
29	IF1	I/O	interface pin, multifunction pin: Can be assigned to host interface SPI, I^2C, I^2C-L
30	IF2	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
31	IF3	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
32	IRQ	O	interrupt request: output to signal an interrupt event
33	VSS	PWR	ground and heat sink connection

[1] This pin is used for connection of a buffer capacitor. Connection of a supply voltage might damage the device.

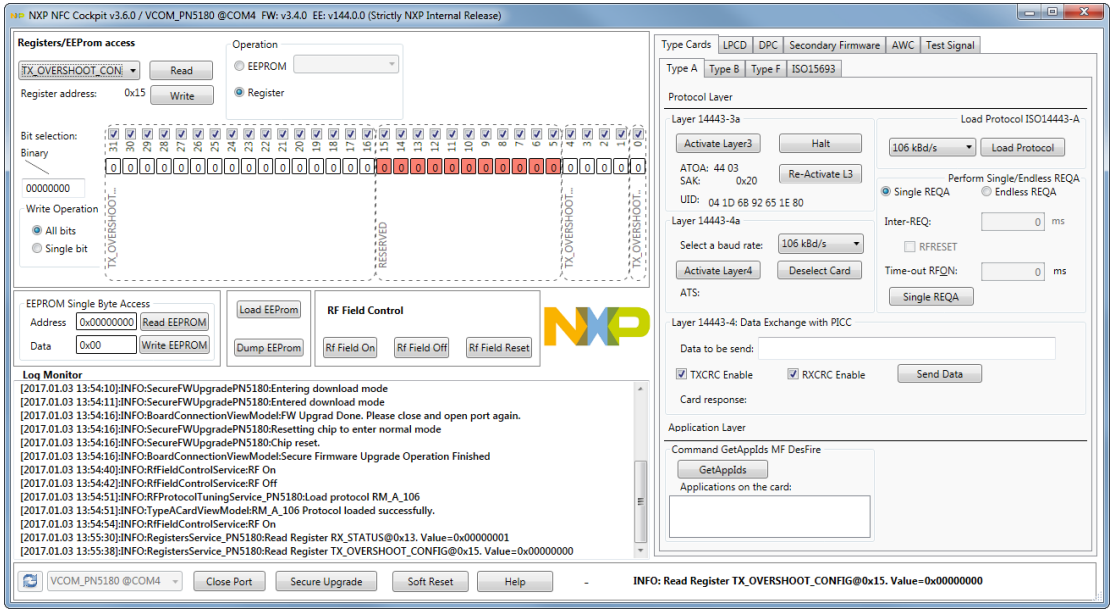
PRODUCT SUPPORT PACKAGE

CLRC663 *plus* – development kit and board



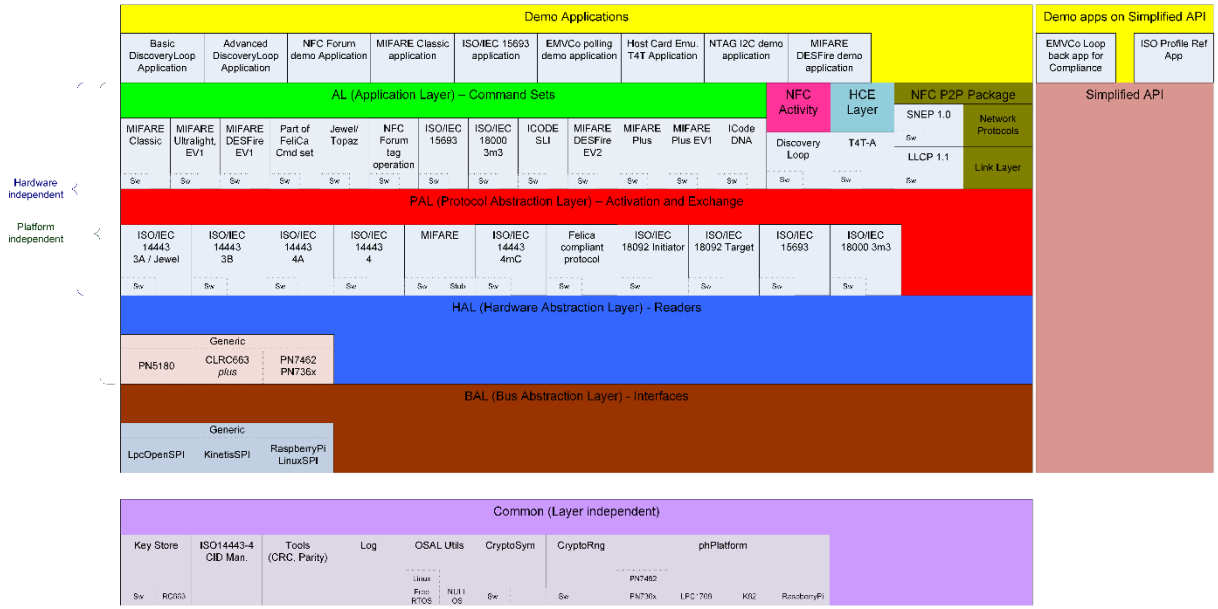
- The **OM26630FDK** is a flexible and easy to use frontend development kit for CLRC663 *plus*
- It contains a **CLEV6630B** board fully supported by the **NFC Cockpit** and the **NFC Reader Library** with a 65*65mm² antenna optimized for EMVCo applications and a 30*50mm² antenna with matching components optimized for Access Management applications
- It also includes, 3 small antenna matching PCBs for implementation of custom antenna matching circuit, NFC sample cards based on NTAG216F (NFC Forum type 2 tag) and DESFire® EV2, and 10 CLRC663 *plus* samples in HVQFN package

CLRC663 *plus* – NFC Cockpit



- **NFC Cockpit** is an intuitive GUI that lets you configure and adapt CLRC663 *plus* settings without writing a single line of software code
- This Windows tool features
  - direct register/EEPROM read/write access and backup of EEPROM settings
  - RF field control and card operation (Type A, Type B, Type F, ISO15693)
  - control of test applications like EMVCo Loopback and test signal configuration
  - LPCD configuration

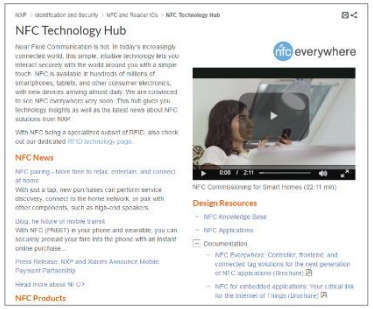
CLRC663 *plus* – NFC Reader library



- **Scalability** – enable only required components and protocol implementations
- **Optimum performance** – built-in MCU support, interrupt-based event handling, free RTOS support and compilers that produce highly compact and efficient code
- **Faster development** – save time and effort by using the APIs and the rich set of sample applications for most common functions
- **Simpler certification** – get ready for certification with test applications for EMVCO L1, NFC Forum and ISO/IEC10373-6 PICC/PCD

Find your NFC toolkit at www.nxp.com

NFC use cases

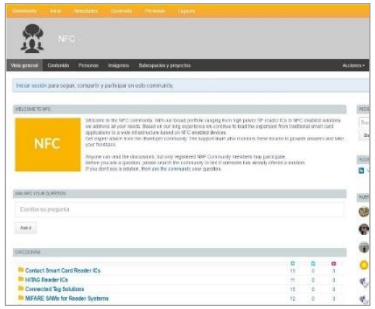


Use cases & products

@ NFC Everywhere

www.nxp.com/NFC

NFC community

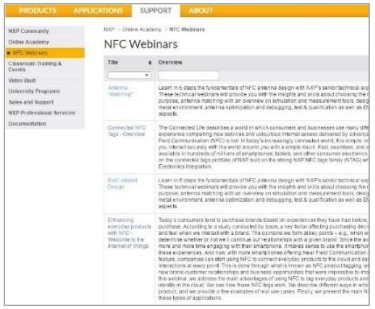


Online community & technical support

Support → NXP community → NFC

NXP community NFC

NFC training

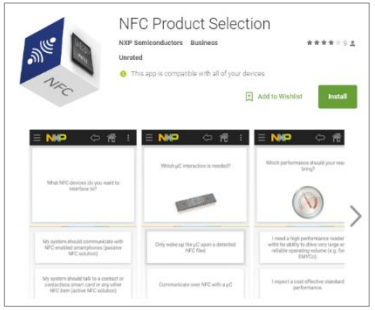


Recorded Webinars

Support → online academy → NFC webinars

NFC webinars

NFC product selection guide



NFC product selection guide app available

Google Play

App Store

CLRC663 *plus* – best performance at lowest power consumption

- Max. operating transmitter current: 350mA (lim. 500mA)
- Enhanced LPCD performance and options
- Broad temperature range from -40°C to +105°C
- Low supply voltage for battery support down to 2.5V

Item	12NC	Comment
CLRC66303HN, 551	9353 062 08551	CLRC663 *plus* on single tray
CLRC66303HN, 518	9353 062 08518	CLRC663 *plus* on reel
OM26630FDK	9353 391 51699	CLRC663 *plus* frontend development kit containing a CLEV6630B development board and - an 30*50mm² antenna with matching components and 3 PCBs for individual antenna matching - NTAG216F and MIFARE DESFire EV2 sample cards and 10 CLRC663 *plus* samples
CLEV6630B	9353 391 49699	CLRC663 *plus* frontend development board with 65*65mm² antenna

www.nxp.com/products/:CLRC66303HN

www.nxp.com/products/:OM26630FDK

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