TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9321F

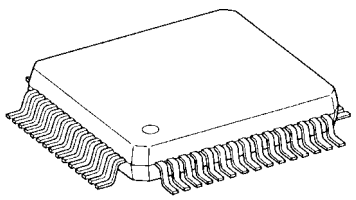
Single Chip DTS Microcontroller (DTS-10)

The TC9321F is a 4 bit CMOS microcontroller for single chip digital tuning system with built-in prescaler, PLL.

The CPU has 4 bit parallel addition/subtraction (AI, SI instructions, etc.) logical operation (OR, AN instructions, etc.) multiple bits judgment, comparison instructions (TM, SL instructions, etc.) and time base functions.

The TC9321F is housed in as pin 60 mini-flat package and is provided with ample I/O ports and exclusive key input ports which are controlled by powerful I/O instructions (IO, KEY instruction, etc.) and output ports.

In addition, the TC9321F has built-in 2 modulus prescaler, PLL circuit, and IF counter that counts intermediate frequency (IF) in FM and AM bands for detecting broadcasting stations.



QFP60-P-1414-0.80D

Weight: 1.10 g (typ.)

Furthermore, the TC9321F has built in serial bus control function (SIO instruction) to powerfully control peripheral ICs, 6 bit A/D converter and D/A converter that are usable for field strength measurement and electronic volume control, and provides with many functions needed for digital tuning system.

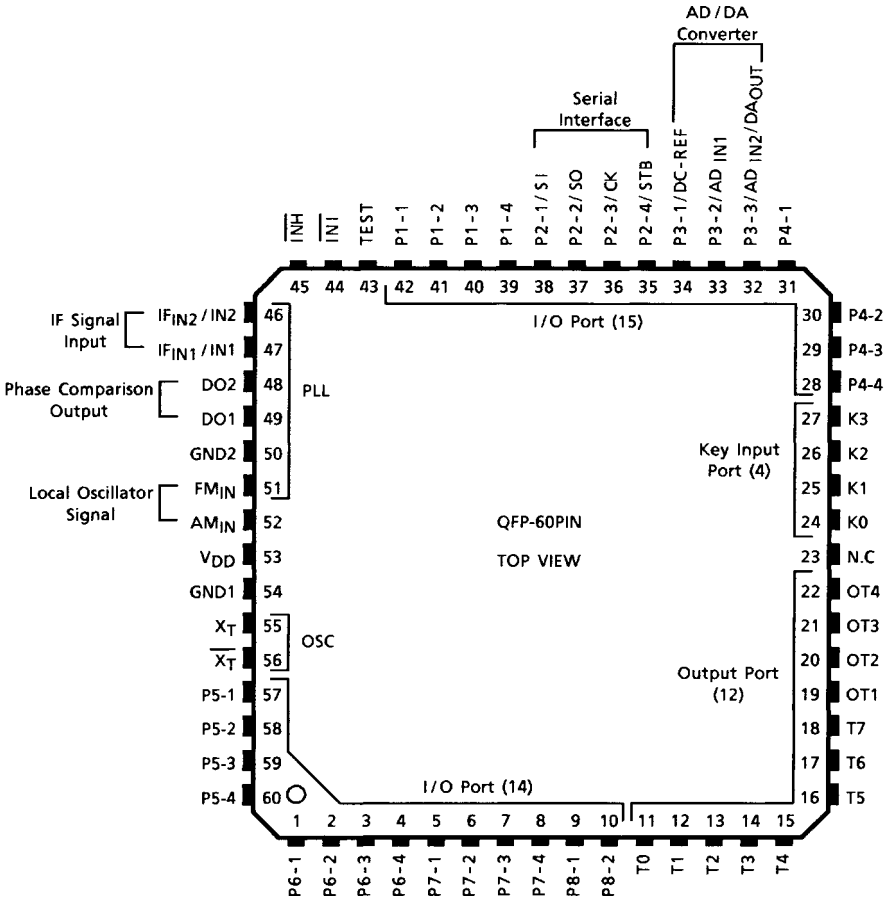
Features

- 4 bit microcontroller single chip digital tuning system.
- 5 V ± 10% single power supply, CMOS structure for low power dissipation.
- Built-in prescaler (max 140 MHz signal is directly input in FM band), PLL.
- Easy back up of data memory (RAM) and various ports (by the $\overline{INH}$ terminal).
- Program memory (ROM): 16 bits × 3968 steps
- Data memory (RAM): 4 bits × 256 words
- 61 kinds of powerful instructions sets (all single word instructions).
- Instruction execution time 11.1 μs (7.2 MHz crystal connection).
- Abundant add and subtract instructions (add instruction: 12, subtract instruction: 12)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF instructions, etc.)
- Data transfer at the same row address is possible.
- Register indirect transfer is possible (MVGD, MVGS instructions)
- Powerful 16 general registers (arranged in RAM)
- Stack level: 2 levels
- Program memory (ROM) has no conception of page and field, and JUMP and CAL instructions can be freely contained in 3968 steps.

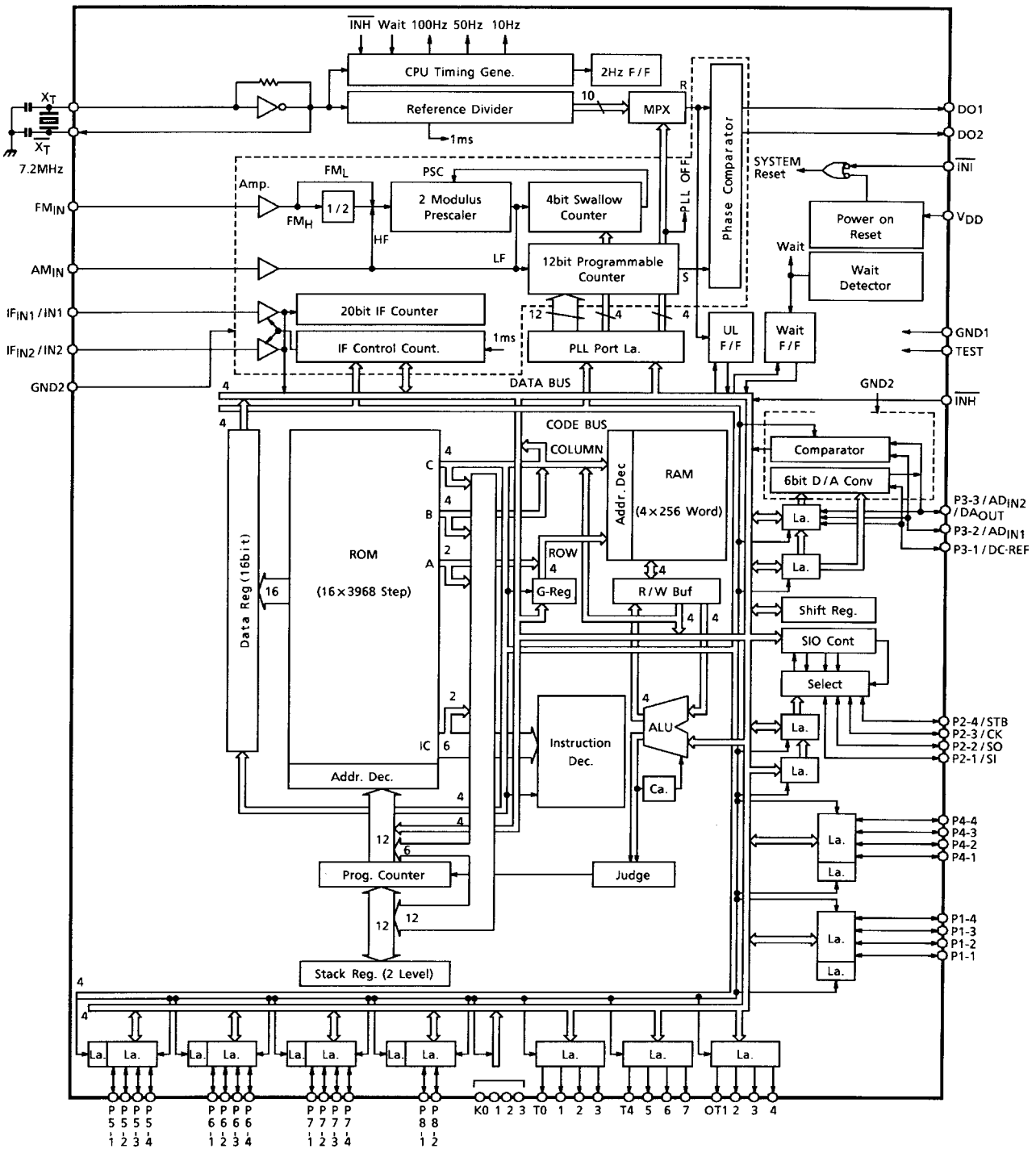
  Further, contents of 16 bits data at any address in 1024 steps can be freely referred (DAL instruction)
- Built-in 20 bit general-use IF counter (IF_{IN1}, IF_{IN2})
- Independent frequency input terminals for FM and AM (FM_{IN}, AM_{IN}), 2 phase comparator outputs (DO1, DO2)
- 10 reference frequencies are programmable selectable (1, 3.125, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz)
- Pulse swallow system and direct frequency division system are selectable by program according to receiving frequency band.
- IF correction at FM band is possible (internal port for IF offset)
- Built-in powerful serial bus control function (I/O port-2 terminals are programmatically selectable.)
- Powerful I/O instructions (IO, KEY, SIO instruction, etc.)
- Exclusive key input port (K0~K3)
- IF counter inputs (IF_{IN1}, IF_{IN2}) and input ports (IN1, IN2) are programmatically selectable.
- Provides a total of up to 44 I/O ports (29 I/O configurable ports, 12 output ports, up to 7 input ports)

- Clock stop is possible programmatically (at CKSP instruction: supply current below 10 μA)
- Built-in 2 Hz timer F/F, 10/100 Hz internal pulse output (internal port for time base)
- Locked state of PLL is detectable (internal port for PLL lock detection)
- Built-in 6 bit A/D and D/A converters (selectable by selecting I/O port-3 terminals (P3-1~P3-3) programmatically).
- OTP product: TC93P21F

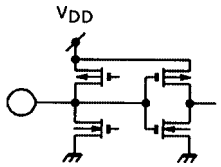
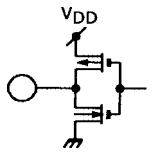
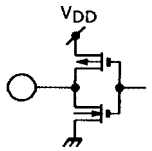
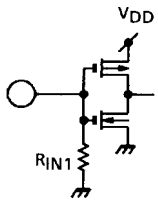
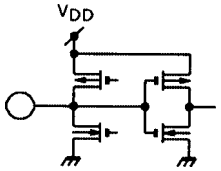
Pin Assignment (top view)

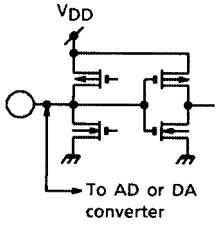
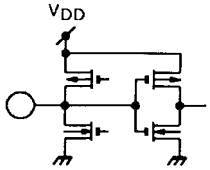
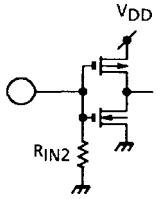


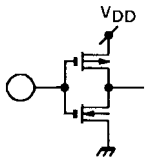
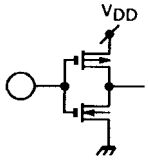
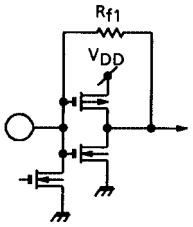
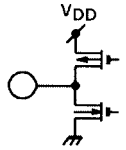
Block Diagram

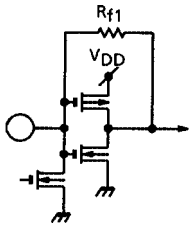
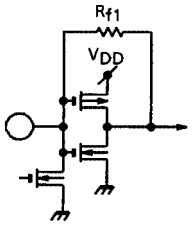


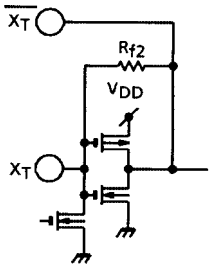
Pin Function

Pin No.	Symbol	Pin Name	Function/Operation	Remarks
57~60 1~4 5~8 9~10	P5-1~P5-4 P6-1~P6-4 P7-1~P7-4 P8-1~P8-2	I/O Port 5 I/O Port 6 I/O Port 7 I/O Port 8	4 bit × 3 (P5-1~P7-3) and 2 bit (P8-1~P8-2) I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal ports called PORT-5~PORT-8 I/O CONTROL. (refer Notes 1, 2 and 3.)	
11~18	T0~T7	Key Timing Output Port	4 bit (T0~T3) and 4 bit (T4~T7) output terminals. These ports are normally used for key return timing signal output of key matrix. (refer to Notes 2 and 3.)	
19~22	OT1~OT4	General-Purpose Output Port	4 bit output ports. (refer to Notes 2 and 3.)	
23	N.C	No Connection	As this terminal is not connected to internal chip, it can be left open or connected to GND or V_{DD} freely. In case of OTP product TC93P21F, this terminal serves as V_{p-p} terminal and TC93P21F is readily usable when connected to V_{DD}.	—
24~27	K0~K3	Key Input Port	4 bit input ports for key matrix input. When KEY instruction these ports specified in the operand is executed, data of these terminals are read in RAM. All terminals have built-in pull-down resistors. Further, the output ports T0~T7 are normally used for key return timing signal.	
28~31 39~42	P4-4~P4-1 P1-4~P1-1	I/O Port 4 I/O Port 1	4 bit (P4-1~P4-4) and 4 bit (P1-1~P1-4) I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal ports called PORT-4~PORT-1 I/O CONTROL. (refer Notes 1, 2 and 3.)	

Pin No.	Symbol	Pin Name	Function/Operation	Remarks
32 33 34	P3-3 /AD_{IN2} /DA_{OUT} P3-2 /AD_{IN1} P3-1 /DC-REF	I/O Port 3 /AD Analog Voltage Input /DA Analog Voltage Output /AD Analog Voltage Input /Reference Voltage Input	3 bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-3 I/O CONTROL. Further, these terminals also serve for the analog input of the built-in 2-channel A/D converter and analog output of 1-channel D/A converter. A/D and D/A converter input/output selection is controlled according to contents of AD_{ON}, DA_{ON}, AD_{SEL} bit. The built-in A/D converter is of programmably sequential comparison type, and P3-1 is the reference voltage input, P3-2 is the analog comparison voltage input, and P3-3 is the analog comparison voltage input or analog voltage output. Note: A ladder resistance that generates internal D/A reference voltage is used commonly by the A/D and D/A converters. When both the A/D and D/A converters are used simultaneously, DA_{ON} bit is set to "0" and D/A output is made to high impedance at time of A/D conversion. It is therefore necessary to hold potential with a capacitor, etc. (refer to Notes 1, 2 and 3.)	
35~38	P2-4/STB P2-3/CK P2-2/SO P2-1/SI	I/O Port 2 /Strobe Pulse Output /Serial Clock Output /Serial Data Output /Serial Data Input	4 bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-2 I/O CONTROL. Further, these terminals are also used as the serial interface (SIO). Selection of SIO is controlled according to contents of SIO ON bit and in case of these serial interface, peripheral optional ICs can be controlled by executing SIO command. Serial transfer in $\overline{NCD}$/NCD mode is programmably selectable. When selectable NCD mode, P2-4/STB and P2-1/SI pins are used as P2-4, P2-1 I/O port. (refer to Notes 1, 2 and 3.)	
43	TEST	Test Mode Control Input	Test mode control input terminal. The device is put in the test mode when "H" level signal is input and becomes the normal operating state when "L" level signal is input or in NC state. (a pull-down resistor has been built-in.)	

Pin No.	Symbol	Pin Name	Function/Operation	Remarks
44	$\overline{INI}$	Initialize Input	Device system reset signal input terminal. As long as the $\overline{INI}$ terminal is kept at "L" level, a system is kept in the reset state and when it becomes "H" level, a program starts from address 0. Normally, the system is reset when 0~3.5 V is supplied to the V_{DD} terminal (power ON reset) and therefore, this terminal is used by fixing at "H" level. Note: After the system reset, I/O ports are set in the input mode. However, the output state of output ports is indefinite and it is necessary to initialize them by program.	
45	$\overline{INH}$	Inhibit Input Terminal	This is the $\overline{INH}$ port input terminal. Normally, this terminal is used for radio mode selecting signal input or battery detection signal input. When CKSTP instruction is used in a program and this CKSTP instruction is executed while the $\overline{INH}$ terminal is at "L" level, it is possible to stop the internal clock generator and CPU operation and put a system in the memory backup state with low current consumption (below 10 μA). Note: CKSTP instruction is effective when the $\overline{INH}$ terminal is at "L" level and when this instruction is executed at "H" level, the same operation as NOOP instruction results. Note: In the radio OFF mode or back-up mode, it is necessary to set reference internal ports (4 bits) at all "1" (PLL OFF mode).	
46 47	IF_{IN2}/IN2 IF_{IN1}/IN1	IF Signal Input 2 /Input port 2 IF Signal Input 1 /Input port 1	IF signal input terminal of IF counter that detects auto stop by counting IF signal in FM and AM bands. Input frequency range is 0.1~20 MHz (0.3 V_{p-p} min) Having a built-in input amplifier, operates at small amplitude in C-connection. These terminals are usable programmably as input ports, and are selectable according to contents of the IN CONTROL Port. Note: When IF counter is used, reference internal ports (4 bits) are set at all "1" or inputs that are not selected by IF_{IN1} bit (input selecting bit) are pulled down. (refer to Note 1)	
48 49	DO2 DO1	Phase Comparator Output	PLL phase comparator output terminal Tri-state output. If devided output signal from the programmable counter is higher than reference frequency, "H" level signal is output and if it is lower, "L" level signal is output and if matched, it becomes high impedance. Signals from DO1 and DO2 are parallelly output.	
50	GND2	Analog GND Terminal	GND terminal only for PLL, IF counter and AD/DA converter analog units.	—

Pin No.	Symbol	Pin Name	Function/Operation	Remarks
51	FM_{IN}	FM Band Signal Input	Programmable counter input terminal for FM band. The 1/2 + pulse swallow system (FM_H mode) and the pulse swallow system (FM_L mode) are selectable by PLL instruction. In case of the pulse swallow system, local oscillation output (VCO output) of 30~140 MHz (0.3 V_{p-p} min) is input and in case of 1/2 prescaler input, 30~185 MHz (0.5 V_{p-p} min) is input. Having a built-in input amplifier, operates at small amplitude with a capacitor connected. Note: When reference internal ports (4 bits) are set at all "1" or LF mode or HF mode is set, this input is pulled down.	
52	AM_{IN}	AM Band Signal Input	Programmable counter input terminal for AM band. The direct dividing system (LF mode) and the swallow system (HF mode) are freely selectable by PLL instruction. In case of the direct dividing system (LF mode), local oscillation output (VCO output) of 0.5~20 MHz (0.3 V_{p-p} min) and in case of the pulse swallow system, 1~40 MHz (0.3 V_{p-p} min) is input. Having a built-in input amplifier, operates at small amplitude with a capacitor connected. Note: When reference internal ports (4 bits) are set at all "1" or FM_H Mode or FM_L Mode is set, this input is pulled down.	
53	V_{DD}	Power Supply Terminal	Power supply terminal. At time of PLL operation, 5 V ± 10% is applied. In the back-up state (when executing CKSTP instruction), voltage can be reduced to 2 V. Further, when voltage drops below 3.5 V during the operation of CPU, CPU stops (CPU wait mode) to prevent malfunction it restarts when voltage increases above 3.5 V. As (wait mode) resulted under this condition can be detected by Wait F/F bit, perform initialization, clock correction, etc. programmatically. Further, when 0 to 3.5 V is applied to this terminal, a device is reset and a program starts from address 0 (power on reset). Note: Rise time of supply voltage on a device shall be 10~100 ms for the power ON reset operation. (refer to Note 1)	—
54	GND1	Digital GND Terminal	GND terminal for CPU and the logic unit.	—

Pin No.	Symbol	Pin Name	Function/Operation	Remarks
55 56	X_T $\overline{X_T}$	Crystal Oscillation Terminal	Crystal resonator connecting terminal. Connect a 7.2 MHz crystal to this terminal. Adjust oscillation frequency (7.2 MHz) while observing LCD segment waveform. When CKSTP instruction is executed. Oscillation stops automatically.	

Note 1: When a device is reset (V_{DD} = 0 → 3.5 V and $\overline{INI}$ = "L" → "H"), I/O ports are set to the input, terminals serving as I/O ports and AD/DA converters are to the input of I/O ports, terminals serving as I/O ports and serial I/O ports are set to the input of I/O ports, and terminals serving as IF counter input and input port are set to IF counter input.

Note 2: When CKSTP instruction is executed, outputs of the output ports and I/O ports are all set at "L" level.

Note 3: When a device is reset, contents of output ports and internal ports are indefinite and it is therefore necessary to initialize them by programmatically.

Operational Description

CPU

The CPU consists of a program counter, stack register, ALU, program memory, data memory, G-register, data register, carry F/F, and judge circuit.

1. Program Counter (PC)

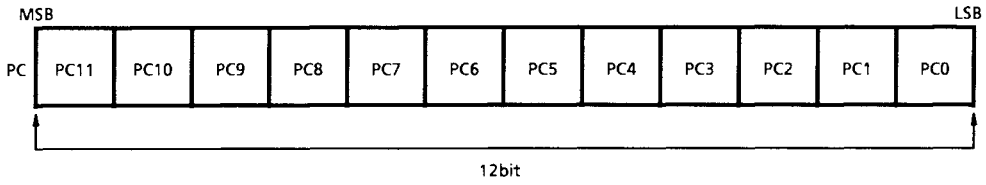
The program counter is a counter for addressing program memory (ROM) and consists of a 12 bit binary up counter.

This counter is cleared by system resetting and a program starts from address 0.

Normally, whenever one instruction is executed, the count value is incremented by one.

When JUMP instruction or CAL instruction is executed, the address designated in the operand of that instruction is loaded.

Further, when an instruction having the skip function (AIS, SLT, TMT, RNS instructions, etc.) is executed and the result is a condition to be skipped, the program counter is incremented by two and skips next instruction.



2. Stack Register (STACK)

This is a register consisting of 2 × 12 bits and a value of the program content +1, that is, return address is stored in this register when the subroutine call instruction is executed.

The content of the stack register is loaded on the program counter when a return instruction (RN, RNS instruction) is executed.

The stack register has 2 stack levels and nesting is 2 levels.

3. ALU

The ALU has the binary 4 bit parallel addition and subtraction, logical operation, comparison and multiple bit judging functions.

Further, this CPU has no accumulator and contents of the data memory are directly treated in all operation.

4. Program Memory (ROM)

The program memory, consisting of 16 bits × 3968 steps, stores programs.

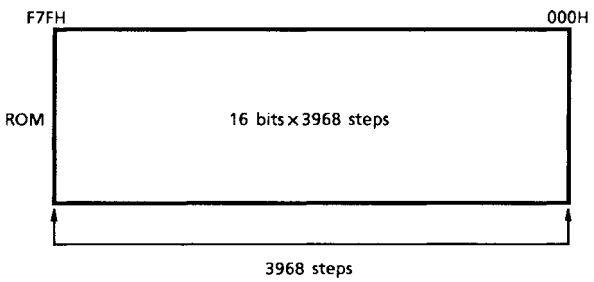
Usable address range is 3968 steps from address 000H to address F7FH.

The program memory has no concept of page and field, and JUMP and CAL instructions are freely usable in 3968 steps.

Further, it is possible to use any address of the program memory as data area and to load its contents in 16 bits in the data register by executing DAL instructions.

Note 4: Data area in the program memory shall be provided at address outside the program loop.

Note 5: Address in the program memory designatable as data area at time of DAL instruction execution is within 1024 steps from 000H to 3FFH.



5. Data Memory (RAM)

The date memory consists of 4 bits × 256 words and is used for data storage.

These 256 words are expressed by row address (4 bits) and column address (4 bits).

192 word (row address = 4H~FH) in the data memory are indirectly addressed by G-register.

Therefore, when data in this area are processed, it is necessary to perform the processing after designating row address in advance with G-register.

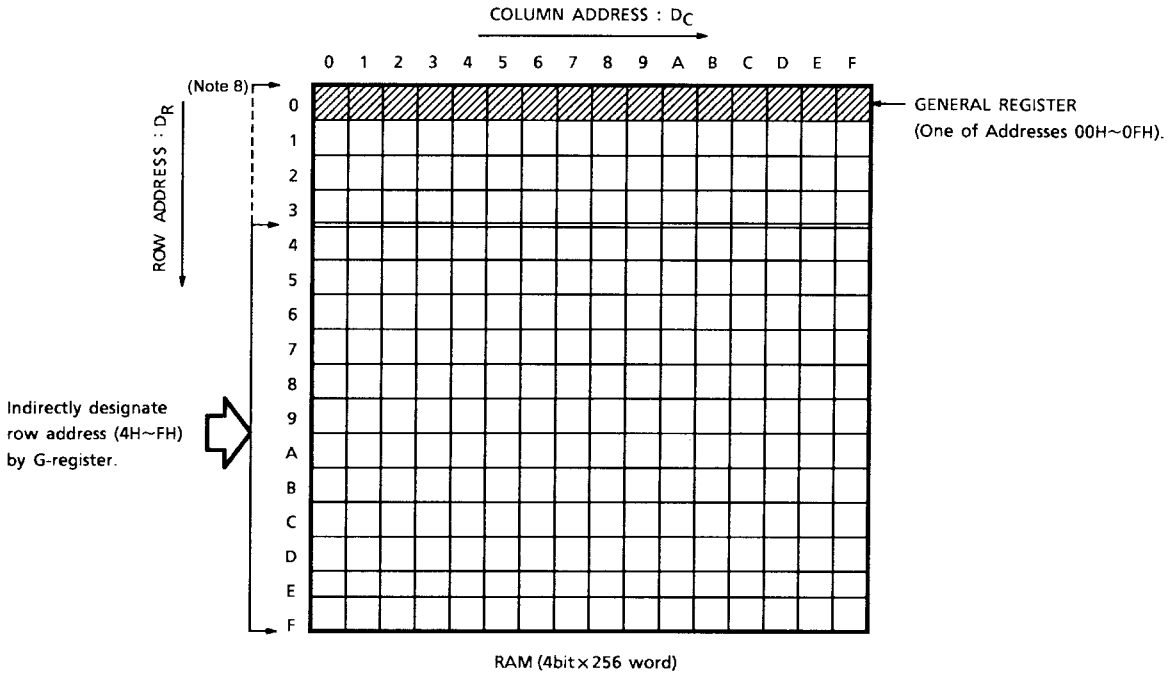
Further, address 00H~0FH in the data memory are called the general register and usable only by designating column address (4 bits).

These 16 general registers can be used for operation and transfer with the data memory.

In addition, it is also possible to use them as ordinary data memories.

Note 6: Column address (4 bits) designating a general register becomes register No. of that general register.

Note 7: It is also possible to indirectly designate all row addresses (0H~BH) by G-register.



Note 8: Indirectly designation of row address 0H~FH is also possible.

6. G-Register (G-REG)

The G-register is a 4 bits register for addressing row addresses (D_R = 4~FH) of 192 words of the data memory.

Contents of this register becomes effective when MVGD/MVGS instruction is executed and have nothing to do with execution of other instructions.

This register is treated as one of ports and its contents are set when IO instruction is executed.

(refer to item 1 of resister ports.)

7. Data Register (DATA REG)

This register consists of 1 × 16 bits and 16 bit data of any address 000H~3FFH of the program memory is loaded when DAL instruction is executed.

This register is treated as one of ports and its contents are read in 4 bits unit into the data memory when KEY instruction out of I/O instructions is executed.

(refer to item 2 of register ports.)

8. Carry F/F (C.F/F)

This carry F/F is set when carry or borrow was generated as a result of execution of the calculation instruction and is reset when there is no carry nor borrow.

Contents of the carry F/F change only when the addition/substraction instruction was executed and remain unchanged when other instructions were executed.

9. Judge Circuit (J)

When any instruction having a skip function was executed, this circuit judges that skip condition. If the skip condition was satisfied, the program counter is incremented by two and skips a following instruction.

There are 29 instructions having the skip function.

(refer to instructions with the *mark on the list of function and operation of in item 11)

10. List of Instructions Sets

Total 61 instruction sets are available and they are all one word instruction.

These instruction are expressed in 6 bits instruction code.

High Order 2 Bits / Low Order 4 Bits		00		01		10		11	
		0		1		2		3	
0000	0	AI	M, I	AD	r, M	CALL $ADDR_1$		SLTI	M, I
0001	1	AIS	M, I	ADS	r, M			SGEI	M, I
0010	2	AIN	M, I	ADN	r, M			SEQI	M, I
0011	3	SI	M, I	SU	r, M			SNEI	M, I
0100	4	SIS	M, I	SUS	r, M	MVSR	M_1, M_2	JUMP $ADDR_1$	
0101	5	SIN	M, I	SUN	r, M	MVIM	M, I		
0110	6	LD	r, M	ORR	r, M	MVGD	r, M		
0111	7	ST	M, r	ANDR	r, M	MVGS	M, r		
1000	8	AIC	M, I	AC	r, M	PLL	M, C	TMTR	r, M
1001	9	AICS	M, I	ACS	r, M	SEG	M, C	TMFR	r, M
1010	A	AICN	M, I	ACN	r, M	MARK	M, C	TMT	M, N
1011	B	SIB	M, I	SB	r, M	IO	M, C	TMF	M, N
1100	C	SIBS	M, I	SBS	r, M	KEY	M, C	TMTN	M, N
1101	D	SIBN	M, I	SBN	r, M	SIO	M, C	TMFN	M, N
1110	E	SEQ	r, M	ORIM	M, I	XORIM	M, I	DAL $ADDR_2$, r	
1111	F	SNE	r, M	ANIM	M, I	XORR	r, M	RN, RNS, CKSTP, NOOP	

11. List of Functions and Operation of Instructions

(explanation of symbols on list)

M: Data Memory Address
Usually, one of data memory addresses 00H~3FH
r: General Register
One of data memory addresses 00H~0FH
PC: Program Counter (12 bits)
STACK: Stack Register (12 bits)
G: G-Register (4 bits)
DATA: Data Register (16 bits)
I: Immediate Data (4 bits)
N: Bit Position (4 bits)
—: ALL "0"
C: Port Code No. (4 bits)
C_N: Low order 3 bits of Port Code No.
R_N: General Register No. (4 bits)
$ADDR_1$: Program Memory Address (12 bits)
$ADDR_2$: High order 6 bits of Program Memory Address in Page 0.
Ca: Carry
b: Borrow
PLL: Port treated by execution of PLL instruction
SEG: Port treated by execution of SEG instruction
MARK: Port treated by execution of MARK instruction
IO: Port treated by execution of IO instruction
KEY: Port treated by execution of KEY instruction
SIO: Port treated by execution of SIO instruction
( ): Contents of register or data memory
[ ] $_C$: Contents of port shown by Code No. C (4 bits)
[ ]: Contents of Data Memory shown by contents of Register or Data Memory
[ ] $_P$: Contents of Program Memory (16 bits)
IC: Instruction Code (6 bits)
*: Instruction with skip function
D_C: Data Memory Column Address (4 bits)
D_R: Data Memory Row Address (2 bits)

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
ADDITION INSTRUCTION	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	D_R	D_C	I
	AIS	M, I	*	Add immediate data to memory, then skip if carry	M ← (M) + I Skip if carry	000001	D_R	D_C	I
	AIN	M, I	*	Add immediate data to memory, then skip if not carry	M ← (M) + I Skip if not carry	000010	D_R	D_C	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	001000	D_R	D_C	I
	AICS	M, I	*	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + ca Skip if carry	001001	D_R	D_C	I
	AICN	M, I	*	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + ca Skip if not carry	001010	D_R	D_C	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	010000	D_R	D_C	R_N
	ADS	r, M	*	Add memory to general register, then skip if carry	r ← (r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN	r, M	*	Add memory to general register, then skip if not carry	r ← (r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	011000	D_R	D_C	R_N
	ACS	r, M	*	Add memory to general register with carry, then skip if carry	r ← (r) + (M) + ca Skip if carry	011001	D_R	D_C	R_N
	ACN	r, M	*	Add memory to general register with carry, then skip if not carry	r ← (r) + (M) + ca Skip if not carry	011010	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
SUBTRACTION INSTRUCTION	SI	M, I		Subtract immediate data from memory	M ← (M) – I	000011	D_R	D_C	I
	SIS	M, I	*	Subtract immediate data from memory, then skip if borrow	M ← (M) – I Skip if borrow	000100	D_R	D_C	I
	SIN	M, I	*	Subtract immediate data from memory, then skip if not borrow	M ← (M) – I Skip if not borrow	000101	D_R	D_C	I
	SIB	M, I		Subtract immediate data from memory, with borrow	M ← (M) – I – b	001011	D_R	D_C	I
	SIBS	M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN	M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU	r, M		Subtract memory from general register	r ← (r) – (M)	010011	D_R	D_C	R_N
	SUS	r, M	*	Subtract memory from general register, then skip if borrow	r ← (r) – (M) Skip if borrow	010100	D_R	D_C	R_N
	SUN	r, M	*	Subtract memory from general register, then skip if not borrow	r ← (r) – (M) Skip if not borrow	010101	D_R	D_C	R_N
	SB	r, M		Subtract memory from general register with borrow	r ← (r) – (M) – b	011011	D_R	D_C	R_N
	SBS	r, M	*	Subtract memory from general register with borrow, then skip if borrow	r ← (r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN	r, M	*	Subtract memory from general register with borrow, then skip if not borrow	r ← (r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N
COMPARISON INSTRUCTION	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	001110	D_R	D_C	R_N
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	001111	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
TRANSFER INSTRUCTION	LD	r, M		Load memory to general register	r ← (M)	000110	D_R	D_C	R_N
	ST	M, r		Store general register to memory	M ← (r)	000111	D_R	D_C	R_N
	MVSR	M_1, M_2		Move memory to memory in the same row	(D_R, D_{C1}) ← (D_R, D_{C2})	100100	D_R	D_{C1}	D_{C2}
	MVIM	M, I		Move immediate data to memory	M ← I	100101	D_R	D_C	I
	MVGD	r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	100110	D_R	D_C	R_N
	MVGS	M, r		Move source memory referring to G-register and general register to memory	M ← [(G), (r)]	100111	D_R	D_C	R_N
INPUT AND OUTPUT INSTRUCTION	PLL	M, C		Input PLL port data to memory	M ← [PLL] $_C$	101000	D_R	D_C	0 C_N
				Output contents of memory to PLL port	[PLL] $_C$ ← (M)		D_R	D_C	1 C_N
	SEG	M, C		Input SEG port data to memory	M ← [SEG] $_C$	101001	D_R	D_C	0 C_N
				Output contents of memory to SEG port	[SEG] $_C$ ← (M)		D_R	D_C	1 C_N
	IO	M, C		Input IO port data to memory	M ← [IO] $_C$	101011	D_R	D_C	0 C_N
				Output contents of memory to IO port	[IO] $_C$ ← (M)		D_R	D_C	1 C_N
	MARK	M, C		Input MARK port data to memory	M ← [MARK] $_C$	101010	D_R	D_C	0 C_N
				Output contents of memory to MARK port	[MARK] $_C$ ← (M)		D_R	D_C	1 C_N
	KEY	M, C		Input KEY port data to memory	M ← [KEY] $_C$	101100	D_R	D_C	0 C_N
				Output contents of memory to KEY port	[KEY] $_C$ ← (M)		D_R	D_C	1 C_N
	SIO	M, C		Serial input port data of external device to memory	M ← [SIO] $_C$	101101	D_R	D_C	0 C_N
				Serial output contents of memory to port of external device	[SIO] $_C$ ← M		D_R	D_C	1 C_N
LOGICAL OPERATION INSTRUCTION	ORR	r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	010110	D_R	D_C	R_N
	ANDR	r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	010111	D_R	D_C	R_N
	ORIM	M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	011110	D_R	D_C	I
	ANIM	M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	011111	D_R	D_C	I
	XORIM	M, I		Logical exclusive OR of memory and immediate data	M ← (M) ⊕ I	101110	D_R	D_C	I
	XORR	r, M		Logical exclusive OR of general register and memory	r ← (r) ⊕ (M)	101111	D_R	D_C	R_N

Inst. Gr.	Mnemonic	Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
					IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
BIT JUDGE INSTRUCTION	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	111000	D_R	D_C	R_N
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	111001	D_R	D_C	R_N
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	111010	D_R	D_C	N
	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	111011	D_R	D_C	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	111100	D_R	D_C	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	111101	D_R	D_C	N
SUBROUTINE INSTRUCTION	CALL $ADDR_1$		Call subroutine	STACK ← (PC) + 1 and PC ← $ADDR_1$	10000	$ADDR_1$ (12 bit)		
	RN		Return to main routine	PC ← (STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	01	—	—
JUMP INSTRUCTION	JUMP $ADDR_1$		Jump to the address specified	PC ← $ADDR_1$	1101	$ADDR_1$ (12 bit)		
OTHER INSTRUCTIONS	DAL $ADDR_2$, r		Load program memory in page 0 to DATA register	DATA ← $[ADDR_2 + (r)]_P$ in page 0	111110	$ADDR_2$ (6 bit)		R_N
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH}$ = "0"	111111	10	—	—
	NOOP		No operation	—	111111	11	—	—

Note 9: When executing I/O instruction, input/output of the instruction is automatically controlled according to a value of the most significant bit of port code No. (C).

- MSB of code No. (C) = "1": Output instruction
- MSB of code No. (C) = "0": Input instruction

Note 10: Basically execution of SIO instruction is treated similar to execution of other I/O instructions (PLL instruction, SEG instruction, etc.) except the following points:

- First, it is necessary to select an external device that becomes a destination of transferring serial data by the chip select code ((C) = FH).

  (refer item 1 of serial interface.)

- SIO instruction execution time is 55.5 μs (5 machine cycle).

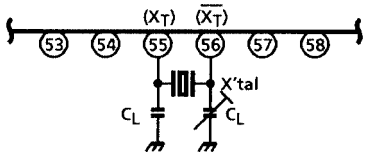
Note 11: As the TC9321F has no input port that is treated in the execution of SEG and MARK instructions, this input instruction cannot be used.

Note 12: Low order 4 bits out of the program memory address 10 bits designated by DAL instruction are to be indirectly addressed according to contents of the general register.

DAL instruction execution time is 22.2 μs (2 machine cycle).

Connection of Crystal Resonator

Connect a crystal resonator to the crystal oscillator terminal (X_T, $\overline{X_T}$ terminal) of a device as illustrated below. This oscillation signal is supplied to the clock generator and the reference frequency divider for generating various CPU timing signals and reference frequency signals.



X'tal = 7.2 MHz

C_L = 10~50 pF (30 pF typ.)

Note 13: Use a crystal resonator having a low CI value and good starting characteristic.

System Reset

When "L" level signal is input to the $\overline{INI}$ terminal or 0~3.5 V is supplied to the V_{DD} terminal (power ON reset), system reset is applied to a device.

After 10 ms of standby time passed after the system reset, a program starts from address 0.

Normally, as the Power ON reset function is used, the $\overline{INI}$ terminal shall be fixed at "H" level.

Note 14: During the system reset, general output port (T0~T7, OT1~OT4) are fixed at "L" level.

Note 15: After the system reset, I/O ports are all set in the input mode.

However, no initialization of output ports and internal ports (G-register, etc.) is performed. In particular, contents of these ports become indefinite when the power source is initially turned on and therefore, it becomes necessary to initialize them programmatically as necessary.

I/O Port

I/O Port / Code No.		PLL (ϕ1)				SEG (ϕ2)				MARK (ϕ3)				IO (ϕ4)				KEY (ϕ5)				SIO (ϕ6)			
		Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
INPUT PORT (K)	0					I/O PORT-5								I/O PORT-1											
						–1	–2	–3	–4					–1	–2	–3	–4								
	1	IF COUNTER				I/O PORT-6								I/O PORT-2											
		F0	F1	F2	F3	–1	–2	–3	–4					–1	–2	–3	–4								
	2	IF COUNTER				I/O PORT-7								I/O PORT-3/DA REF DATA				KEY INPUT							
		F4	F5	F6	F7	–1	–2	–3	–4					–1/AR0	–2/AR1	–3/AR2	–4/AR3	K0	K1	K2	K3				
	3	IF COUNTER				I/O PORT-8								I/O PORT4				$\overline{\text{AD OUT}}$	0	0	0				
		F8	F9	F10	F11	–1	–2	0	0					–1	–2	–3	–4					SERIAL INPUT			
	4	IF COUNTER												$\overline{\text{INH}}$	0	0	0	DATA REGISTER				CODE No. (C) = 0H~7H			
		F12	F13	F14	F15													d0	d1	d2	d3				
	5	IF COUNTER												2 Hz F/F	10 Hz	100 Hz	Wait F/F	DATA REGISTER							
		F16	F17	F18	F19													d4	d5	d6	d7				
	6	IF COUNTER CONTROL			0													DATA REGISTER							
		BUSY	MANUAL	OVFLW														d8	d9	d10	d11				
	7	IN1	IN2	UNLOCK PORT														DATA REGISTER							
				ENABLE	UNLOCK													d12	d13	d14	d15				
OUTPUT PORT (K)	8	HF	IF OFFSET		FM	I/O PORT-5				PORT-5 I/O CONTROL				I/O PORT-1				PORT-1 I/O CONTROL							
			+1	–1		–1	–2	–3	–4	–1	–2	–3	–4	–1	–2	–3	–4	–1	–2	–3	–4				
	9	PROGRAMMABLE COUNTER				I/O PORT-6				PORT-6 I/O CONTROL				I/O PORT-2				PORT-2 I/O CONTROL							
		P0	P1	P2	P3	–1	–2	–3	–4	–1	–2	–3	–4	–1	–2	–3	–4	–1	–2	–3	–4				
	A	PROGRAMMABLE COUNTER				I/O PORT-7				PORT-7 I/O CONTROL				I/O PORT-3/DA REF DATA				PORT-3 I/O CONTROL/DA REF DATA			AD ON				
		P4	P5	P6	P7	–1	–2	–3	–4	–1	–2	–3	–4	–1/AR0	–2/AR1	–3/AR2	–4/AR3	–1/AR4	–2/AR5	–3/AD SEL					
	B	PROGRAMMABLE COUNTER				I/O PORT-8				PORT-8 I/O CONTROL				I/O PORT-4				PORT-4 I/O CONTROL				SERIAL OUTPUT			
		P8	P9	P10	P11	–1	–2	*	*	–1	–2	*	*	–1	–2	–3	–4	–1	–2	–3	–4	CODE No. (C) = 8H~EH			
	C	PROGRAMMABLE COUNTER												G-REGISTER				SIO ON	SIO NCD	DISP OFF	DA ON				
		P12	P13	P14	P15									#0	#1	#2	#3								
	D	REFERENCE PORT												2 Hz F/F RESET	CLOCK RESET	*	*								
		#0	#1	#2	#3																				
	E	IF COUNTER CONTROL												KEY TIMING PORT				OUT PORT							
		STA/$\overline{\text{STP}}$	MANUAL	#0	#1									T0	T1	T2	T3	OT1	OT2	OT3	OT4				
	F	IN CONTROL		IF1	UNLOCK RESET									KEY TIMING PORT				TEST		*	*				
		IN1	IN2											T4	T5	T6	T7	#1	#2						

I/O Map

All ports in the device are expressed by a matrix of 6 I/O instructions (PLL, SEG, MARK, IO, KEY and SIO, instruction) with 4 bit Code No. C. Allocation of these ports are shown above as the I/O Map. In this Map, port names treated in execution of I/O instructions are assigned on the axis of ordinates and port code numbers on the axis of abscissas. G-register and data register are also treated as ports.

Basically, data of all ports are treated in unit of 4 bits, and Code No. (C) = 0H~7H are designated as the input ports and Code No. (C) = 8H~FH as the output ports.

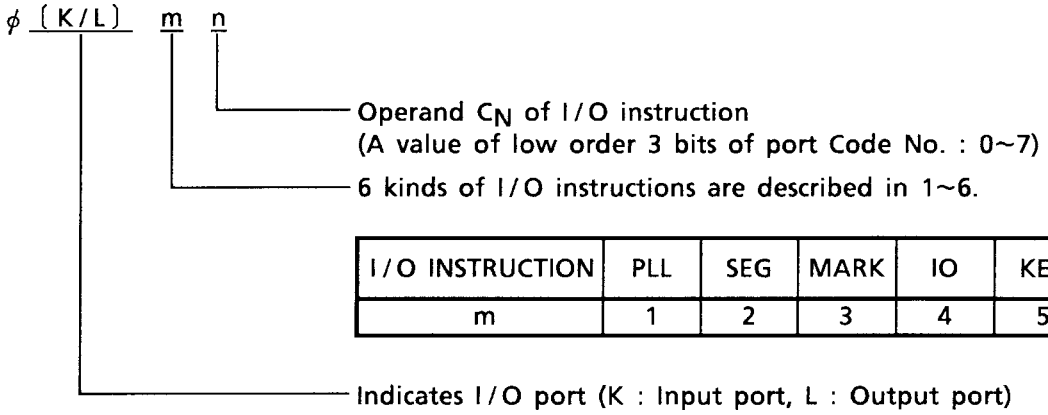
Note 16: The oblique lined ports shown on the I/O map are actually not existed in the device. If data was output to an unexisted port when an output instruction was executed, contents of other parts and the data memory are not especially affected.

If an unexisting input port was designated when executing an input instruction, contents of data to be read in the data memory will become indefinite.

Note 17: Ports with *mark out of output ports on the I/O map are unused ports. Data being output to these ports will become don't care.

Note 18: Contents of ports expressed in 4 bits, that is, Y1 corresponds to LSB of data of the data memory and Y8 corresponds to MSB. Data of all ports are treated in positive logic.

Note 19: Ports that are designated by 6 I/O instructions and code No. C are expressed by encoding as shown below.



I/O INSTRUCTION	PLL	SEG	MARK	IO	KEY	SIO
m	1	2	3	4	5	6

Programmable Counter

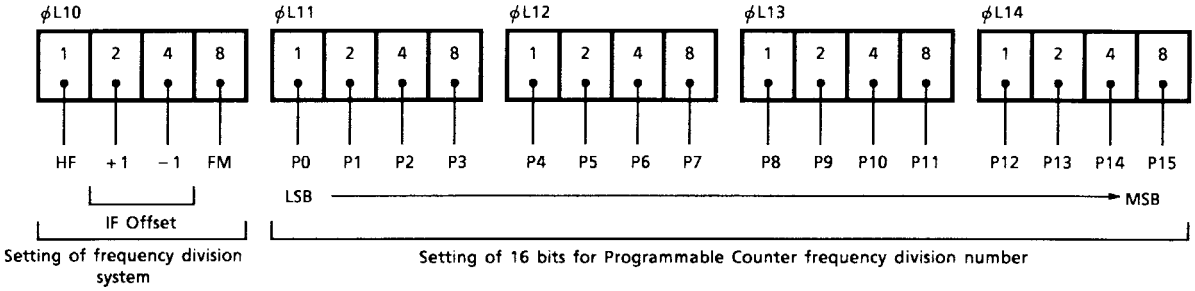
The programmable counter consists of 2-modulus prescaler, 4 bit + 12 bit programmable binary counter, and PLL I/O port group that controls these prescaler and counter.

Further, the programmable counter is turned ON/OFF according to contents of the reference port, that is, when contents of the reference port (4 bits) are all "1", the programmable counter is put in the PLL OFF Mode and otherwise, it is put in the PLL ON Mode.

1. PLL I/O Ports (ϕKL10~ϕKL14)

These are exclusive ports for PLL to control all of frequency division number, frequency division system, and IF correction (IF offset) at FM band, and are accessed by PLL output instructions designated [C_N = 0~4] in the operand field (ϕL10~ϕL14).

(1) Construction of PLL ports



(2) Setting of frequency division system

The pulse swallow system or the direct frequency division system are selected according to HF and FM ports.

Select any of 4 systems available as shown in the following table according to frequency band to be used.

Mode	HF	FM	Frequency Division System	Example of Receiving Band	Input Frequency Range	Input Terminal	Frequency Division Number
LF	0	0	Direct frequency division system	LW, MW, SW_L	0.5~20 MHz	AM_{IN}	n
HF	1	0	$\left(\frac{1}{15}/\frac{1}{16}\right)$ pulse swallow system	SW_H	1~40 MHz	AM_{IN}	n
FM_L	0	1	$\left(\frac{1}{15}/\frac{1}{16}\right)$ pulse swallow system	FM	30~140 MHz	FM_{IN}	n
FM_H	1	1	$\left(\frac{1}{2}\times\frac{1}{15}/\frac{1}{16}\right)$ pulse swallow system	WB (Note 20)	30~185 MHz	FM_{IN}	2·n

Note 20: Weather band

Note 21: n denotes a programmed divided frequency value.

(3) IF correction function at FM band

When the pulse swallow system was selected, actual frequency division number is variable of ±1 without changing programmed frequency division value by ΔIF ± 1 port.

This function can be used for IF offset at FM band.

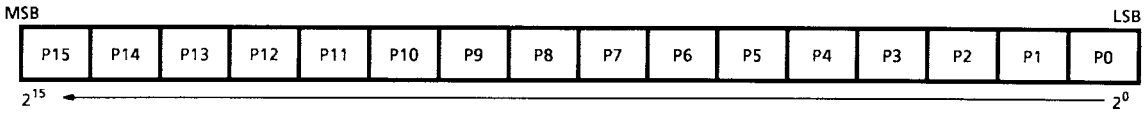
And when the direct division system was selected, the IF offset function does not operate.

ΔIF + 1	ΔIF − 1	Frequency Division Number (FM_H)	Frequency Division Number (FM_L)
0	0	2·n	n
0	1	2·(n − 1)	n − 1
1	0	2·(n + 1)	n + 1
1	1	2·(n − 1)	n − 1

(4) Setting of frequency division number

Set frequency division number of the program counter in binary number in P0~P15 ports.

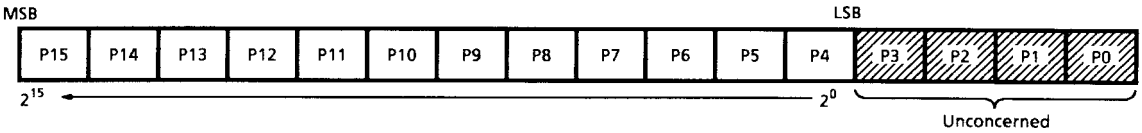
- Pulse swallow system (16 bit)



Note 22: Frequency division number setting range (pulse swallow system)

n = 210H~FFFFH (528~65535)

- Direct frequency division system (12 bit)



Note 23: Frequency division number setting range (direct frequency division system)

n = 10H~FFFH (16~4095)

Note 24: Since no offset is provided to the program counter, a programmed division number will become an actual division number. However, it will become 2 times of a programmed value in case of FM_H mode.

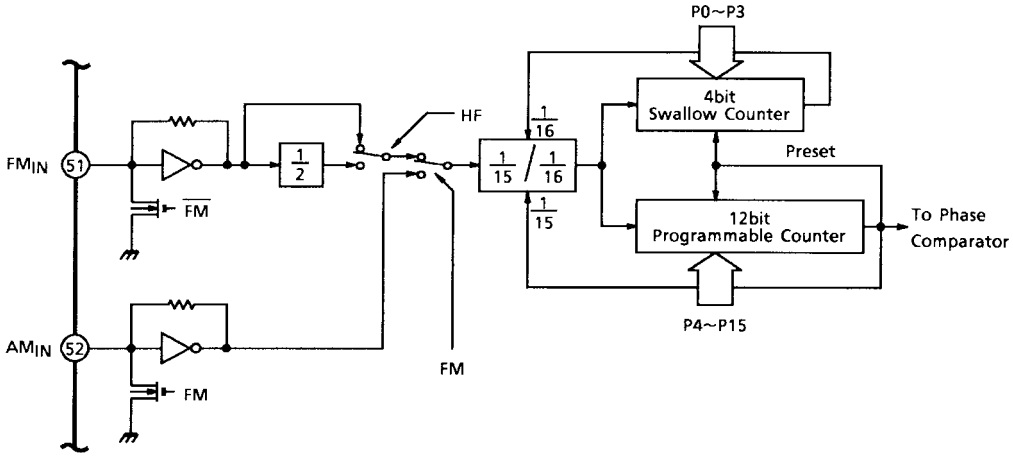
Note 25: In case of the direct division system, data of P0~P3 ports (ϕL11) become unconcerned and P4 port becomes LSB.

Note 26: All data of frequency division number are updated at the same time when MSB port (ϕL14) data are set. This is to prevent the lock-up time from being adversely affected by successive change of frequency division number. Therefore, MSB port (ϕL14) data must be set lastly when frequency division numbers are set. Further, even if data set is considered unnecessary (if data is the same as the previous data), it is necessary to execute data setting only for MSB port (ϕL14).

2. Circuit Configuration of Prescaler and Programmable Counter

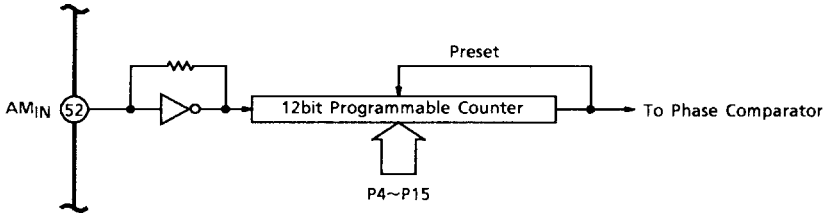
(1) Circuit configuration in case of pulse swallow system

The circuit consists of 1/15/1/16 2-modulus prescaler, a 4 bit swallow counter, and a 12 bit binary programmable counter. Further, in case of FM mode, 2 1/2 divider is added to the front stage of the prescaler.



(2) Circuit configuration in case of direct frequency division system

In this case, a 12 bit programmable counter is only used instead of the prescaler.



Note 27: Both the FM_{IN} and AM_{IN} terminals have built-in an amplifier respectively, and are operable at small amplitude with coupled capacitors. Further, when the input terminal not selected according to the frequency division system and the reference port data (4 bits) are all “1”, the inputs are pulled down.

Reference Frequency Divider

This frequency divider generates 10 kinds of PLL reference frequency signals 1, 3.125, 5, 6.25, 9, 10, 12.5, 25, 50, and 100 kHz by dividing external 7.2 MHz crystal oscillation frequency signals.

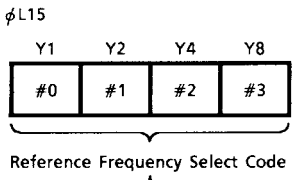
These frequency signals are selected according to the reference port data.

A selected signal is supplied as the reference frequency of the phase comparator described below.

Further, according to the contents of the reference port, PLL ON/OFF is performed.

1. Reference Port (ϕL15)

This is the internal port to select 10 kinds of reference frequency signals. It is normally accessed by PLL output instruction having [C_N = 5] designated in the operand. Further, when the contents of the reference port are all "1", the programmable counter and the reference counter stop and it becomes PLL OFF mode.



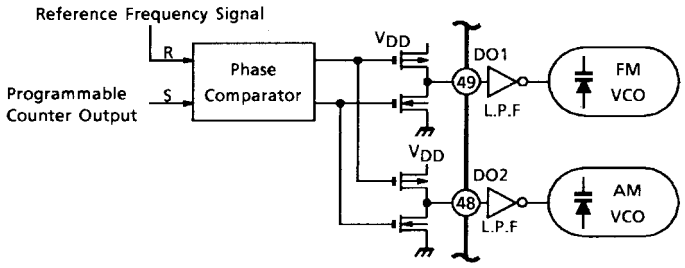
Reference Frequency Table

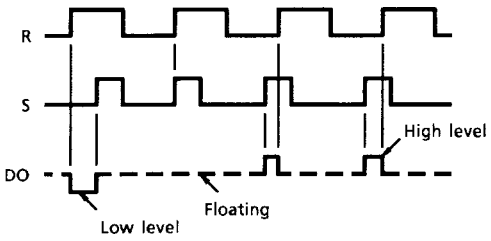
#3	#2	#1	#0		REFERENCE FREQUENCY
0	0	0	0	0	1kHz
0	0	0	1	1	50kHz
0	0	1	0	2	5kHz
0	0	1	1	3	100kHz
0	1	0	0	4	9kHz
0	1	0	1	5	10kHz
0	1	1	0	6	12.5kHz
0	1	1	1	7	25kHz
1	0	0	0	8	3.125kHz
1	0	0	1	9	6.25kHz
1 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	A ↓ E	Inhibit
1	1	1	1	F	PLL OFF Mode

Phase Comparator

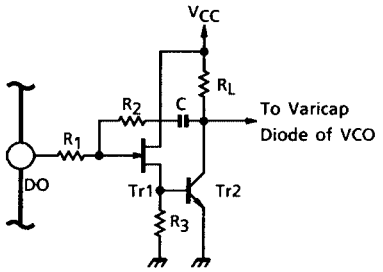
The phase comparator compares phase difference between the reference frequency signal supplied from the reference frequency divider and the programmable counter division output and transmits their difference and then, controls VCO through a low-pass filter so that these two signal frequencies and phases agree with each other.

As there are two parallel tri-state buffer terminals DO1 and DO2 for output from the phase comparator, it is possible to design optimum filter constant for every FM/AM band.





DO Output Timing Chart



Standard
Tr1 : 2SC1815
Tr2 : 2SK246
Examples of Low-Pass Filter Constants (Reference Values at FM band)
$C = 0.33\mu F$
$R_1 = 10k\Omega$
$R_2 = 8.2k\Omega$
$R_3 = 330\Omega$
$R_L = 10k\Omega$

Example of Active Low-Pass Filter Circuit

A DO output timing chart and an example of the active low-pass filter circuit through the Darlington connection of FET and transistors are shown in the above diagram.

Further, the filter circuit shown in the above diagram is one example for reference and an actual circuit shall be examined and designed according to the receiving band structure of a system and desired characteristics.

Unlock Detecting Bit (ϕLK17)

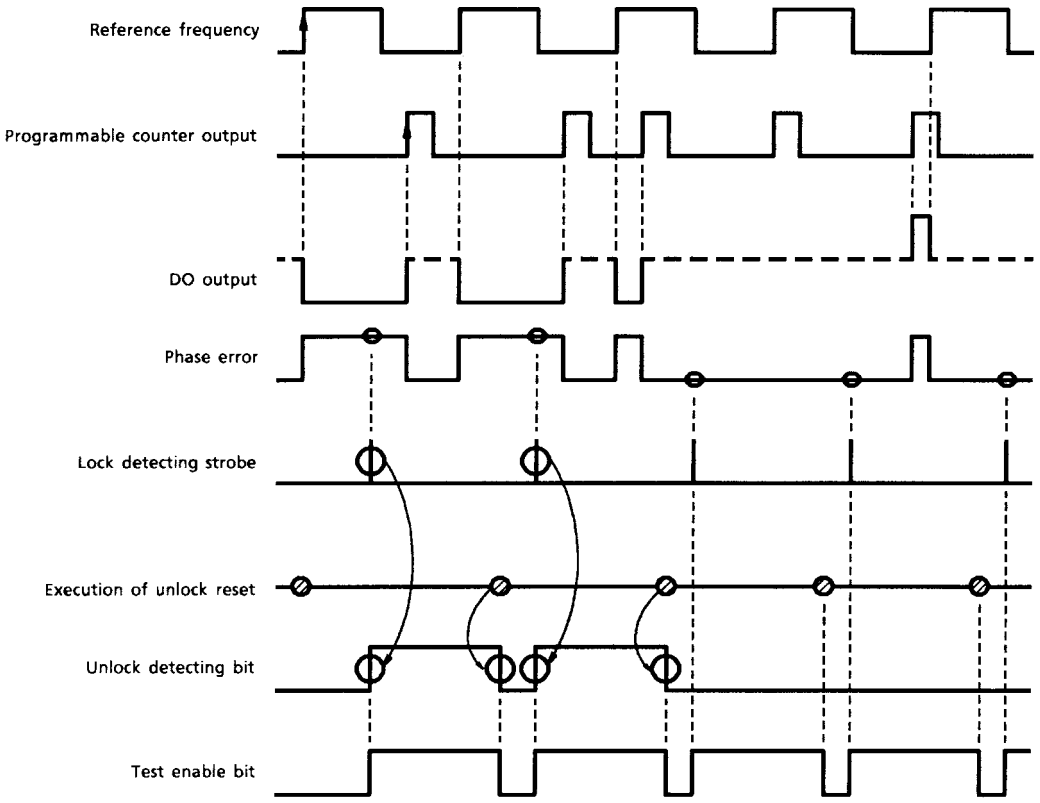
This is a bit to detect the lock state of PLL system. In the unlocked state, that is, the state where reference frequency is not in accord with the programmable counter division output, (phase error) pulses are output to the unlock F/F at reference frequency cycle from the phase comparator. The unlock F/F is set by these phase pulses. Further, whenever the unlock reset bit is set to "1" by the PLL output instruction designated [C_N = 7] in the operand, the unlock F/F is reset (ϕL17).

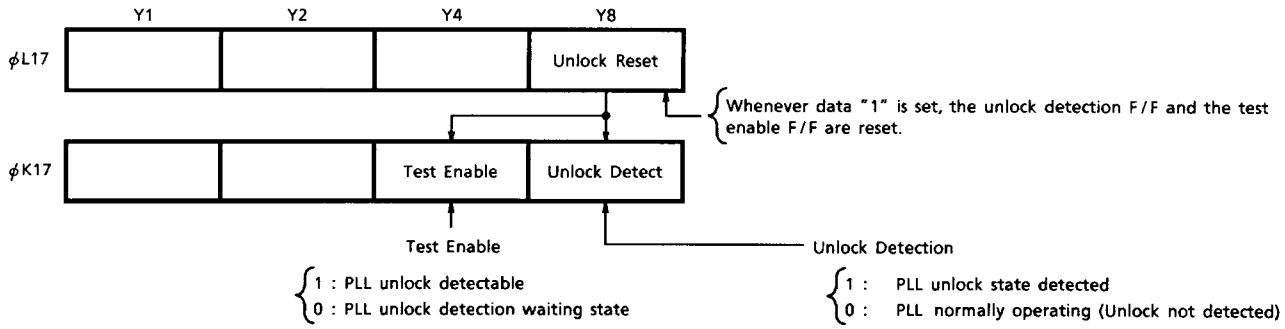
After resetting the unlock F/F, the lock state can be detected by accessing the unlock detecting bit by the PLL input instruction designated [C_N = 7] in the operand (ϕL17).

Since pulses are input at reference frequency cycle, it is necessary to access the unlock detecting bit with providing a time more than reference frequency cycle after resetting the unlock F/F.

If this time was short, the proper lock state cannot be detected.

Therefore, the test enable F/F is provided. This test enable F/F is reset whenever "1" is set for the unlock reset bit and is set to "1" at the unlock detection timing. That is, the unlock state can be properly detected only when this test enable bit (ϕK17) is set at "1".





General Purpose IF Counter

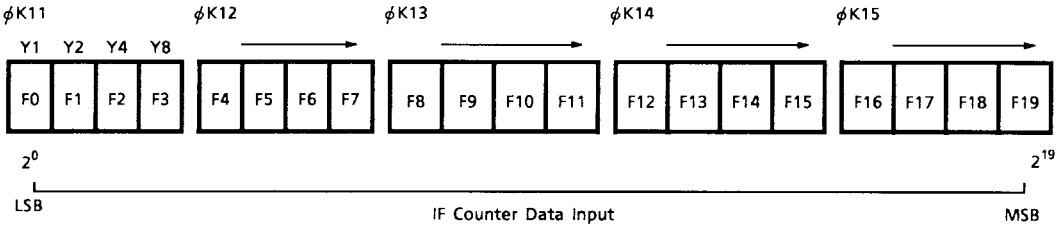
This is a 20 bit general purpose IF counter that is used to count FM or AM intermediate frequency (IF) and is usable for detection of auto stop signal, etc.

The IF counter consists of a 20 bit binary counter and IF counter control ports.

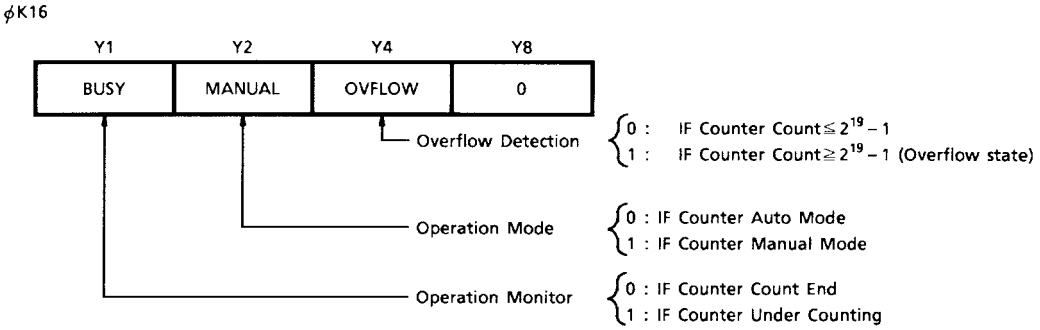
1. IF Counter Data Ports (ϕK11~ϕK16)

These are the data input ports for reading count data and operating state of the IF counter.

Data are read in the data memory by the PLL input instruction designated [C_N = 1~5] in the operand.



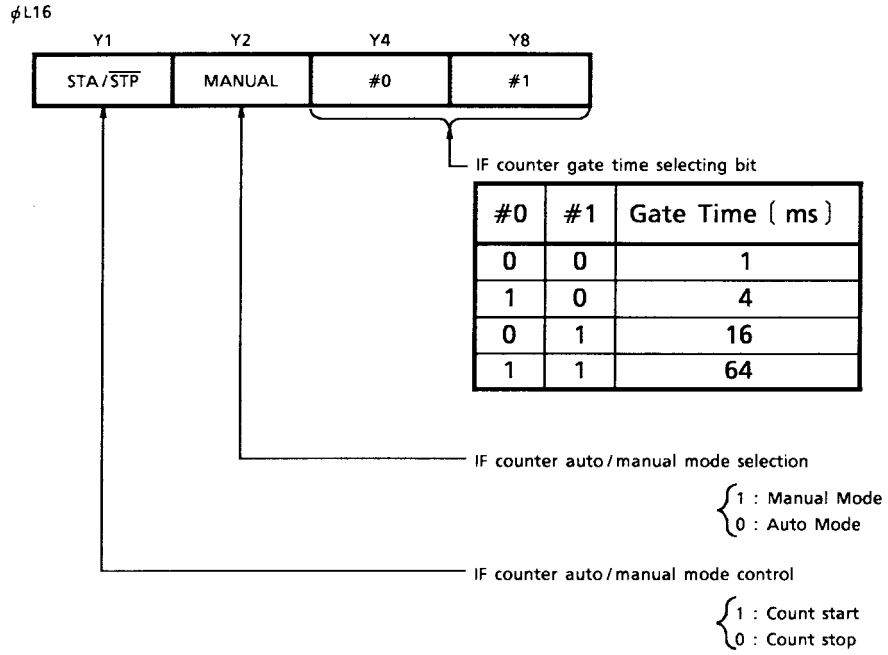
Date counted by the IF counter can be input in binary number through the input ports F0~F19.



This is an input port (ϕK16) to detect the operating state of the IF Counter. When using the IF counter, count data (F0~F19) shall be processed after confirming that BUSY bit is "0" (count end) and OVFLOW bit is "0" (no overflow).

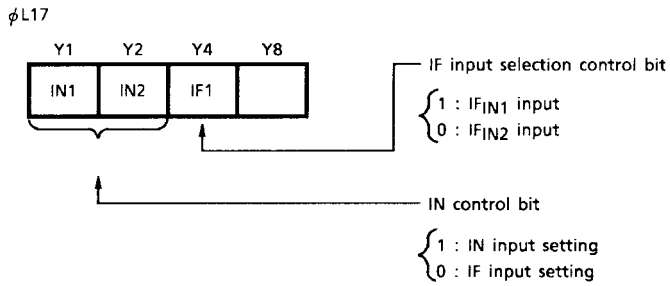
2. IF Counter Control Ports (ϕL16, ϕL17)

These are ports to output data for control of IF counter operation, and are accessible by the PLL output instruction designated [C_N = 6 or 7] in the operand.



#0	#1	Gate Time (ms)
0	0	1
1	0	4
0	1	16
1	1	64

In the auto mode (MANUAL bit is set to "0"), IF count starts whenever STA/$\overline{\text{STP}}$ bit set to "1". IF count ends automatically after passing a gate time selected by #0 or #1 bit. Further, in the manual mode, when STA/$\overline{\text{STP}}$ is set to "1", IF count starts and continues till STA/$\overline{\text{STP}}$ bit is set to "0".



Note 28: Input ports and IF input are selectable in 1 bit unit.

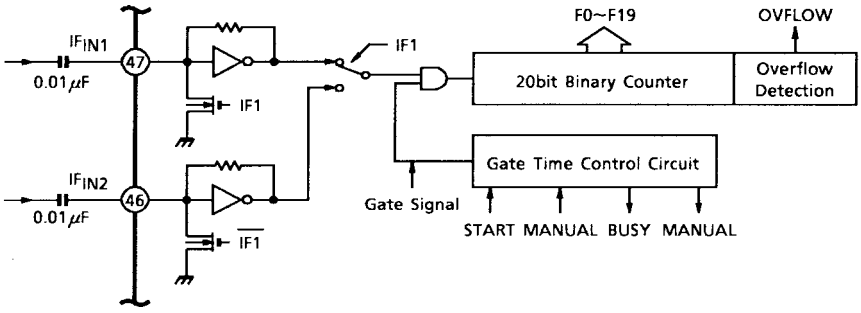
In case that IF counter is used, IN control bit that corresponds to an input terminal to be used shall be set to "0" and IF input selection control bit shall be designated.

Note 29: In the PLL OFF mode, IF counter is reset by force and IF counter input is pulled down. Further, the input that is not selected by IF input selection control bit (IF 1 bit) at the IF counter is pulled down.

Note 30: After system reset, IN control bit is set to "0" and IF input selection control bit is set to "1".

3. IF Counter Circuit Configuration

The IF counter consists of input amplifiers, gate time control circuit, and 20 bit binary counter.



Note 31: IF_{IN} terminals have built-in amplifiers and are capable of operating at small amplitude with coupled capacitors.

I/O Ports

1. I/O Ports-1, -2, -3, -4, -5, -6, -7, -8

I/O Ports-1, -2, -4, -5, -6, -7 are 4 bit ports where input/output are selectable in a unit of each bit, I/O Port-3 is 3 bit port and I/O Port-8 is 2 bit port where input/output are selectable in a unit of each bit. Input/output are set in I/O ports according to the contents of I/O control inner port. To set input in I/O port, set "0" in I/O control port bit corresponding to that I/O port and to set output in I/O port, set "1".

In case of setting input port, data that have been currently input to I/O ports are read in the data memory when IO input instructions corresponding to respective I/O ports are executed. At this time, the contents of the output side latch gives no effect on input data.

In case of setting output port, the I/O port output state is controlled by executing IO output instructions corresponding to respective I/O ports. Further, the contents of data currently being output are read in the data memory when IO input instruction is executed.

Further, I/O Port-3 is also used as the analog input/output of 6 bit A/D and D/A converters, and I/O Port-2 is also used as the serial interface. Therefore, when I/O Port-2 and -3 are used, the contents of A/D ON bit and SIO ON bit should be set to "0".

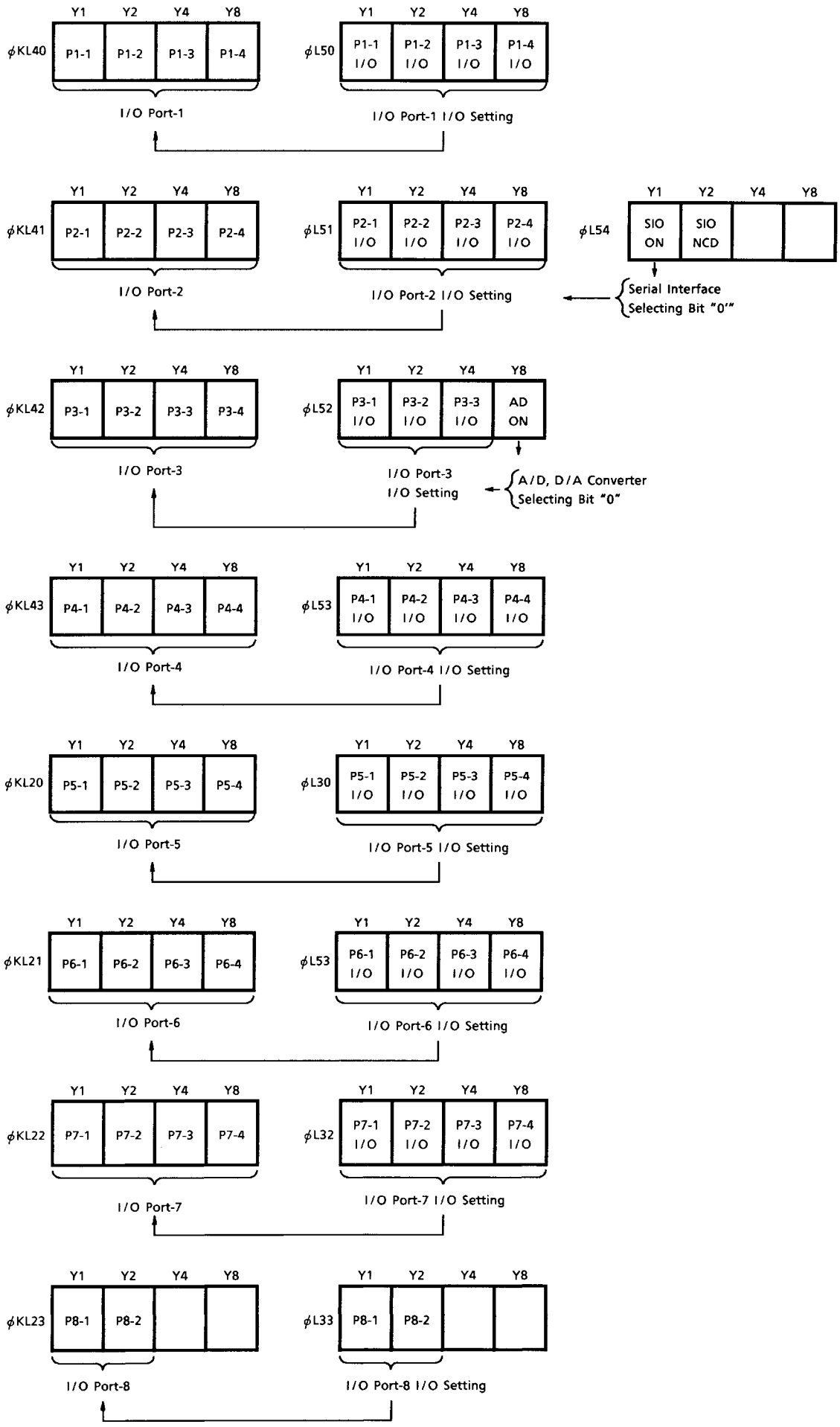
(refer to items of A/D and D/A converters and serial interface.)

Note 32: Output side latch P3-4 data are input from Input port P3-4.

Note 33: Output side latch P3-4 data are normally unconcerned, and when A/D converter is in operation it becomes effective. Further, after system reset, the contents of AD ON bit and SIO ON bit are reset to "0", and D/A converter and serial interface terminal becomes I/O port.

Note 34: After system reset, the contents of I/O control ports are all reset to "0" and all I/O ports are set in the input mode.

Note 35: During the clock stop mode, the output state of all I/O ports that have been set in the output mode is automatically fixed at "L" level but the contents of all output latches are kept at the preceding data.

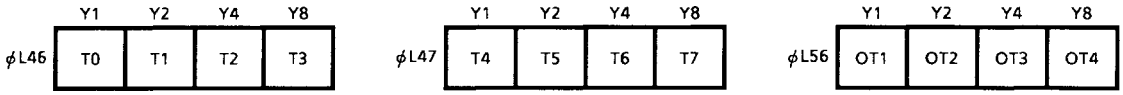

Y1 Y2 Y4 Y8
φKL40 P1-1 P1-2 P1-3 P1-4
I/O Port-1
φL50 P1-1 I/O P1-2 I/O P1-3 I/O P1-4 I/O
I/O Port-1 I/O Setting
φKL41 P2-1 P2-2 P2-3 P2-4
I/O Port-2
φL51 P2-1 I/O P2-2 I/O P2-3 I/O P2-4 I/O
I/O Port-2 I/O Setting
φL54 SIO ON SIO NCD
Serial Interface Selecting Bit "0"
φKL42 P3-1 P3-2 P3-3 P3-4
I/O Port-3
φL52 P3-1 I/O P3-2 I/O P3-3 I/O AD ON
I/O Port-3 I/O Setting
A/D, D/A Converter Selecting Bit "0"
φKL43 P4-1 P4-2 P4-3 P4-4
I/O Port-4
φL53 P4-1 I/O P4-2 I/O P4-3 I/O P4-4 I/O
I/O Port-4 I/O Setting
φKL20 P5-1 P5-2 P5-3 P5-4
I/O Port-5
φL30 P5-1 I/O P5-2 I/O P5-3 I/O P5-4 I/O
I/O Port-5 I/O Setting
φKL21 P6-1 P6-2 P6-3 P6-4
I/O Port-6
φL53 P6-1 I/O P6-2 I/O P6-3 I/O P6-4 I/O
I/O Port-6 I/O Setting
φKL22 P7-1 P7-2 P7-3 P7-4
I/O Port-7
φL32 P7-1 I/O P7-2 I/O P7-3 I/O P7-4 I/O
I/O Port-7 I/O Setting
φKL23 P8-1 P8-2
I/O Port-8
φL33 P8-1 P8-2
I/O Port-8 I/O Setting

2. Key Timing Output (T0~T7), General Purpose Output Ports (OT1~OT4)

T0~T7 are CMOS 8 bit output and OT1~OT4 are CMOS 4 bit output ports. Normally T0~T7 are used for output of key return timing signal of the key matrix and OT1~OT4 are used for control of mute signal, linear circuit, etc.

T0~T7 are accessed by the IO output instruction designated [C_N = 6 or 7] in the operand, and OT1~OT4 are accessed by the KEY output instruction designated [C_N = 6] in the operand. (ϕL46 or ϕL47 or ϕL56)

Note 36: During the clock stop mode, T0~T7 and OT1~OT4 outputs are automatically fixed at "L" level but the contents of the ports are kept at the preceding data.

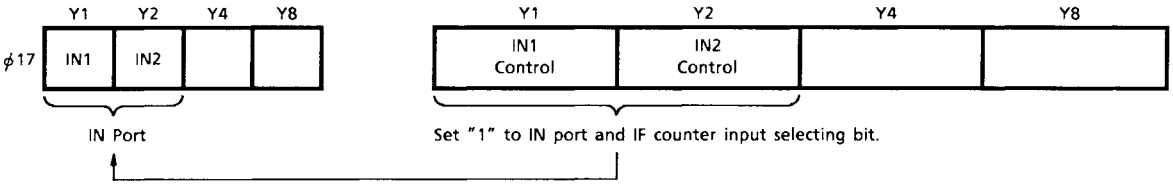


3. General Purpose Input Ports (IN1, IN2)

IN1 and IN2 are CMOS 2 bit input ports. These ports are also used as the IF counter input and they are selected according to the contents of IN control port.

(refer to item of general purpose IF counter.)

In case of setting the input ports, IN control port bit shall be set to "1" by the PLL output instruction designated [C_N = 7] in the operand and data of the input terminals are read in the data memory by executing the PLL input instruction designated [C_N = 7] in the operand.



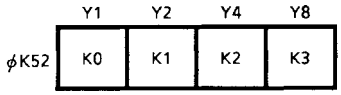
Note 37: When IF counter is used, the contents of IN port becomes "0".

Note 38: After system reset, the contents of IN control port are reset to "0".

4. Key Input Ports (K0~K3)

K0~K3 are the 4 bit exclusive key input terminals for key matrix input. Each of these 4 terminals has a built-in pull-down resistor.

Data is read in the data memory from the key input terminal when the key input instruction designated [C_N = 2] in the operand is executed.



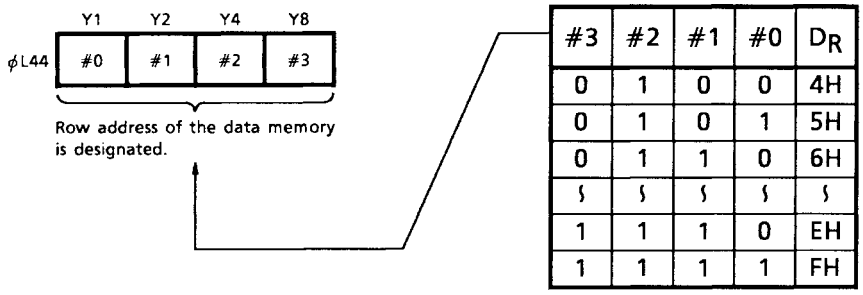
Register Ports

G-Register and Data Registers described in the explanation of CPU are also treated as the inner ports.

1. G-Register (ϕL44)

This is a register for addressing row addresses (D_R = 4H~FH) of the data memory when MVGD/MVGS instruction are executed. This register is accessed by IO output instruction designated [C_N = 4] in the operand.

Note 39: The contents of this register becomes valid only when MVGD/MVGS instruction are executed, and are not concerned with other instructions.



#3	#2	#1	#0	D_R
0	1	0	0	4H
0	1	0	1	5H
0	1	1	0	6H
≀	≀	≀	≀	≀
1	1	1	0	EH
1	1	1	1	FH

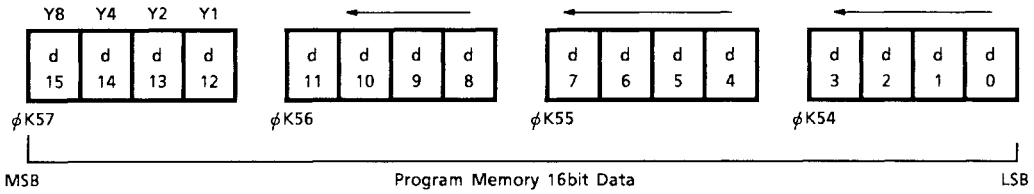
Note 40: All row address of the data memory also can be designated indirectly by setting data 0H~FH in the G-register. (D_R = 0H~FH)

2. Data Register (ϕK54~ϕK57)

This register is a 16 bit register into which the program memory data are loaded.

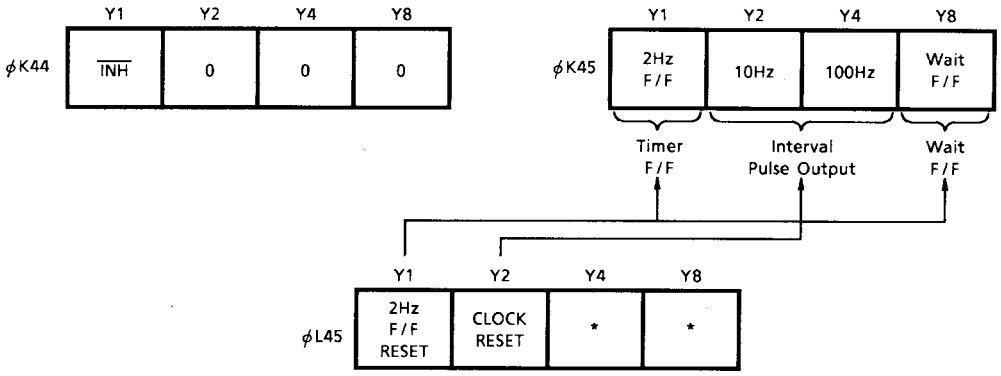
The contents of this register are read in the data memory in a unit of 4 bits when KEY input instruction designated [C_N = 4~7] in the operand are executed.

This register can be used for LCD segment decoding operation and taking radio band edge data, coefficient data of Binary to BCD conversion, etc.



Internal Control Ports

The internal control ports are used for reading the internal state of a device into the data memory, that is needed to know for program execution, and for resetting the internal state of a device.



1. $\overline{INH}$ Input Port (ϕK44)

This is a single bit input port for input the $\overline{INH}$ terminal data. The contents of this port are read in the data memory by executing IO input instruction designated [C_N = 4] in the operand. When CKSTP instruction is executed during "L" level being applied to this terminal, the device is put in the clock stop mode.

Note 41: In executing the CKSTP instruction, make sure that the contents of the $\overline{INH}$ input port is "0" and set the PLL OFF mode (set the contents of the reference port to all "1".) before executing the CKSTP instruction.

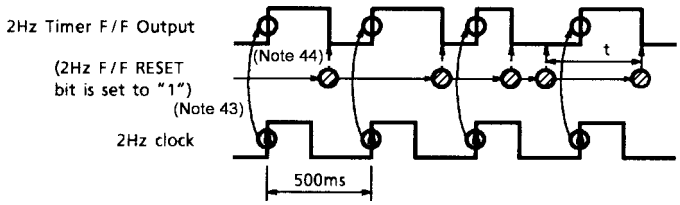
2. 2 Hz Timer F/F (ϕK45)

The 2 Hz timer F/F is set by 2 Hz (500 ms) signal, and is reset when data "1" is set to 2 Hz F/F RESET bit by executing the IO output instruction designated [C_N = 5] in the operand. This F/F output is read in the data memory when the IO input instruction designated [C_N = 5] in the operand is executed.

Since the 2 Hz timer F/F is automatically set at intervals of 500 ms, it can be used for ordinary clock count.

The 2 Hz timer F/F can be reset only by 2 Hz F/F RESET bit, therefore, if data "1" can not be set to the 2 Hz RESET bit within the 500 ms period, a count error is caused and a correct time may not be obtained.

Note 42: When the power source is applied or after the CKSTP instruction was executed, the state of 2 Hz timer F/F output becomes uncertain.



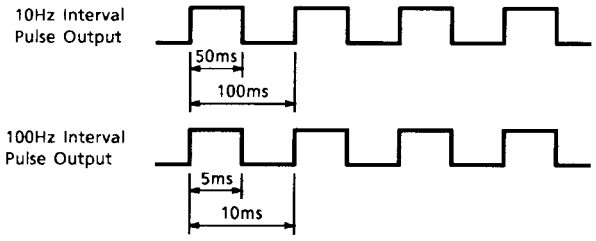
t < 500 ms

Note 43: Set

Note 44: Reset

3. 10 Hz/100 Hz Interval Pulses (ϕK45)

10 Hz interval pulse is a 100 ms period, 50% duty pulse, and 100 Hz interval pulse is a 10 ms period, 50% duty pulse and both are output to 10 Hz and 100 Hz bits. These pulses are read in the data memory when the IO input instruction designated [C_N = 5] in the operand is executed. These outputs have no flip-flop and are available for counting of muting time, and scanning time of tuning, etc.



4. CLOCK RESET Bit (ϕL45)

Whenever data "1" is set to this bit, time base below 50 Hz is reset. (10 Hz interval pulse is also reset but 100 Hz interval pulse is not reset.)

This bit is used for adjustment of clock time. Accuracy of clock at the time is +0.02/−0 s.

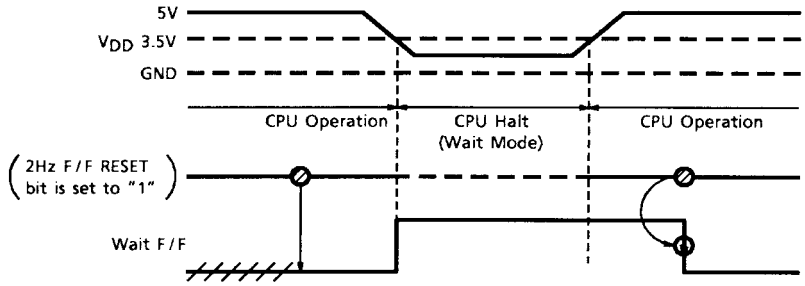
5. Wait F/F Bit (ϕK45)

IF the power supply voltage at the V_{DD} terminal dropped below 2.5~3.5 V during CPU operation, CPU comes to halt to prevent its malfunction at a timing when voltage drops below 2.5~3.5 V (wait mode).

The Wait F/F is set under this state, and when voltage at the V_{DD} terminal rises above 3.5 V, CPU restarts to run.

Therefore, if Wait F/F bit data was read in the data memory by executing the KEY input instruction designated [C_N = 5] in the operand and Wait F/F bit was set to "1", the initialization, clock correction, etc. shall be performed when necessary.

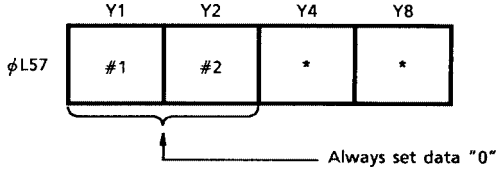
Wait F/F bit is also reset when "1" is set to 2 Hz F/F RESET bit.



Note 45: In the wait mode, the inner data just before the wait mode are retained and no instruction can be executed.

6. TEST Port (ϕL57)

This TEST Port is an internal port for testing function of device. This port is accessed by executing the KEY output instruction designated [C_N = 7] in the operand. In case of ordinary Program, data "0" shall be always set.



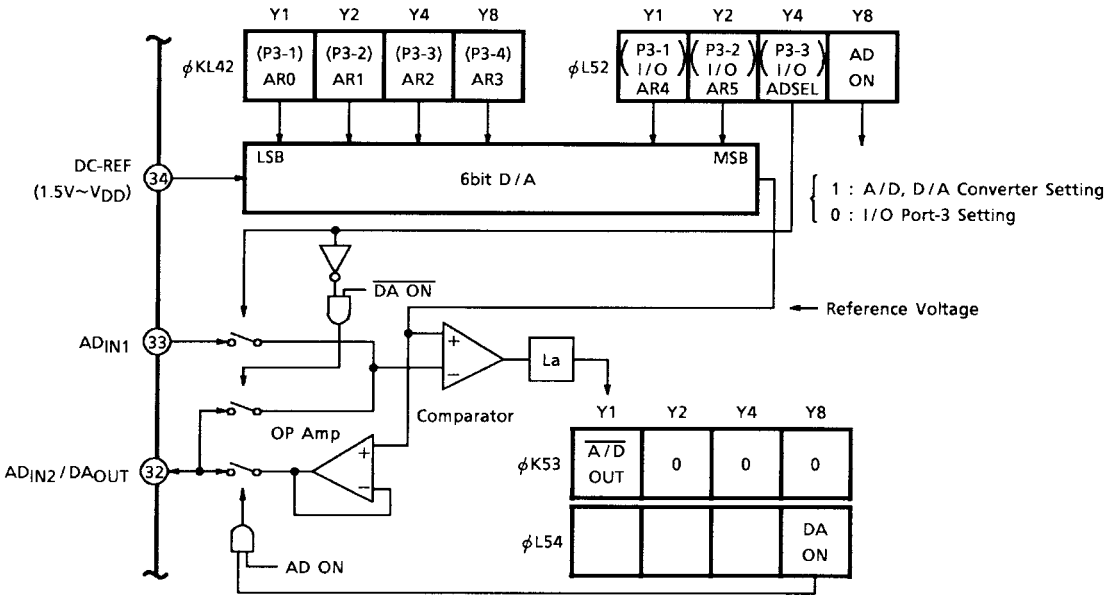
A/D and D/A Converters

The TC9321F has built-in programmatic sequential comparison type 6 bit A/D and D/A converters. 3 I/O port terminals are used for the A/D and D/A converters, which are selected by AD ON bit.

When data "1" is set to AD ON bit, P3-1 is switched to the reference voltage input (DC-REF), P3-2 to the analog voltage input (AD_{IN1}), and P3-3 to the analog voltage input/output (AD_{IN2}/DA_{OUT}).

In this case, 4 bits of I/O port-3 output side latch, (ϕL42) and 3 bits of I/O Control Port-3 output side latch (ϕL52) become A/D and D/A converter control data ports.

The A/D, D/A converter consists of 2 6 bit D/A converter, comparator, operational amplifier, and control circuit.



Construction of A/D, D/A Converters

Note 46: After system reset, AD ON bit, DA ON bit, ADSEL bit, AR5 bit are all reset to "0".

Note 47: The 6 bit D/A circuit for generating reference voltage is commonly used for the A/D converter and D/A converter.

1. A/D Converter

The A/D converter is of 2 channel multiplex type and can be used for field strength measurement, analog voltage level detection, etc.

When AR0~AR3 bits data (φL42) are set after setting of AD ON bit, ADSEL bit, and AR4/AR5 bits (φL52) data, comparison voltage corresponding to AR0~AR5 data is compared with input voltage (AD input) in the A/D converter, and the result of this comparison is stored in the comparator output latch.

This comparison result is output to the $\overline{\text{AD OUT}}$ Port (φK53), and this data is read in the data memory when the KEY input instruction designated [C_N = 3] in the operand is executed.

The relation between input voltage and comparison voltage, and the result of comparison to be output is as follows:

$\overline{\text{AD OUT}}$ = "0" when input voltage > comparison voltage

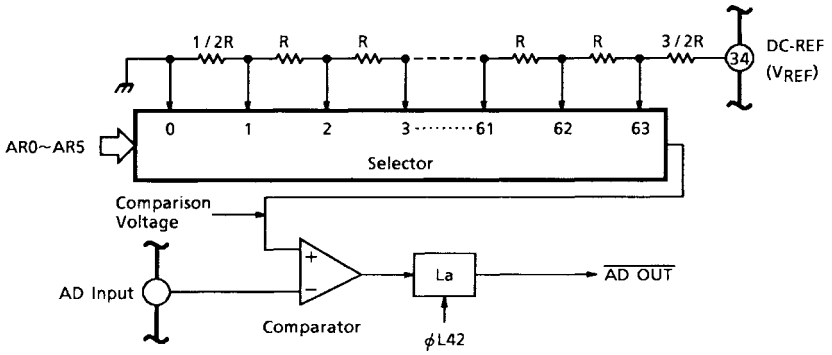
$\overline{\text{AD OUT}}$ = "1" when input voltage < comparison voltage

Further, comparison voltage is caluculated according to the following equation:

$$\text{Comparison Voltage} = V_{REF} \times \frac{n - 0.5}{64} \quad (n \text{ is AR0~AR5 data value [decimal number] } 63 \geqq n \geqq 1)$$

AD input of AD_{IN1} or AD_{IN2} is selected according to the contents of ADSEL bit.

That is, AD_{IN2} input is selected when ADSEL bit is "0" and AD_{IN1} input is selected when ADSEL bit is "1".



Construction of A/D Converter

AD ON	DA ON	AD SEL	AD Input
1	0	0	AD_{IN2}
1	0	1	AD_{IN1}
1	1	*	Invalid

Note 48: Whenever AR0~AR3 data are set, comparison carried out.

Note 49: *: Don't care.

Note 50: In case of A/D converter used, DA ON bit shall be set to "0".

Even if DA ON bit is set to "1" and the comparing operation is carried out (data is set to AR0~AR3 bit), the contents of $\overline{\text{AD OUT}}$ become indefinite.

Note 51: String resistor of A/D converter is set at values lower by 1/2 LSB.

2. D/A Converter

The D/A converter is available for control of electronic volume which is controlled by analog voltage, etc.

In case of D/A converter used, when "1" is set to both AD ON bit and DA ON bit, D/A output corresponding to AR0~AR5 data is output from the DA output terminal.

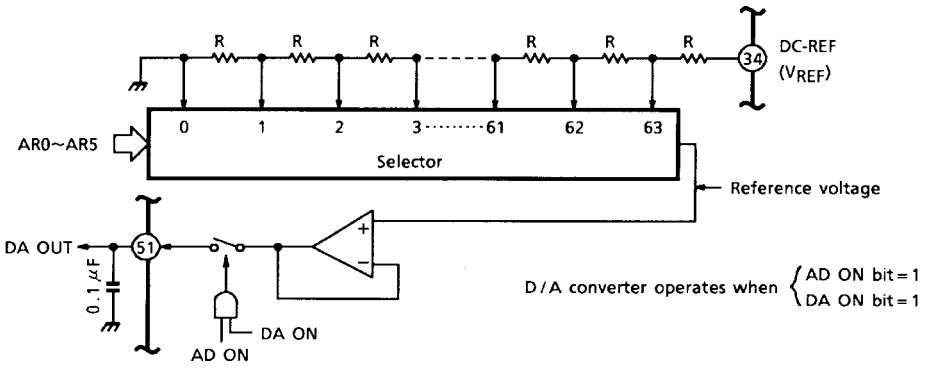
When AR0~AR5 data is changed successively, output ripple is generated at time of carry to AR4 because I/O memory layout differs between AR0~AR3 data and AR4~AR5 data.

Therefore, at time of carry to AR4, the carry shall be performed after making output to high impedance by setting DA ON bit to "0". In this case, a voltage holding capacitor is connected to the output because of being high impedance.

Further, D/A output voltage is calculated according to the following equation:

$$\text{D/A output voltage} = V_{REF} \times \frac{n}{64} \quad (n \text{ is AR0~AR5 data [decimal number]}\ 63 \geqq n \geqq 1)$$

When the A/D converter and the D/A converter are simultaneously used, perform A/D conversion with D/A ON bit set at "0" and thereafter, output D/A analog voltage by setting DA ON bit at "1".



Construction of D/A Converter

Note 52: Add an external buffer circuit to the D/A output if necessary, although it has a built-in buffer.

Note 53: D/A output range is 0 V~V_{DD} − 1.0 V and so, be careful when $V_{REF} = V_{DD}$.

Note 54: DA ON bit becomes invalid when AD ON bit is "0".

Note 55: Voltage value of string resistor of D/A converter is a 64 divided V_{REF} value.

Serial Interface

I/O Port-2 can be programmatically switched to the serial interface. The serial interface is a serial I/O dedicated for powerful control of a group of peripheral optional ICs.

When switched to the serial interface, 4 terminals of I/O port-2 are switched to SI, SO, CK and STB terminals. These terminals are connected to external device with 4 serial bus lines for data transfer.

By connecting peripheral optional ICs on these bus lines according to system, functions can be expanded.

Various external devices such as I/O port extension IC, static display driver, etc. are available.

Serial data transfer is carried out by executing the SIO instruction and during this instruction execution time (55.5 μs), all data transfer is completed.

It is possible to handle all ports of external devices simply as inner ports that are handled through execution of other I/O instructions. Further, two kinds of serial transfer are programmatically selectable.

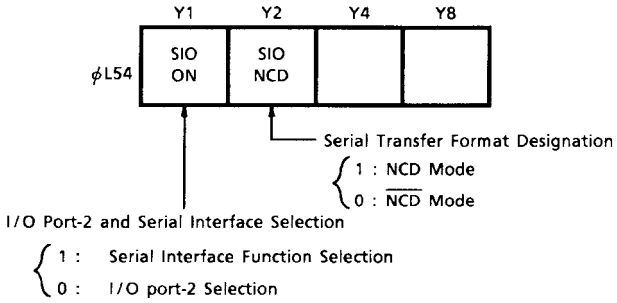
1. Serial Transfer Control Port (ϕKL53)

I/O Port-2 and the serial interface are selected and controlled by the KEY output instruction designated [C_N = 4] in the operand (ϕL54).

When SIO ON bit is set to "0", I/O port-2 is selected and when "1" is set, the serial interface is selected. Further, two kinds of the serial transfer formats are selectable by SIO NCD bit.

When SIO NCD bit is set to "0", $\overline{\text{NCD}}$ mode serial transfer format is selected.

In the $\overline{\text{NCD}}$ Mode, Port Code No. designated in the operand of SIO is serially transferred together with data. When "1" is set, the NCD Mode results. In the NCD mode, Code No. is not transferred and data only are exchanged. (C_N value in the operand of SIO instruction becomes don't care.)



Note 56: After system reset, the contents of SIO ON bit and SIO NCD bit are automatically cleared to "0".

(I/O port-2 has been selected.)

Note 57: In the NCD mode, P2-1/SI and P2-4/STB terminal is selected P2-1 and P2-4.

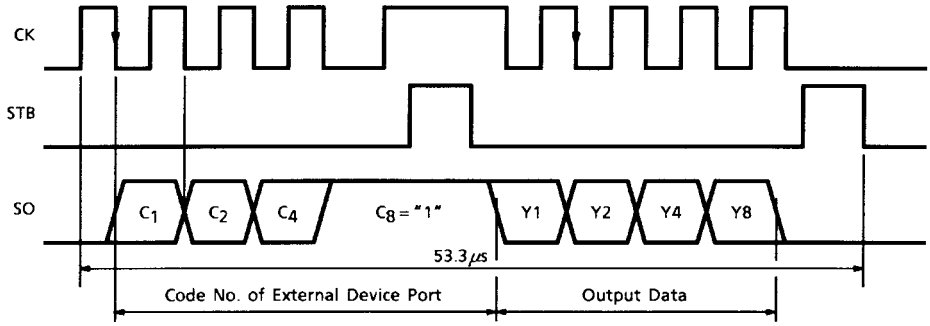
It can uses as normal I/O port.

Note 58: In the NCD mode, SO terminal becomes data I/O structure. It must select input/output of SO terminal by PORT2-2 I/O CONTROL bit (ϕL51) before executing SIO instruction.

Note 59: It is inhibited to program by executing SIO input instruction next to SIO output instruction. If in case of programming to SIO input instruction after SIO output instruction, NOOP instruction (etc.) is inserted between SIO output and SIO input instruction.

2. Serial I/O Timing Chart

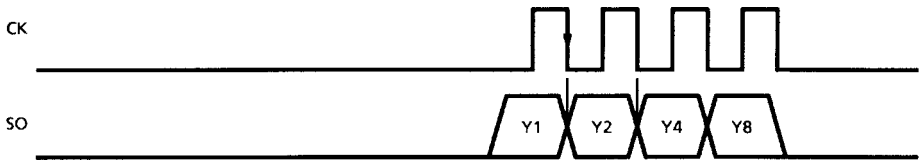
- $\overline{\text{NCD}}$ mode output timing



At the timing shown in the above chart, Code No. (C_1~C_8: 4 bits) of the output port of destination device to which data is sent and data (Y1~Y8: 4 bits) are output serially from LSB synchronizing with the fall timing of CK signal.

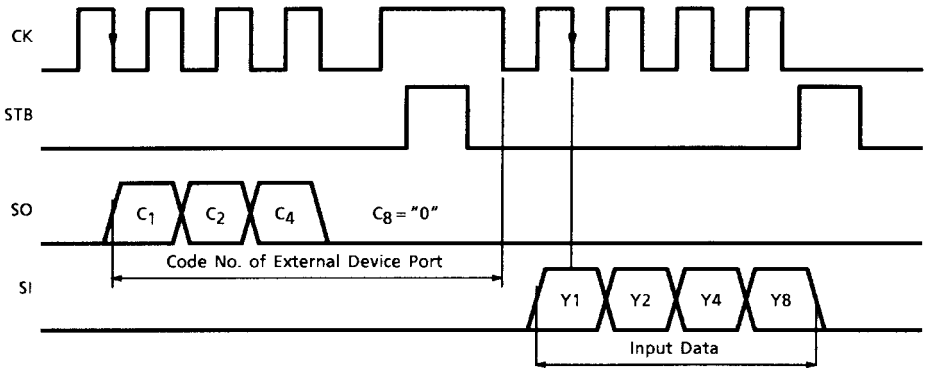
Note 60: When excuting the SIO output instruction ($\overline{\text{NCD}}$ mode), C_8 bit of code No. becomes "1".

- NCD mode output timing



Serial output in the NCD Mode will be 4 bit data only. Further, STB output is always fixed at "L" level.

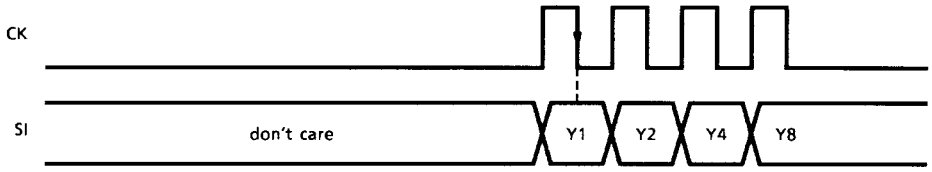
- $\overline{\text{NCD}}$ mode input timing



When Code No. (C_1~C_8: 4 bits) of the input port of destination device is output from the SO terminal at the timing shown in the above timing chart, the contents (Y1~Y8: 4 bits) of that input port are serially input into the SI terminal from LSB. SO data is output synchronizing with the fall timing of CK signal and similarly, SI data is input synchronizing with the fall timing of CK signal.

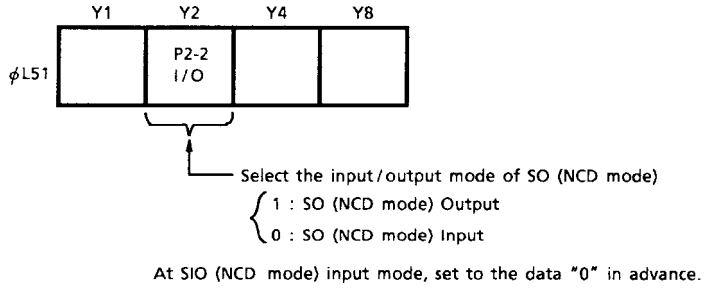
Note 61: When executing the SIO input instruction ($\overline{\text{NCD}}$ mode), C_8 bit code No. becomes "0".

- NCD mode input timing



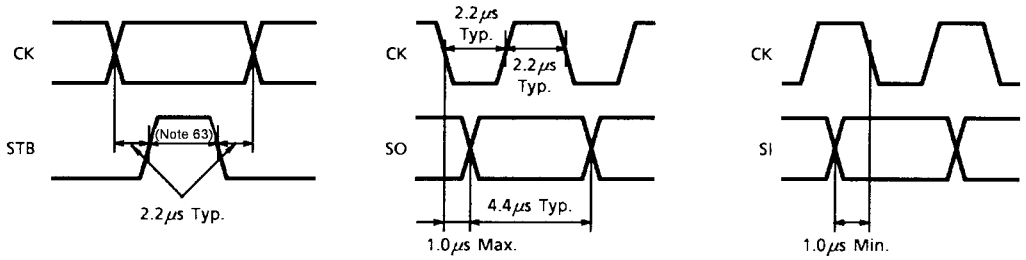
At time of serial input in the NCD Mode, STB output and SO output are always fixed at "L" level. SI data is input synchronizing with the all timing of CK signal.

Note 62: In NCD mode, SO terminal becomes data I/O structure. It must be set the data "0" to PORT2-2 I/O CONTROL bit before executing SIO input instruction (NCD mode) and SO terminal is set to input mode.



3. Serial Timing Pulse Width

Pulse width of each timing signal is shown below.



Note 63: 4.4 μs typ.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	400	mW
Operation temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

Electrical Characteristics (unless otherwise specified, Ta = –40~85°C, V_{DD} = 4.5~5.5 V)

CPU Operation/PLL Stop

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD1}	—	PLL Stop/CPU Operation	3.5	5.0	5.5	V
Memory holding voltage range	V_{HD}	—	Cristal oscillation stop	2.0	~	5.5	V
Operating power supply current	I_{DD1}	—	PLL Stop/CPU Operation V_{DD} = 5 V, Ta = 25°C	—	0.7	1.5	mA
Memory holding power supply circuit	I_{HD1}	—	V_{DD} = 5 V, Cristal oscillation stop	—	0.1	10	μA
	I_{HD2}	—	V_{DD} = 2 V, Cristal oscillation stop	—	—	5	
Crystal oscillation frequency	f_{XT}	—	—	—	7.2	—	MHz

CPU/PLL Operation

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD2}	—	CPU/PLL Operation	4.5	5.0	5.5	V
Operating power supply current	I_{DD2}	—	CPU/PLL Operation (FM_{IN} = 140 MHz), V_{DD} = 5 V Ta = 25°C	—	10	25	mA

PLL Operating Frequency Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN} (FM_H mode)	f_{FMH}	—	V_{IN} = 0.5 V_{p-p}	30	~	185	MHz
FM_{IN} (FM_L mode)	f_{FML}	—	V_{IN} = 0.3 V_{p-p}	30	~	140	MHz
AM_{IN} (HF mode)	f_{HF}	—	V_{IN} = 0.3 V_{p-p}	1	~	40	MHz
AM_{IN} (LF mode)	f_{LF}	—	V_{IN} = 0.3 V_{p-p}	0.5	~	20	MHz
IF_{IN1}	f_{IF1}	—	V_{IN} = 0.3 V_{p-p}	0.1	~	20	MHz
IF_{IN2}	f_{IF2}	—	V_{IN} = 0.3 V_{p-p}	0.1	~	20	MHz

PLL Operating Input Amplitude Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN} (FM_H mode)	V_{IN} (FM_H)	—	f_{IN} = 30~185 MHz	0.5	~	V_{DD} − 0.5	V_{p-p}
FM_{IN} (FM_L mode)	V_{IN} (FM_L)	—	f_{IN} = 30~140 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
AM_{IN} (HF mode)	V_{IN} (HF)	—	f_{IN} = 1~40 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
AM_{IN} (LF mode)	V_{IN} (LF)	—	f_{IN} = 0.5~20 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
IF_{IN1}	V_{IN} (IF_{IN1})	—	f_{IN} = 0.1~20 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
IF_{IN2}	V_{IN} (IF_{IN2})	—	f_{IN} = 0.1~20 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}

P1-1~P1-4, P2-1~P2-4 (SO, CK, STB), P3-1~P3-3, P4-1~P4-4, T0~T7, OT1~OT4 Output Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 4.5 V, V_{DD} = 5 V	−1.0	−3.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.5 V, V_{DD} = 5 V	1.0	3.0	—	

P5-1~P5-4, P6-1~P6-4, P7-1~P7-4, P8-1~P8-2 Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH2}	—	V_{OH} = 4.5 V, V_{DD} = 5 V	−0.1	−3.0	—	mA
	"L" level	I_{OL2}	—	V_{OL} = 0.5 V, V_{DD} = 5 V	2.5	7.5	—	

$\overline{INH}$ Input Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
$\overline{INH}$ input voltage	"H" level	V_{IH2}	—	—	V_{DD} × 0.85	~	V_{DD}	V
	"L" level	V_{IL2}	—	—	0	~	V_{DD} × 0.4	
Input leak current	"H" level	I_{IH1}	—	V_{IH} = V_{DD} = 5.5 V	—	—	2	μA
	"L" level	I_{IL1}	—	V_{IL} = 0 V, V_{DD} = 5.5 V	—	—	2	

Key Input Port (K0~K3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH1}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" level	V_{IL1}	—	—	0	~	V_{DD} × 0.3	
Pull-down resistance		R_{IN1}	—	V_{IH} = V_{DD} = 5 V Ta = 25°C	50	100	200	kΩ

$\overline{INI}$, IN1, IN2, P1-1~P1-4, P2-1~P2-4 (SI, SO), P3-1~P3-3, P4-1~P4-4 Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH1}	—	—	$V_{DD} \times 0.7$	~	V_{DD}	V
	"L" level	V_{IL1}	—	—	0	~	$V_{DD} \times 0.3$	
Input leak current	"H" level	I_{IH1}	—	$V_{IH} = V_{DD} = 5.5$ V	—	—	2	μA
	"L" level	I_{IL1}	—	$V_{IL} = 0$ V, $V_{DD} = 5.5$ V	—	—	2	

P5-1~P5-4, P6-1~P6-4, P7-1~P7-4, P8-1~P8-2 Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH3}	—	—	$V_{DD} \times 0.7$	~	V_{DD}	V
	"L" level	V_{IL3}	—	—	0	~	$V_{DD} \times 0.12$	
Input leak current	"H" level	I_{IH1}	—	$V_{IH} = V_{DD} = 5.5$ V	—	—	±2	μA
	"L" level	I_{IL1}	—	$V_{IL} = 0$ V, $V_{DD} = 5.5$ V	—	—	±2	

DO1, DO2 Outputs

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	$V_{OH} = 4.5$ V, $V_{DD} = 5$ V	−1.0	−3.0	—	mA
	"L" Level	I_{OL1}	—	$V_{OL} = 0.5$ V, $V_{DD} = 5$ V	1.0	3.0	—	
Tri-state leak current		I_{TL}	—	$V_{TLH} = V_{DD} = 5.5$ V $V_{TLL} = 0$ V	—	—	±1	μA

A/D, D/A Converter (DC·REF, A/D_{IN1}, A/D_{IN2}, D/A_{OUT})

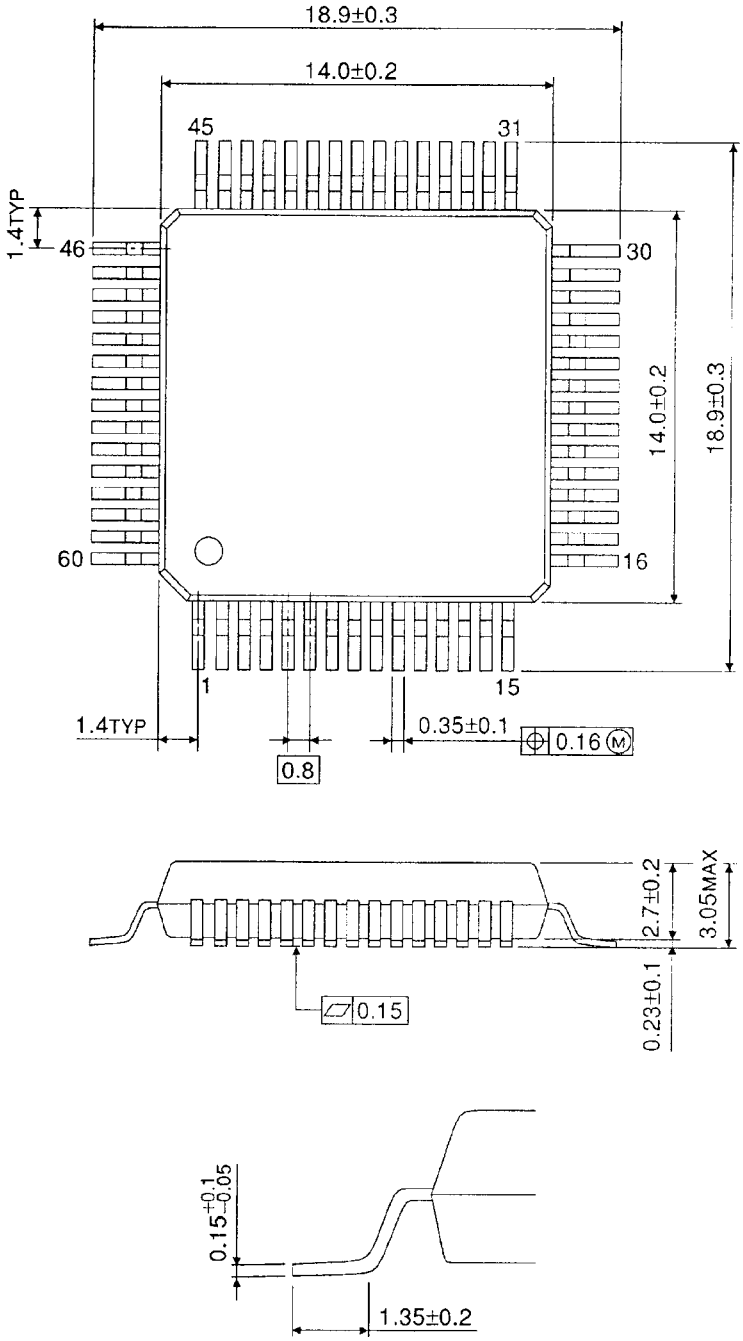
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analogue input voltage range	V_{ADI}	—	AD_{IN1}, AD_{IN2}	0	~	V_{DD}	V
Analogue reference voltage range	V_{REF}	—	DC·REF	1.5	~	V_{DD}	V
Resolution	V_{RES}	—	—	—	—	6	bit
Analogue reference voltage input current	I_{REF}	—	DC·REF, Ta = 25°C $V_{IH} = V_{DD} = 5$ V	—	0.5	1.0	mA
Analogue output voltage range	V_{DAO}	—	DA_{OUT}	0	~	$V_{DD} - 1.0$	V
Analogue output voltage deviation	ΔV_{DA}	—	$I_{DA} = \pm 100$ μA $V_{DD} = 5$ V, Ta = 25°C	—	±50	±150	mV
Conversion total error	—	—	—	—	±0.5	±1.5	LSB

Other

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN}, AM_{IN}, IF_{IN} input feedback resistance	R_{f1}	—	$V_{DD} = 5$ V, Ta = 25°C	250	500	1000	kΩ
X_T input feedback resistance	R_{f2}	—	$V_{DD} = 5$ V, Ta = 25°C	500	1000	2000	kΩ
TEST input pull-down resistance	R_{IN2}	—	$V_{IH} = V_{DD} = 5$ V Ta = 25°C	15	30	60	kΩ

Package Dimensions

QFP60-P-1414-0.80D Unit : mm



Weight: 1.10 g (typ.)

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