CEL

uPG2301TQ

InGaP / GaAs HBT PA IC

for Bluetooth Class1

Application Information

August 2004

NEC
A Business Partner of NEC Compound Semiconductor Devices, Ltd.

CEL Power Amplifier for Bluetooth Class 1

uPG2301TQ

Features

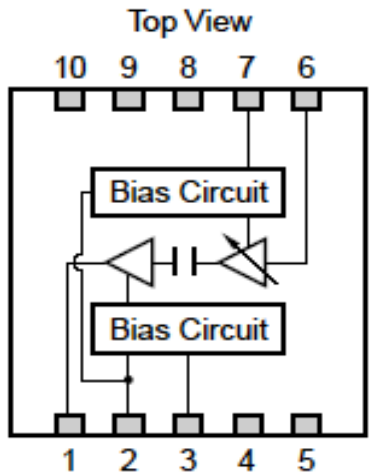
- Low Current Consumption
- 20dB Variable Gain Control
- Shut Down Function

Application

- Bluetooth Class 1

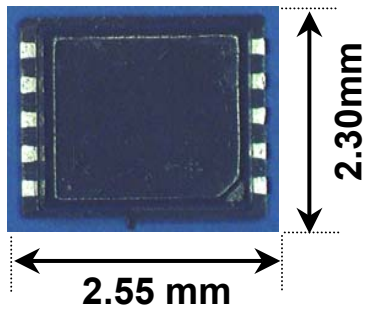
RF Performance

- Operating Frequency: 2.4 to 2.5GHz
- Supply voltage: $V_{CC1,2} = V_{bias} = 3.3V$, $V_{enable} = 2.9V$
- Output Power : 23dBm typ. @V_{cont} = 2.5V, Pin=+4dBm
- Gain Control Range: 23dB typ. @V_{cont} = 0 to 2.5V, Pin=+4dBm
- Operating Current: 120mA typ. @ Pin=+4dBm, Vcont = 2.5V



In Mass Production

10pinTSON PKG



Thickness: 0.6mm MAX
Lead Pitch: 0.4mm

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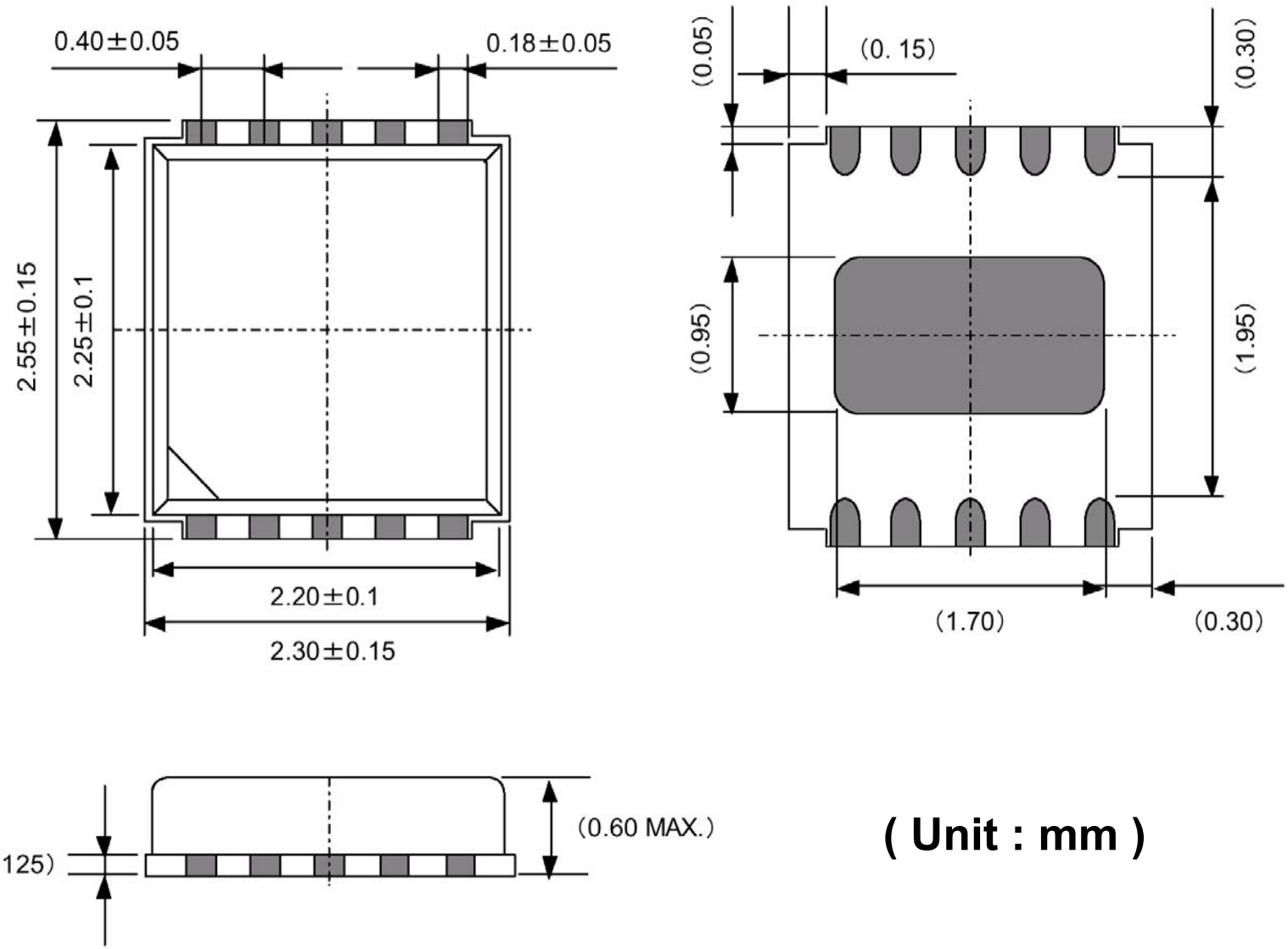
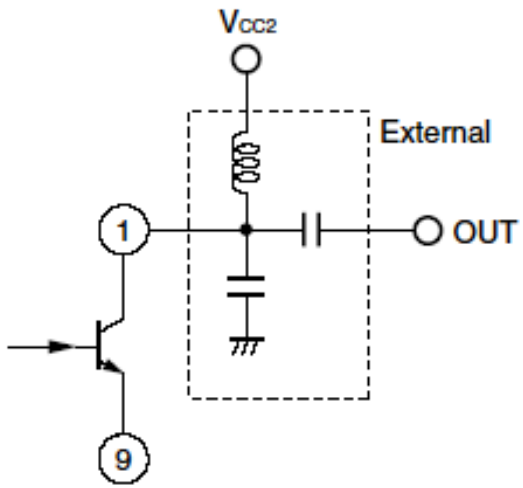
Package Dimensions

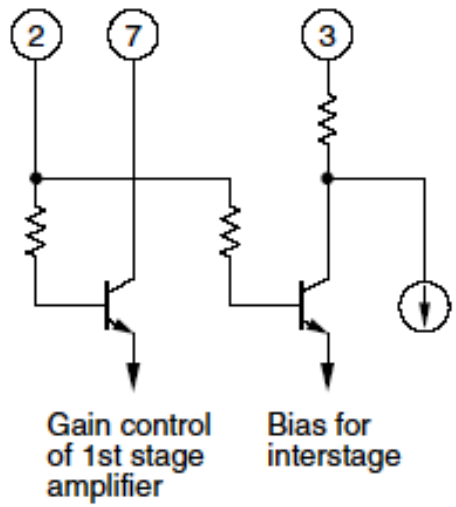


(Unit : mm)

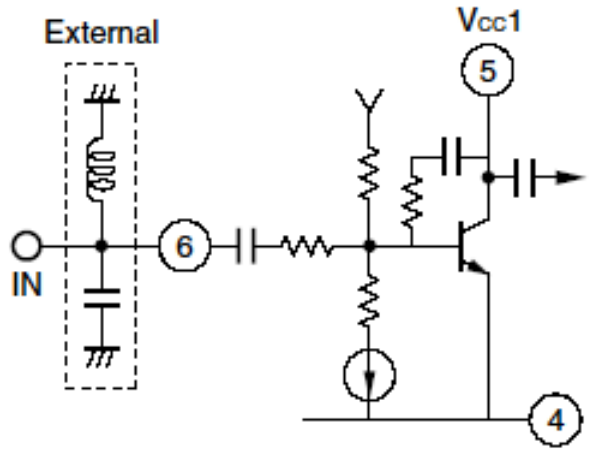
Pin Functions and Internal Circuit (1)

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)	Function and Applications	Internal Equivalent Circuit
1	OUT/V_{CC2}	2.7 to 3.6	–	Supply voltage and output pin of final stage amplifier. This collector output pin should supply voltage through external inductor, optimize external LC value for matching impedance and couple with capacitor to obtain output power.	
9	GND	0	–	GND pin of final stage amplifier. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	

Pin Functions and Internal Circuit (2)

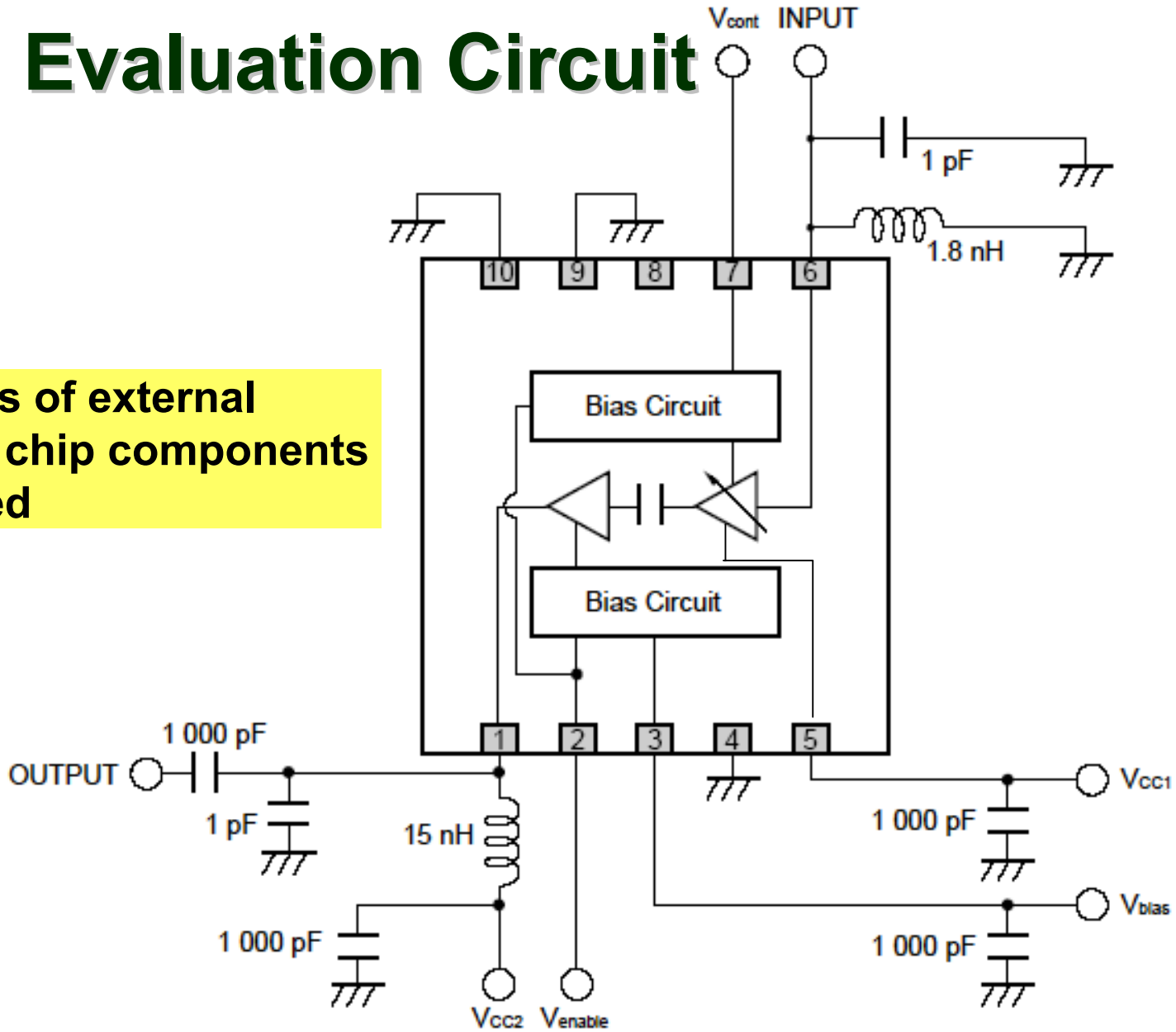
2	V_{enable}	0 to 3.1	–	Enable pin. This pin can control the operation of bias circuit and gain control circuit. The applied voltage should be minimized to shut down the operation. The worst current into this pin is approximately 1 mA.	
3	V_{bias}	2.7 to 3.6	–	Bias pin. Apply voltage to the bias circuit via this pin.	
7	V_{cont}	0 to 3.6	–	Gain control pin of 1st stage amplifier. Since this device is a reverse control type, AGC control voltage should be maximized to get maximum gain. Current into this pin is approximately 0.3 mA.	

Pin Functions and Internal Circuit (3)

4	GND	0	–	GND pin of 1st stage amplifier. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
5	V_{CC1}	2.7 to 3.6	–	Supply voltage pin of 1st stage amplifier. This pin should be externally equipped with bypass capacitor (example: 1 000 pF) to minimize its impedance.	
6	INPUT	–	–	Input pin of RF signal. This port is internally coupled with capacitor for DC blocking. The impedance matching circuit is externally needed.	

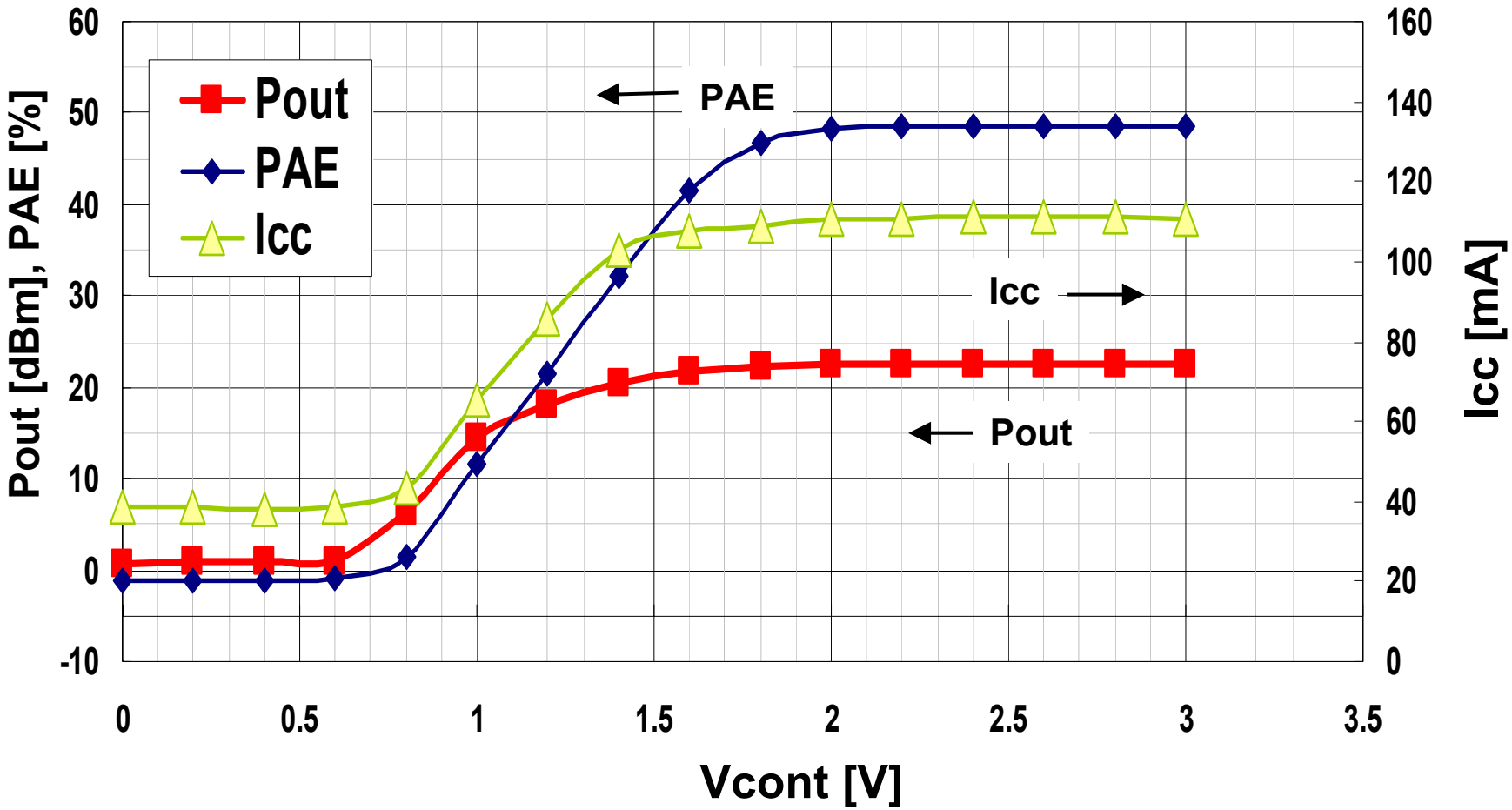
Evaluation Circuit

Only 8 pcs of external 0603 size chip components are needed



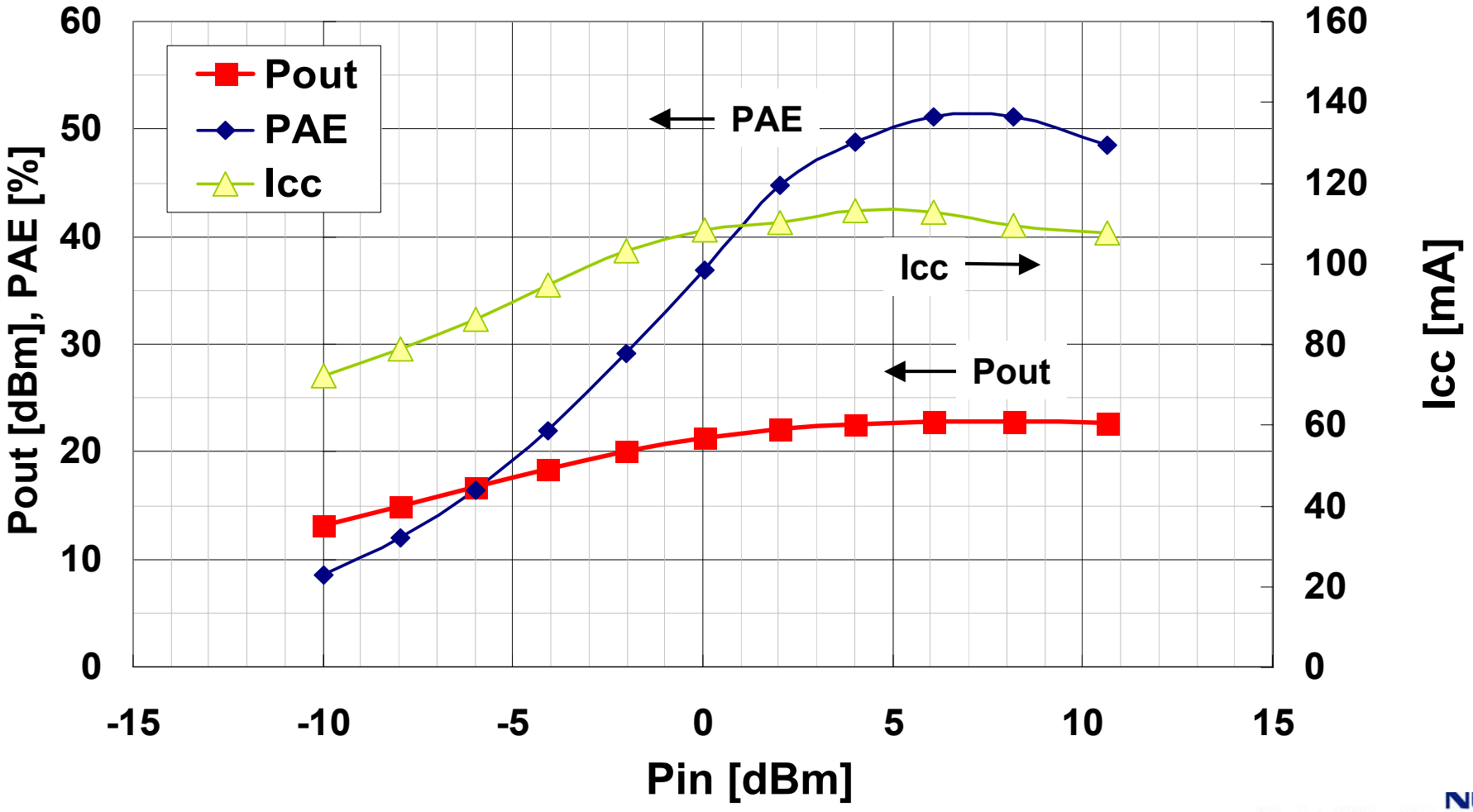
RF Performance of uPG2301TQ (1)

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Venable=2.9V,
Pin=+4dBm, with external input & output matching circuits



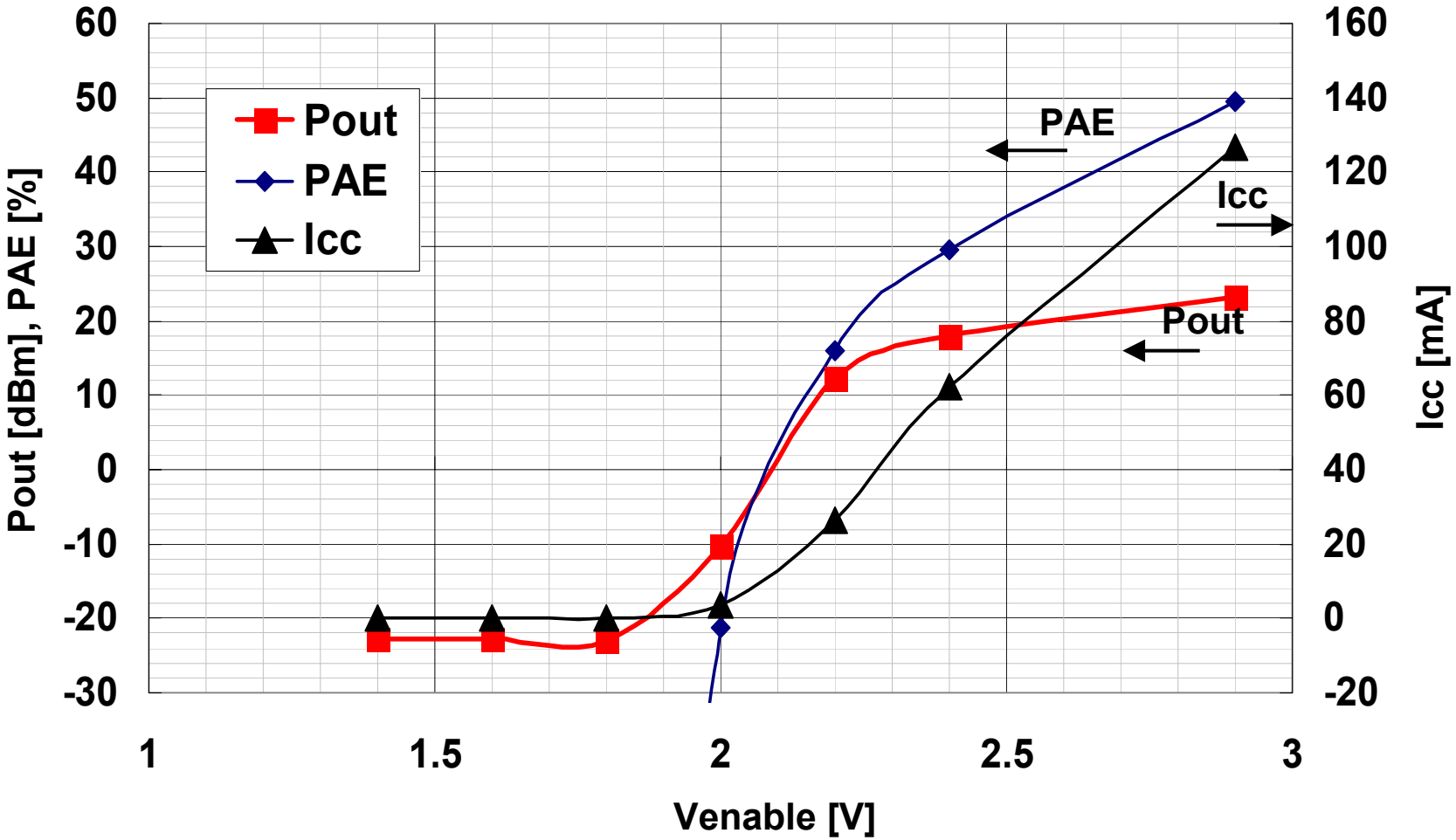
RF Performance of uPG2301TQ (2)

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Venable=2.9V, Vcont=2.5V, with external input & output matching circuits



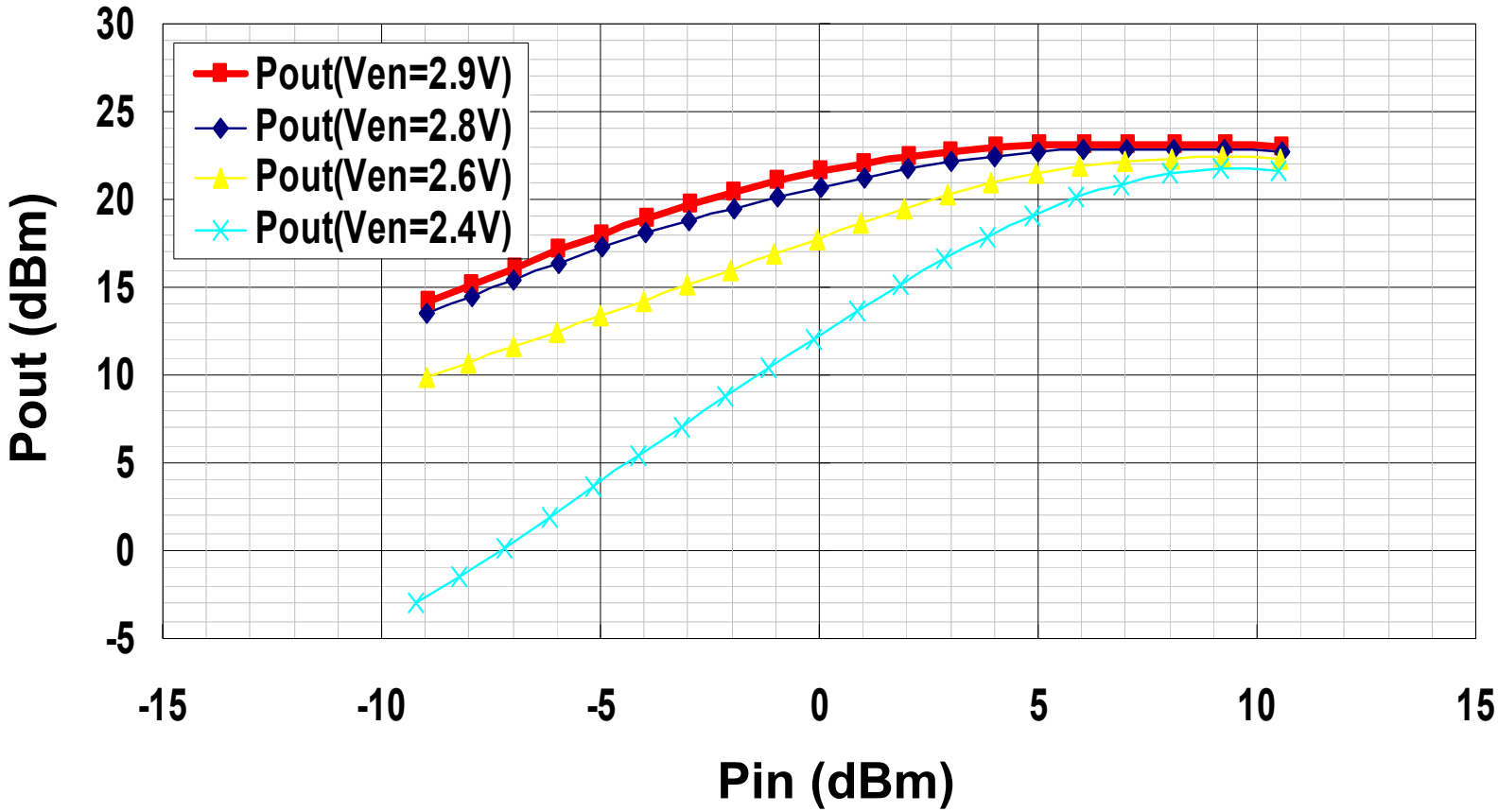
Venable vs. Pout, PAE, Icc Characteristics

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Vcont=2.5V,Pin=+4dBm,
With external input & output matching circuits



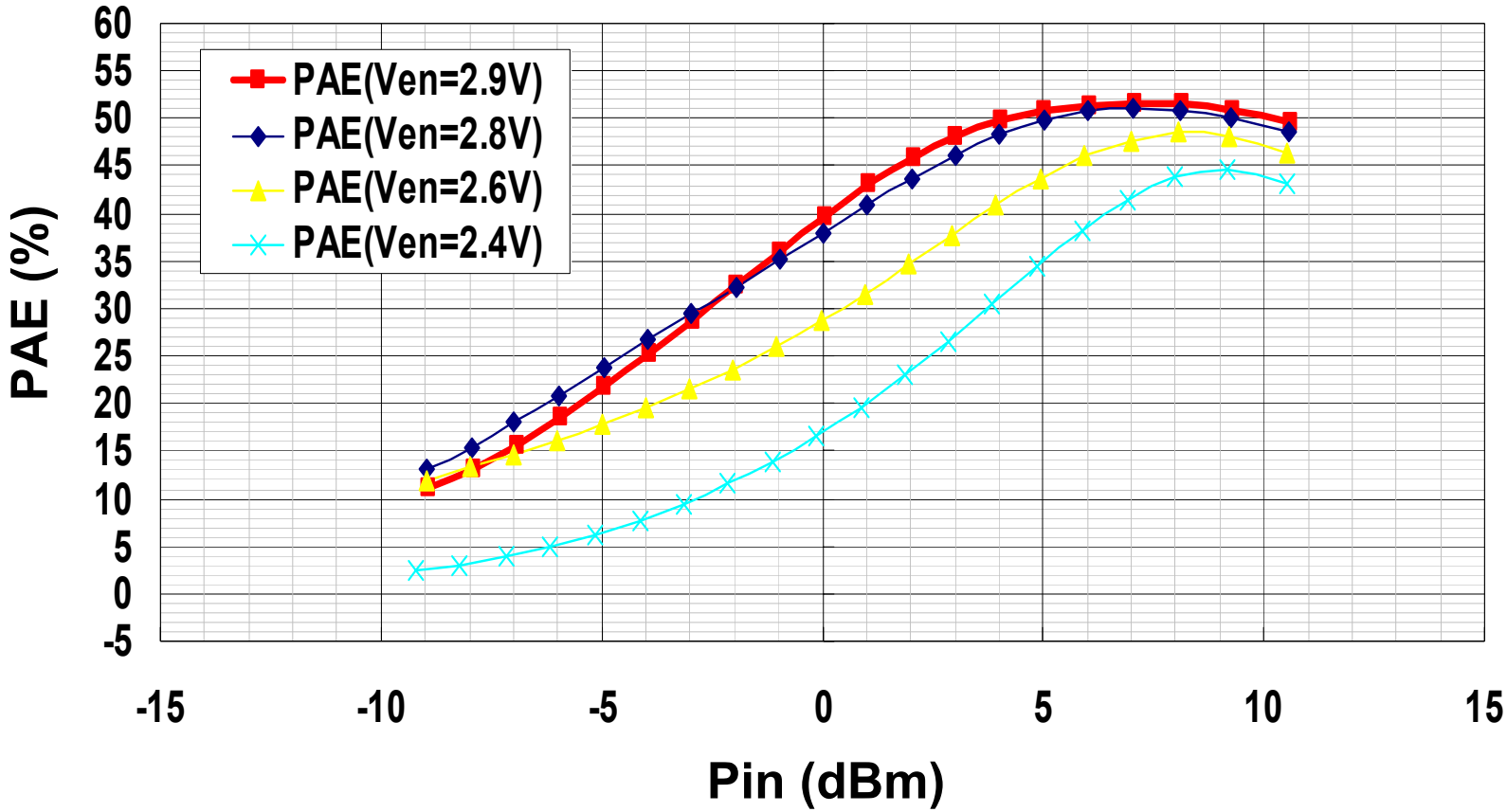
CEL Venable Dependency for Pin vs. Pout

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Vcont=2.5V,
with external input & output matching circuits



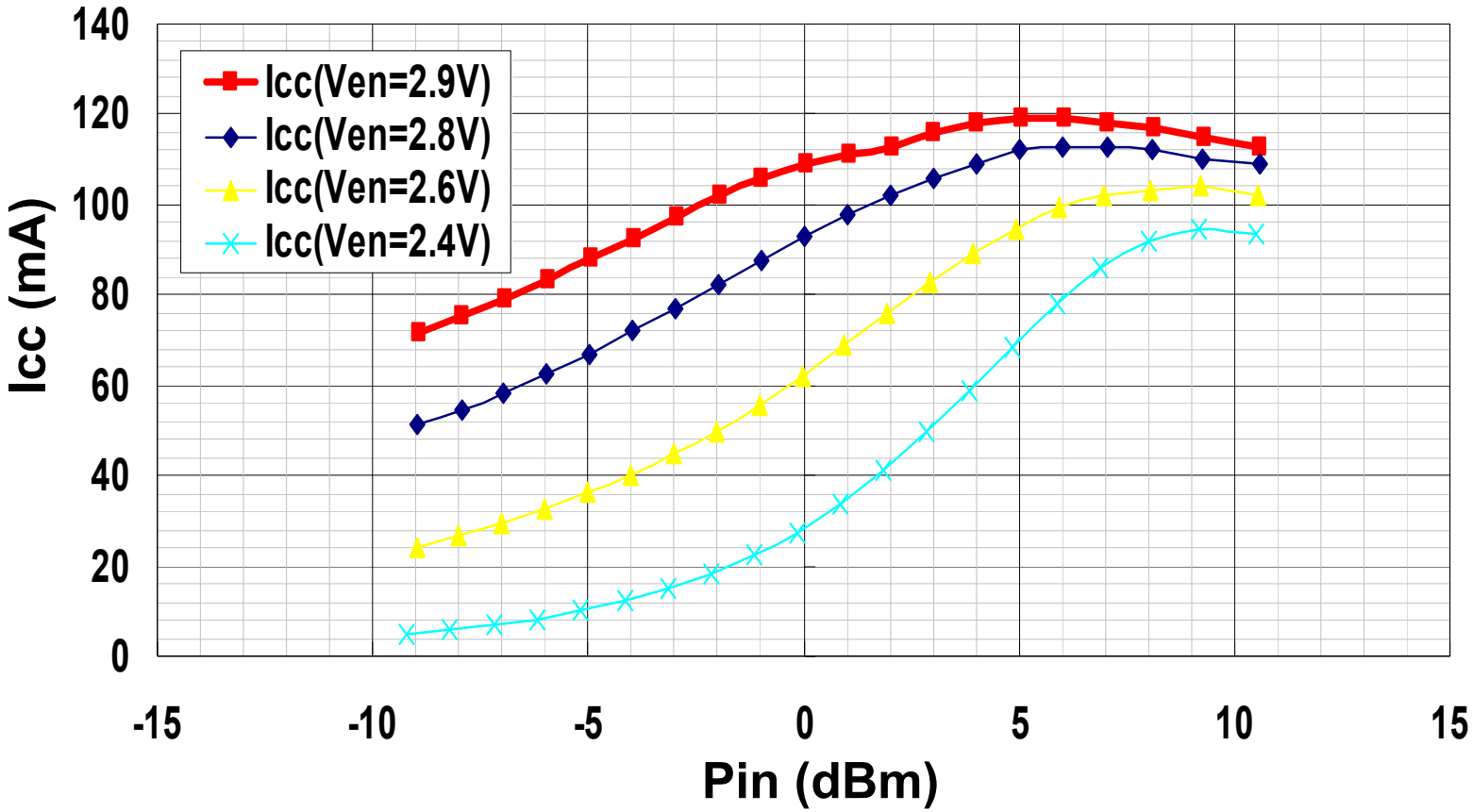
Venable Dependency for Pin vs. PAE

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Vcont=2.5V,
with external input & output matching circuits



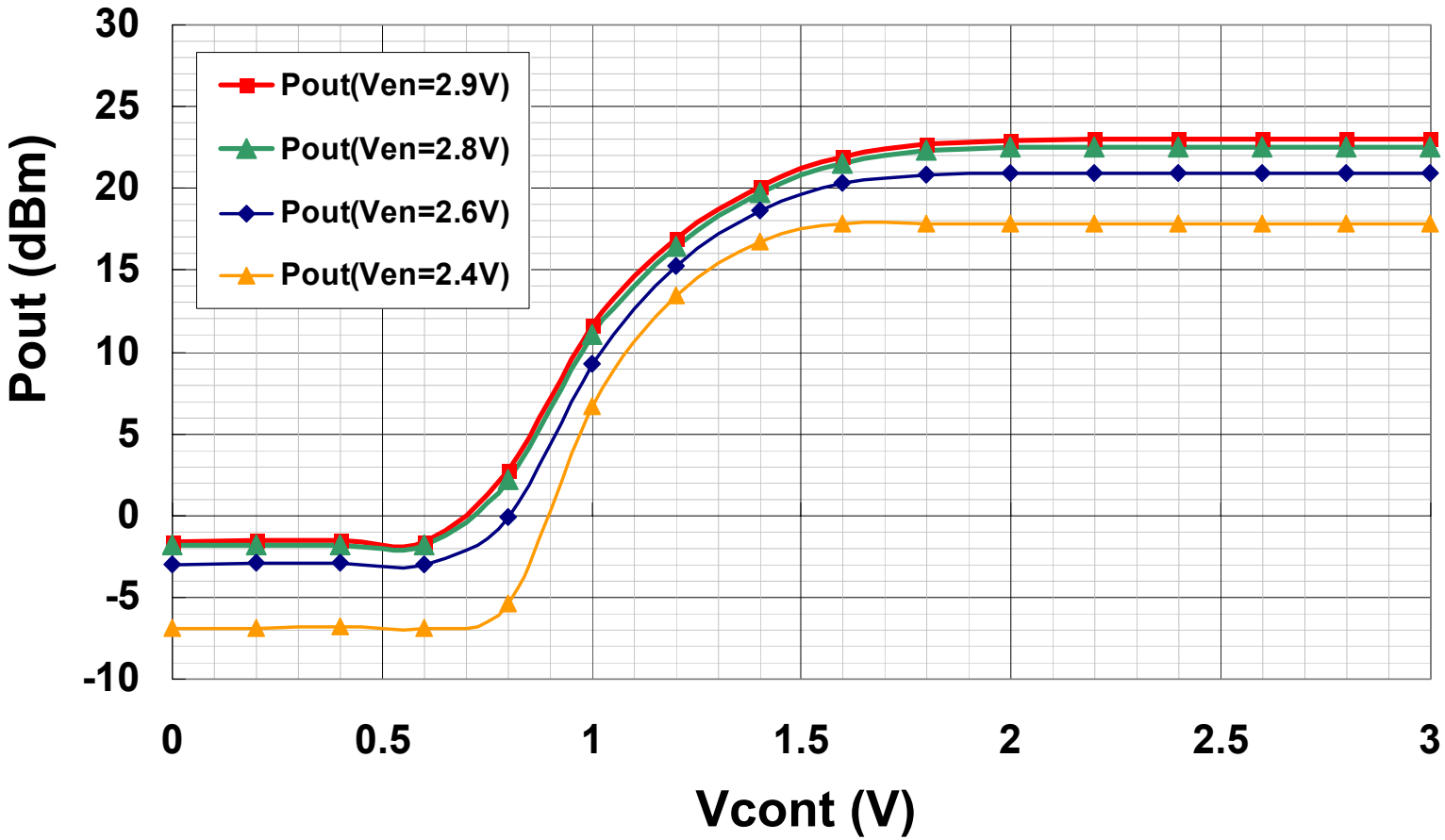
Venable Dependency for Pin vs. Icc

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V,Vcont=2.5V,
with external input & output matching circuits



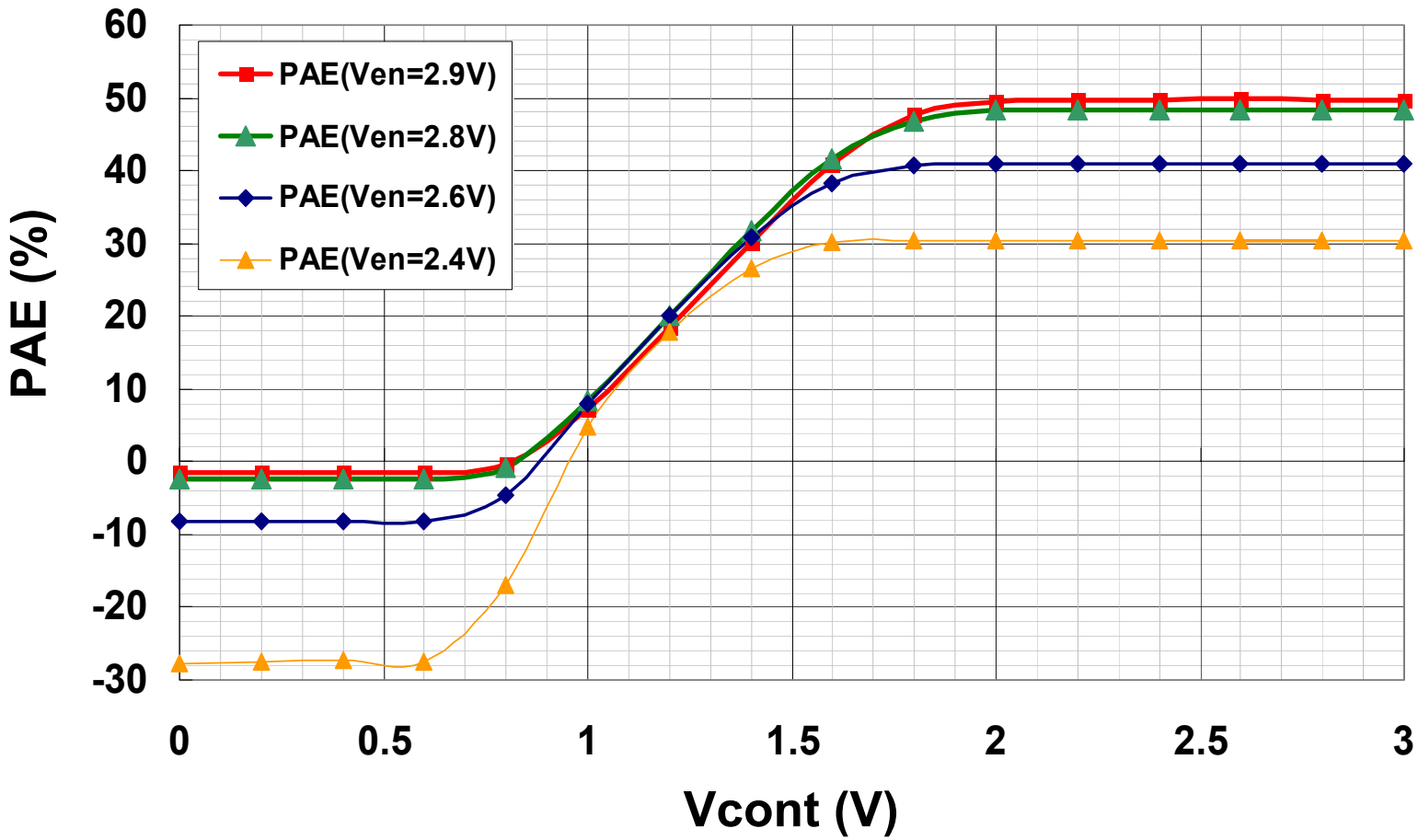
Venable Dependency for Vcont vs. Pout

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V, Pin=+4dBm,
with external input & output matching circuits



Venable Dependency for Vcont vs. PAE

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V, Pin=+4dBm, with external input & output matching circuits



Venable Dependency for Vcont vs. Icc

Test Conditions : f = 2450MHz,Vcc1=Vcc2=Vbias=3.3V, Pin=+4dBm,
with external input & output matching circuits