LED Drivers for Automotive Light

BD8381AEFV-M

General Description

BD8381AEFV-M is a white LED driver with the capability of withstanding high input voltage (50V MAX). It has also an integrated current-mode, buck-boost DC/DC controller to achieve stable operation against high input voltage and to remove the constraint of the number of LEDs in series connection.

The LED brightness is controlled by either linear or PWM signal and is also possible to be controlled even without using a microcomputer, but instead, by means of the built-in PWM brightness signal generation circuit.

Features

- Integrated buck-boost current-mode DC/DC controller
- Built-in CR timer for PWM brightness
- PWM linear brightness
- Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
- LED error status detection function (OPEN/ SHORT)

Applications

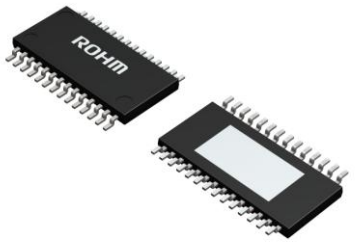
Headlight and Daytime Running Light etc.

Key Specifications

- Input Supply Voltage Range: 5.0V to 30V
- Operating Temperature Range: -40°C to +125°C

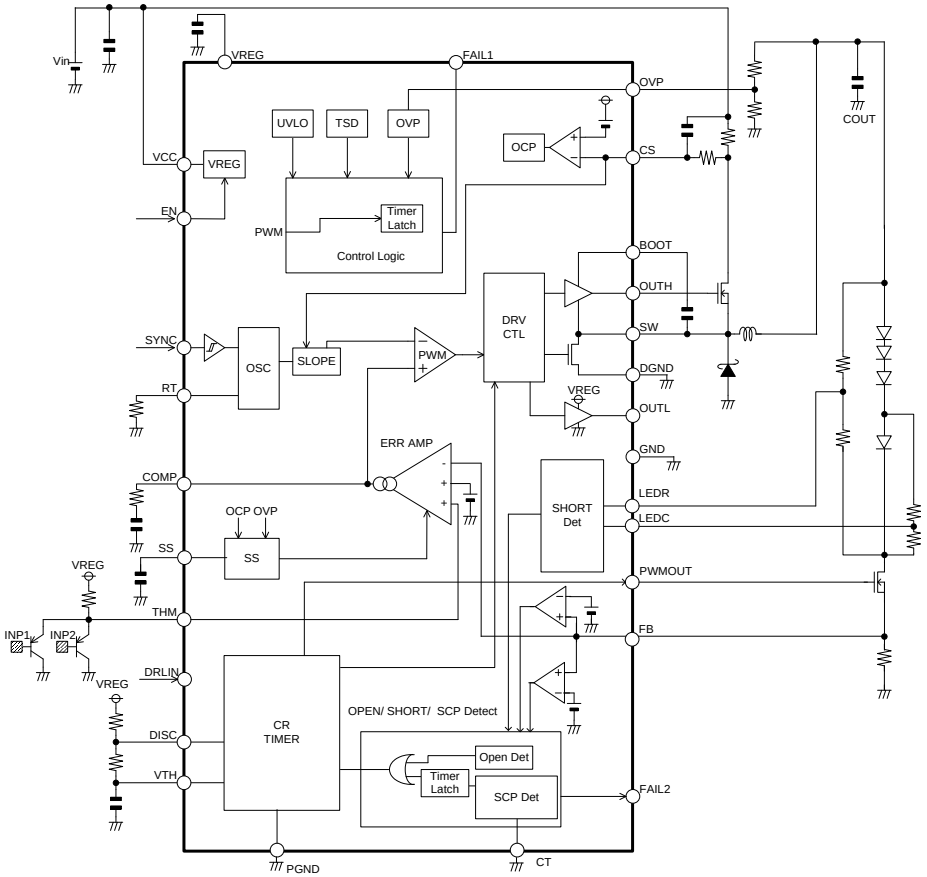
Package

W(Typ) x D(Typ) x H(Max)



HTSSOP-B28
9.70mm x 6.40mm x 1.00mm

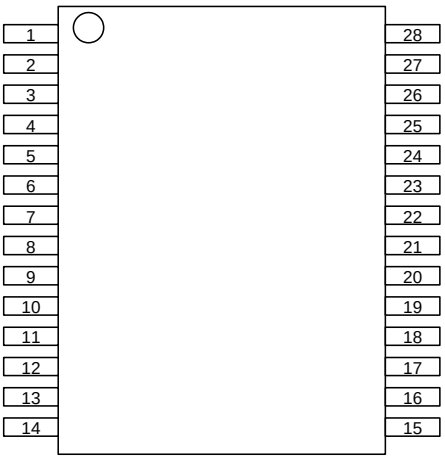
Typical Application Circuit and Block Diagram



○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

(TOP VIEW)



Pin Descriptions

Pin	Symbol	Function
1	COMP	Error amplifier output
2	SS	Soft start setting input
3	VCC	Input power supply
4	EN	Enable input
5	RT	Oscillation frequency-setting resistance input
6	SYNC	External synchronization signal input
7	GND	Small-signal GND
8	THM	Thermally sensitive resistor connection pin
9	FB	ERRAMP FB signal input pin
10	DISC	CR Timer discharge pin
11	VTH	CR Timer threshold pin
12	DRLIN	DRL switch pin (Pulse output setting pin)
13	FAIL1	Failure signal output
14	FAIL2	LED open/short detection signal output
15	OVP	Over-voltage detection input
16	LEDC	LED short detection pin (LED detection side)
17	LEDR	LED short detection pin (Resistor detection side)
18	N.C.	-
19	PGND	PWM brightness source pin
20	PWMOUT	PWM brightness signal output pin
21	CT	GND short protection timer setting pin
22	OUTL	Low-side external FET Gate Drive out put
23	DGND	Low-side FET driver source pin
24	SW	High-side FET Source pin
25	OUTH	High-side external FET Gate Drive out put
26	CS	DC/DC output current detection pin
27	BOOT	High-side FET driver source pin
28	VREG	Internal reference voltage output

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	50	V
Boot Voltage	V_{BOOT}	55	V
SW,CS,OUTH Voltage	V_{SW}, V_{CS}, V_{OUTH}	50	V
BOOT-SW Voltage	$V_{BOOT-SW}$	7	V
VREG,OVP,OUTL,FAIL1,FAIL2,THM,SS, COMP,RT,SYNC,EN,DISC,VTH,FB,LEDR, LEDC,DRLIN, PWMOUT,CT Voltage	V_{REG}, V_{OVP}, V_{OUTL}, V_{FAIL1}, V_{FAIL2}, V_{THM}, V_{SS}, V_{COMP}, V_{RT}, V_{SYNC}, V_{EN}, V_{DISC}, V_{VTH}, V_{FB}, V_{LEDR}, V_{LEDC}, V_{DRLIN}, V_{PWMOUT}, V_{CT}	-0.3 to +7 < V_{CC}	V
Power Consumption	Pd	1.45 (Note 1)	W
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) IC mounted on glass epoxy board measuring 70mm x 70mm x 1.6mm, power dissipated at a rate of 11.60mW/°C at temperatures above 25°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings..

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	5.0 to 30	V
Oscillating Frequency Range	f_{OSC}	100 to 600	kHz
External Synchronization Frequency Range (Note 2) (Note 3)	f_{SYNC}	f_{OSC} to 600	kHz
External Synchronization Pulse Duty Range	f_{SDUTY}	40 to 60	%

(Note 2) Connect SYNC to GND or OPEN when not using external frequency synchronization.
(Note 3) Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

Electrical Characteristics (Unless otherwise specified, V_{CC}=12V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	4.5	7.0	mA	EN=Hi, SYNC=Hi, RT=OPEN, C_{IN}=10µF
Standby Current	I_{STBY}	-	0	8	µA	EN=Low
[VREG Block (VREG)]						
Reference Voltage	V_{REG}	4.5	5.0	5.5	V	I_{REG}=-5mA, C_{REG}=10µF
[OUTH Block]						
OUTH High-Side ON-Resistance	R_{ONHH}	1.5	3.5	7.0	Ω	I_{ON}=-10mA
OUTH Low-Side ON-Resistance	R_{ONHL}	1.0	2.5	5.0	Ω	I_{ON}=10mA
Over-Current Protection Operating Voltage	V_{OLIMIT}	V_{CC} -0.68	V_{CC} -0.60	V_{CC} -0.52	V	
SS Charge Current	I_{SS}	3	5	7	µA	V_{SS}=0V
[OUTL Block]						
OUTL High-Side ON-Resistance	R_{ONLH}	2.0	4.0	8.0	Ω	I_{ON}=-10mA
OUTL Low –Side ON-Resistance	R_{ONLL}	1.0	2.5	5.0	Ω	I_{ON}=10mA
[SW Block]						
SW Low -Side ON-Resistance	R_{ONSW}	2.0	4.5	9.0	Ω	I_{ONSW}=10mA
[PWMOUT Block]						
PWMOUT High-Side ON-Resistance	R_{ONPWMH}	2.0	4.0	8.0	Ω	I_{ONPWMH}=-10mA
PWMOUT Low-Side ON-Resistance	R_{ONPWML}	1.0	2.5	5.0	Ω	I_{ONPWML}=10mA
[Error Amplifier Block]						
Reference Voltage1	V_{REF1}	0.194	0.200	0.206	V	FB-COMP Short,1MΩ/250kΩ
Reference Voltage2	V_{REF2}	0.190	0.200	0.210	V	FB-COMP Short,1MΩ/250kΩ Ta=-40°C to +125°C
The Amount of Change of VREF by Temperature	dV_{REF2}	-0.090	-0.045	-0.003	mV/°C	
COMP Sink Current	$I_{COMPSINK}$	50	75	100	µA	V_{FB}=0.4V, V_{COMP}=1V
COMP Source Current	$I_{COMPSOURCE}$	-100	-75	-50	µA	V_{FB}=0V, V_{COMP}=1V
Max Duty Output	Dmax	83	90	-	%	f_{OSC}=300kHz
[Oscillator Block]						
Oscillating Frequency	f_{OSC}	285	300	315	KHz	R_{RT}=200kΩ
[OVP Block]						
Over-Voltage Detection Reference Voltage	V_{OVP}	1.9	2.0	2.1	V	V_{OVP}=Sweep up
OVP Hysteresis Width	V_{OHYS}	0.45	0.55	0.65	V	V_{OVP}= Sweep down
[UVLO Block]						
UVLO Voltage	V_{UVLO}	4.0	4.35	4.7	V	V_{CC}= Sweep down
UVLO Hysteresis Width	V_{UHYS}	50	150	250	mV	V_{CC}= Sweep up
[PWM Generation Circuit Block]						
VTH Threshold Voltage	V_{TH1}	3	2/3V_{REG}	3.7	V	
VTH Threshold Voltage	V_{TH2}	1	1/3V_{REG}	2	V	
PWM Minimum ON Width	t_{PWMON}	25	-	-	µs	
LED OPEN Detection Function	V_{OPEN}	30	50	70	mV	
LED SHORT Detection Function	V_{SHORT}	100	200	400	mV	$V_{SHORT} \geq \lvert V_{LEDR}-V_{LEDC} \rvert$
LED GND Short Protection Timer	t_{SHORT}	100	150	200	ms	C_{CT}=0.1µF
[Logic Inputs]						
Input HIGH Voltage	V_{INH}	3.0	-	-	V	
Input LOW Voltage	V_{INL}	GND	-	1.0	V	
Input Current 1	I_{IN}	20	35	50	µA	V_{IN}=5V (SYNC/DRLIN)
Input Current 2	I_{EN}	15	30	45	µA	V_{EN}=5V (EN)
[FAIL Output (Open Drain)]						
Fail LOW Voltage	V_{OL}	-	0.1	0.2	V	I_{OL}=0.1mA

Typical Performance Curves

(Unless otherwise specified, Ta=25°C)

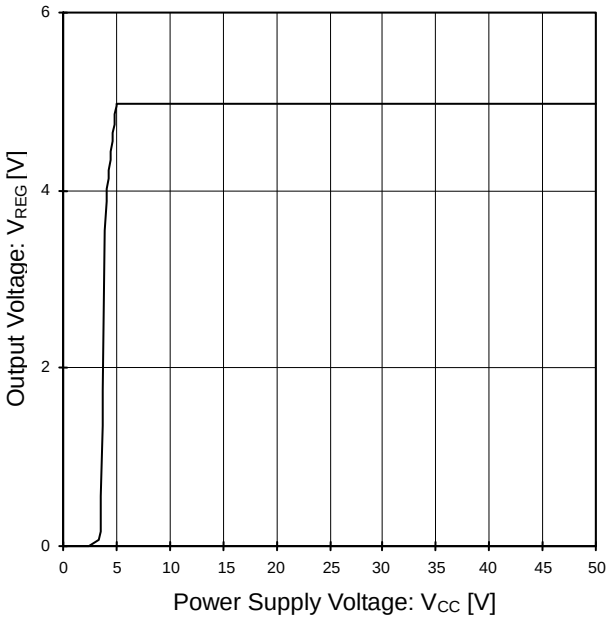


Figure 1. Output Voltage vs Power Supply Voltage
(VREG Voltage Characteristic)

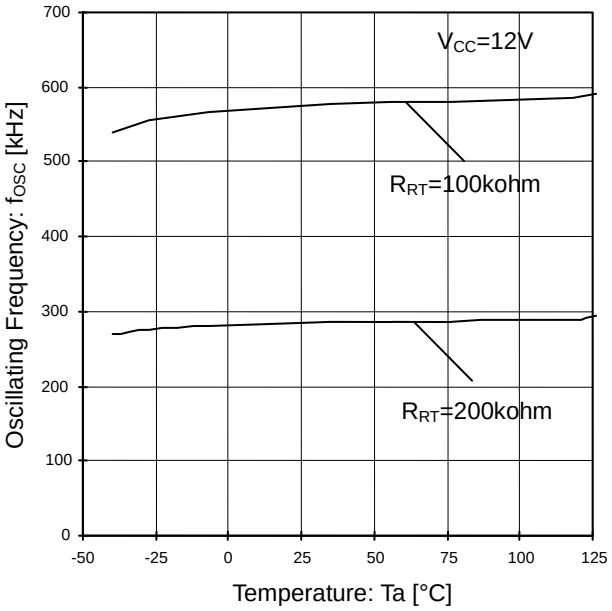


Figure 2. Oscillating Frequency vs Temperature
(f_{OSC} Temperature Characteristic)

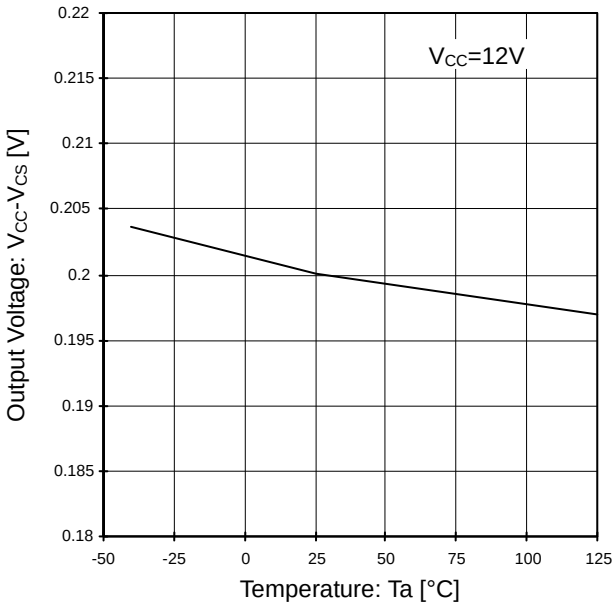


Figure 3. Output Voltage vs Temperature
(Standard Voltage Temperature Characteristic)

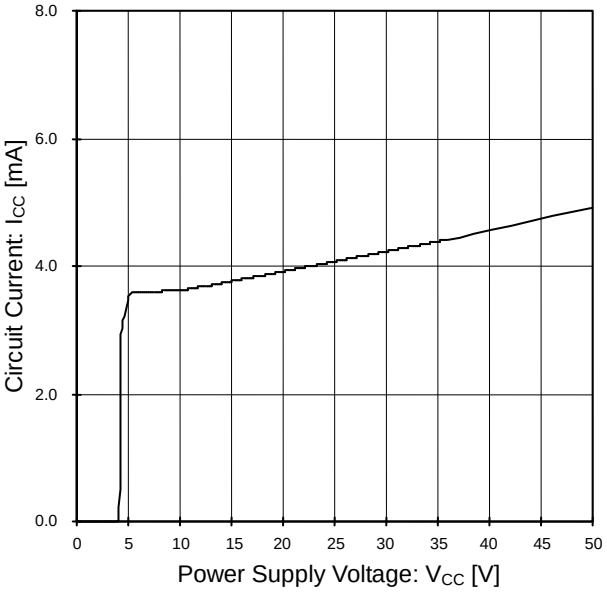


Figure 4. Circuit Current vs Power Supply Voltage

Typical Performance Curves – continued

(Unless otherwise specified, Ta=25°C)

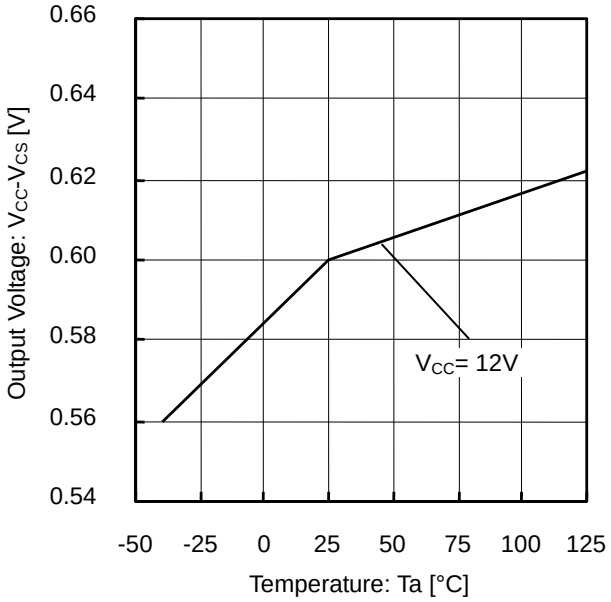


Figure 5. Output Voltage vs Temperature (Overcurrent Detection Voltage Temperature Characteristic)

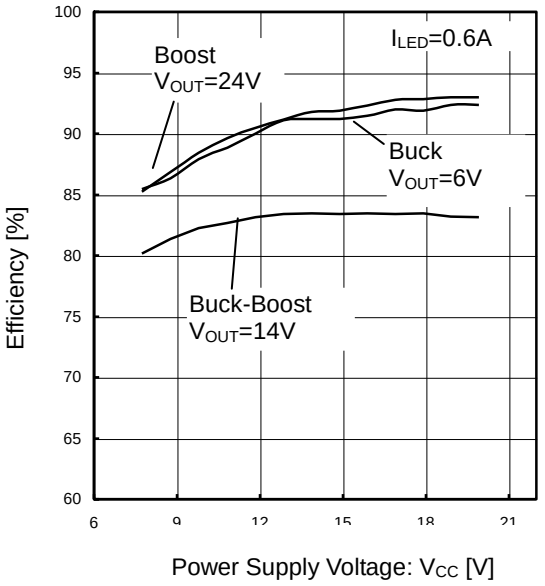


Figure 6. Efficiency vs Power Supply Voltage (Input Voltage Dependence)

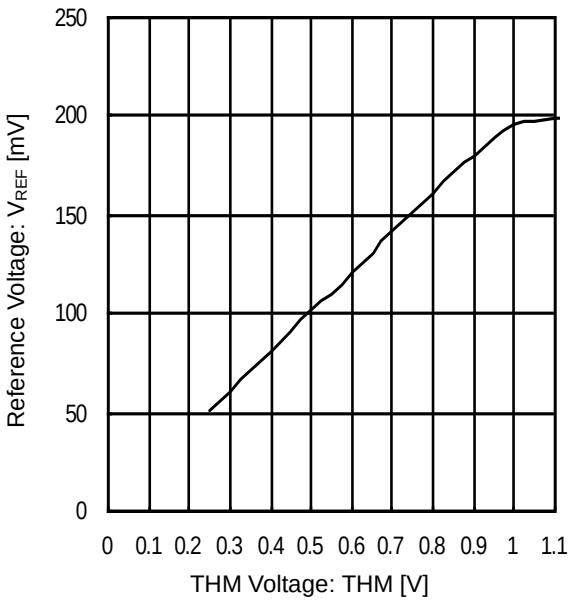


Figure 7. Reference Voltage vs THM Voltage (THM Gain)

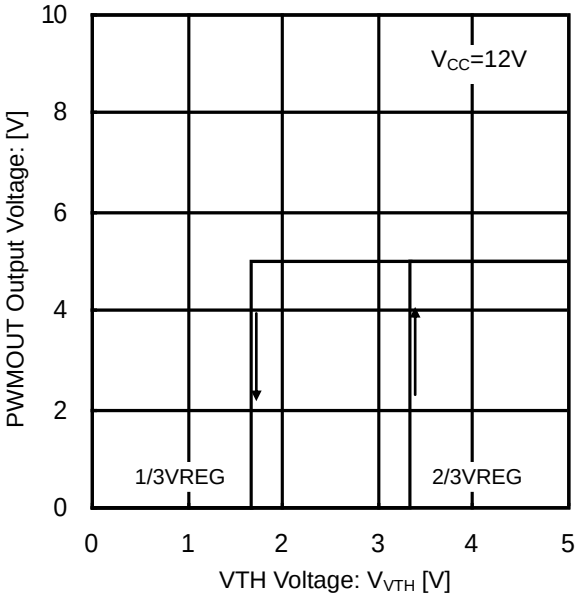


Figure 8. PWMOUT Output Voltage vs VTH Threshold Voltage

Typical Performance Curves – continued
(Unless otherwise specified, Ta=25°C)

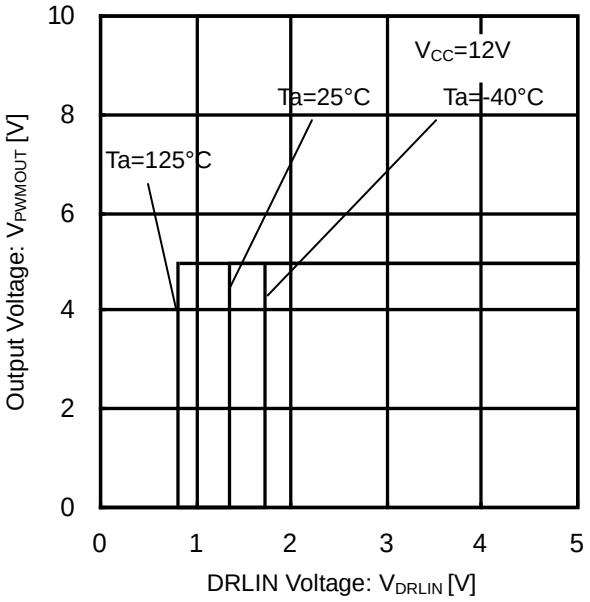


Figure 9. Output Voltage vs DRLIN Threshold Voltage

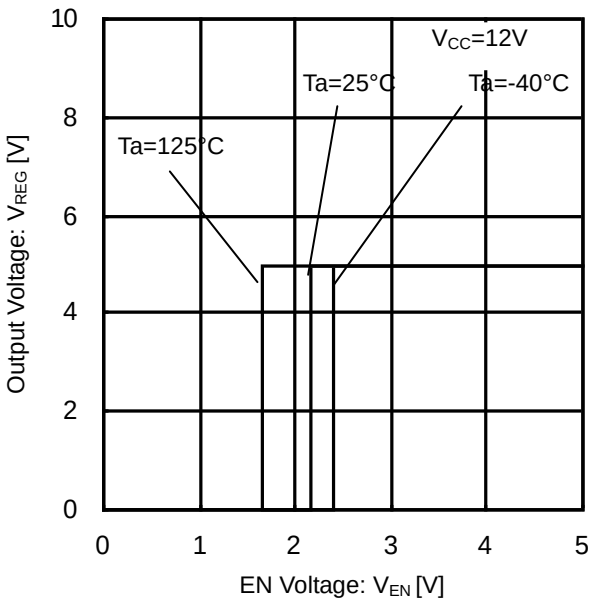


Figure 10. Output Voltage vs EN Threshold Voltage (DRLIN=VREG)

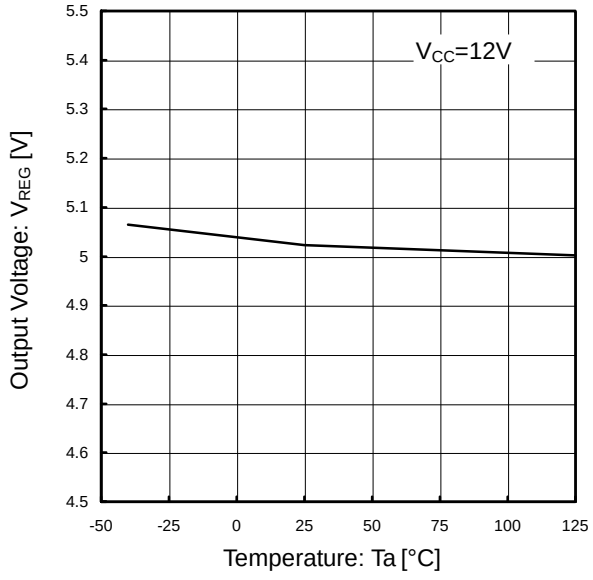


Figure 11. Output Voltage vs Temperature
(VREG Voltage Temperature Characteristic)

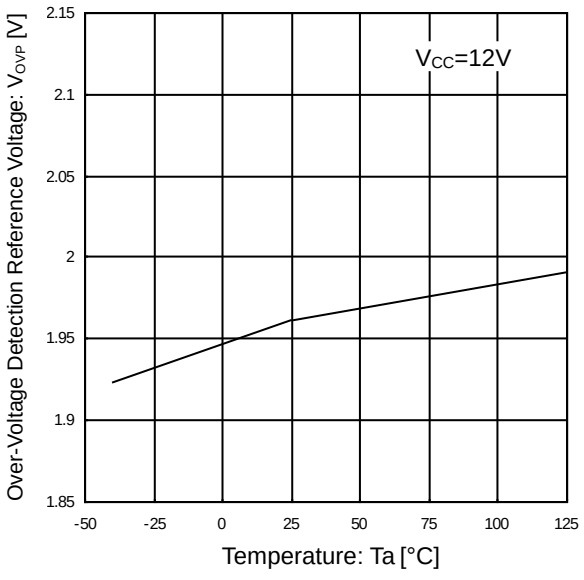


Figure 12. Over-Voltage Detection Reference Voltage vs Temperature
(OVP Voltage Temperature Characteristic)

Typical Performance Curves – continued

(Unless otherwise specified, Ta=25°C)

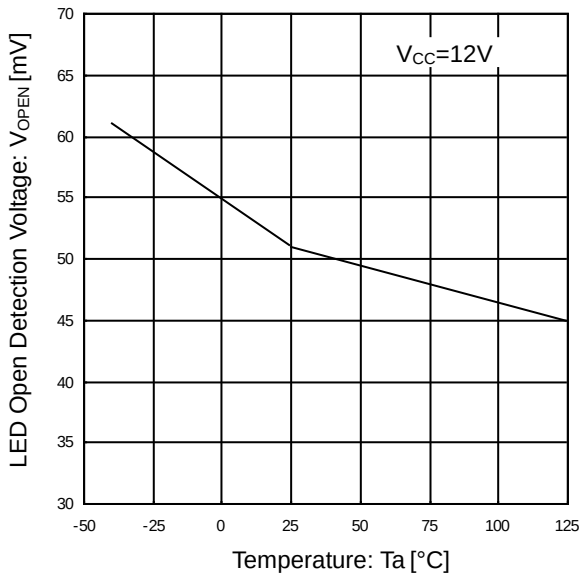


Figure 13. LED Open Detection Voltage vs Temperature

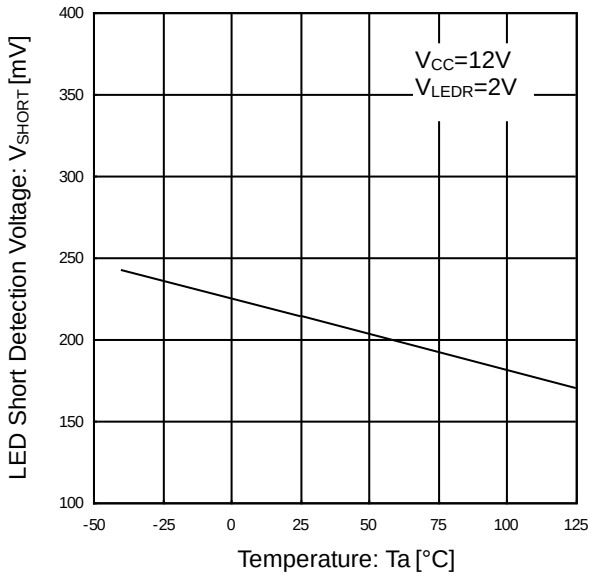


Figure 14. LED Short Detection Voltage vs Temperature

Application Information

1. Application Circuit

Application Circuit 1

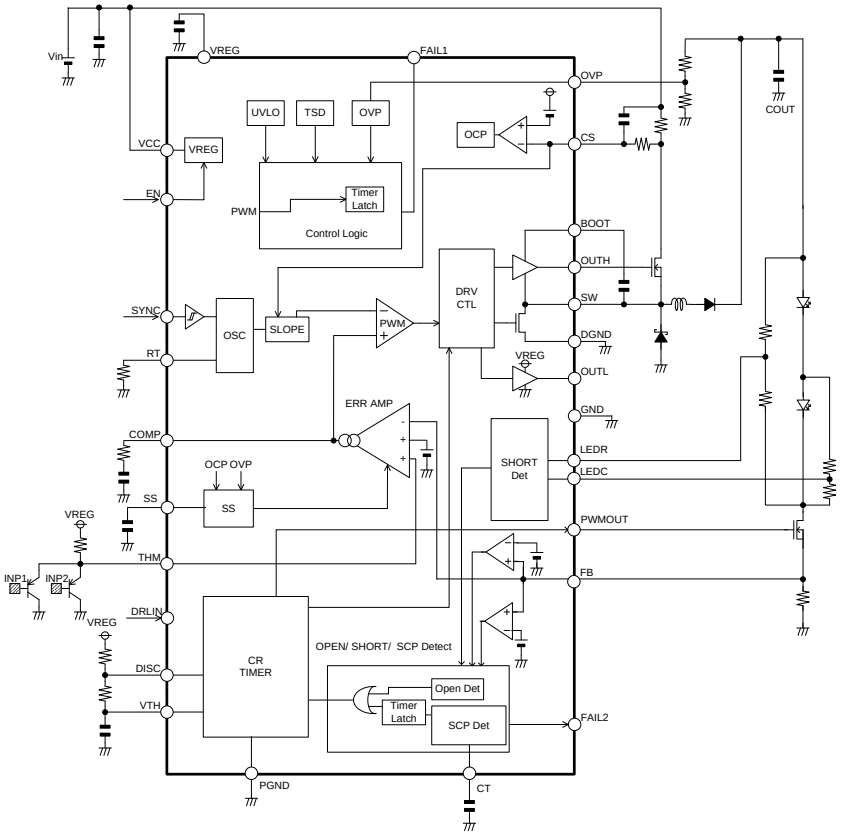


Figure 15
Buck application composition (It is INP1, INP2 and two input selector function and EN connected direct to VCC)

Application Circuit 2

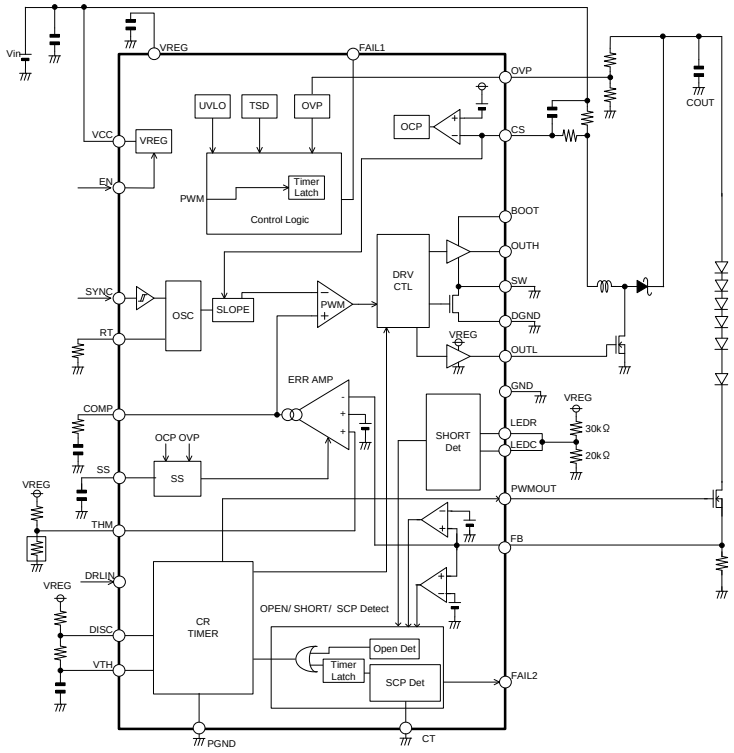


Figure 16
Boost application composition (When invalidating short detection and EN is inputted by a voltage divider)

2. Reference PCB Setting

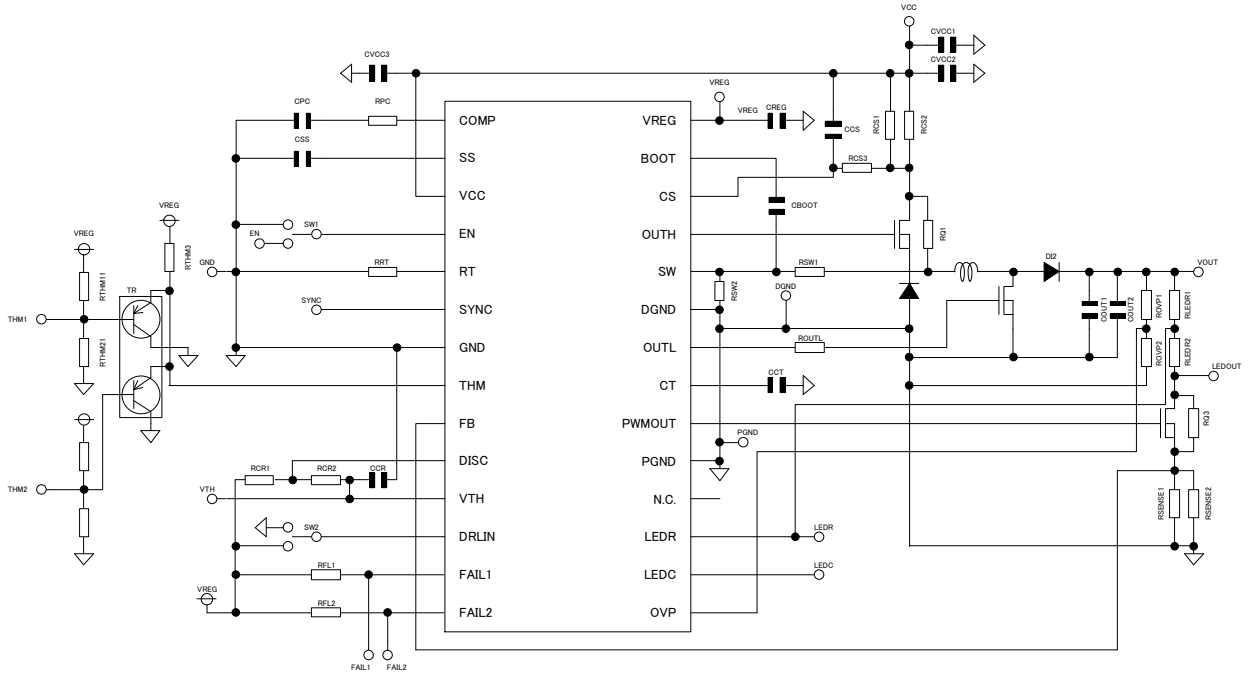


Figure 17

V_{CC}=8V to 16V, V_{OUT}=16V, I_{LED}=1A, f_{OSC}=300kHz, PWM dummign25%, PWM Frequency 130Hz

No.	Component Name	Component Value	Product Name	No.	Component Name	Component Value	Product Name
1	CVCC1	10μF	GCM32ER71E106KA42	23	CCS	N.M	-
2	CVCC2	10μF	GCM32ER71E106KA42	24	CBOOT	0.1μF	GCM188R11H104KA42
3	CVCC3	0.1μF	GRM31CB31E104KA75B	25	Q1	RSS070N05	-
4	CPC	0.1μF	GCM188R11H104KA42	26	DI1	RB050L-40	-
5	RPC	820Ω	MCR03 Series	27	RSW1	0Ω	-
6	CSS	0.1μF	GCM188R11H104KA42	28	RSW2	N.M	-
7	RRT	200kΩ	MCR03 Series	29	RQ1	N.M	-
8	RTHM11	100kΩ	MCR03 Series	30	L	10μH	SLF12575T100M5R4-H
9	RTHM12	100kΩ	MCR03 Series	31	ROUTL	0Ω	MCR03
10	RTHM21	100kΩ	MCR03 Series	32	Q2	RSS070N05	-
11	RTHM22	100kΩ	MCR03 Series	33	DI2	RF201L2S	-
12	RTHM3	0Ω	-	34	COUT1	10μF	GCM32ER71E106KA42
13	TR	-	-	35	COUT2	10μF	GCM32ER71E106KA42
14	RCR1	30kΩ	MCR03 Series	36	CCT	0.1μF	GCM188R11H104KA42
15	RCR2	10kΩ	MCR03 Series	37	ROVP1	270kΩ	MCR03
16	CCR	0.22μF	GCM21BR11H224KA01	38	ROVP2	30kΩ	MCR03
17	FRL1	100kΩ	MCR03 Series	39	RLEDR1	90kΩ	MCR03
18	FRL2	100kΩ	MCR03 Series	39	RLEDR2	30kΩ	MCR03
19	CREG	10μF	GCM32ER71E106KA42	40	Q3	RSS070N0	-
20	RCS1	110mΩ	MCR100JZHFSR110	41	RQ3	N.M	-
21	RCS2	N.M	-	42	RSENSE1	200mΩ	MCR100JZHFSR510
22	RCS3	0Ω	-	43	RSENSE2	N.M	-

(Note)

- When no PWM dimming, DI2 should be a schottky diode instead of a Fast Recovery diode to improve efficiency. When dimming with External PWM signal, DISC should be pulled up to VREG with 10KΩ,then input PWM signal to VTH.(when no PWM dimming, remove Q3 and replace R_{Q3}=0Ω and short to DS)
- Efficiency improvement is possible by making DI2 a schottky Diode .However, since high temperature leakage current is large and output voltage ripple is large as well, LED may flicker when PWM dimming ratio is very low. So it is recommended to use a Fast recovery Diode.
- Values of the capacitors can be smaller than the amount that was selected by the DC bias characteristics of the capacitor when using ceramic capacitors.
- For EMI reduction, please insert resistance to ROUTL and RBOOT. It is recommended to be below 20Ω.
- The output voltage ripple is larger in Boost application than in Buck application. Hence, it is recommended to use at least 100μ F output capacitor.

3. 5V Voltage Reference (VREG)

5V (Typ) is generated from the VCC input voltage when the enable pin is set high. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HIGH.
UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for output voltages higher than 4.5 V (Typ), but if output voltage drops to 4.3 V (Typ) or lower, UVLO engages and turns the IC off.
Connect a capacitor (C_{REG} = 10µF Typ) to the VREG terminal for phase compensation. Operation may become unstable if C_{REG} is not connected.

4. LED Current Setting and Control Method.

(1) Method of setting the LED current

The LED current can be calculated by the following formula.

THM ≥1.0V→I_{LED}＝0.2V(Typ) / R_{SET}

THM <1.0V→I_{LED}＝V_{THM} / (GAIN x R_{SET})

(GAIN：the gain of internal AMP 5(Typ))

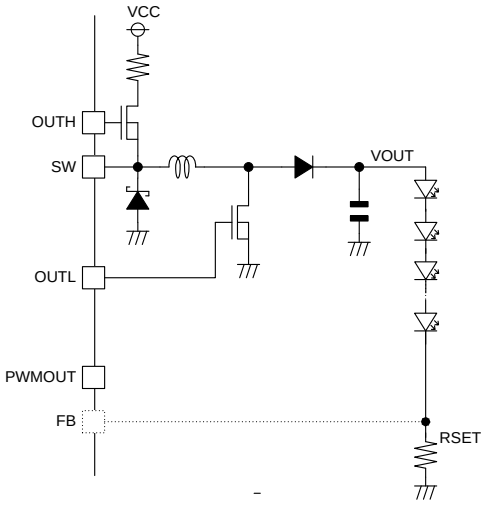


Figure 18. LED current setting block diagram

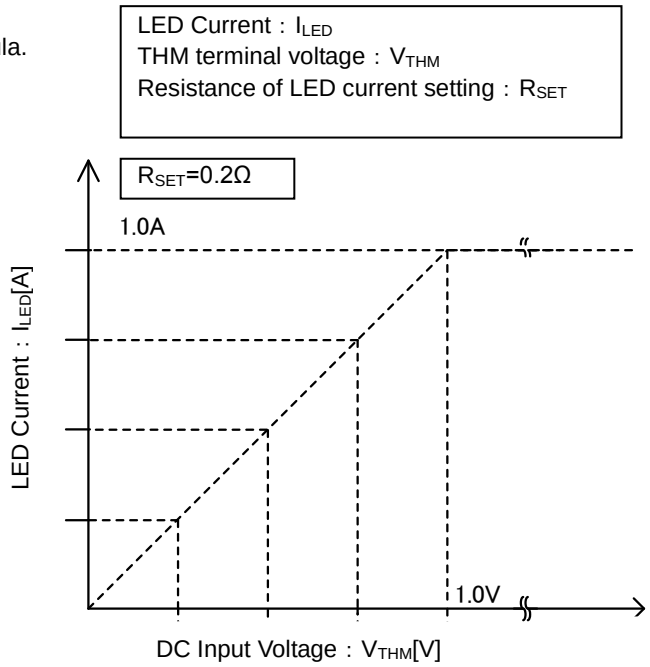
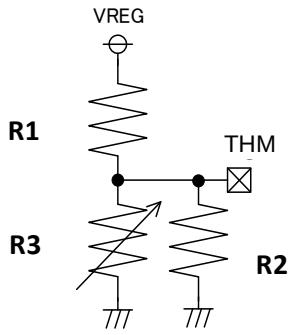


Figure 19. The LED current derating by THM terminal

(2) Linear dimming function

LED current can be controlled linearly by using the THM terminal which is commonly used as a derating function.
For example, THM terminal is used when suppressing the degradation at high temperature of the LED (Figure 20) and controlling the excessive current to the external components under the conditions likely to occur in the power supply voltage fluctuations in the idling stop function. V_{THM} input range is recommended V_{THM} ≥ 0.4V.



product	value	unit
VREG	5	V
R1	20	kΩ
R2	47	kΩ
R3	47	kΩ
R3:NTCG104BF473F		

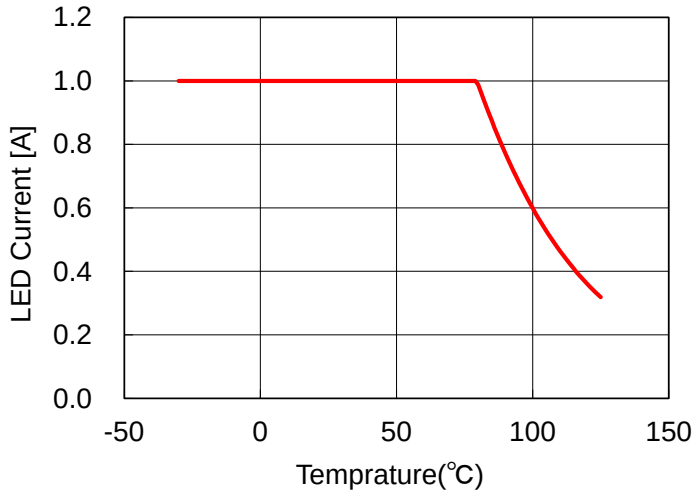
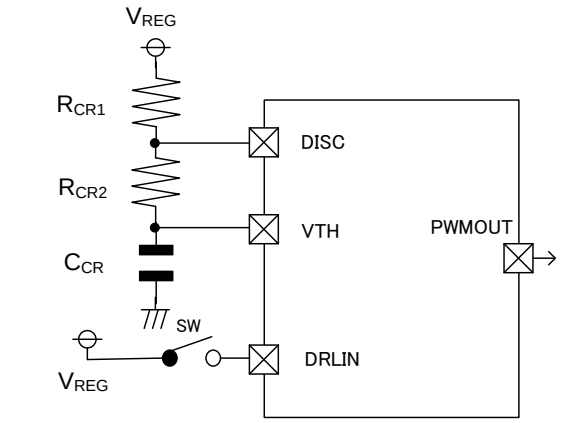
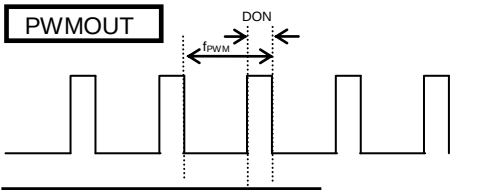


Figure 20. The derating use case with thermistor resister.

5. Setting of CR Timer Dimming

It is possible to set the PWM frequency (f_{PWM}) and the PWM on Duty (DON) with the external resistor and capacitor by using the built-in CR timer function. This function can be used to set the Dimming range from 2%up to 45% and the frequency range from 100Hz up to 20kHz. When a Hi voltage is applied at DRLIN terminal, 100% On-Duty is outputted at the PWMOUT terminal and at the LED current, independent of the PWM signal and the CR Timer. The minimum PWM pulse width is 25μs.



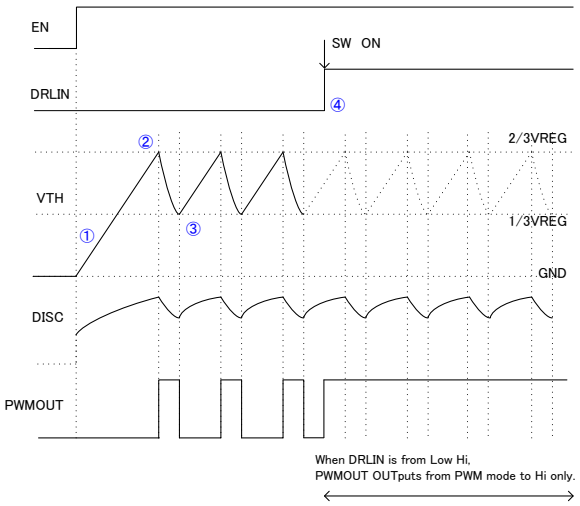


PWM Frequency (f_{PWM})

$$f_{PWM} = \frac{1.44}{(R_{CR1} + 2 \times R_{CR2})C_{CR}}$$

PWM on Duty (DON)

$$DON = \frac{R_{CR2}}{(R_{CR1} + 2 \times R_{CR2})} \times 100$$



① Turning on EN, VTH voltage is increased and C_{CR} starts charging.
②,③C_{CR} is discharged in the DISC to 1/3VREG, when VTH voltage reaches 2/3VREG.
④ PWMOUT is Hi when the DRLIN is Hi.

Figure 21. The setting of PWM dimming using CR Timer and Timing chart

Synchronization of the PWM dimming signal with an external signal is possible by inputting the external signal at the VTH terminal. The Hi voltage of the external signal can be more than 3.7V and the Low voltage can be less than 1.0V.

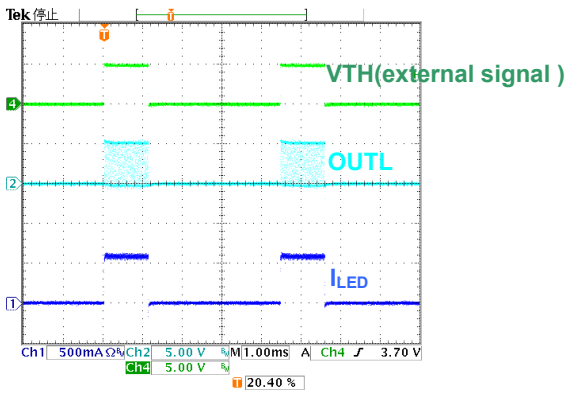


Figure 22. The waveform of PWM dimming in synchronization with an external signal

6. Relationship between PWM dimming and SCP protection

If the PWM ON-Time is short, even if it is an internal or an external PWM dimming, it will cause the rise time of the output voltage to be delayed and there is likely to have a false detection of the SCP. Figure 23 and Figure 24 indicates the relation between SCP and PWM dumming. Detail explanation of SCP is described in P.16.

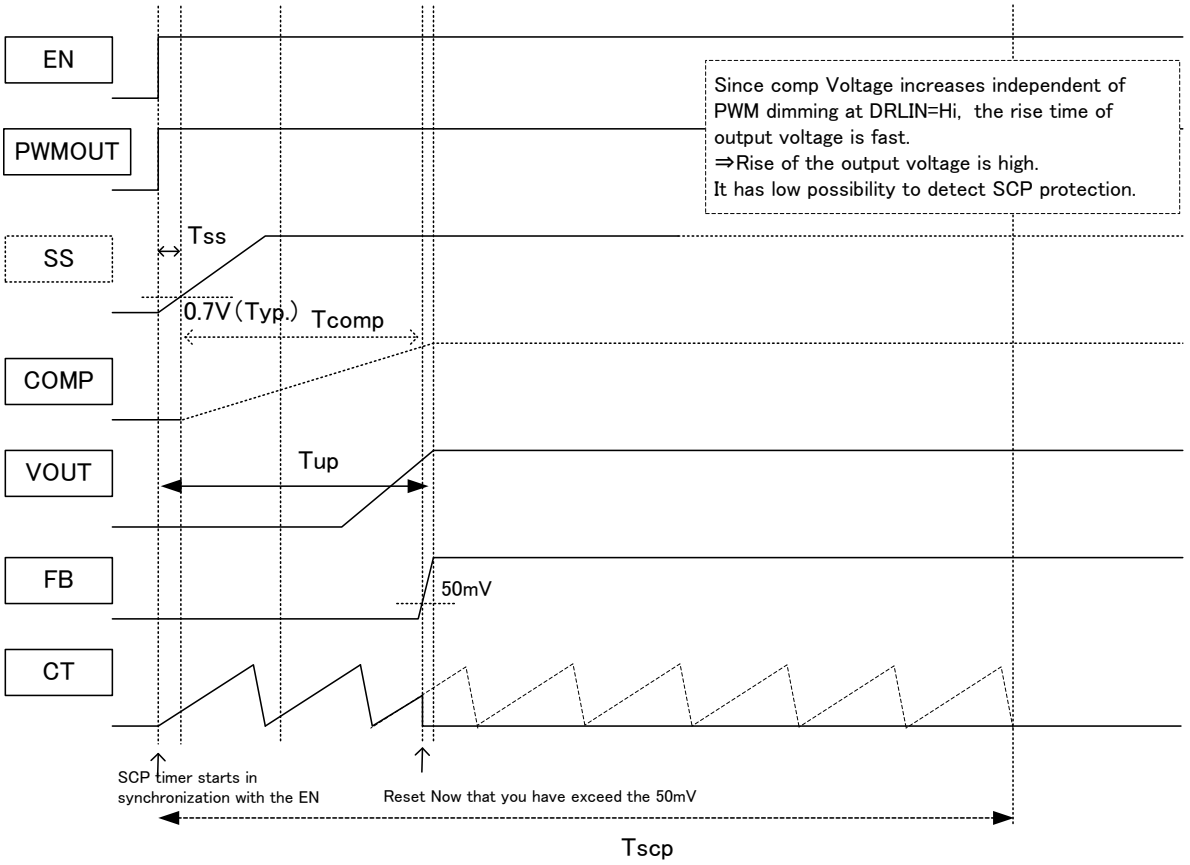


Figure 23. The relation of the output voltage rise time and SCP protection (not at PWM 100% dimming)

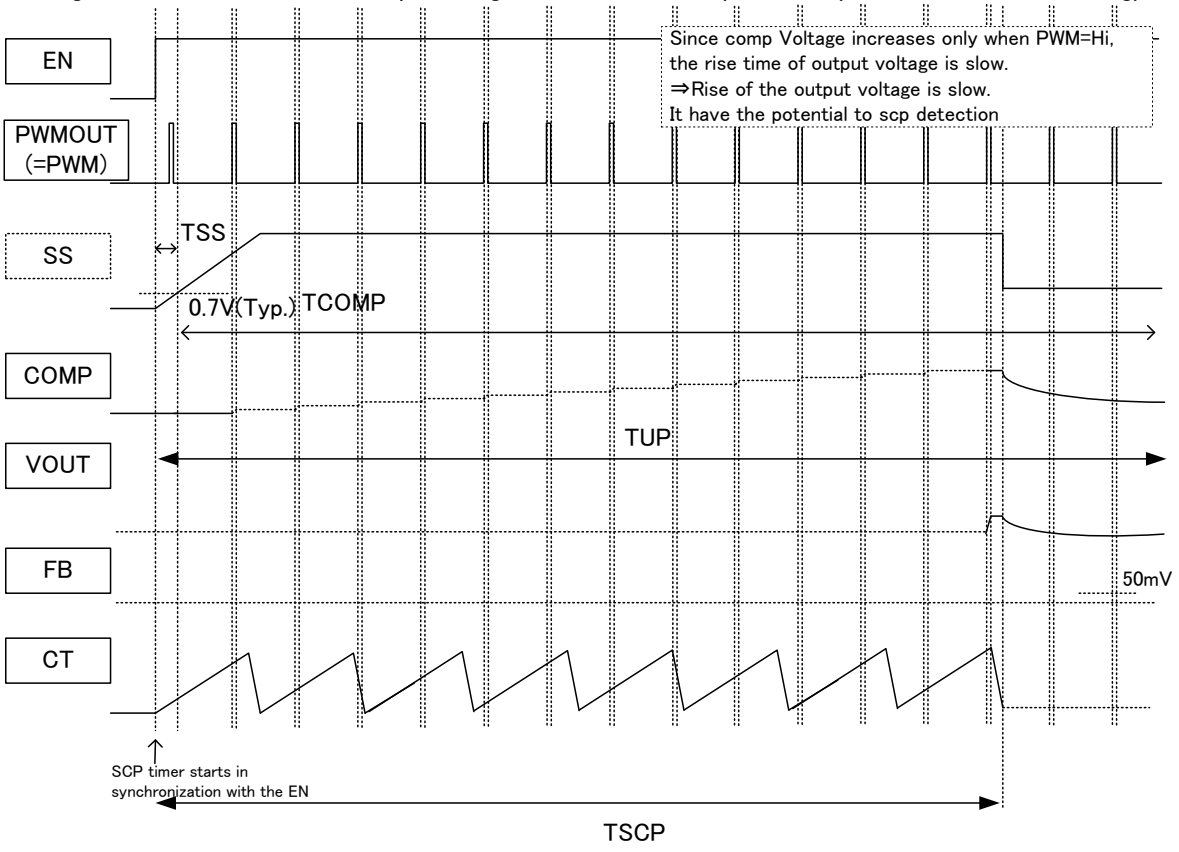


Figure 24. The relation of the output voltage rise time and SCP protection (at PWM dimming)

The rise time of the output voltage at PWM dimming is calculated as follows. The COMP voltage starts to increase when PWM=Hi and the switching output of the DC/DC circuit depends on the C_{PC} capacitor connected at the COMP terminal .It also affects the soft start time during start-up to prevent the rush current. (Refer to P.15 for more details.)
Base on the above explanation, the time (t_{UP}) it takes for the output voltage to reach the steady state level is calculated as follows.

$$t_{UP} = t_{SS} + t_{COMP}$$

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

$$t_{COMP} = \frac{V_{SWMAX}[V] \times C_{PC}[\mu F]}{I_{COMPSOURCE}[\mu A]} \times \frac{1}{DON}$$

Rise Time of COMP voltage : t_{COMP}
COMP source current : $I_{COMPSOURCE}$
Capacitor of COMP : C_{PC}
Soft start time : t_{SS}
SS Charged current : I_{SS}
Capacitor of SS : C_{SS}
PWM Dimming rate : DON
Soft start release voltage 0.85V (Max) : t_{SWST}
MaxDuty output voltage 2.0V (Max) : V_{SWMAX}

During the rise time of the output voltage which is calculated above, SCP detection starts the timer operation which is synchronized with EN. If the PWM dimming ratio is low and the rise time of output voltage is delayed, there is a possibility for a false detection of SCP.

Ex)
The condition that
$I_{COMPSOURCE}$=75μA,C_{PC}=0.1μF,I_{SS}=5μA,C_{SS}=0.1μF,
DON=5% are t_{SS}=17ms,t_{COMP}=53.3ms.
So, t_{UP} is about 60ms

From the above, when using the PWM dimming, it must establish the below relationship. (t_{SCP} indicates the SCP mask time. It indicates P.16 in detail.)

$$t_{UP} < t_{SCP}$$

As a reference, it is recommended that $1.2 \times t_{UP} < t_{SCP}$.

There is a need to reduce C_{PC} or C_{SS} in order to achieve fast rise time. If the C_{SS} is decreased, the overshoot of the output voltage increases as the inrush current increases. On the other hand, if the C_{PC} is decreased, the phase margin becomes unstable due to the failure to start at the right timing when the recommended range of $1.2 \times t_{UP} < t_{SCP}$ is not met. Also, always confirm that , CT terminal is connected to GND. The power supply voltage VCC after applying a PWM signal input, please input always earlier than the EN control signal when used in external input PWM as stated in P.19.

7. DC/DC controller

(1) Over-voltage protection circuit (OVP)

The output of the DCDC converter should be connected to the OVP pin via a voltage divider. In determining the appropriate trigger voltage of the OVP block, consider the total number of LEDs in series and the maximum V_F variation. The OVP terminal voltage, V_{OVP} is recommended to be in the range of 1.2V<V_{OVP}<1.4V during normal operation. If V_{OVP} is not at the normal operating range, it is possible to detect LED open protection. And the role of the OVP function is for the protection of the half-short mode of FB terminal short (V_{FB} ≈ 0.1V).

(2) DC/DC converter oscillation frequency (f_{OSC})

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 5). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillation frequency. Refer to the following theoretical formula when setting RT:

$$f_{OSC} = \frac{60 \times 10^6}{R_{RT}[\Omega]} \times \alpha \, [kHz]$$

60×10^6 (V/A/S) is a constant (±5%) determined by the internal circuitry, and α is a correction factor that varies in relation to RT: (RT: α = 100kΩ: 1.0, 150kΩ: 0.99, 200kΩ: 0.98, 280kΩ: 0.97)

A resistor in the range of 100kΩ to 280kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, causing the device operation to be unstable.

Please consider the parasitic capacitance of RT terminal at PCB board design. It must be less than 50pF.

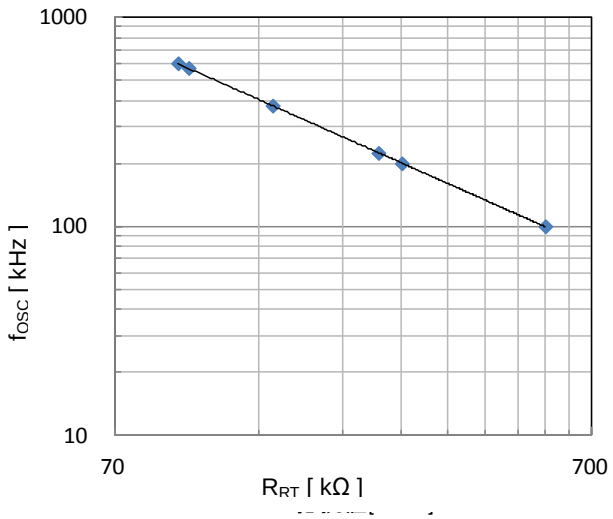


Figure 25. f_{OSC} vs R_{RT}

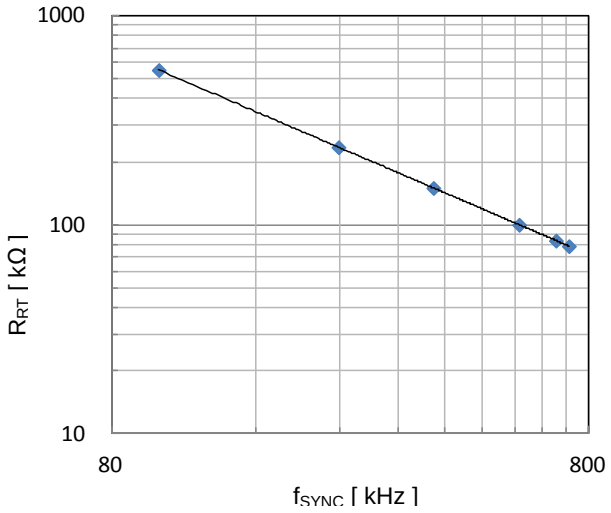


Figure 26. R_{RT} vs f_{SYNC}

(3) External DC/DC converter oscillation frequency synchronization (f_{SYNC})

Please do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about 30 µs (typ) occurs before the internal oscillation circuit starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Consider that; if the external sync is already running and is switched to internal synchronization from external synchronization. It may cause the output voltage overshoot and erroneous open detection may occur.

In addition, whenever an external synchronization is used, please set the R_{RT} such that the external synchronization frequency is f_{SYNC} < f_{OSC} x 1.2.

(4) Soft Start Function

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to the prevention of the overshoot of the output voltage and the inrush current. The SS voltage is Low when the OCP and the OVP is detected. Switching is stopped and operation is resumed.

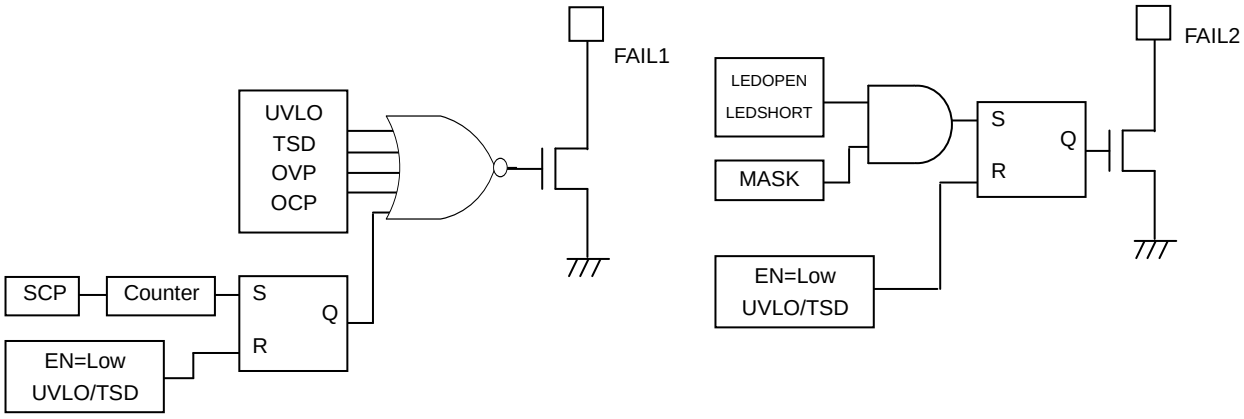
t_{SS} (soft-start time) is calculated using the formula below. Please refer to P.23 for more detailed application of the setting method.

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

Soft start time: t_{SS}
Soft start charge current 5µA (Typ): I_{SS}
Capacitor of SS: C_{SS}
Soft start release voltage 0.85V (Max): V_{SWST}

(5) Self-diagnostic functions

The operating status of the built-in protection circuit is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, OCP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected.



(6) Operation of the Protection Circuit

(a) Under-Voltage Lock Out (UVLO)

The UVLO shuts down all the circuits except for VREG when VCC ≤ 4.3V (TYP).

(b) Thermal Shut Down (TSD)

The TSD shuts down all the circuits except for REG when the Tj reaches 175°C (TYP), and releases when the Tj becomes below 150°C (TYP).

(c) Over Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor and activates when the CS voltage becomes less than V_{CC}-0.6V (TYP). When the OCP is activated, the external capacitor of the SS pin will discharge and the switching operation of the DCDC turns off.

(d) Over Voltage Protection (OVP)

The output voltage of the DCDC is detected with the OVP-pin voltage and the protection activates when the OVP-pin voltage becomes greater than 2.0V (TYP). When the OVP is activated, the external capacitor of the SS pin will discharge and the switching operation of the DCDC turns off.

(7) Short Circuit Protection (SCP) (Following Figure 36 in P.21)

SCP is independent from PWM dimming. When the FB-pin voltage becomes less than 0.05V (TYP), the internal counter starts operating and latches off the circuit approximately after 150ms (when C_{CT} = 0.1µF). If the FB-pin voltage becomes over 0.05V before 150ms, then the counter resets. When the LED anode (i.e. DCDC output voltage) is shorted to ground, the LED current turns off and the FB-pin voltage becomes low. Furthermore, the LED current also turns off when the LED cathode is shorted to ground. Hence in summary, the SCP works in both cases when the LED anode and the LED cathode is being shorted.

SCP mask timer (t_{SCP}) can be calculated using the following expression.

$$t_{SCP} = \frac{C_{CT}[\mu F] \times V_{CT}[V]}{I_{CT}[\mu A]} \times 8count$$

SCP mask timer : t_{SCP}
CT charge current 5µA (Typ) : I_{CT}
Capacitor of CT : C_{CT}
CT terminal Voltage 0.8V (Typ) : V_{CT}

The need for SCP varies depending on the application. The OCP is detected and limited by High side SW, when the output is shorted to GND in the Buck / Buck-Boost application. Since the current continues to flow continuously, set the SCP timer to stop after an error is detected. On the other hand, the current path can not be cut off and large current continues to flow in the Boost application because there is no High side SW in Buck / Buck-Boost application. Therefore, please mask the SCP function in boost application. (CT terminal short to GND)

(8) LED Open Detection(Following Figure 34 in P.20)

When the FB-pin voltage < 50mV (TYP) as well as OVP-pin voltage ≥ 1.7V (TYP) operates in these ranges, the device detects LED open and latches off that particular channel.

(9) LED Short Detection(Following Figure 35 in P.20)

Less brightness of the light source will be produced whenever one LED is shorted somewhere within the load. If the guaranteed luminance of the light source is required, detection of the failure in the circuit must be performed. LED short detection is activated whenever one of the LEDs in the circuit, is shorted. In case of a short circuit, problem of LED short detection is informed. When one of the LEDs used is shorted somewhere in the circuit, |LEDR-LEDC| ≥ 0.2 (TYP), the internal counter starts operating, and approximately after 100ms (when f_{OSC} = 300 kHz) the operation latches off. With the PWM brightness control, the detection operation only proceeds when PWM=Hi. If the condition of the detection operation is released before 100ms (when f_{OSC} = 300 kHz), then the internal counter resets.

$$t_{SHORT} = 1/f_{OSC} \times 32770 / DON$$

LED short timer : t_{SHORT}
DC/DC oscillator frequency : f_{OSC}
PWM dimming ratio : DON

There is a possibility that the LED short detection malfunctions when the difference of V_F is large. Therefore, please adjust external resistance connected for V_F. It is recommended to be 1V-3V of the input voltage range of LEDR and LEDC.

(Note) The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

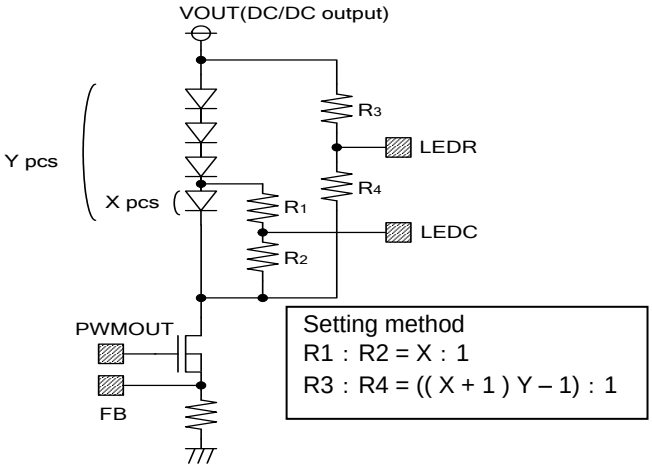


Figure 27. High luminance LED (multichip) when using Y piece

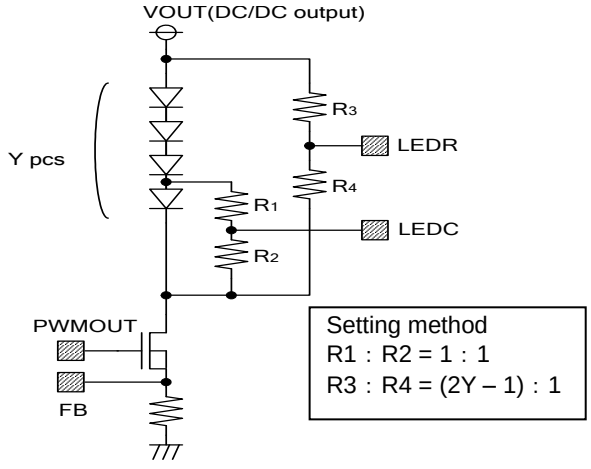


Figure 28. When using the single chip (White LED)

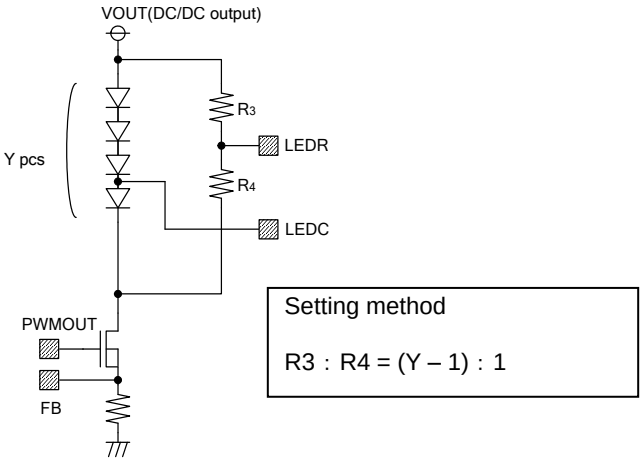


Figure 29. When using the Low V_F LED as Red LED

8. Error all condition

Protection	Detecting Condition		Operation after detect
	[Detect]	[Release]	
UVLO	V_{CC}<4.35V	V_{CC}>4.5V	All blocks (but except VREG) shut down
TSD	Tj>175°C	Tj<150°C	All blocks (but except VREG) shut down
OVP	V_{OVP}>2.0V	V_{OVP}<1.45V	SS discharged
OCP	$V_{CS} \leq V_{CC}$-0.6V	V_{CS}>V_{CC}-0.6V	SS discharged
SCP	V_{FB}<0.05V (150ms delay when C_{CT}=0.1μF)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED open	V_{FB}<0.05V & V_{OVP}>1.7V	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED short	I_{VLEDR}-$V_{LEDCI} \geq$ 0.2V (100ms delay when f_{OSC}=300kHz)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)

9. Effectiveness of the protection of each application

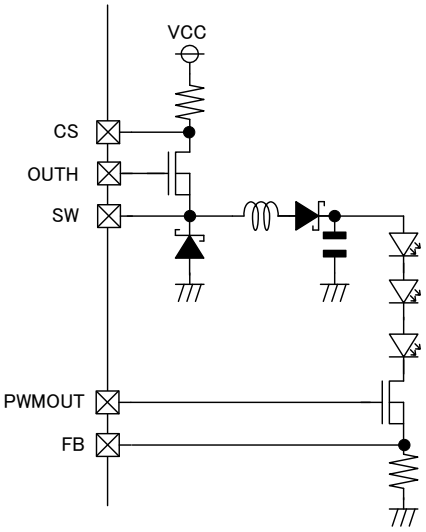


Figure 30. Buck Application

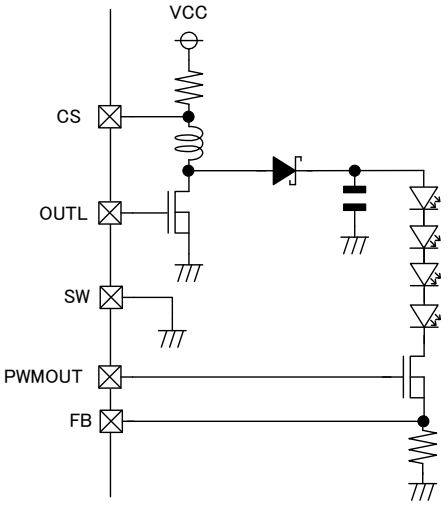


Figure 31. Boost Application

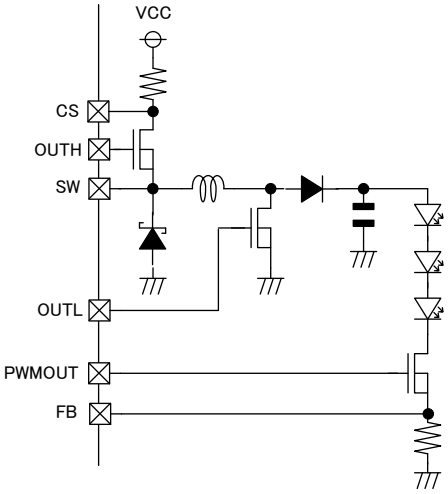


Figure 32. Buck-Boost Application

	DC/DC Application		
PROTECTION	Buck	Boost	Buck-Boost
UVLO	✓	✓	✓
OCP	✓	✓	✓
OVP	✓	✓	✓
DC/DC Output short GND detection	✓	Note1	✓
LED short detection	✓	✓	✓
LED Open detection	✓	✓	✓
LED Anode/Casode short detection	Note2	Note2	Note2

Note1：When the DC/DC output is shorted to GND using Boost application, there is a possibility of high current flow which lead to the destruction of the external components. For the reduction of current in the external components, CT terminal is connected to GND.

Note2：LED doesn't light when LED is shorted between anode and cathode. Under shorting LED, when using Buck/Buck-Boost application, may cause the large current not to flow while when using Boost application, there is a large current flowing from VCC to GND.

10. Power supply turning on sequence

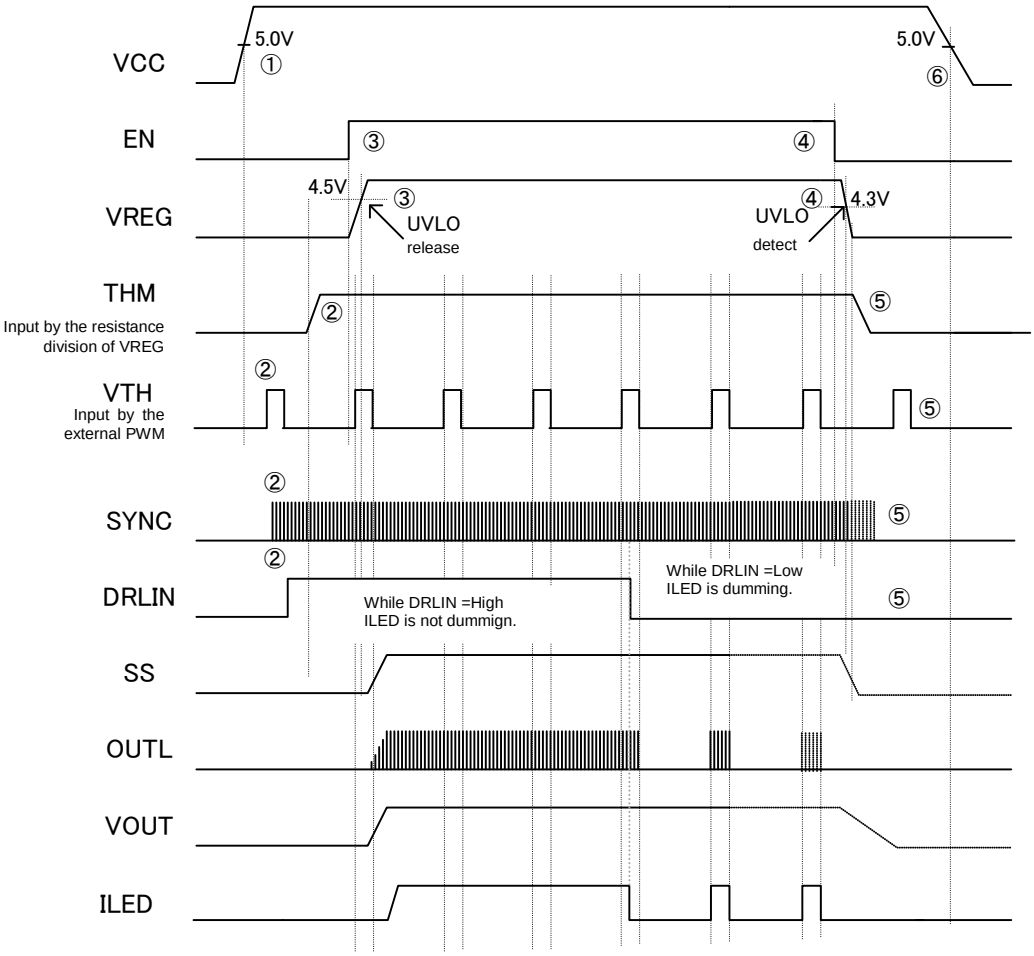


Figure 33

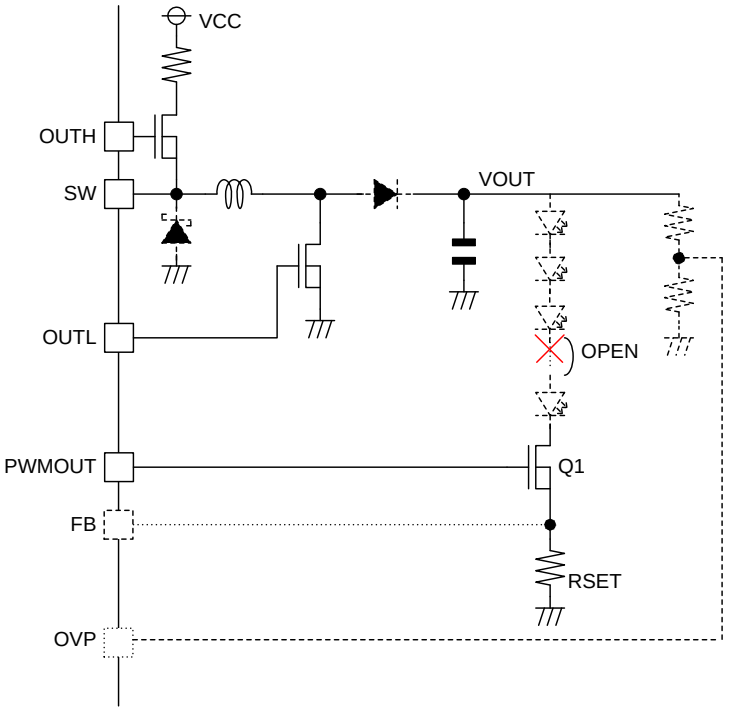
Power supply turning on sequence

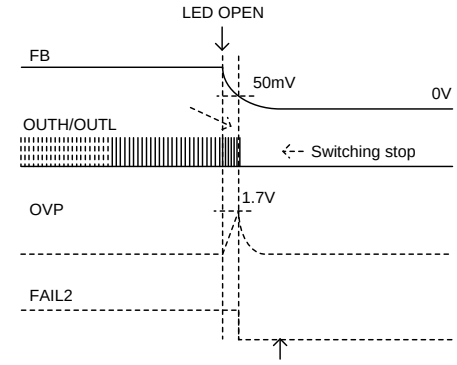
① After becoming V_{CC}>5V, the input of the other signals is possible.
② Before EN inputs, please fix VTH, THM, DRLIN, SYNC terminal voltage. An input order is not related.
③ VREG rises simultaneously with the input of EN, UVLO protection releases and switching starts.
④ VREG falls simultaneously with EN=Off.
⑤ Please stop input signal of VTH, THM, DRLIN, SYNC terminal voltage. An input order is not related.
⑥ VCC is OFF.

Note: It leads to the destruction of IC and external parts because it doesn't error output according to an external constant of adjacent pin 24pin SW terminal, 25pin OUTH terminal, 26pin CS terminal and 27pin BOOT terminal.

11. Operation in error circumstances of LED

(1) LED open detection

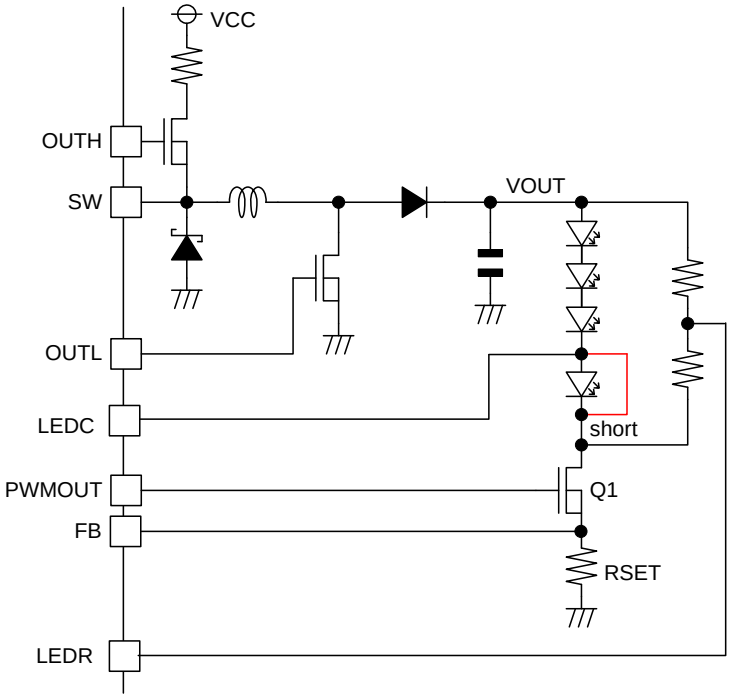


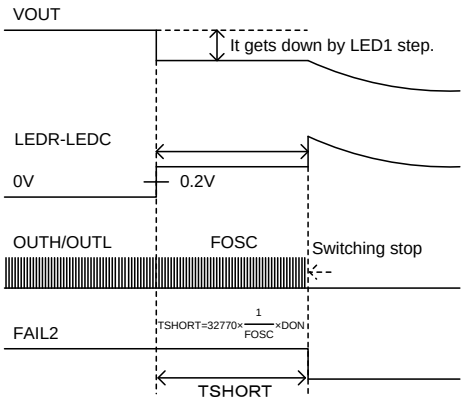


LED OPEN detection when VOVP>1.7 and VFB<50mV
（When it achieves the detection condition, the FP latch is done.）

Figure 34

(2) LED short detection





It detects short and error is detected with FAIL2 after the timer TSHORT.
Ex)
TSHORT is about 100ms under the condition that FOSC=300kHz and dimming=100%.
TSHORT is about 200ms under the condition that FOSC=300kHz and dimming=50%.

Figure 35

(3) LED anode short to GND detection

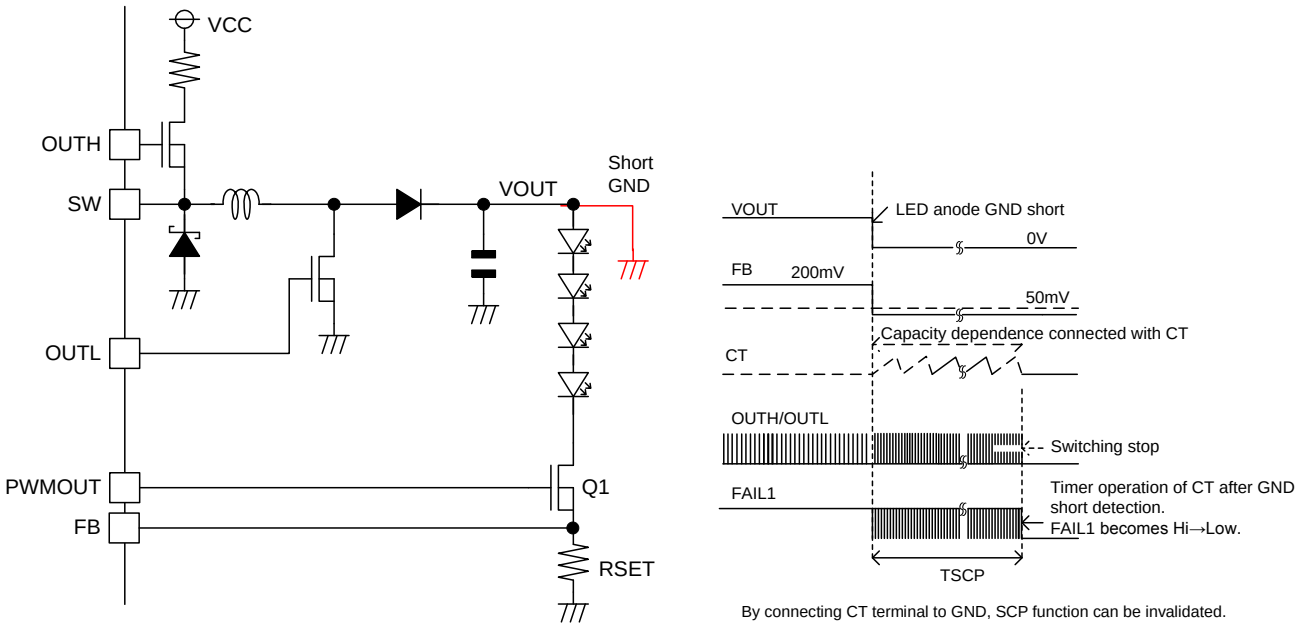
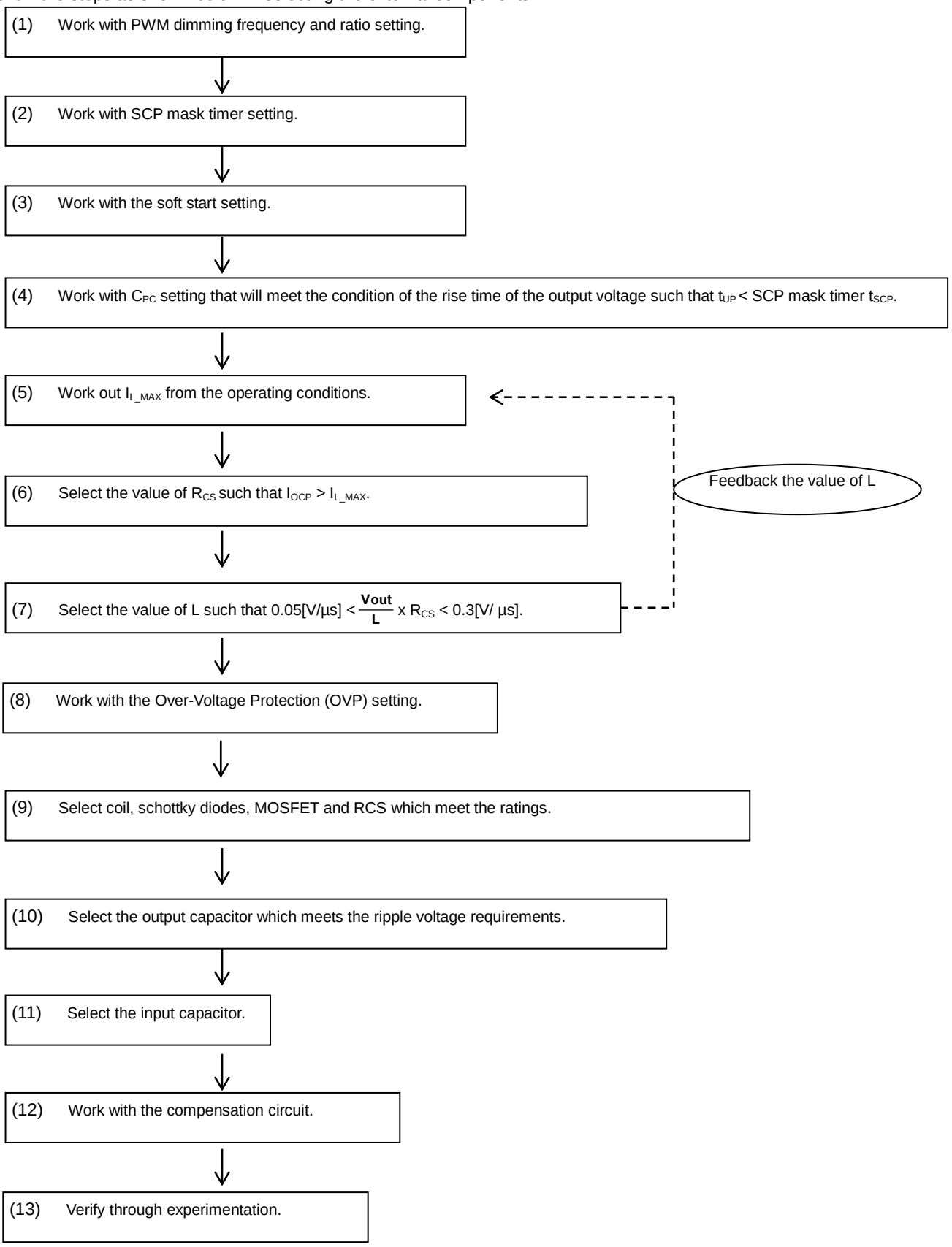


Figure 36

Note: When GND short-circuits by the DC/DC output by Boost application, high current flows and may lead to the destruction of external parts. The boost application does not enable the GND short protection of the DC/DC output.

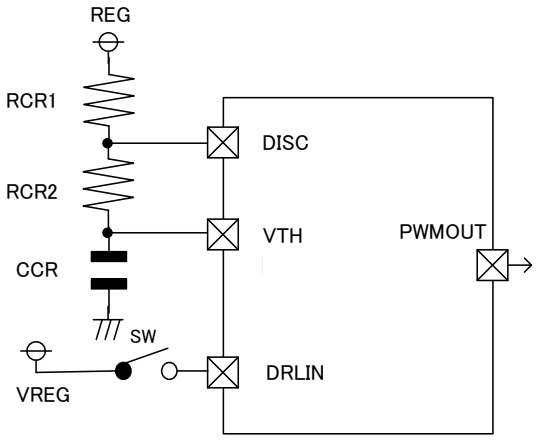
12. Procedure for external components selection

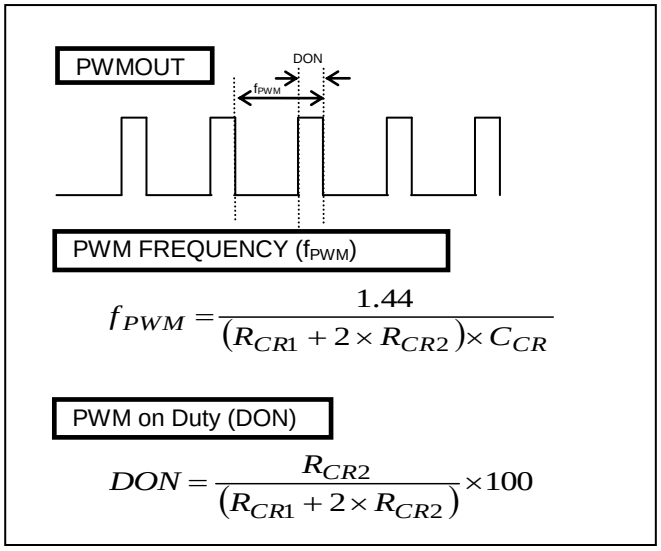
Follow the steps as shown below in selecting the external components



(1) PWM dimming frequency and ratio setting

It is possible to set the PWM frequency (f_{PWM}) and the PWM on Duty (DON) in the external resistor and capacitor using the built-in CR timer function.





(2) SCP mask timer setting

SCP mask timer (t_{SCP}) is determined by the CT terminal capacitor which is calculated using the following expression.

$$t_{SCP} = \frac{C_{CT}[\mu F] \times V_{CT}[V]}{I_{CT}[\mu A]} \times 8count$$

SCP mask timer : t_{SCP}
CT charge current 5μA (Typ) : I_{CT}
Capacitor of CT : C_{CT}
CT terminal Voltage 0.8V (Typ) : V_{CT}

In the P.14, when LED number is large or PWM dimming ratio is low, it may not satisfy the relational formula which has been described in P.14. Please connect CT terminal to GND in case the relational formula is not satisfied.

(3) Setting of the soft-start

The soft-start allows the coil current as well as the overshoot of the output voltage at the start-up to be minimized.
For the capacitance, it is recommended to be in the range of 0.001μF ~ 0.1μF. If the capacitance is less than 0.001μF, it may cause an overshoot on the output voltage while if the capacitance is greater than 0.1μF, it may cause massive reverse current through the parasitic elements of the IC and may damage the whole device.

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

(4) C_{PC} setting that meets the condition of the rise time of the output voltage such that t_{UP} < SCP mask timer t_{SCP}

The rise time of the output voltage (t_{UP}) can be calculated using the following formula.

$$t_{UP} = t_{SS} + t_{COMP}$$

$$t_{COMP} = \frac{V_{SWMAX}[V] \times C_{PC}[\mu F]}{I_{COMPSOURCE}[\mu A]} \times \frac{1}{DON}$$

Rise Time of the COMP voltage : t_{COMP}
COMP source current : $I_{COMPSOURCE}$
Capacitor of COMP : C_{PC}
PWM Dimming rate : DON
MaxDuty output voltage 2.0V (Max) : V_{SWMAX}

Please adjust C_{PC} and C_{CT} to satisfy the following relationship.

$t_{UP} < t_{SCP}$

For a guide, it is recommended that $1.2 \times t_{UP} < t_{SCP}$.

If the above formula is not satisfied, failure in the activation of the SCP may occur regardless of which application. So it is important to connect CT terminal to GND to prevent the false detection of SCP protection circuit.

(5) I_{L_MAX} from the operating conditions.

(a) Calculation of the maximum output voltage (V_{OUT})

To calculate the V_{OUT}, it is necessary to take into account the V_F variation and the number of LEDs connected in series connection.

$$V_{OUT} = (V_F + \Delta V_F) \times N + V_{REF} + R_{PWMON} \times I_{OUT}$$

V_F of LED : V_F
V_F distribution : ΔV_F
Series of LED : N
DC/DC feedback Ref voltage 0.2V (Typ) : V_{REF}
ON Resistance of PWM dimming : R_{PWMON}
LED current : I_{LED}
PWM dimming ratio : DON
Resistance of LED current setting : R_{SET}
Coil max current : I_{L_MAX}
Coil average current : I_{L_AVG}
Ripple current : ΔI_L
Power supply voltage : V_{CC}
Output voltage : V_{OUT}
Efficiency : η
DC/DCFrequency : f_{OSC}

(b) Calculation of the output current I_{LED}

$$I_{LED} = \frac{V_{REF}}{R_{SET}}$$

(c) Calculation of the input peak current I_{L_MAX}

Buck-Boost

$$I_{L\_MAX} = I_{L\_AVG} + 1/2\,\Delta I_L$$
$$I_{L\_AVG} = (V_{CC} + V_{OUT}) \times I_{LED} / (\eta \times V_{CC})$$
$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{1}{f_{OSC}} \times \frac{V_{OUT}}{V_{CC} + V_{OUT}}$$

Boost

$$I_{L\_MAX} = I_{L\_AVG} + 1/2\,\Delta I_L$$
$$I_{L\_AVG} = V_{OUT} \times I_{LED} / (\eta \times V_{CC})$$
$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{V_{OUT} - V_{CC}}{V_{OUT}} \times \frac{1}{f_{OSC}}$$

Buck

$$I_{L\_MAX} = I_{L\_AVG} + 1/2\,\Delta I_L$$
$$I_{L\_AVG} = I_{LED}$$
$$\Delta I_L = \frac{V_{OUT}}{L} \times \frac{V_{CC} - V_{OUT}}{V_{OUT}} \times \frac{1}{f_{OSC}}$$

- The worst case scenario for VCC is when it is at the minimum, and thus the minimum value should be applied in the equation.
- The L value of 6.8µH to 33µH is recommended. The current-mode type of DC/DC conversion is adopted for BD8381AEFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.
- η (Efficiency) is approximately 80% in Buck-Boost application and approximately 90% in Buck / Boost application.

(6) The setting of over-current protection

Choose R_{CS} µsing the formula $V_{OCP\_MIN}(=0.52V) / R_{CS} > I_{L\_MAX}$. When investigating the margin, please note that the L value may vary by approximately ±30%. And $I_{OCP\_MAX} = V_{OCP\_MAX}(0.68V) \div R_{CS}$.

(7) The selection of the L

In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the ranges indicated below:

Buck/Buck-Boost

$$0.05\,[V/\mu s] < \frac{V_{OUT} \times R_{CS}}{L} < 0.3 \quad [V/\mu s]$$

Boost

$$0.05\,[V/\mu s] < \frac{(V_{OUT} - V_{CC}) \times R_{CS}}{L} < 0.3 \quad [V/\mu s]$$

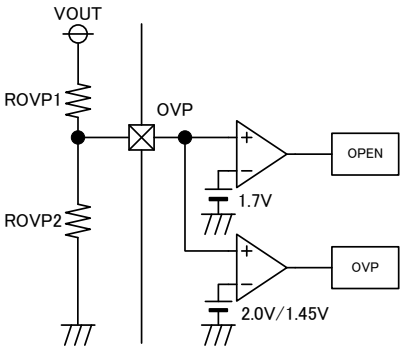
Stability will be greatly increased by reducing the calculated value but there is also a possibility that the response will be lowered.

(8) The setting of OVP voltage

It is recommended that OVP terminal voltage is set from 1.2V to 1.4V. When V_{OVP}<1.2V, it is necessary that the external components are in high voltage ratings.. When V_{OVP}>1.4V, there is a possibility that LED open protection may malfunction and by determining R_{OVP1} and R_{OVP2}, V_{OUT_MAX} can be calculated using the following formula.

$$V_{OUT\_OVPMAX} = \frac{R_{OVP1}\,[k\Omega] + R_{OVP2}\,[k\Omega]}{R_{OVP2}\,[k\Omega]} \times V_{OVP}$$

Output voltage at OVP detection : V_{OUT_OVPMAX}
OVP resistance : R_{OVP1}, R_{OVP2}
OVP detection voltage 2.1V (MAX) : V_{OVP}



$$1.2V < \frac{VOUT}{ROVP1 + ROVP2} \times ROVP < 1.4V$$

Figure 37. The circuit of OVP terminal

(9) Select coil, schottky diodes, MOSFET and R_{CS} which meet the ratings

(a) Buck-Boost application

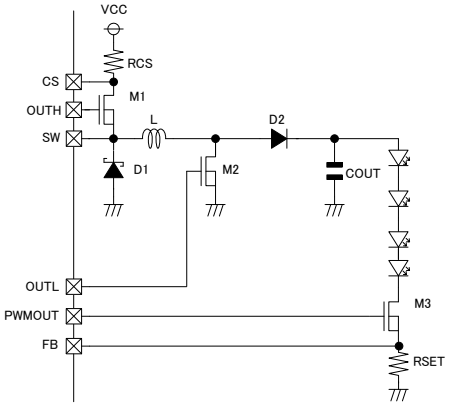


Figure 38. Buck-Boost application

	Rated current	Rated Voltage	Heat Loss
Coil L	$>I_{OCP\_MAX}$	—	—
Diode D_1	$>I_{OCP\_MAX}$	$> V_{CC\_MAX}$	—
Diode D_2	$>I_{OCP\_MAX}$	$> V_{OUT\_MAX}$	—
MOSFET M_1	$>I_{OCP\_MAX}$	$> V_{CC\_MAX}$	—
MOSFET M_2	$>I_{OCP\_MAX}$	$> V_{OUT\_MAX}$	—
R_{CS}	—	—	$> I_{OCP\_MAX2} \times R_{CS}$
C_{OUT}	—	$> V_{OUT\_MAX}$	—
MOSFET M_3	$> I_{LED\_MAX}$	$> V_{OUT\_MAX}$	—
R_{SET}	—	—	$> I_{OCP\_MAX2} \times R_{SET}$

Note: In consideration of the external component variations, please design with sufficient margin.

Note: V_{CC_MAX} is the maximum supply voltage, V_{OUT_MAX} is the maximum output voltage detect by OVP.

(b) Boost application

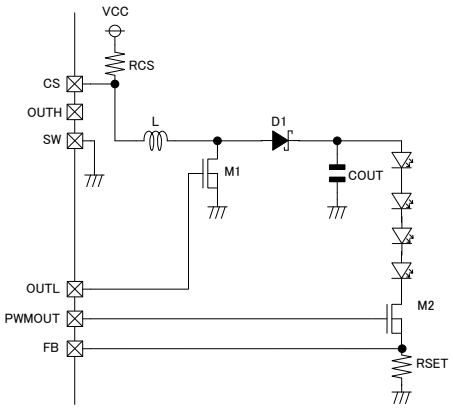


Figure 39. Boost application

	Rated current	Rated Voltage	Heat Loss
Coil L	$>I_{OCP\_MAX}$	—	—
Diode D_1	$>I_{OCP\_MAX}$	$> V_{OUT\_MAX}$	—
MOSFET M_1	$>I_{OCP\_MAX}$	$> V_{OUT\_MAX}$	—
R_{CS}	—	—	$> I_{OCP\_MAX2} \times R_{CS}$
C_{OUT}	—	$> V_{OUT\_MAX}$	—
MOSFET M_2	$> I_{LED\_MAX}$	$> V_{OUT\_MAX}$	—
R_{SET}	—	—	$> I_{OCP\_MAX2} \times R_{SET}$

Note: In consideration of the external component variations, please design with sufficient margin.

Note: V_{CC_MAX} is the maximum supply voltage, V_{OUT_MAX} is the maximum output voltage detect by OVP.

(c) Buck application

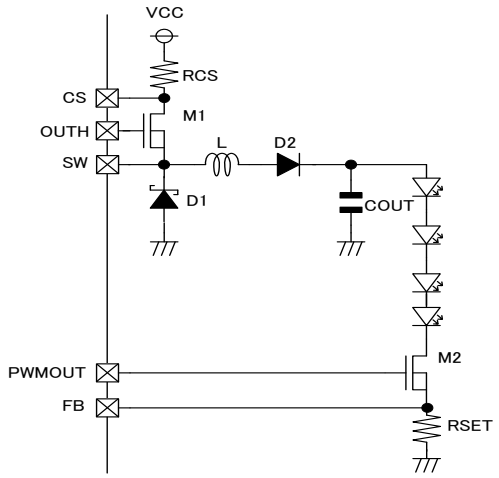


Figure 40. Buck application

	Rated current	Rated Voltage	Heat Loss
Coil L	$>I_{OCP\_MAX}$	—	—
Diode D_1	$>I_{OCP\_MAX}$	$> V_{CC\_MAX}$	—
Diode D_2	$>I_{OCP\_MAX}$	$> V_{OUT\_MAX}$	—
MOSFET M_1	$>I_{OCP\_MAX}$	$> V_{CC\_MAX}$	—
R_{CS}	—	—	$> I_{OCP\_MAX2} \times R_{CS}$
C_{OUT}	—	$> V_{CC\_MAX}$	—
MOSFET M_2	$> I_{LED\_MAX}$	$> V_{CC\_MAX}$	—
R_{SET}	—	—	$> I_{OCP\_MAX2} \times R_{SET}$

Note: In consideration of the external component variations, please design with sufficient margin.
Note: V_{CC_MAX} is the maximum supply voltage, V_{OUT_MAX} is the maximum output voltage detect by OVP.

(10) Selection of the output capacitor

Select the output capacitor C_{OUT} based on the requirement of the ripple voltage Vpp.

Buck-Boost

$$Vpp = \frac{I_{LED}}{C_{OUT}} \times \frac{V_{CC}}{V_{OUT} + V_{CC}} \times \frac{1}{f_{OSC}} + (I_{L\_MAX} + \Delta I_L / 2) \times R_{ESR}$$

ESR of output capacitor :R_{ESR}

Buck

$$Vpp = \frac{1}{C_{OUT}} \times \frac{I_{LED}}{\eta} \times \frac{1}{f_{OSC}} + (I_{L\_MAX} \times R_{ESR})$$

Boost

$$Vpp = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{8} \times \frac{1}{C_{OUT}} \times \frac{1}{f_{OSC}}$$

(11) Selection of the input capacitor

A capacitor at the input is also required as the peak current flows between the input and the output terminals in DC/DC conversion. We recommend an input capacitor greater than 10µF with the ESR smaller than 100mΩ. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence may lead to malfunction.

(12) Phase Compensation Guidelines

In general, the negative feedback loop is stable when the following condition is met:

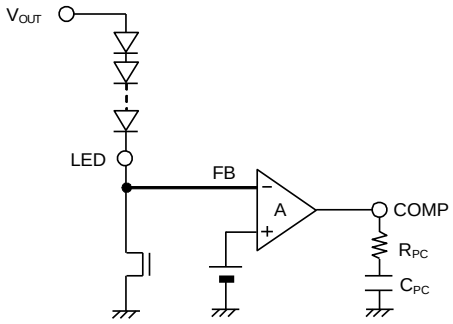
(a) Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., Phase margin of 30º or more)
However, as the DC/DC converter constantly samples the switching frequency, the gain-bandwidth (GBW) product of the entire series should be set to 1/10 of the switching frequency of the system. Therefore, the overall stability characteristics of the application are as follows:
(b) Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., Phase margin of 30º or more)
(c) GBW (frequency at gain 0dB) of 1/10 of the switching frequency
Thus, to improve response within the GBW product limits, the switching frequency must be increased.

The key for achieving stability is to place fz near to the GBW. GBW is decided by phase delay fp1 in terms of C_{OUT} and output impedance R_L. fz and fp1 are defined by the following formula.

$$Phase-lead \quad fz = \frac{1}{2\pi CpcRpc} \quad [Hz]$$

$$Phase-lag \quad fp1 = \frac{1}{2\pi RLC_{OUT}} \quad [Hz]$$

$$R_L = \frac{V_{OUT}}{I_{OUT}} [\Omega]$$



Good stability would be obtained when the fz is set between 1kHz to 10kHz.
Please substitute the value of the maximum load for RL.

In Buck-Boost/ Buck application, Right-Hand-Plane (RHP) Zero exists. This Zero has no gain but a pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, it is necessary to bring this zero before the GBW.

$$f_{RHP} = \frac{V_{OUT} \times (V_{CC}/(V_{OUT}+V_{CC}))^2}{2\pi \times I_{OUT} \times L} \quad [Hz]$$

where:
I_{OUT}: Maximum Load Current

It is important to keep in mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuit. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

(13) Verification of the operation by taking measurements

The overall characteristic may change by load current, input voltage, output voltage, inductance, load capacitance, switching frequency and the PCB layout. We strongly recommend verifying your design by taking the actual measurements.

13. Calculation of the Power consumption

(1) Buck-Boost application

$$Pc(N) = I_{CC} \times V_{CC} + \frac{1}{2} \times Ciss1 \times (V_{REG})^2 \times f_{OSC} \times 2 \times 2 + \frac{1}{2} \times Ciss2 \times (V_{REG})^2 \times f_{PWM} \times 2$$

LSI Operation Power consumtio — IC power consumption of external FET driver for DC/DC switching — OUTH/OUTL FET 2conponents — IC power consumption of external FET driver for PWM dimming

(2) Boost or Buck application

$$Pc(N) = I_{CC} \times V_{CC} + \frac{1}{2} \times Ciss1 \times (V_{REG})^2 \times f_{OSC} \times 2 \times 1 + \frac{1}{2} \times Ciss2 \times (V_{REG})^2 \times f_{PWM} \times 2$$

LSI Operating Power consumption — IC power consumption of external FET driver for DC/DC switching — OUTH/OUTL FET 1conponent — IC power consumption of external FET driver for PWM dimming

Where:

I_{CC} : Maximum circuit Current
V_{CC} : Power supply voltage
C_{iss1} : External FET capacity of DC/DC switching
f_{OSC} : DC/DC switching frequency
C_{iss2} : External FET capacity of PWM dimming
f_{PWM} : PWM frequency
N : PCB layers

<Sample Calculation > When we assume value for Pc such as:
I_{CC}=7mA, V_{CC}=30V, C_{iss1}=500pF, f_{OSC}=300kHz, f_{PWM}=200Hz, C_{iss2}=1500pF, N=4Layer

$$Pc(4) = 7mA \times 30V + \frac{1}{2} \times 500\,pF \times 5V \times 300\,kHz \times 5V \times 2 \times 2 + \frac{1}{2} \times 1500\,pF \times 5V \times 200\,Hz \times 5V \times 2$$

it becomes Pc = approximately 210mW.

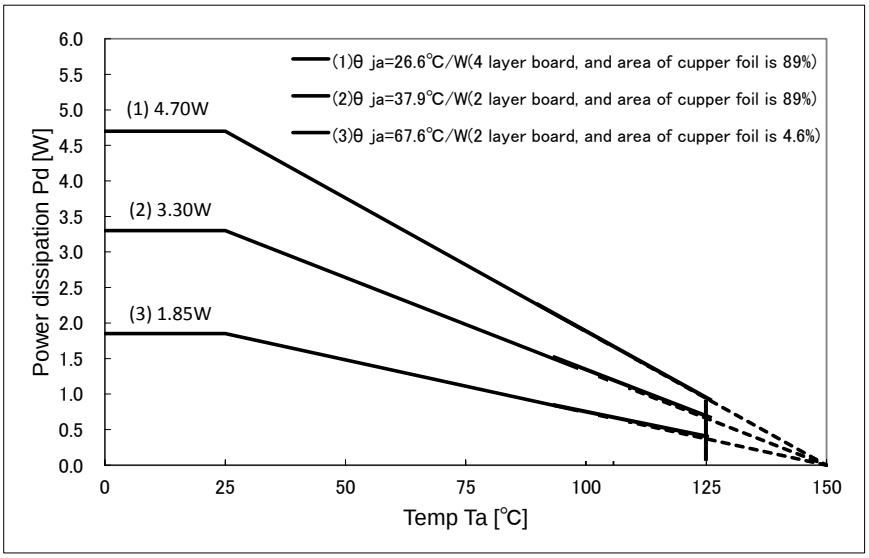


Figure 41

Note1: The value of Power consumption: on glass epoxy board measuring 70mmx70mmx1.6mm
(1 layer board/Copper foil thickness 18um)
Note2: The value changes depending on the density of the board copper foil.
However, this value is an actual measurement value and no guarantee value.

HTSSOP-B28

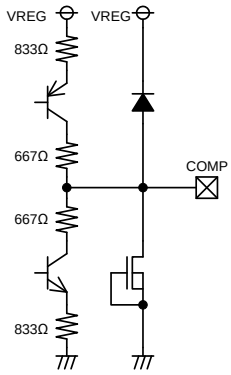
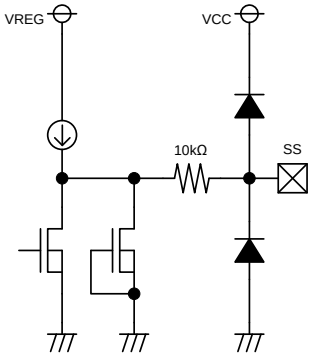
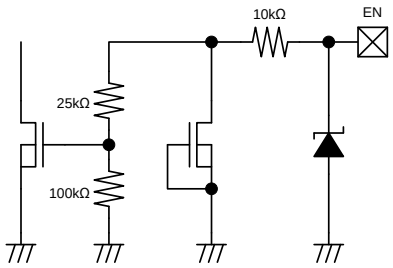
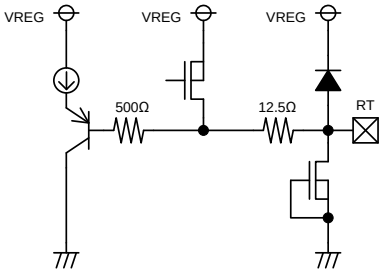
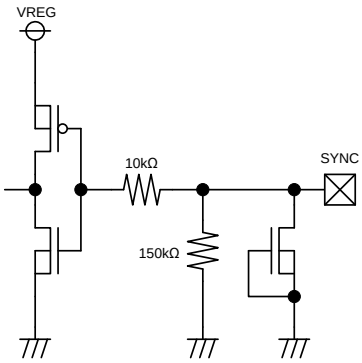
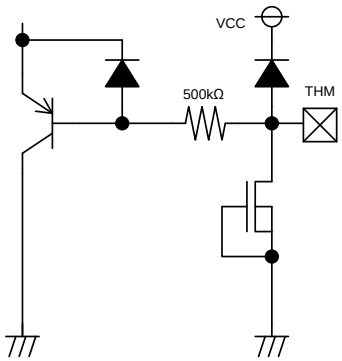
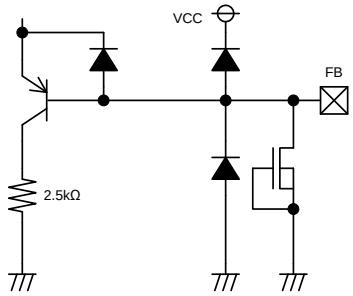
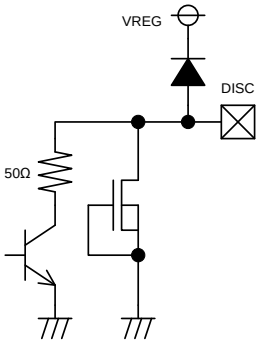
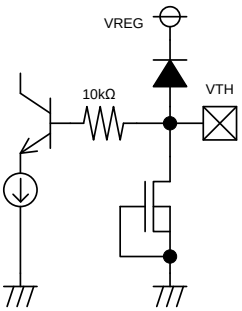
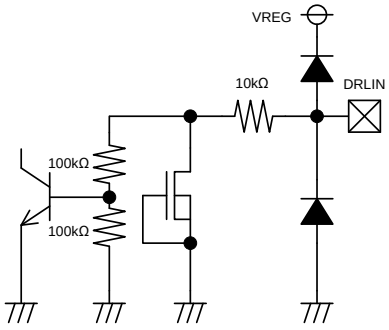
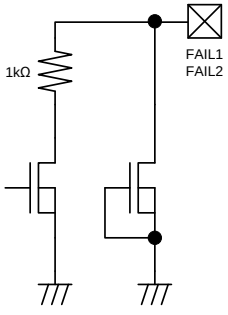
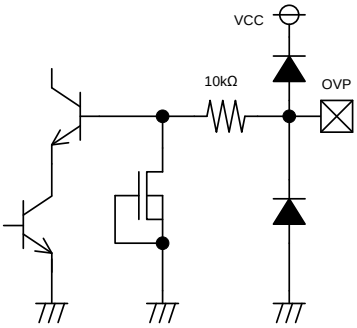
Pd=1.85W (0.37W): Board copper foil area 225mm^2

Pd=3.30W (0.66W): Board copper foil area 4900mm^2

Pd=4.70W (0.94W): Board copper foil area 4900mm^2

The value in () is an power dissipation in Ta = 125 degrees.

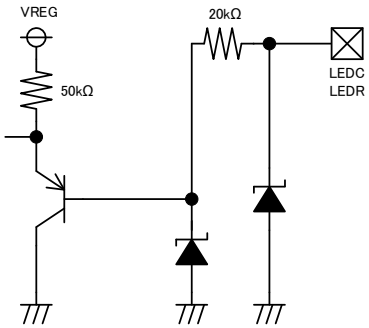
I/O Equivalent Circuits

1. COMP	2. SS	4. EN
		
5. RT	**6. SYNC**	**8. THM**
		
9. FB	**10. DISC**	**11. VTH**
		
12. DRLIN	**13,14. FAIL1,FAIL2**	**15. OVP**
		

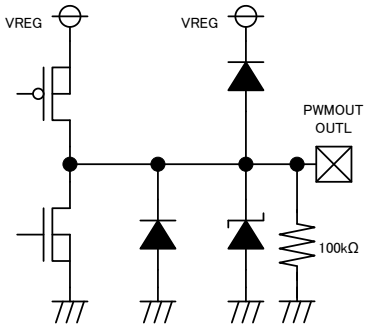
(Note) The values are all Typ value.

I/O Equivalent Circuits – continued

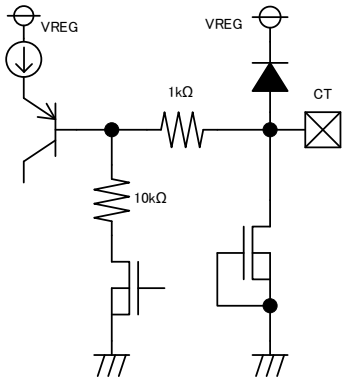
16,17. LEDC, LEDR



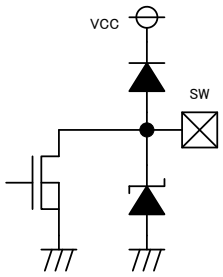
19,22. PWMOUT, OUTL



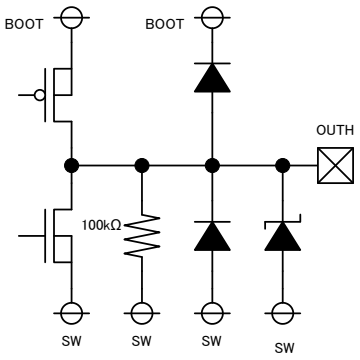
20. CT



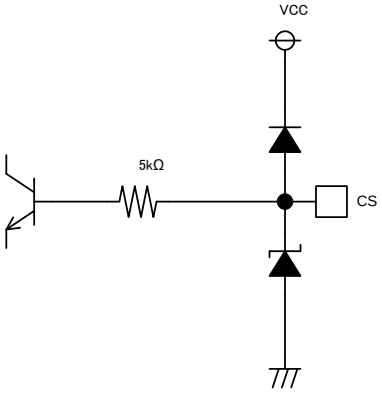
24. SW



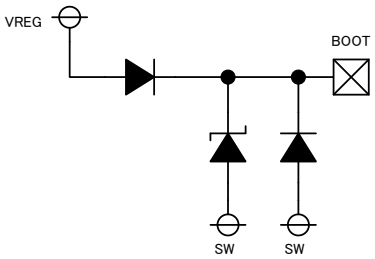
25. OUTH



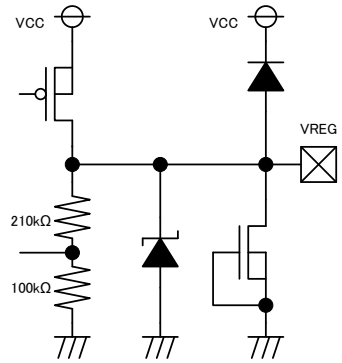
26. CS



27. BOOT



28. VREG



(Note) The values are all Typ value.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

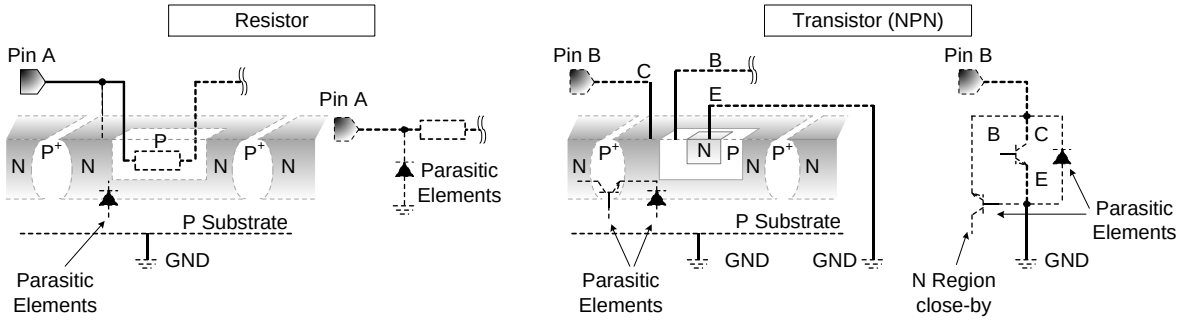


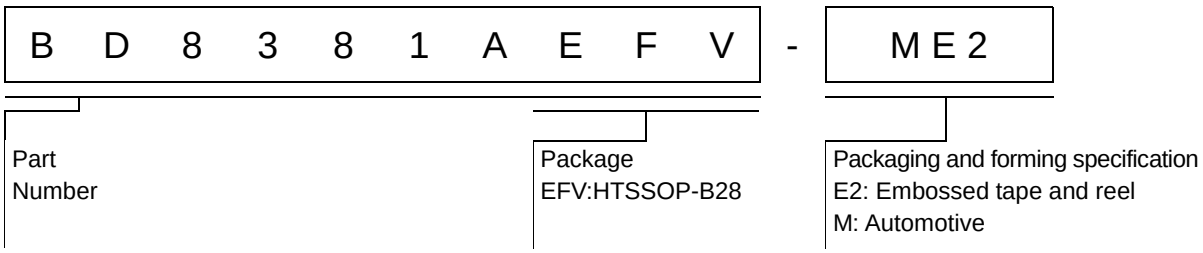
Figure 42. Example of monolithic IC structure

13. **Area of Safe Operation (ASO)**
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

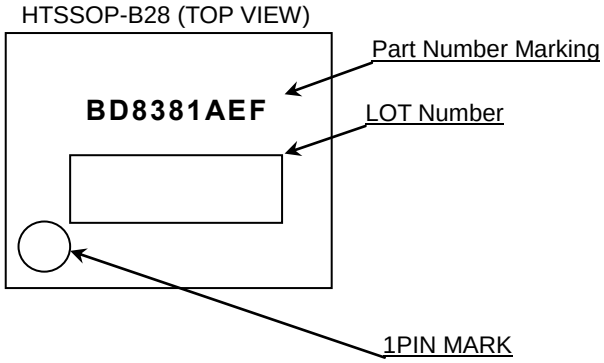
14. **Thermal Shutdown Circuit(TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

TSD ON temperature [°C] (typ)	Hysteresis temperature [°C] (typ)
175	25

Ordering Information

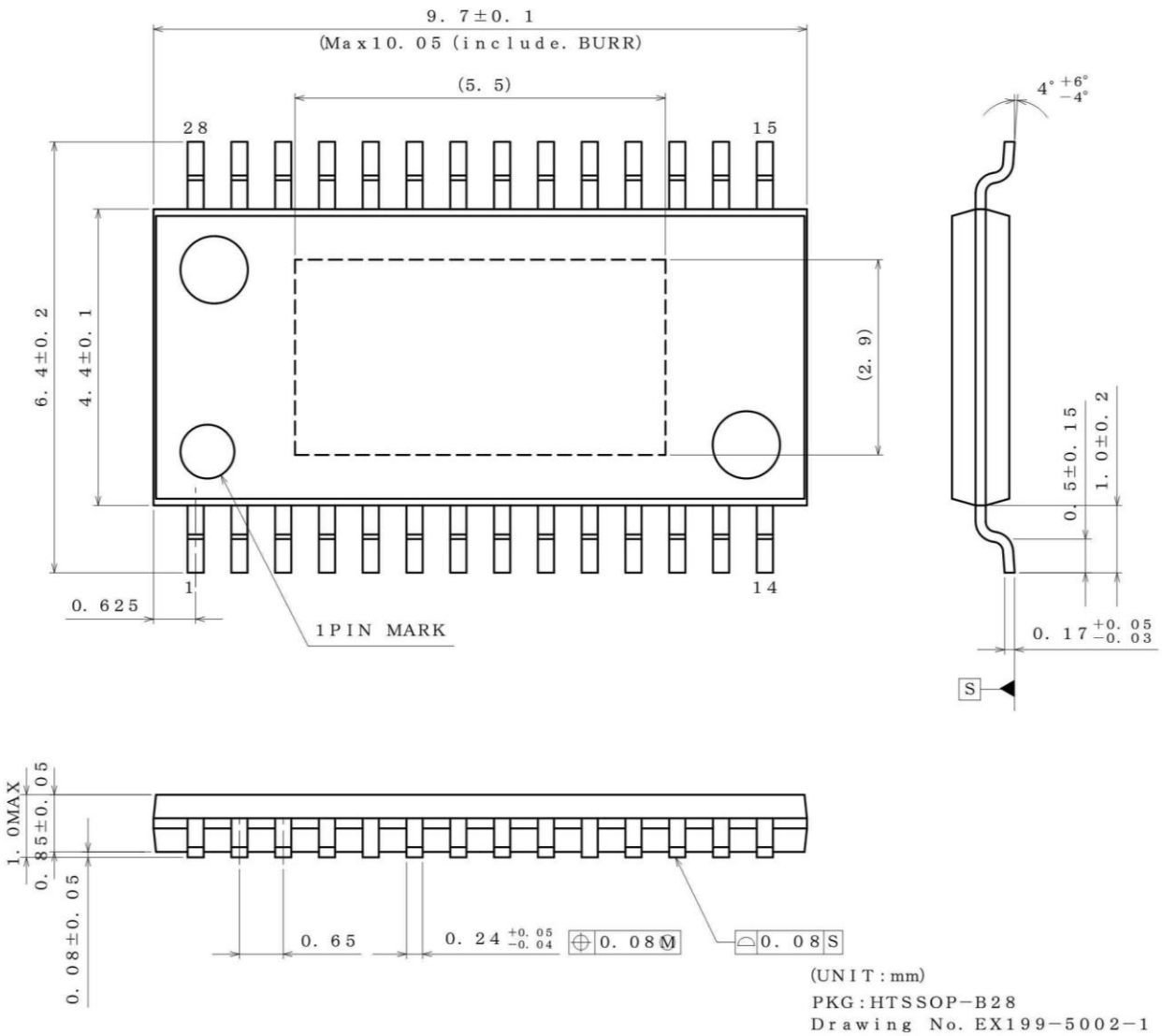


Marking Diagram



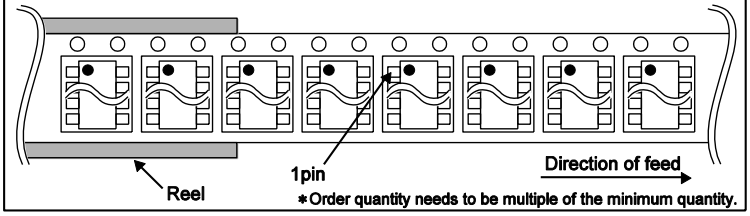
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
31.Oct.2014	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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