DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

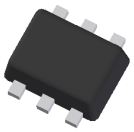
Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Very Low Gate Threshold Voltage, 1.2V max
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

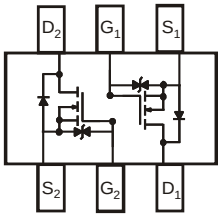
Mechanical Data

- Case: SOT563
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.006 grams (Approximate)

SOT563



Top View



Top View
Schematic and Transistor Diagram

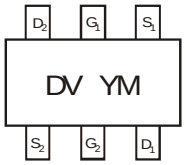
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN32D2LV-7	SOT563	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html

Marking Information

SOT563



DV = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: U = 2007)
M = Month (ex: 9 = September)

Date Code Key

Year	2007	---	2014	2015	2016	2017	2018	2019	2020	2021
Code	U	---	B	C	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±10	V
Drain Current (Note 5)	I_D	400	mA

Thermal Characteristics

Total Power Dissipation (Note 5)	P_D	450	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	313	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)							
Drain-Source Breakdown Voltage		BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	@T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 30V, V_{GS} = 0V
Gate-Body Leakage	@T_J = +25°C	I_{GSS}	—	— — ±1	±10 ±500 ±100	µA nA nA	V_{GS} = ±10V, V_{DS} = 0V V_{GS} = ±5V, V_{DS} = 0V V_{GS} = ±2.5V, V_{DS} = 0V
Gate-Body Leakage (Note 7)	@T_J = +105°C @T_J = +125°C	I_{GSS}	—	±8 ±15	±100 ±100	nA nA	V_{GS} = ±2.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)							
Gate Threshold Voltage		$V_{GS(TH)}$	0.6	—	1.2	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance		$R_{DS(ON)}$	— — —	— — —	2.2 1.5 1.2	Ω	V_{GS} = 1.8V, I_D = 20mA V_{GS} = 2.5V, I_D = 20mA V_{GS} = 4.0V, I_D = 100mA
Forward Transconductance		$\|Y_{FS}\|$	100	—	—	mS	V_{DS} =10V, I_D = 0.1A
Source-Drain Diode Forward Voltage		V_{SD}	0.5	—	1.4	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 7)							
Input Capacitance		C_{ISS}	—	39	—	pF	V_{DS} = 3V, V_{GS} = 0V f = 1.0MHz
Output Capacitance		C_{OSS}	—	10	—	pF	
Reverse Transfer Capacitance		C_{RSS}	—	3.6	—	pF	
Switching Time	Turn-On Time	t_{ON}	—	11	—	ns	V_{DD} = 5V, I_D = 10 mA, V_{GS} = 5V
	Turn-Off Time	t_{OFF}	—	51	—	ns	

Notes: 5. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found at http://www.diodes.com/datasheets/ap02001.pdf.
6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

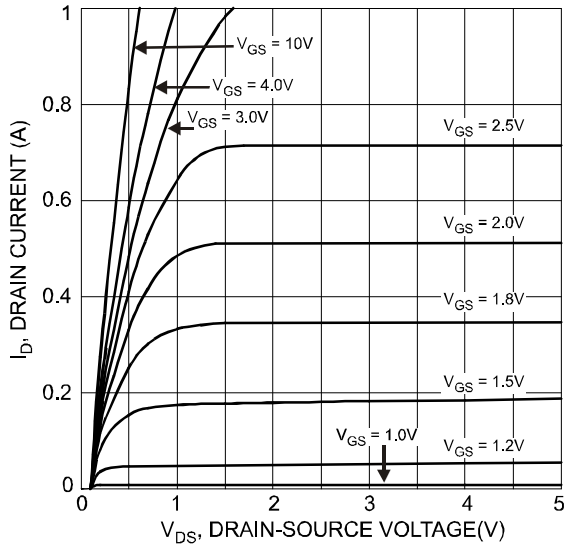


Fig. 1 Typical Output Characteristics

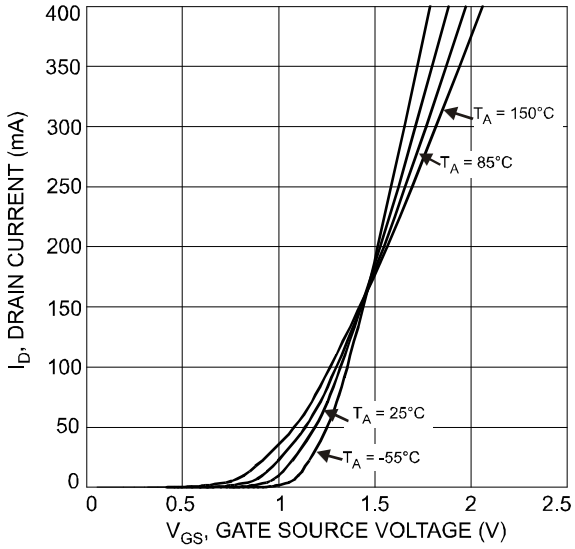


Fig. 2 Typical Transfer Characteristics

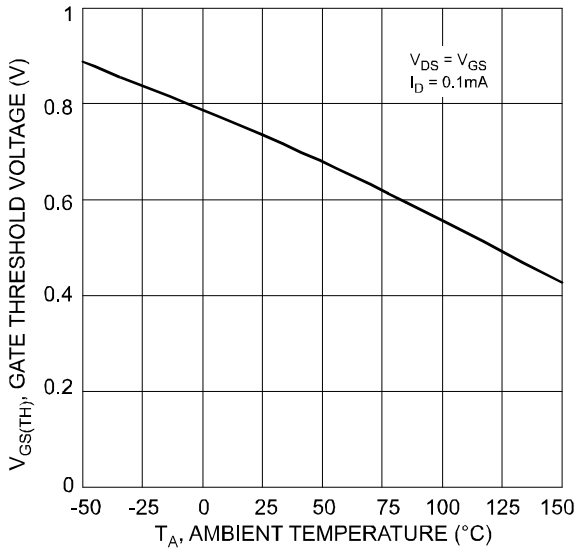


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

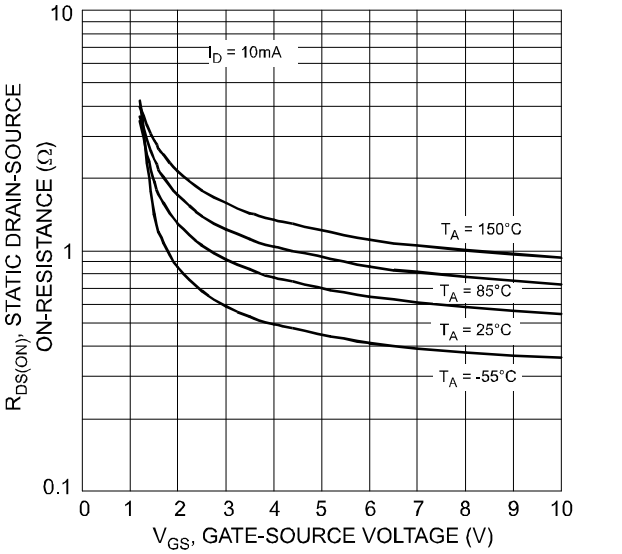


Fig. 4 Static Drain-Source On-Resistance vs. Gate-Source Voltage

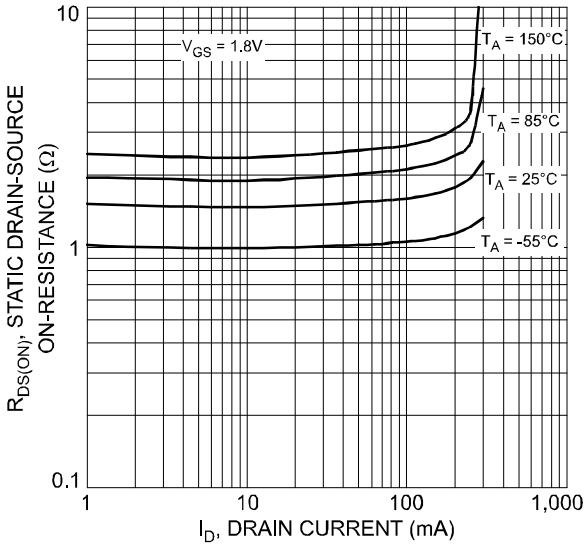


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

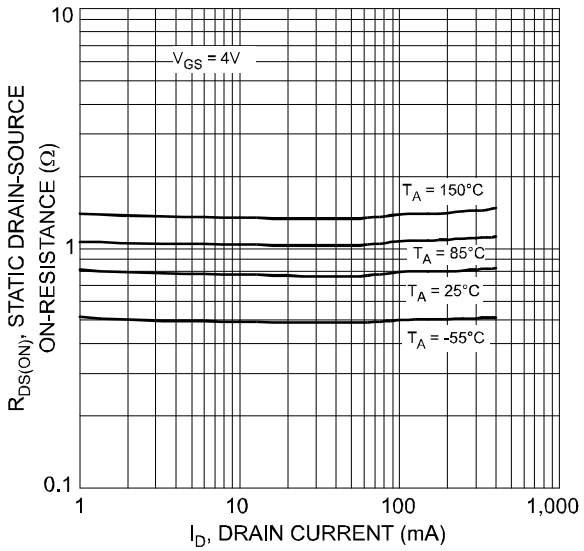


Fig. 6 Static Drain-Source On-Resistance vs. Drain Current

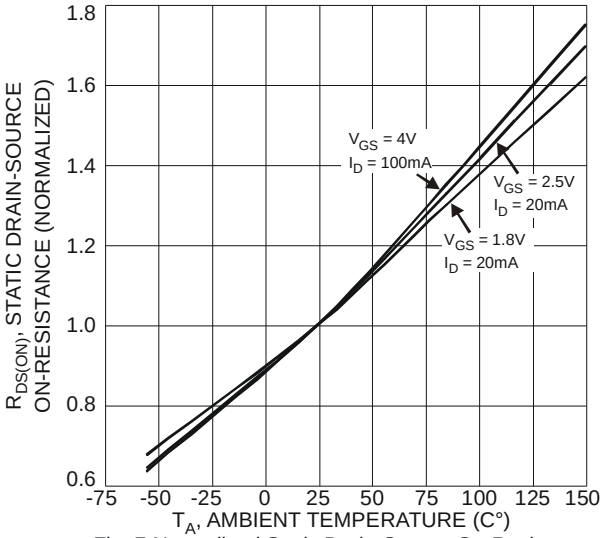


Fig. 7 Normalized Static Drain-Source On-Resistance vs. Ambient Temperature

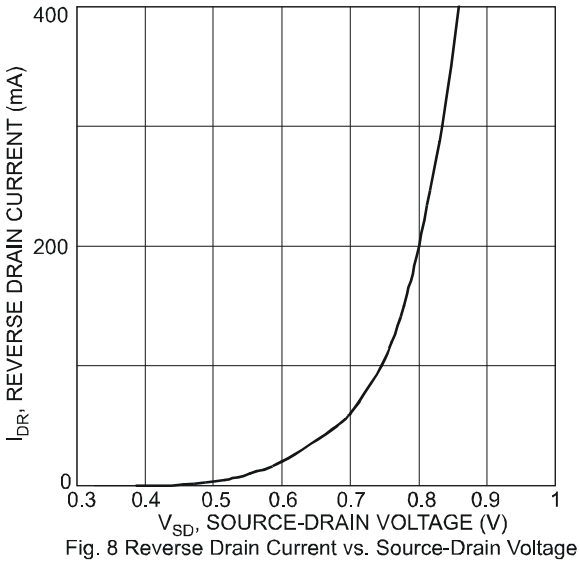


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

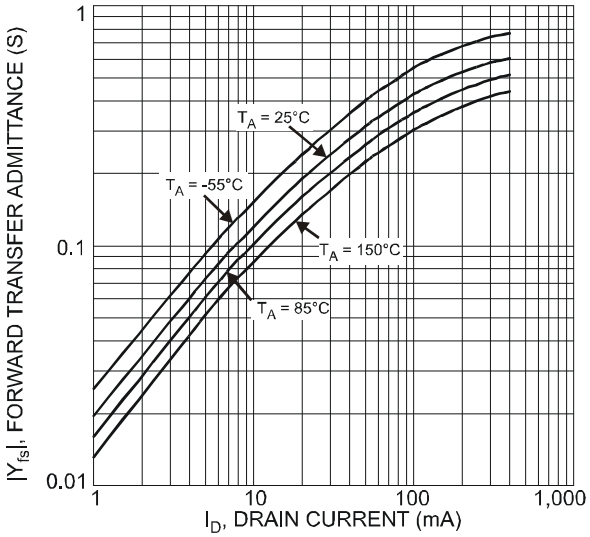


Fig. 9 Forward Transfer Admittance vs. Drain Current

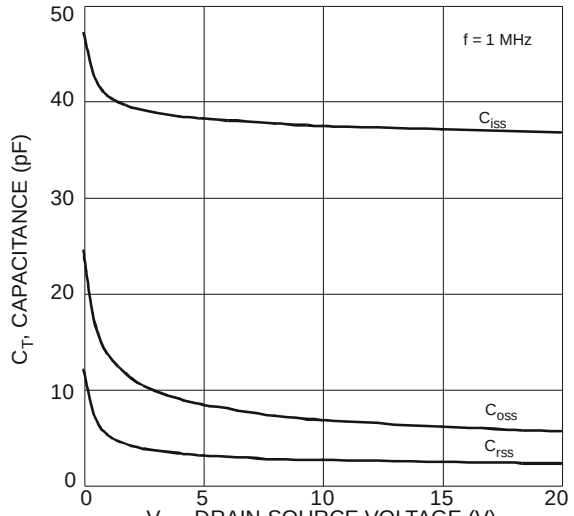


Fig. 10 Typical Capacitance

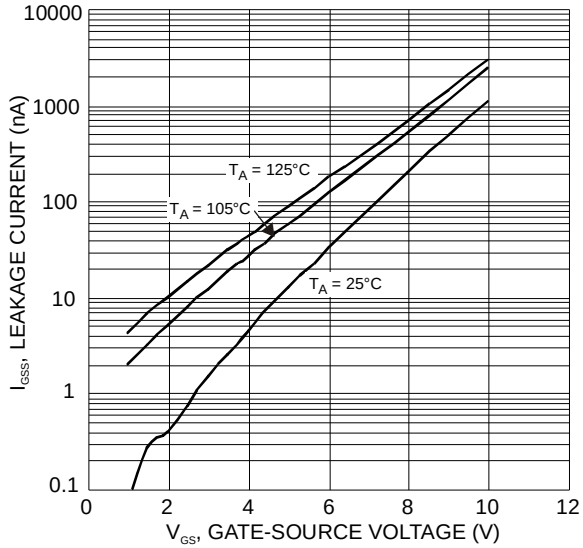


Fig.11 Gate-Source Leakage Current vs Voltage

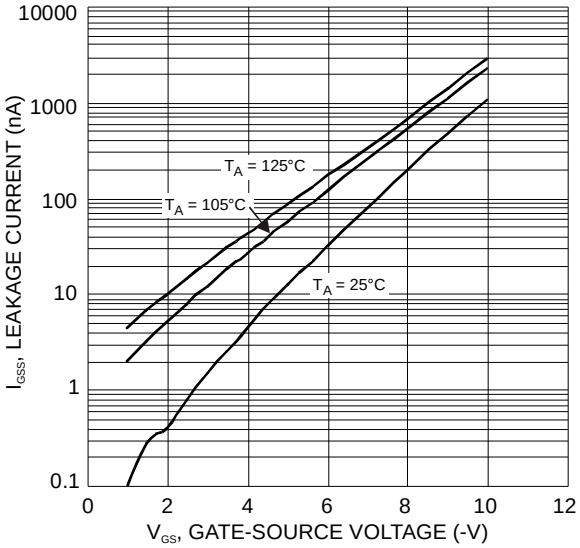
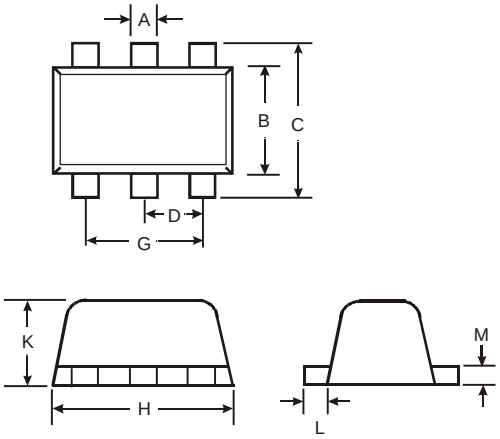


Fig.12 Gate-Source Leakage Current vs Voltage

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

SOT563



SOT-563			
Dim	**Min**	**Max**	**Typ**
A	0.15	0.30	0.20
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D	—	—	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.55	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

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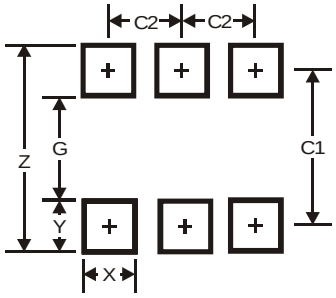

Dimensions	Value (in mm)
Z	2.2
G	1.2
X	0.375
Y	0.5
C1	1.7
C2	0.5

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