HARRIS SEMICONDUCTOR

CA3227, CA3246

High-Frequency NPN Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

August 1996

Features

- **Gain-Bandwidth Product (f_T) . . . . . >3GHz**
- **Five Transistors on a Common Substrate**

Applications

- **VHF Amplifiers**
- **VHF Mixers**
- **Multifunction Combinations-RF/Mixer/Oscillator**
- **IF Converter**
- **IF Amplifiers**
- **Sense Amplifiers**
- **Synthesizers**
- **Synchronous Detectors**
- **Cascade Amplifiers**

Description

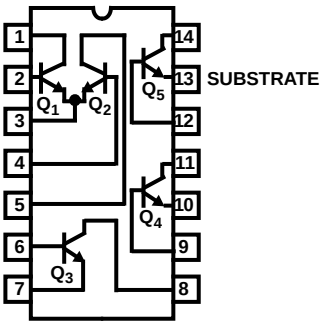
The CA3227 and CA3246 consist of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

Ordering Information

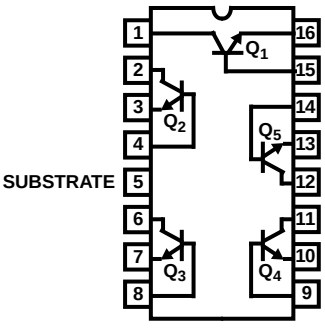
PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3227E	-55 to 125	16 Ld PDIP	E16.3
CA3227M (3227)	-55 to 125	16 Ld SOIC	M16.15
CA3227M96 (3227)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3246E	-55 to 125	14 Ld PDIP	E14.3
CA3246M (3246)	-55 to 125	14 Ld SOIC	M14.15
CA3246M96 (3246)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinouts

CA3246
(PDIP, SOIC)
TOP VIEW



CA3227
(PDIP, SOIC)
TOP VIEW



File Number **1345.3**

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}) 8V
Collector-to-Base Voltage (V_{CBO}) 12V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Collector Current (I_C) 20mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
14 Ld PDIP Package	100
14 Ld SOIC Package	185
16 Ld PDIP Package	90
16 Ld SOIC Package	175

Maximum Power Dissipation (Any One Transistor) 85mW
Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (Terminal 5 (CA3227) and Terminal 13 (CA3246)) must be connected to the most negative point in the external circuit to maintain isolation be tween transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		12	20	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		8	10	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{C1} = 10\mu A$, $I_B = 0$, $I_E = 0$		20	-	-	V
Emitter-Cutoff-Current (Note 3)	I_{EBO}	$V_{EB} = 4.5V$, $I_C = 0$		-	-	10	µA
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 5V$, $I_B = 0$		-	-	1	µA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 8V$, $I_E = 0$		-	-	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 6V$	$I_C = 10mA$	-	110	-	
			$I_C = 1mA$	40	150	-	
			$I_C = 0.1mA$	-	150	-	
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6V$	$I_C = 1mA$	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$		-	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$		0.74	-	0.94	V

NOTES:

3. On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse break-down. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

Electrical Specifications

$T_A = 25^oC$, 200MHz, Common Emitter, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL		TEST CONDITION	TYPICAL VALUES	UNITS
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR					
Input Admittance	Y_{11}	b_{11}	I_C = 1mA, V_{CE} = 5V	4	mS
		g_{11}		0.75	mS
Output Admittance	Y_{22}	b_{22}	I_C = 1mA, V_{CE} = 5V	2.7	mS
		g_{22}		0.13	mS
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 1mA, V_{CE} = 5V	29.3	mS
		θ_{21}		-33	Degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 1mA, V_{CE} = 5V	0.38	mS
		θ_{12}		-97	Degrees
Input Admittance	Y_{11}	b_{11}	I_C = 10mA, V_{CE} = 5V	4.8	mS
		g_{11}		2.85	mS
Output Admittance	Y_{22}	b_{22}	I_C = 10mA, V_{CE} = 5V	2.75	mS
		g_{22}		0.9	mS
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 10mA, V_{CE} = 5V	95	mS
		θ_{21}		-62	Degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 10mA, V_{CE} = 5V	0.39	mS
		θ_{12}		-97	Degrees
Small Signal Forward Current Transfer Ratio	h_{21}		I_C = 1mA, V_{CE} = 5V	7.1	
			I_C = 10mA, V_{CE} = 5V	17	
TYPICAL CAPACITANCE AT 1MHz, THREE-TERMINAL MEASUREMENT					
Collector-to-Base Capacitance	C_{CB}		V_{CB} = 6V	0.3	pF
Collector-to-Substrate Capacitance	C_{CI}		V_{CI} = 6V	1.6	pF
Collector-to-Emitter Capacitance	C_{CE}		V_{CE} = 6V	0.4	pF
Emitter-to-Base Capacitance	C_{EB}		V_{EB} = 3V	0.75	pF

Spice Model (Spice 2G.6)

.model NPN

+	BF = 2.610E + 02	BR = 4.401E + 00	IS = 6.930E - 16	RB = 130.0E + 00
+	RC = 1.000E + 01	RE = 7.396E - 01	VA = 6.300E + 01	VB = 2.208E + 00
+	IK = 1.000E - 01	ISE = 1.87E - 14	NE = 1.653E + 00	IKR = 1.000E - 02
+	ISC = 9.25E - 14	NC = 1.333E + 00	TF = 1.775E - 11	TR = 1.000E - 09
+	CJS = 1.800E - 12	CJE = 1.010E - 12	PE = 8.350E - 01	ME = 4.460E - 01
+	CJC = 9.100E - 13	PC = 3.850E - 01	MC = 2.740E - 01	KF = 0.000E + 00
+	AF = 1.000E + 00	EF = 1.000E + 00	FC = 5.000E - 01	PJS = 5.410E - 01
+	MJS = 3.530E - 01	RBM = 30.00	RBV = 100	IRB = 0.00

Please Note: No measurements have been made to model the reverse AC operation (tr is an estimation).

Typical Performance Curves

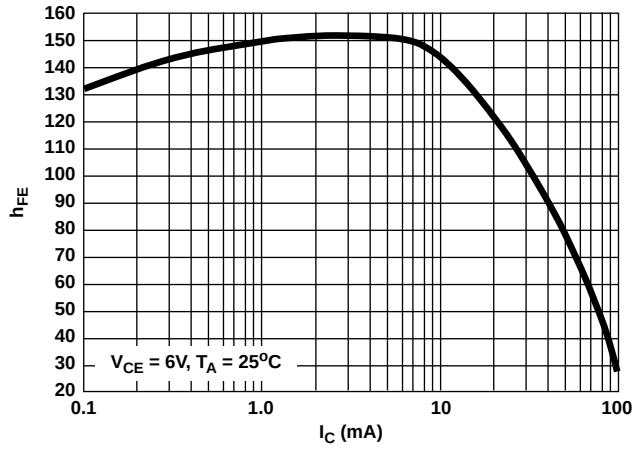


FIGURE 1. h_{FE} vs COLLECTOR CURRENT

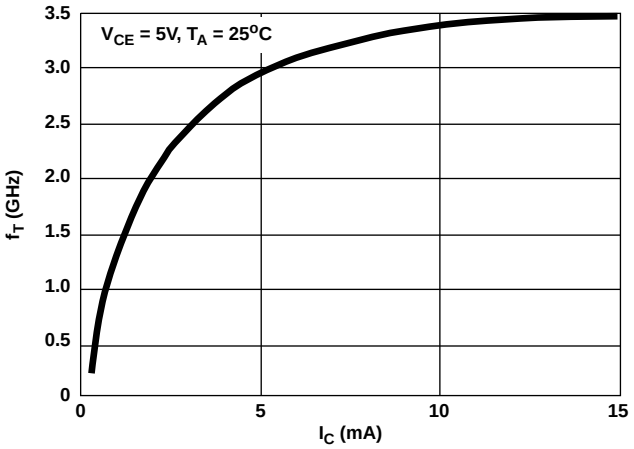


FIGURE 2. f_T vs COLLECTOR CURRENT

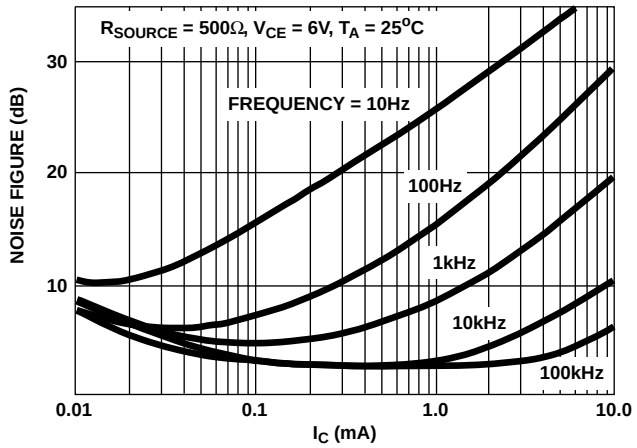


FIGURE 3. NOISE FIGURE vs COLLECTOR CURRENT

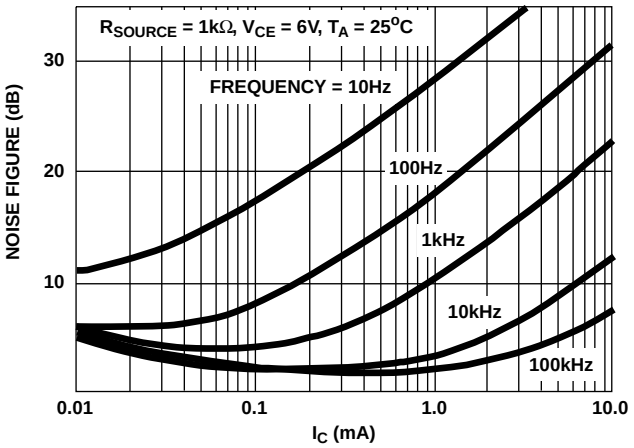


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

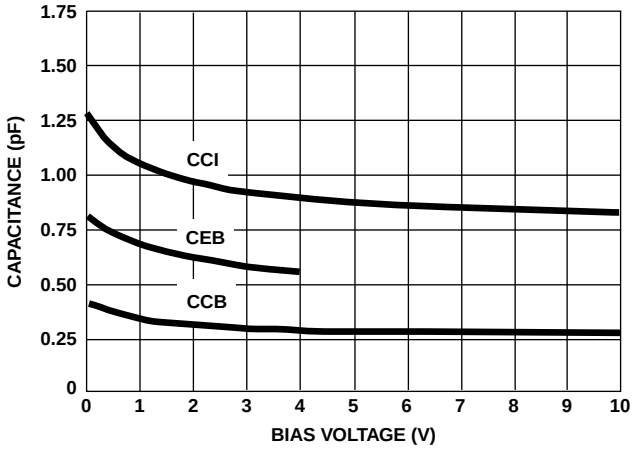


FIGURE 5. CAPACITANCE vs BIAS VOLTAGE

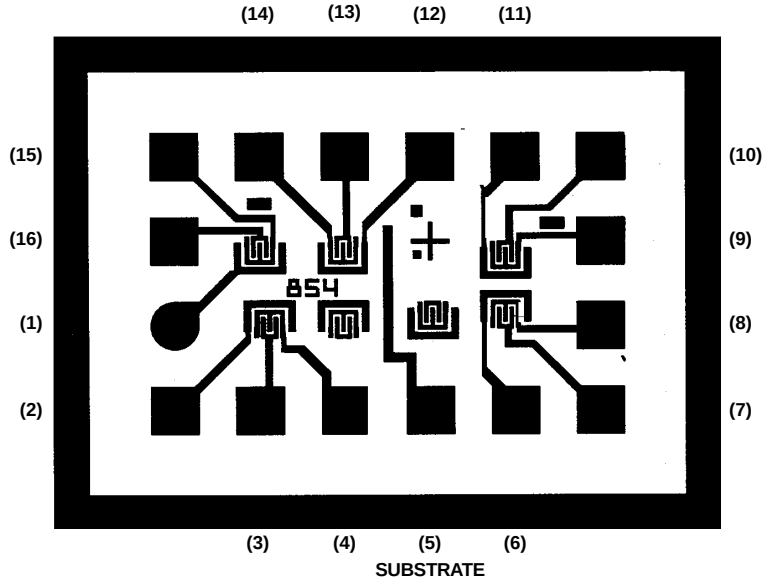
Die Characteristics

DIE DIMENSIONS:

46 mils x 32 mils - CA3227
47 mils x 33 mils - CA3246

Metallization Mask Layout

CA3227



CA3246