Product Selector
Compare Development Boards

Development Boards
All Development Kits
All Daughter Cards

Boards By Device
Stratix
Arria
Cyclone
MAX

Boards By Technology
ASIC Prototyping
DSP
Embedded Processors
Transceivers
General Purpose

Board Partners
List of Board Partners

Programming Hardware
Download Cables
Programming Adapters

100G Development Kit, Stratix V GX Edition

Home > Design Tools & Services > Development Kits/Cables > 100G Development Kit, Stratix V GX Edition

from *Altera*

Altera's 100G Development Kit, Stratix® V GX Edition enables a thorough evaluation of 100G designs by allowing you to:

- Support 10G/40G and 100G line interfaces through optical modules
- Support applications requiring external memory interfaces, through 6x32-bit DDR3 and 1x36- and 1x18-bit QDRII BL2 memory banks
- Use system-side interfaces via two pairs of FCI AirMax connectors
- Complete line-side (optical modules) to system-side (AirMax connector) datapath analysis
- Evaluate transceiver performance up to 12.5 Gbps
- Verify physical medium attachment (PMA) compliance to 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, and other major standards
- Validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP

Ordering Information

Table 1. Altera's 100G Development Kit, Stratix V GX Edition Ordering Information

Ordering Code	Price	Ordering Information
DK-100G-5SGXEA7N	$24,995	In North America, call 1-888-800-0631 or contact your local distributor. For International Sales, contact your local distributor.

Development Kit Contents

The 100G Development Kit, Stratix V GX Edition has the following features:

- Stratix V GX development board (see Figure 1)
  - Featured device: 5SGXEA7N2F45C2N
  - EPM2210F324C3N, MAX® II 324-pin CPLD
- FPGA configuration
  - Fast Passive Parallel (FPP) configuration
  - 1-Gb flash storage for two configuration images (factory and user)
  - On-board USB-Blaster™ II cable for use with the Quartus® II Programmer, Nios® II software and System Console
  - JTAG header for external USB-Blaster cable
- Memory
  - Twelve 2-Gb DDR3 SDRAM
  - Two 72-Mb QDR II SRAM
- General user input/output
  - Four user push buttons
  - Two DIP switches
  - Eight user LEDs
  - Two-line character LCD
  - Ten configuration status LEDs
- Components and interfaces
  - 10/100/1000 Ethernet PHY and RJ-45 jack
  - 48 transceiver channels
    - Two channels for SMA interface
    - Four channels for SFP+ interface
    - Eight channels for QSFP interface
    - 10 channels for CFP interface
    - 24 channels for Interlaken interface
- Temperature measurement circuitry
  - Die temperature
- Power
  - 19-V DC input
  - 2.5-mm barrel jack for DC power input
  - On/off power slide switch
  - On-board power measurement circuitry
- Quartus II software license is not included as part of this kit

Figure 1. Stratix V GX 100G Development Kit

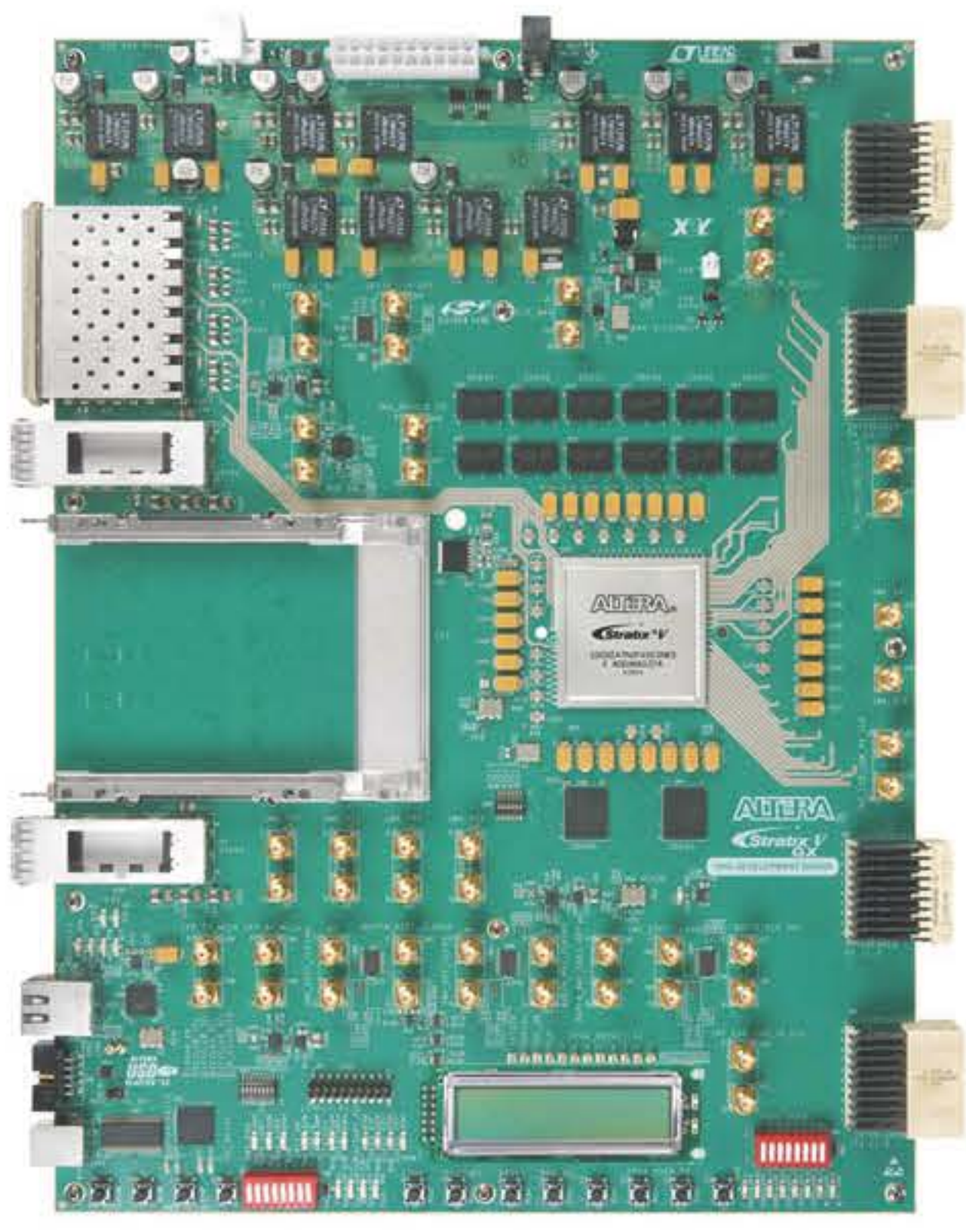

Table 2. Collateral for the 100G Development Kit, Stratix V GX Edition

Document	Description	Version
***User Guide* (PDF)**	Information about setting up the 100G Development Kit and using the included software.	11.1
***Reference Manual* (PDF)**	Detailed information about board components and interfaces.	11.1
Kit Installation (For boards with ES Silicon)	Full installation of all files included in the development kit, including the reference manual, user guide, quick-start guide, BOM, layout, PCB, schematics, Board Update Portal example file, and so on.	11.1
Kit Installation	Full installation of all files included in the development kit, including the reference manual, user guide, quick-start guide, BOM, layout, PCB, schematics, Board Update Portal example file, and so on.	12.0

Rate This Page

Please give us feedback