

MN1020012A / 0012AFA / 0012-3V

Type			MN1020012A / 0012AFA / 0012-3V
ROM (x8-bit / x16-bit)			Maximum 16M in total (Special Register 1K, Reserve Space 3K included)
RAM (x8-bit / x16-bit)			External ROM, RAM
Minimum Instruction Execution Time			MN1020012A / 0012AFA : 100ns (at 4.5 to 5.5V, 20MHz) MN1020012-3V : 200ns (at 3.0 to 3.6V, 10MHz)
Interrupts			• RESET • Watchdog • Timer Counter 0 to 9 • Timer Counter 10 to 12 • Timer Counter 10 to 12 Compare Capture A • Timer Counter 10 to 12 Compare Capture B • DMA 0 to 7 Transfer finish • External 0 to 3 • Serial ch 0, 1 Transmission • Serial ch 0, 1 Reception • $\overline{\text{KI}}$ Pin (OR) • A/D Conversion finish
Timer Counter			Timer Counter 0,2 to 6 : 8-bit x 1 (Timer Output, Event Count) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceUnderflow of Timer Counter 0,2 to 6 Timer Counter 7 : 8-bit x 1 (Timer Output, Event Count, A/D Conversion Start up) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceUnderflow of Timer Counter 7 Timer Counter 1 : 8-bit x 1 (Timer Output, Event Count, Synchronous Output [4-bit x 2ch]) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceUnderflow of Timer Counter 1 Timer Counter 8,9 : 8-bit x 1 (Timer Output, Event Count, UART Baud Rate Generator, Synchronous Serial Clock Generator) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceUnderflow of Timer Counter 8,9 Timer Counter 10,11 : 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceCoincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 10,11 Timer Counter 12 : 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, Synchronous Output [4-bit x 2ch]) Clock Source1/(1 to 256) of System Clock, External Clock Interrupt SourceCoincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture Connectable Timer Counter 0 to 9
Serial Interface			Serial 0 : 7,8-bit x 1 (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source1/8 of Timer Counter 8, 1/8 of Timer Counter 9, External Clock Serial 1 : 7,8-bit x 1 (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source1/8 of Timer Counter 8, 1/8 of Timer Counter 9, External Clock UART x 2 (Common use with Serial 0, 1)
I/O Pins	I/O	25	• Common use : 25 (by -bit)
	Input	4	• Common use : 4
A/D Inputs			8-bit x 8ch (with S/H)
PWM			16-bit x 3ch
Special Ports			2 (4-state Synchronous Output)

Notes	DRAM Refresh Controller, DMA Controller, DRAM High Speed Page Mode Support
Package	MN1020012A : QFP128-P-1818 MN1020012AFA / 0012-3V : LQFP128-P-1818B
Electrical Characteristics	

A/D Characteristics (MN1020012A / 0012AFA)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D Conversion Absolute Error		AVDD=5V, AVSS=0V			±3	LSB
A/D Conversion Time			4.0			μs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta=25°C, VDD=5.0V, VSS=0V)

A/D Characteristics (MN1020012-3V)

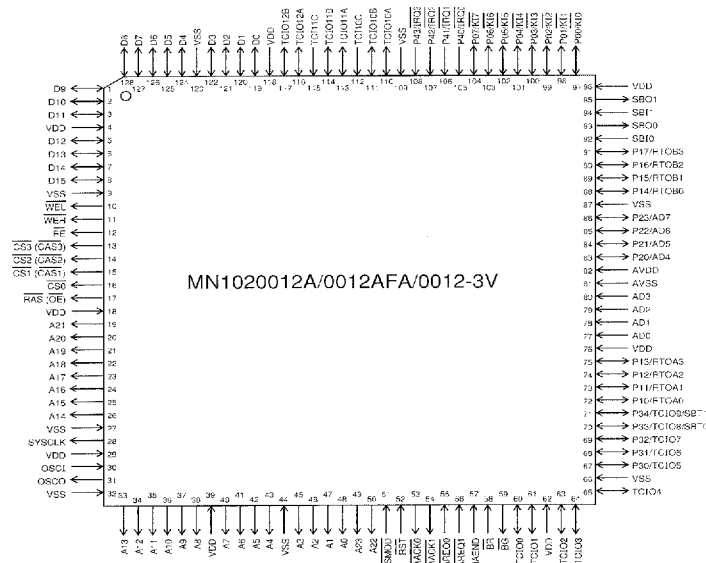
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D Conversion Absolute Error		AVDD=3.3V, AVSS=0V			±3	LSB
A/D Conversion Time			8.0			μs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta=25°C, VDD=3.3V, VSS=0V)

Support Tool

In-Circuit Emulator	PX-ICE102L00 + PX-PRB1020012 PARTNER - EX1020012
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Pin Assignment



QFP128-P-1818 (MN1020012A)
LQFP128-P-1818B (MN1020012AFA / 0012-3V)