

# 18-Bit Registered Transceivers

## Features

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6 mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

### CY74FCT16501T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### CY74FCT162501T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### CY74FCT162H501T Features:

- Bus hold retains last active state
- Eliminates the need for external pull-up or pull-down resistors

## Functional Description

These 18-bit universal bus transceivers can be operated in transparent, latched or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output enable (OEAB and OEBA), latch enable (LEAB and LEBA), and clock inputs (CLKAB and CLKBA). For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by OEBA, LEBA, and CLKBA.

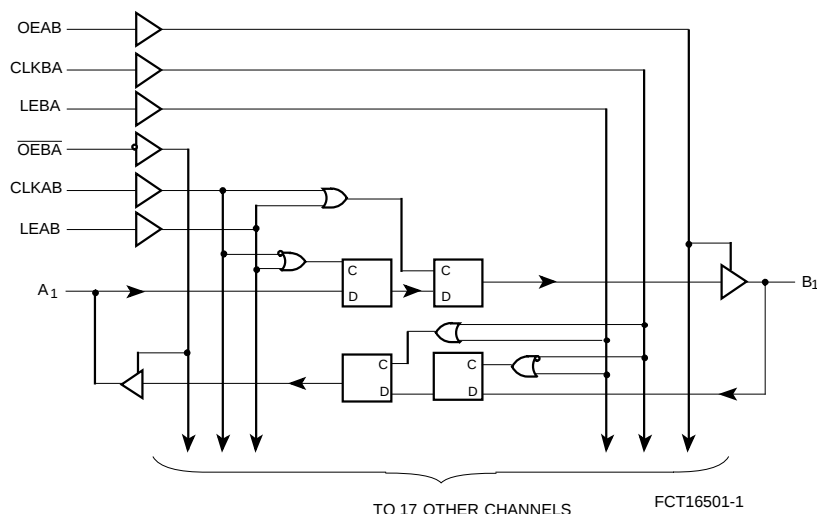
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16501T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

THE CY74FCT162501T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162501T is ideal for driving transmission lines.

The CY74FCT162H501T is a 24-mA balanced output part, that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

## Functional Block Diagram



## Pin Configuration SSOP/TSSOP Top View

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| OEAB            | 1  | 56 | GND             |
| LEAB            | 2  | 55 | CLKAB           |
| A <sub>1</sub>  | 3  | 54 | B <sub>1</sub>  |
| GND             | 4  | 53 | GND             |
| A <sub>2</sub>  | 5  | 52 | B <sub>2</sub>  |
| A <sub>3</sub>  | 6  | 51 | B <sub>3</sub>  |
| V <sub>CC</sub> | 7  | 50 | V <sub>CC</sub> |
| A <sub>4</sub>  | 8  | 49 | B <sub>4</sub>  |
| A <sub>5</sub>  | 9  | 48 | B <sub>5</sub>  |
| A <sub>6</sub>  | 10 | 47 | B <sub>6</sub>  |
| GND             | 11 | 46 | GND             |
| A <sub>7</sub>  | 12 | 45 | B <sub>7</sub>  |
| A <sub>8</sub>  | 13 | 44 | B <sub>8</sub>  |
| A <sub>9</sub>  | 14 | 43 | B <sub>9</sub>  |
| A <sub>10</sub> | 15 | 42 | B <sub>10</sub> |
| A <sub>11</sub> | 16 | 41 | B <sub>11</sub> |
| A <sub>12</sub> | 17 | 40 | B <sub>12</sub> |
| GND             | 18 | 39 | GND             |
| A <sub>13</sub> | 19 | 38 | B <sub>13</sub> |
| A <sub>14</sub> | 20 | 37 | B <sub>14</sub> |
| A <sub>15</sub> | 21 | 36 | B <sub>15</sub> |
| V <sub>CC</sub> | 22 | 35 | V <sub>CC</sub> |
| A <sub>16</sub> | 23 | 34 | B <sub>16</sub> |
| A <sub>17</sub> | 24 | 33 | B <sub>17</sub> |
| GND             | 25 | 32 | GND             |
| A <sub>18</sub> | 26 | 31 | B <sub>18</sub> |
| OEBA            | 27 | 30 | CLKBA           |
| LEBA            | 28 | 29 | GND             |

FCT16501-2

## Pin Description

| Name  | Description                                                     |
|-------|-----------------------------------------------------------------|
| OEAB  | A-to-B Output Enable Input                                      |
| OEBA  | B-to-A Output Enable Input (Active LOW)                         |
| LEAB  | A-to-B Latch Enable Input                                       |
| LEBA  | B-to-A Latch Enable Input                                       |
| CLKAB | A-to-B Clock Input                                              |
| CLKBA | B-to-A Clock Input                                              |
| A     | A-to-B Data Inputs or B-to-A Three-State Outputs <sup>[1]</sup> |
| B     | B-to-A Data Inputs or A-to-B Three-State Outputs <sup>[1]</sup> |

## Function Table<sup>[2, 3]</sup>

| Inputs |      |       |   | Outputs          |
|--------|------|-------|---|------------------|
| OEAB   | LEAB | CLKAB | A | B                |
| L      | X    | X     | X | Z                |
| H      | H    | X     | L | L                |
| H      | H    | X     | H | H                |
| H      | L    | ┐     | L | L                |
| H      | L    | ┐     | H | H                |
| H      | L    | L     | X | B <sup>[4]</sup> |
| H      | L    | H     | X | B <sup>[5]</sup> |

### Notes:

- On the 74FCT162H501T these pins have bus hold.
- A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-impedance  
┐ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

## Maximum Ratings<sup>[6, 7]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with

Power Applied..... –55°C to +125°C

DC Input Voltage..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current

(Maximum Sink Current/Pin)..... –60 to +120 mA

Power Dissipation..... 1.0W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Industrial | –40°C to +85°C      | 5V ± 10%        |

**Electrical Characteristics** Over the Operating Range

| Parameter                              | Description                                                  |          | Test Conditions                                             |                      | Min. | Typ. <sup>[8]</sup> | Max. | Unit |
|----------------------------------------|--------------------------------------------------------------|----------|-------------------------------------------------------------|----------------------|------|---------------------|------|------|
| V <sub>IH</sub>                        | Input HIGH Voltage                                           |          |                                                             |                      | 2.0  |                     |      | V    |
| V <sub>IL</sub>                        | Input LOW Voltage                                            |          |                                                             |                      |      |                     | 0.8  | V    |
| V <sub>H</sub>                         | Input Hysteresis <sup>[9]</sup>                              |          |                                                             |                      |      | 100                 |      | mV   |
| V <sub>IK</sub>                        | Input Clamp Diode Voltage                                    |          | V <sub>CC</sub> =Min., I <sub>IN</sub> =−18 mA              |                      |      | −0.7                | −1.2 | V    |
| I <sub>IH</sub>                        | Input HIGH Current                                           | Standard | V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>      |                      |      |                     | ±1   | μA   |
|                                        |                                                              | Bus Hold |                                                             |                      |      |                     | ±100 |      |
| I <sub>IL</sub>                        | Input LOW Current                                            | Standard | V <sub>CC</sub> =Max., V <sub>I</sub> =GND                  |                      |      |                     | ±1   | μA   |
|                                        |                                                              | Bus Hold |                                                             |                      |      |                     | ±100 | μA   |
| I <sub>BBH</sub><br>I <sub>BBL</sub>   | Bus Hold Sustain Current on Bus Hold Input <sup>[10]</sup>   |          | V <sub>CC</sub> =Min.,                                      | V <sub>I</sub> =2.0V | −50  |                     |      | μA   |
|                                        |                                                              |          |                                                             | V <sub>I</sub> =0.8V | +50  |                     |      | μA   |
| I <sub>BHHO</sub><br>I <sub>BHLO</sub> | Bus Hold Overdrive Current on Bus Hold Input <sup>[10]</sup> |          | V <sub>CC</sub> =Max., V <sub>I</sub> =1.5V                 |                      |      |                     | TBD  | mA   |
| I <sub>OZH</sub>                       | High Impedance Output Current (Three-State Output pins)      |          | V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V               |                      |      |                     | ±1   | μA   |
| I <sub>OZL</sub>                       | High Impedance Output Current (Three-State Output pins)      |          | V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V               |                      |      |                     | ±1   | μA   |
| I <sub>OS</sub>                        | Short Circuit Current <sup>[11]</sup>                        |          | V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND                |                      | −80  | −140                | −200 | mA   |
| I <sub>O</sub>                         | Output Drive Current <sup>[11]</sup>                         |          | V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V               |                      | −50  |                     | −180 | mA   |
| I <sub>OFF</sub>                       | Power-Off Disable                                            |          | V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[12]</sup> |                      |      |                     | ±1   | μA   |

**Output Drive Characteristics for CY74FCT16501T**

| Parameter       | Description         | Test Conditions                                | Min. | Typ. <sup>[8]</sup> | Max. | Unit |
|-----------------|---------------------|------------------------------------------------|------|---------------------|------|------|
| V <sub>OH</sub> | Output HIGH Voltage | V <sub>CC</sub> =Min., I <sub>OH</sub> =−3 mA  | 2.5  | 3.5                 |      | V    |
|                 |                     | V <sub>CC</sub> =Min., I <sub>OH</sub> =−15 mA | 2.4  | 3.5                 |      |      |
|                 |                     | V <sub>CC</sub> =Min., I <sub>OH</sub> =−32 mA | 2.0  | 3.0                 |      |      |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA  |      | 0.2                 | 0.55 | V    |

**Output Drive Characteristics for CY74FCT162501T, CY74FCT162H501T**

| Parameter        | Description                         | Test Conditions                                                                                   | Min. | Typ. <sup>[8]</sup> | Max. | Unit |
|------------------|-------------------------------------|---------------------------------------------------------------------------------------------------|------|---------------------|------|------|
| I <sub>ODL</sub> | Output LOW Current <sup>[11]</sup>  | V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V | 60   | 115                 | 150  | mA   |
| I <sub>ODH</sub> | Output HIGH Current <sup>[11]</sup> | V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V | −60  | −115                | −150 | mA   |
| V <sub>OH</sub>  | Output HIGH Voltage                 | V <sub>CC</sub> =Min., I <sub>OH</sub> =−24 mA                                                    | 2.4  | 3.3                 |      | V    |
| V <sub>OL</sub>  | Output LOW Voltage                  | V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA                                                     |      | 0.3                 | 0.55 | V    |

**Notes:**

8. Typical values are at V<sub>CC</sub>= 5.0V, T<sub>A</sub>= +25°C ambient.
9. This parameter is specified but not tested.
10. Pins with bus hold are described in Pin Description.
11. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
12. Tested at +25°C.

**Capacitance**<sup>[9]</sup> ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

| Parameter | Description        | Test Conditions | Typ. <sup>[8]</sup> | Max. | Unit |
|-----------|--------------------|-----------------|---------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $V_{IN} = 0V$   | 4.5                 | 6.0  | pF   |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$  | 5.5                 | 8.0  | pF   |

## Power Supply Characteristics

| Sym.            | Parameter                                      | Test Conditions <sup>[13]</sup>                                                                                                                                                                                         |                                                   | Min. | Typ. <sup>[8]</sup> | Max.                 | Unit                     |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|------|---------------------|----------------------|--------------------------|
| $I_{CC}$        | Quiescent Power Supply Current                 | $V_{CC} = \text{Max.}$                                                                                                                                                                                                  | $V_{IN} \leq 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ | —    | 5                   | 500                  | $\mu\text{A}$            |
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL inputs HIGH | $V_{CC} = \text{Max.}$ , $V_{IN} = 3.4V$ <sup>[14]</sup>                                                                                                                                                                |                                                   | —    | 0.5                 | 1.5                  | mA                       |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>[15]</sup>   | $V_{CC} = \text{Max.}$ , Outputs Open<br>$OEAB = \overline{OEBA} = V_{CC}$ or GND<br>One Input Toggling,<br>50% Duty Cycle                                                                                              | $V_{IN} = V_{CC}$ or<br>$V_{IN} = \text{GND}$     | —    | 75                  | 120                  | $\mu\text{A}/\text{MHz}$ |
| $I_C$           | Total Power Supply Current <sup>[16]</sup>     | $V_{CC} = \text{Max.}$ , Outputs Open<br>$f_0 = 10\text{MHz}$ (CLKAB)<br>50% Duty Cycle<br>$OEAB = \overline{OEBA} = V_{CC}$<br>$LEAB = \text{GND}$ , One Bit Toggling<br>$f_1 = 5\text{MHz}$ , 50% Duty Cycle          | $V_{IN} = V_{CC}$ or<br>$V_{IN} = \text{GND}$     | —    | 0.8                 | 1.7                  | mA                       |
|                 |                                                |                                                                                                                                                                                                                         | $V_{IN} = 3.4V$ or<br>$V_{IN} = \text{GND}$       | —    | 1.3                 | 3.2                  |                          |
|                 |                                                | $V_{CC} = \text{Max.}$ , Outputs Open<br>$f_0 = 10\text{MHz}$ (CLKAB)<br>50% Duty Cycle<br>$OEAB = \overline{OEBA} = V_{CC}$<br>$LEAB = \text{GND}$<br>Eighteen Bits Toggling<br>$f_1 = 2.5\text{MHz}$ , 50% Duty Cycle | $V_{IN} = V_{CC}$ or<br>$V_{IN} = \text{GND}$     | —    | 3.8                 | 6.5 <sup>[17]</sup>  |                          |
|                 |                                                |                                                                                                                                                                                                                         | $V_{IN} = 3.4V$ or<br>$V_{IN} = \text{GND}$       | —    | 8.5                 | 20.8 <sup>[17]</sup> |                          |

### Notes:

13. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

14. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

15. This parameter is not directly testable, but is derived for use in Total Power Supply.

16.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamps and all frequencies are in megahertz.

17. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[18]</sup>

| Parameter                            | Description                                               |            | CY74FCT16501AT<br>CY74FCT162501AT |      | CY74FCT162501CT<br>CY74FCT162H501CT |      | Unit | Fig. No. <sup>[19]</sup> |
|--------------------------------------|-----------------------------------------------------------|------------|-----------------------------------|------|-------------------------------------|------|------|--------------------------|
|                                      |                                                           |            | Min.                              | Max. | Min.                                | Max. |      |                          |
| t <sub>MAX</sub>                     | CLKAB or CLKBA frequency <sup>[20]</sup>                  |            | —                                 | 150  | —                                   | 150  | MHz  | —                        |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>A to B or B to A                     |            | 1.5                               | 5.1  | 1.5                                 | 4.6  | ns   | 1,3                      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LEBA to A, LEAB to B                 |            | 1.5                               | 5.6  | 1.5                                 | 5.3  | ns   | 1,5                      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLKBA to A,<br>CLKAB to B            |            | 1.5                               | 5.6  | 1.5                                 | 5.3  | ns   | 1,5                      |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>OEBA to A, OEAB to B                |            | 1.5                               | 6.0  | 1.5                                 | 5.6  | ns   | 1,7,8                    |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>OEBA to A, OEAB to B               |            | 1.5                               | 5.6  | 1.5                                 | 5.2  | ns   | 1,7,8                    |
| t <sub>SU</sub>                      | Set-Up Time, HIGH or LOW<br>A to CLKAB,<br>B to CLKBA     |            | 3.0                               | —    | 3.0                                 | —    | ns   | 4                        |
| t <sub>H</sub>                       | Hold Time HIGH or LOW<br>A to CLKAB,<br>B to CLKBA        |            | 0                                 | —    | 0                                   | —    | ns   | 4                        |
| t <sub>SU</sub>                      | Set-Up Time, HIGH or LOW<br>A to LEAB,<br>B to LEBA       | Clock LOW  | 3.0                               | —    | 3.0                                 | —    | ns   | 4                        |
|                                      |                                                           | Clock HIGH | 1.5                               | —    | 1.5                                 | —    | ns   | 4                        |
| t <sub>H</sub>                       | Hold Time, HIGH or LOW, A to LEAB,<br>B to LEBA           |            | 1.5                               | —    | 1.5                                 | —    | ns   | 4                        |
| t <sub>W</sub>                       | LEAB or LEBA Pulse Width HIGH <sup>[20]</sup>             |            | 3.0                               | —    | 3.0                                 | —    | ns   | 5                        |
| t <sub>W</sub>                       | CLKAB or CLKBA Pulse Width HIGH or<br>LOW <sup>[20]</sup> |            | 3.0                               | —    | 3.0                                 | —    | ns   | 5                        |
| t <sub>SK(O)</sub>                   | Output Skew <sup>[21]</sup>                               |            | —                                 | 0.5  | —                                   | 0.5  | ns   | —                        |

**Notes:**

18. Minimum limits are specified, but not tested, on propagation delays.

19. See "Parameter Measurement Information" in the General Information section.

20. This parameter is guaranteed but not tested.

21. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

**Ordering Information CY74FCT16501T**

| Speed (ns) | Ordering Code          | Package Name | Package Type           | Operating Range |
|------------|------------------------|--------------|------------------------|-----------------|
| 5.1        | CY74FCT16501ATPVC/PVCT | O56          | 56-Lead (300-Mil) SSOP | Industrial      |

**Ordering Information CY74FCT162501T**

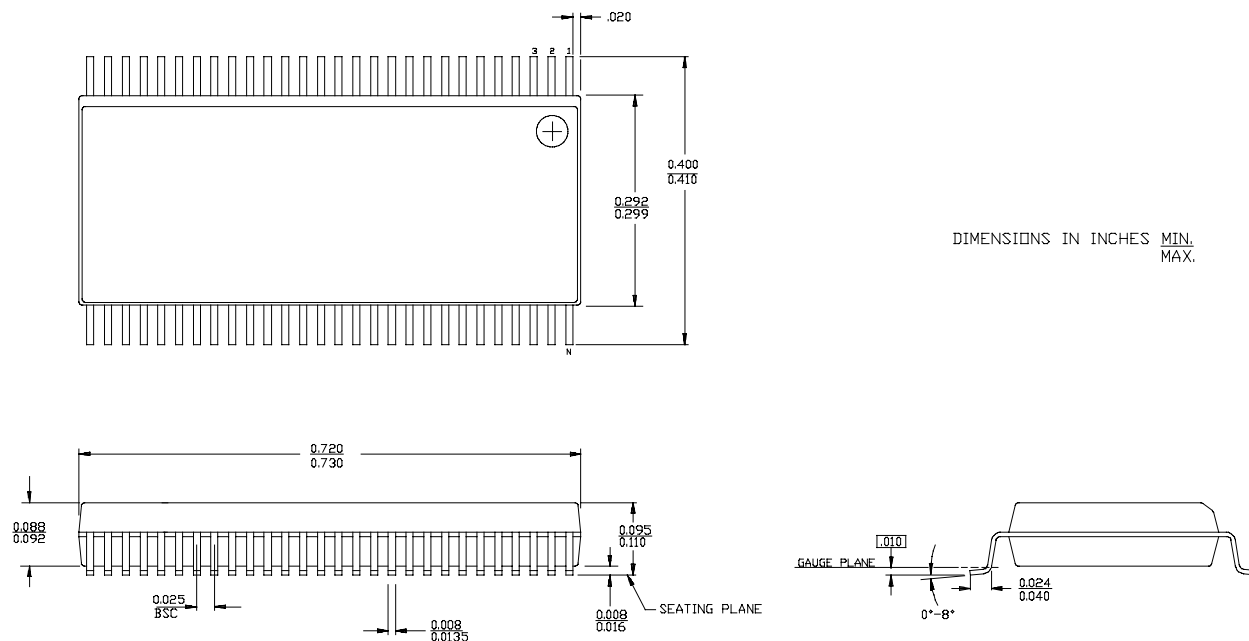
| Speed (ns) | Ordering Code      | Package Name | Package Type            | Operating Range |
|------------|--------------------|--------------|-------------------------|-----------------|
| 4.6        | 74FCT162501CTPACT  | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |
|            | CY74FCT162501CTPVC | O56          | 56-Lead (300-Mil) SSOP  |                 |
|            | 74FCT162501CTPVCT  | O56          | 56-Lead (300-Mil) SSOP  |                 |
| 5.1        | 74FCT162501ATPACT  | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |
|            | CY74FCT162501ATPVC | O56          | 56-Lead (300-Mil) SSOP  |                 |
|            | 74FCT162501ATPVCT  | O56          | 56-Lead (300-Mil) SSOP  |                 |

**Ordering Information CY74FCT162H501T**

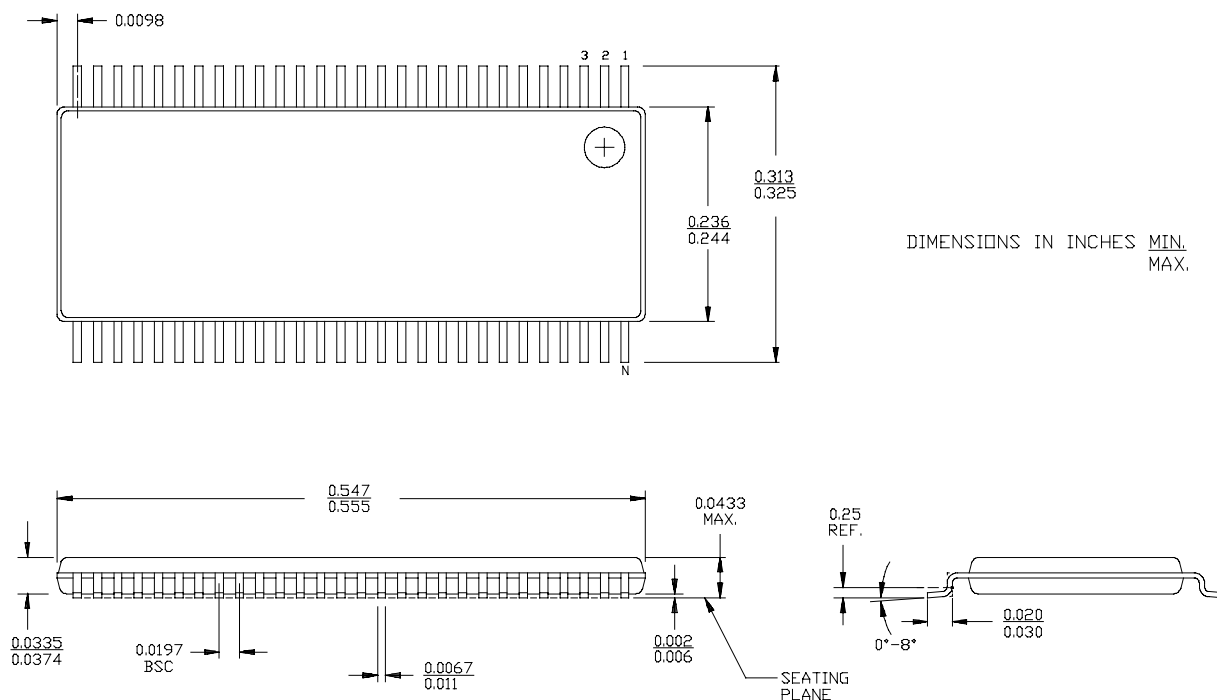
| Speed (ns) | Ordering Code          | Package Name | Package Type            | Operating Range |
|------------|------------------------|--------------|-------------------------|-----------------|
| 4.6        | 74FCT162H501CTPACT     | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |
|            | 74FCT162H501CTPVC/PVCT | O56          | 56-Lead (300-Mil) SSOP  |                 |

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



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