

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- Bidirectional
- Dual 1024 by 9 Bits
- Programmable Almost-Full/Almost-Empty Flag
- Empty, Full, and Half-Full Flags
- Access Times of 25 ns With a 50-pF Load
- Data Rates up to 50 MHz
- Fall-Through Times of 22 ns Maximum
- High Output Drive for Direct Bus Interface
- Package Options Include 44-Pin Plastic Leaded Chip Carriers (FN) and 64-Pin Thin Quad Flat (PAG, PM) Packages

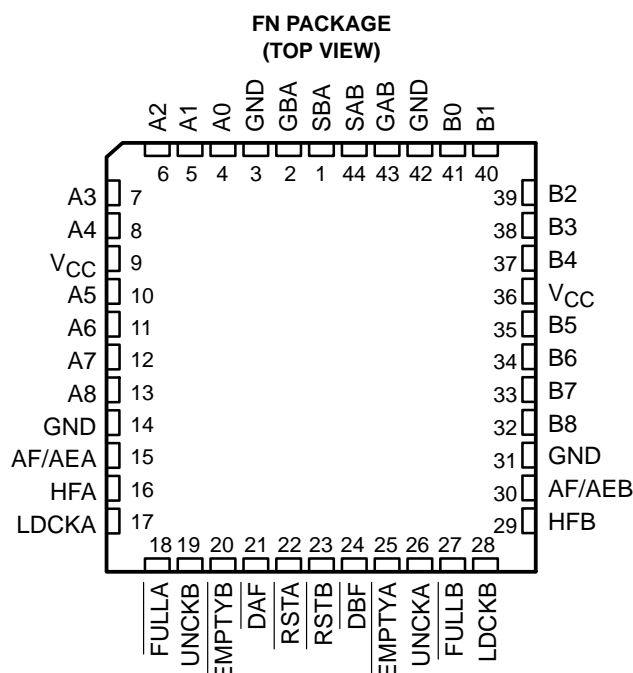
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2235 is arranged as two 1024 × 9-bit FIFOs for high speed and fast access times. It processes data at rates up to 50 MHz, with access times of 25 ns in a bit-parallel format.

The SN74ACT2235 consists of bus-transceiver circuits, two 1024 × 9-bit FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable (GAB and GBA) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 2 shows the eight fundamental bus-management functions that can be performed with the SN74ACT2235.

For more information on this device family, see the application report, *1K × 9 × 2 Asynchronous FIFO SN74ACT2235*, literature number SCAA010.

The SN74ACT2235 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

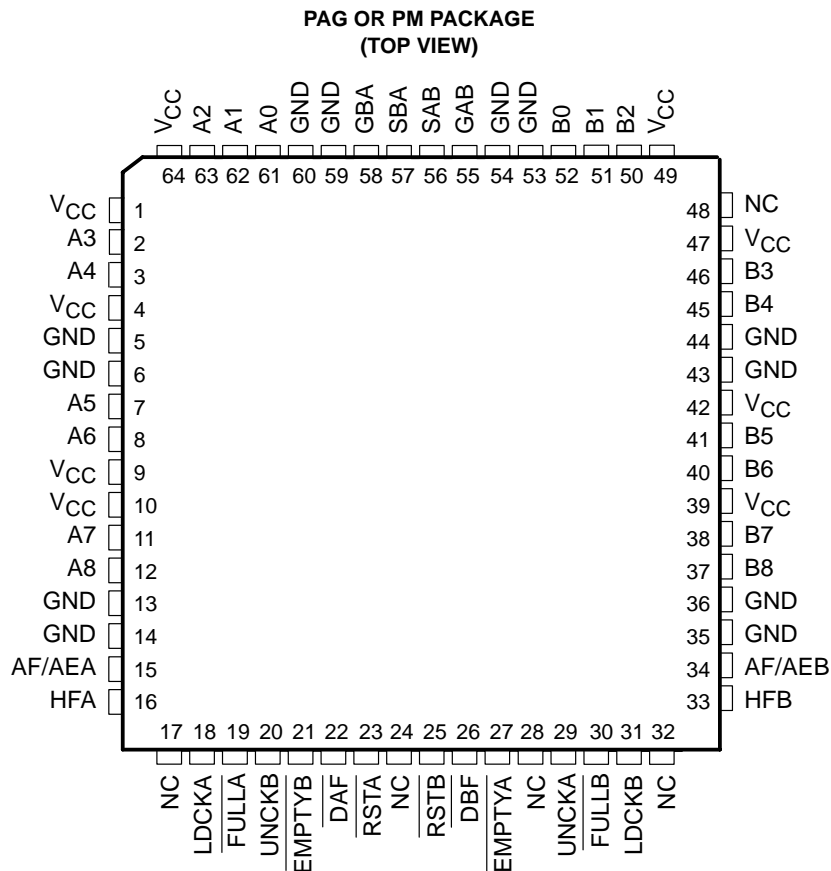
Copyright © 2003, Texas Instruments Incorporated

SN74ACT2235

1024 × 9 × 2

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

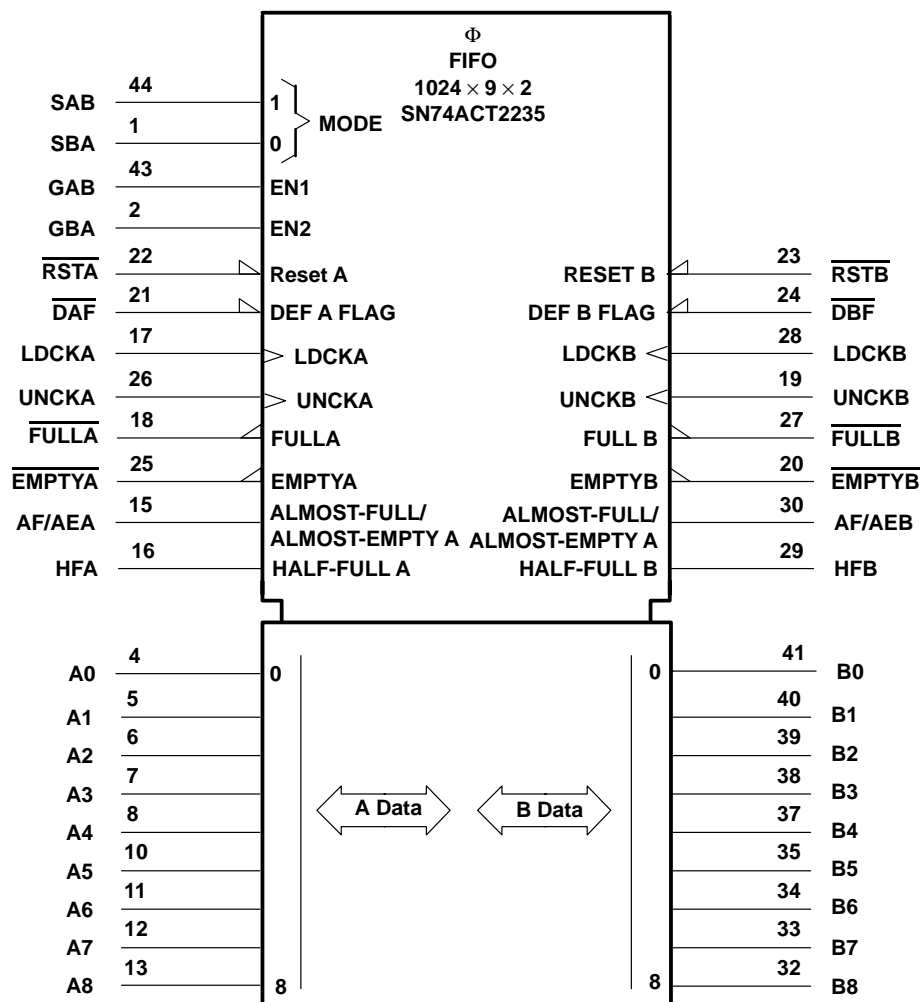


NC – No internal connection

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

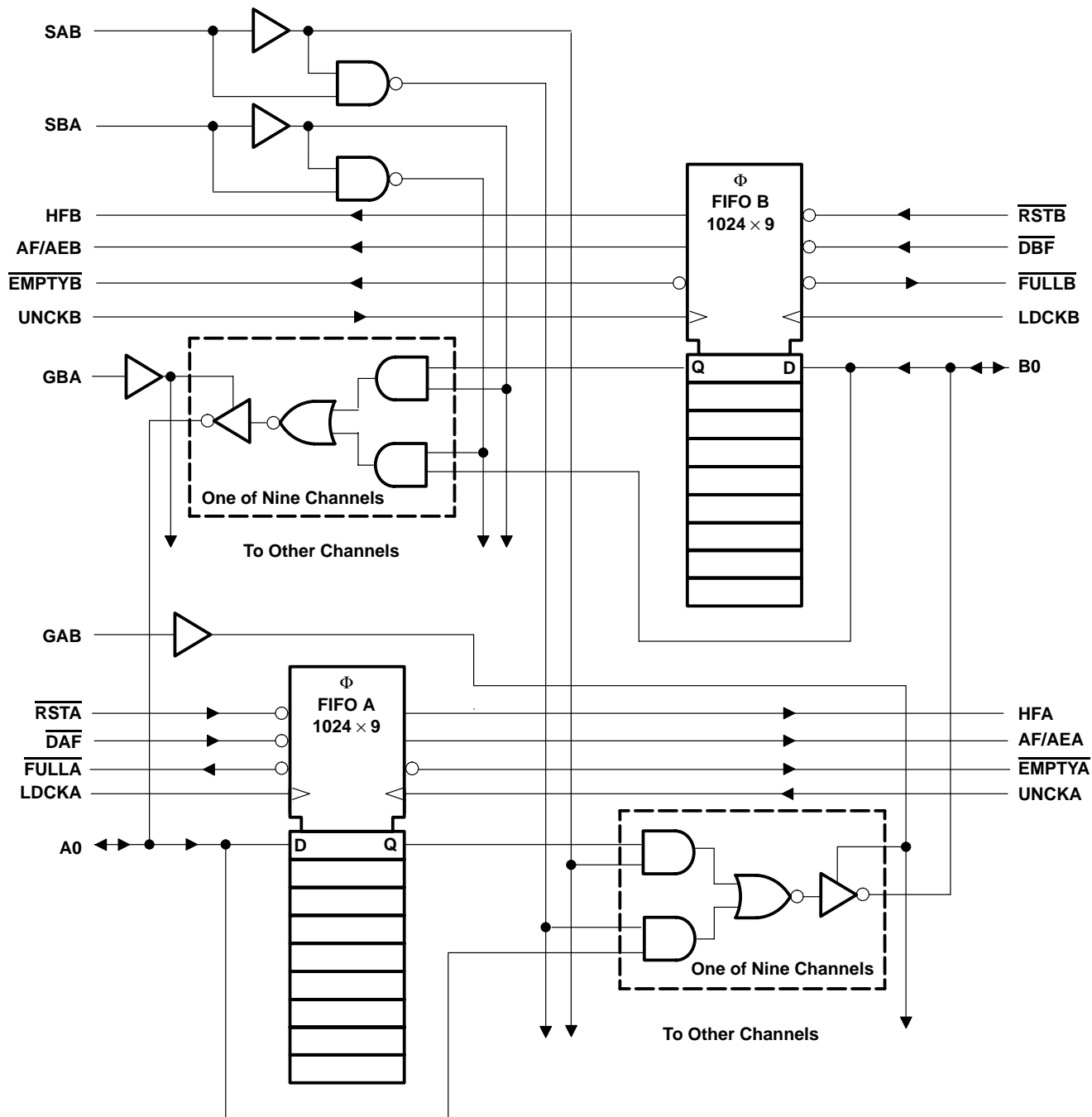
SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

logic diagram (positive logic)



ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

Terminal Functions

TERMINAL† NAME	NO.	I/O	DESCRIPTION
AF/AEA AF/AEB	15 30	O	Almost full/almost empty flags. The almost-full/almost-empty A flag (AF/AEA) is defined by the almost-full/almost-empty offset value for FIFO A (X). AF/AEA is high when FIFO A contains X or fewer words or 1024 – X words. AF/AEA is low when FIFO A contains between (X + 1) or (1023 – X) words. The operation of the almost-full/almost-empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.
A0–A8	4–8, 10–13	I/O	A-data inputs and outputs
B0–B8	32–35, 37–41	I/O	B-data inputs and outputs
$\overline{\text{DAF}}$ $\overline{\text{DBF}}$	21 24	I	Define-flag inputs. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value on A0–A8 as the almost-full/almost-empty offset value for FIFO A (X). The high-to-low transition of $\overline{\text{DBF}}$ stores the binary value of B0–B8 as the almost-full/almost-empty offset value for FIFO B (Y).
$\overline{\text{EMPTYA}}$ $\overline{\text{EMPTYB}}$	25 20	O	Empty flags. $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ are low when their corresponding memories are empty and high when they are not empty.
$\overline{\text{FULLA}}$ $\overline{\text{FULLB}}$	18 27	O	Full flags. $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are low when their corresponding memories are full and high when they are not full.
HFA HFB	16 29	O	Half-full flags. HFA and HFB are high when their corresponding memories contain 512 or more words and low when they contain 511 or fewer words.
LDCKA LDCKB	17 28	I	Load clocks. Data on A0–A8 is written into FIFO A on a low-to-high transition of LDCKA. Data on B0–B8 is written into FIFO B on a low-to-high transition of LDCKB. When the FIFOs are full, LDCKA and LDCKB have no effect on the data residing in memory.
GAB GBA	43 2	I	Output enables. GAB, GBA control the transceiver functions. When GBA is low, A0–A8 are in the high-impedance state. When GAB is low, B0–B8 are in the high-impedance state.
$\overline{\text{RSTA}}$ $\overline{\text{RSTB}}$	22 23	I	Reset. A reset is accomplished in each direction by taking $\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ low. This sets $\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$, $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, and AF/AEB high. Both FIFOs must be reset upon power up.
SAB SBA	44 1	I	Select-control inputs. SAB and SBA select whether real-time or stored data is transferred. A low level selects real-time data and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 2.
UNCKA UNCKB	26 19	I	Unload clocks. Data in FIFO A is read to B0–B8 on a low-to-high transition of UNCKA. Data in FIFO B is read to A0–A8 on a low-to-high transition of UNCKB. When the FIFOs are empty, UNCKA and UNCKB have no effect on data residing in memory.

† Terminals listed are for the FN package.

programming procedure for AF/AEA

The almost-full/almost-empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost-full/almost-empty offset value for FIFO A (X) and for FIFO B (Y) is either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

user-defined X

Take $\overline{\text{DAF}}$ from high to low. This stores A0–A8 as X.

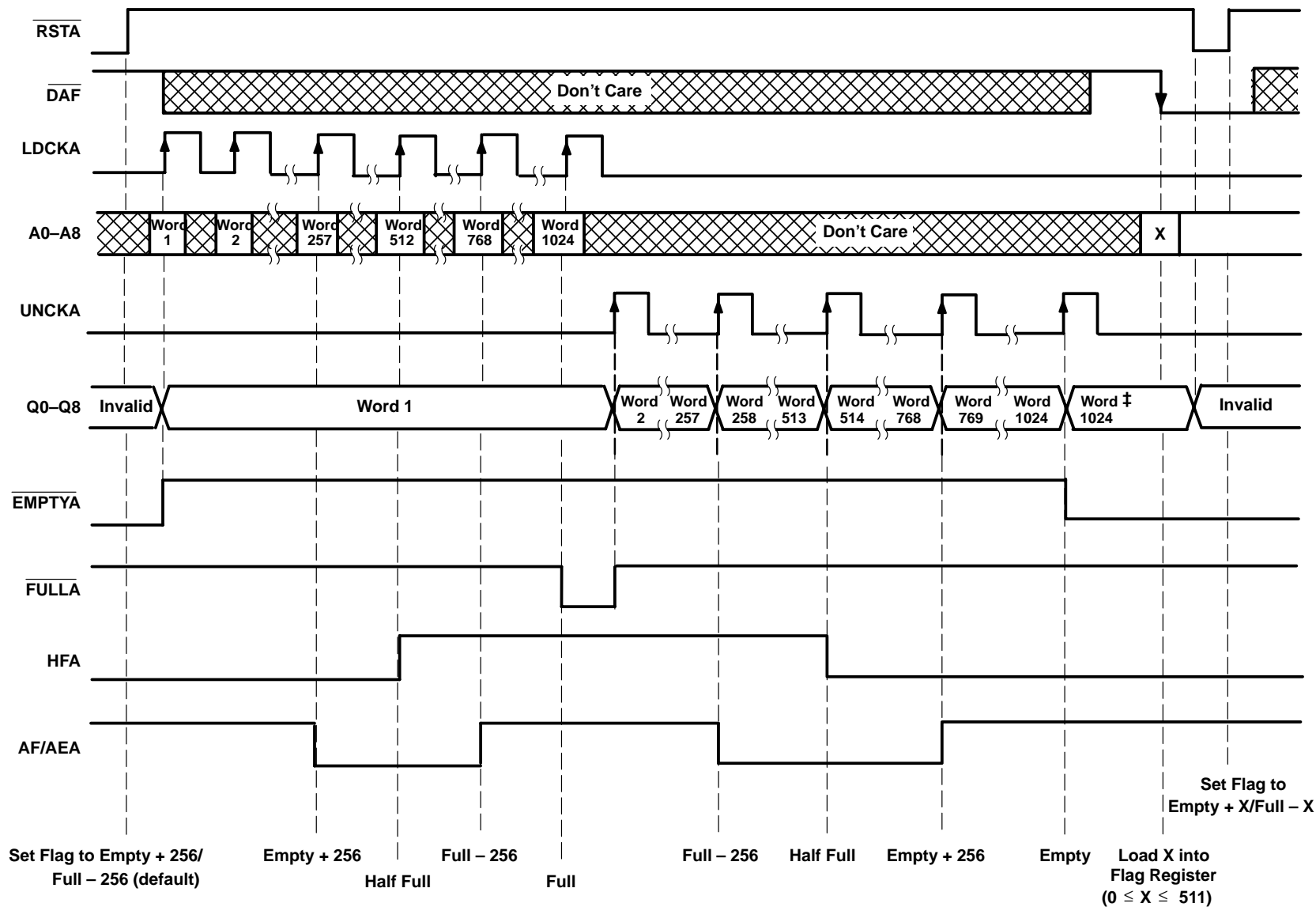
If $\overline{\text{RSTA}}$ is not already low, take $\overline{\text{RSTA}}$ low.

With $\overline{\text{DAF}}$ held low, take $\overline{\text{RSTA}}$ high. This defines AF/AEA using X.

To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

default X

To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.



† Operation of FIFO B is identical to that of FIFO A.
 ‡ Last valid data stays on outputs when FIFO goes empty due to a read.

Figure 1. Timing Diagram for FIFO A†

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

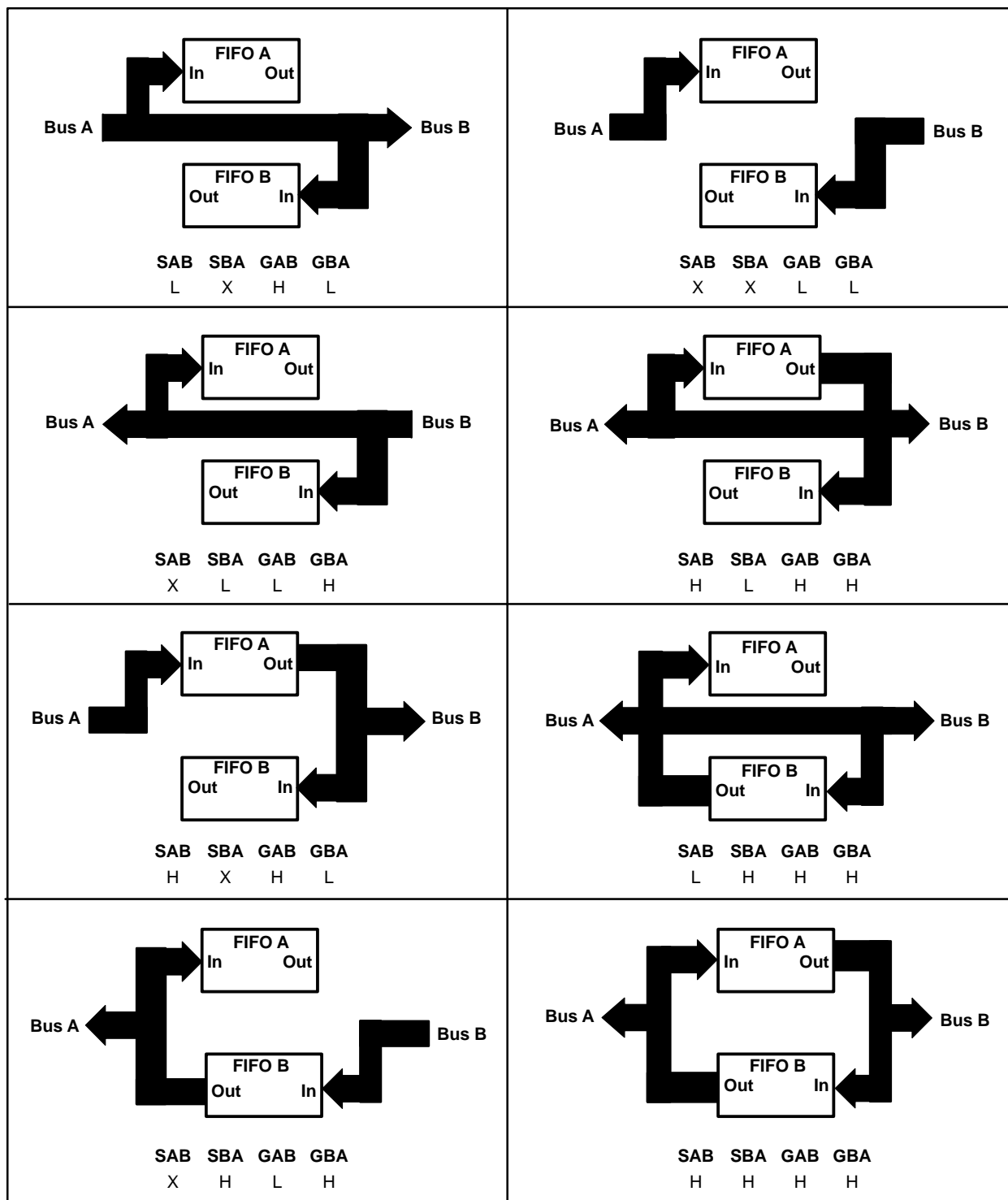


Figure 2. Bus-Management Functions

SELECT-MODE CONTROL

CONTROL		OPERATION	
SAB	SBA	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL

CONTROL		OPERATION	
GAB	GBA	A BUS	B BUS
H	H	A bus enabled	B bus enabled
L	H	A bus enabled	Isolation/input to B bus
H	L	Isolation/input to A bus	B bus enabled
L	L	Isolation/input to A bus	Isolation/input to B bus

Figure 2. Bus-Management Functions (Continued)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Control inputs	–0.5 V to 7 V
I/O ports	–0.5 V to 5.5 V
Voltage range applied to a disabled 3-state output	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): FN package	46°C/W
PAG package	58°C/W
PM package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C
Maximum junction temperature, T_J	150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			ACT2235-20		ACT2235-30		ACT2235-40		ACT2235-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		2		2		V
V _{IL}	Low-level input voltage		0.8		0.8		0.8		0.8		V
I _{OH}	High-level output current	A or B ports	−8		−8		−8		−8		mA
		Status flags	−8		−8		−8		−8		
I _{OL}	Low-level output current	A or B ports	16		16		16		16		mA
		Status flags	8		8		8		8		
T _A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}		$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -8\text{ mA}$	2.4			V
V_{OL}	Flags	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 8\text{ mA}$			0.5	V
	I/O ports	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 16\text{ mA}$			0.5	
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = V_{CC}$ or 0			±5	μA
I_{OZ}		$V_{CC} = 5.5\text{ V}$,	$V_O = V_{CC}$ or 0			±5	μA
I_{CC}^{\ddagger}		$V_I = V_{CC} - 0.2\text{ V}$ or 0			10	400	μA
ΔI_{CC}^{\S}		$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i		$V_I = 0$,	$f = 1\text{ MHz}$		4		pF
C_o		$V_O = 0$,	$f = 1\text{ MHz}$		8		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ I_{CC} is tested with outputs open.

§ This is the supply current when each input is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 3)

			'ACT2235-20		'ACT2235-30		'ACT2235-40		'ACT2235-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	LDCKA or LDCKB	50		33		25		16.7		MHz
		UNCKA or UNCKB	50		33		25		16.7		
t _w	Pulse duration	RSTA or RSTB low	20		20		25		25		ns
		LDCKA or LDCKB low	8		10		14		20		
		LDCKA or LDCKB high	8		10		14		20		
		UNCKA or UNCKB low	8		10		14		20		
		UNCKA or UNCKB high	8		10		14		20		
		DAF or DBF high	10		10		10		10		
t _{su}	Setup time	Data before LDCKA or LDCKB↑	4		4		5		5		ns
		Define AF/AE: D0–D8 before DAF or DBF↓	5		5		5		5		
		Define AF/AE: DAF or DBF↓ before RSTA or RSTB↑	7		7		7		7		
		Define AF/AE (default): DAF or DBF high before RSTA or RSTB↑	5		5		5		5		
		RSTA or RSTB inactive (high) before LDCKA or LDCKB↑	5		5		5		5		
t _h	Hold time	Data after LDCKA or LDCKB↑	1		1		2		2		ns
		Define AF/AE: D0–D8 after DAF or DBF↓	0		0		0		0		
		Define AF/AE: DAF or DBF low after RSTA or RSTB↑	0		0		0		0		
		Define AF/AE (default): DAF or DBF high after RSTA or RSTB↑	0		0		0		0		



TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT2235-20			'ACT2235-30		'ACT2235-40		'ACT2235-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{\max}	LDCK		50			33		25		16.7		MHz
	UNCK		50			33		25		16.7		
t_{pd}	LDCK↑, LDCKB↑	B or A	8		22	8	22	8	24	8	26	ns
	UNCKA↑, UNCKB↑		12	17	25	12	25	12	35	12	45	
t_{PLH}	LDCK↑, LDCKB↑	\overline{EMPTYA} , \overline{EMPTYB}	4		15	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	\overline{EMPTYA} , \overline{EMPTYB}	2		17	2	17	2	19	2	21	ns
	$\overline{RSTA}\downarrow$, $\overline{RSTB}\downarrow$		2		18	2	18	2	20	2	22	
	LDCK↑, LDCKB↑	\overline{FULLA} , \overline{FULLB}	4		15	4	15	4	17	4	19	
t_{PLH}	UNCKA↑, UNCKB↑	\overline{FULLA} , \overline{FULLB}	4		15	4	15	4	17	4	19	ns
	$\overline{RSTA}\downarrow$, $\overline{RSTB}\downarrow$	\overline{FULLA} , \overline{FULLB}	2		15	2	15	2	17	2	19	
		AF/AEA, AF/AEB	2		15	2	15	2	17	2	19	
	LDCK↑, LDCKB↑	HFA, HFB	2		15	2	15	2	17	2	19	
t_{PHL}	UNCKA↑, UNCKB↑	HFA, HFB	4		18	4	18	4	20	4	22	ns
	$\overline{RSTA}\downarrow$, $\overline{RSTB}\downarrow$		1		15	1	15	1	17	1	19	
t_{pd}	SAB or SBA‡	B or A	1		11	1	11	1	12	1	14	ns
	A or B		1		11	1	11	1	12	1	14	
	LDCK↑, LDCKB↑	AF/AEA, AF/AEB	2		18	2	18	2	20	2	22	
	UNCKA↑, UNCKB↑		2		18	2	18	2	20	2	22	
t_{en}	GBA or GAB	A or B	2		11	2	11	2	13	2	15	ns
t_{dis}	GBA or GAB	A or B	1		9	1	9	1	11	1	13	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	Outputs enabled	$C_L = 50$ pF, $f = 5$ MHz	71	pF
		Outputs disabled		57	

ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS148F – DECEMBER 1990 – REVISED JUNE 2003

PARAMETER MEASUREMENT INFORMATION

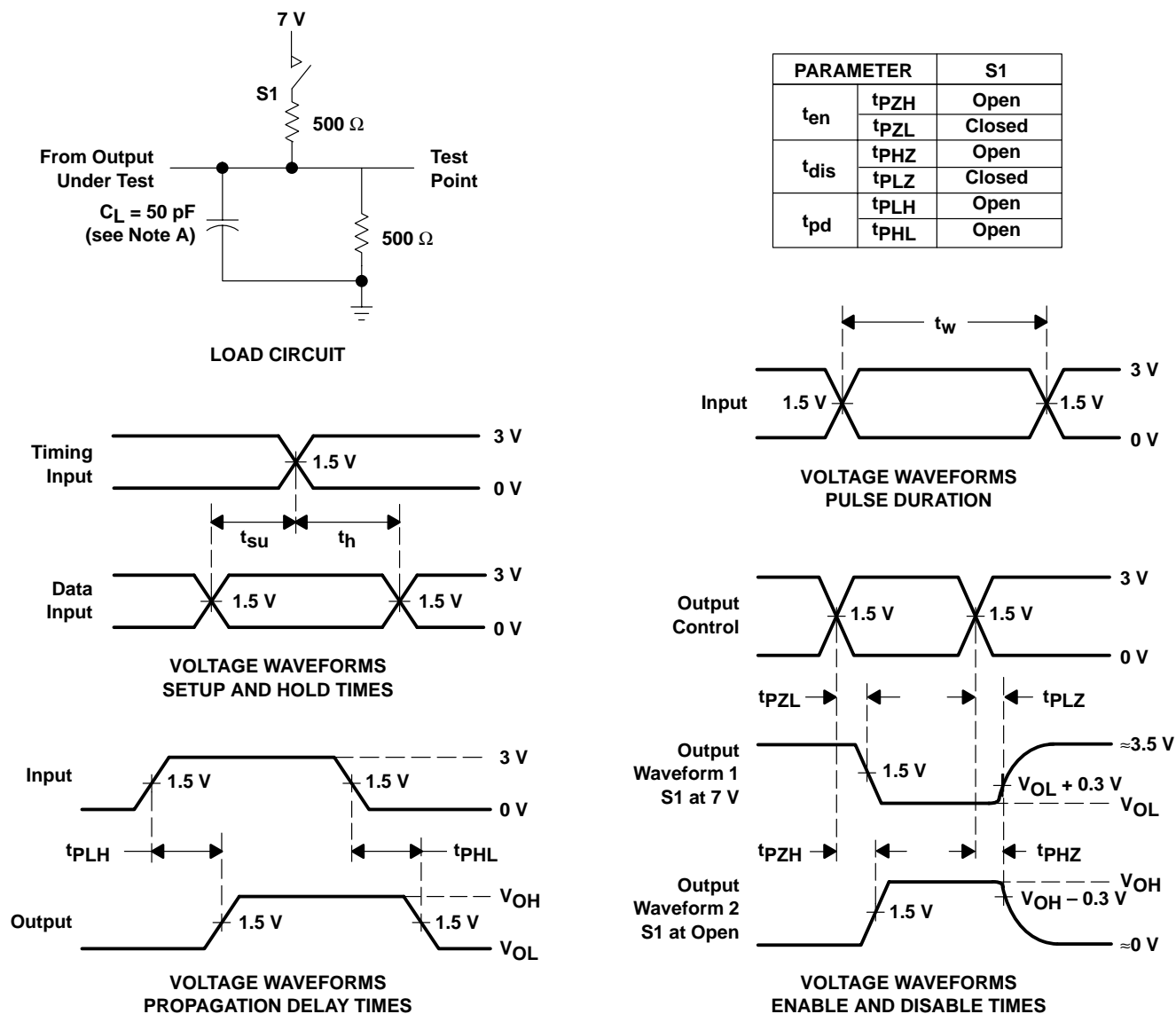
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

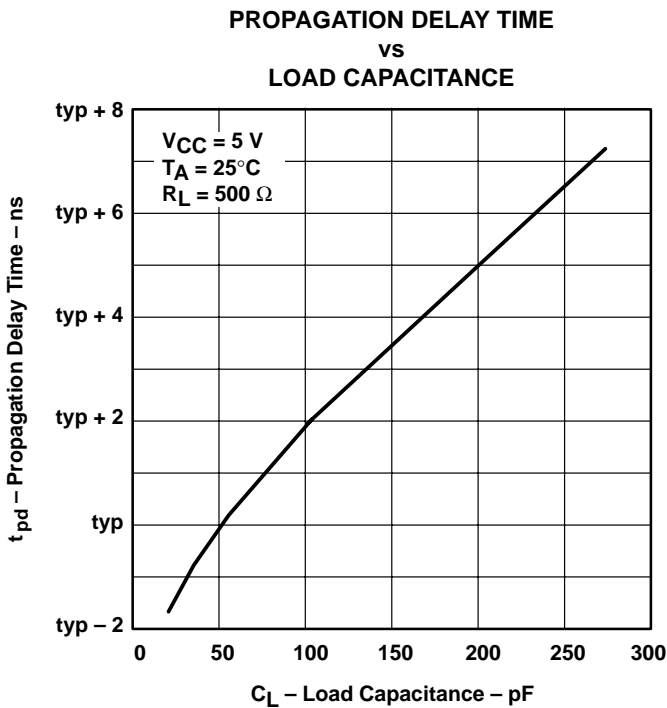


Figure 4

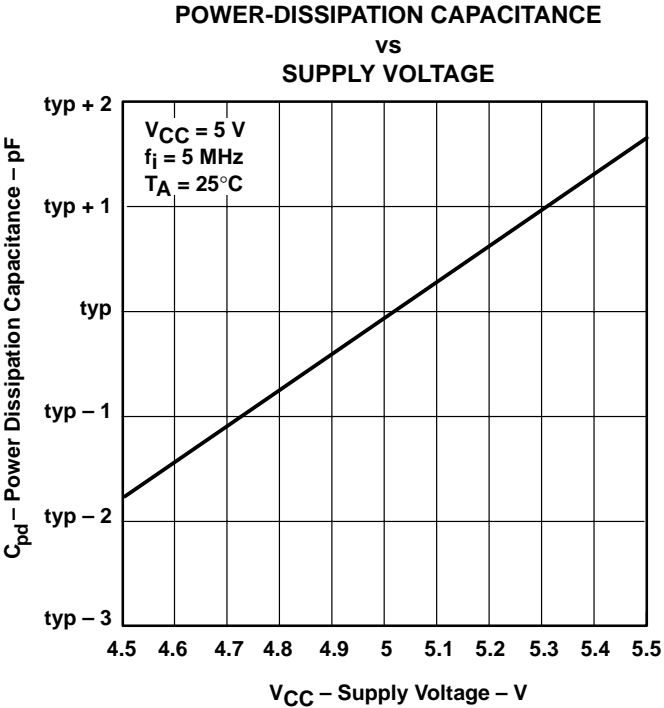
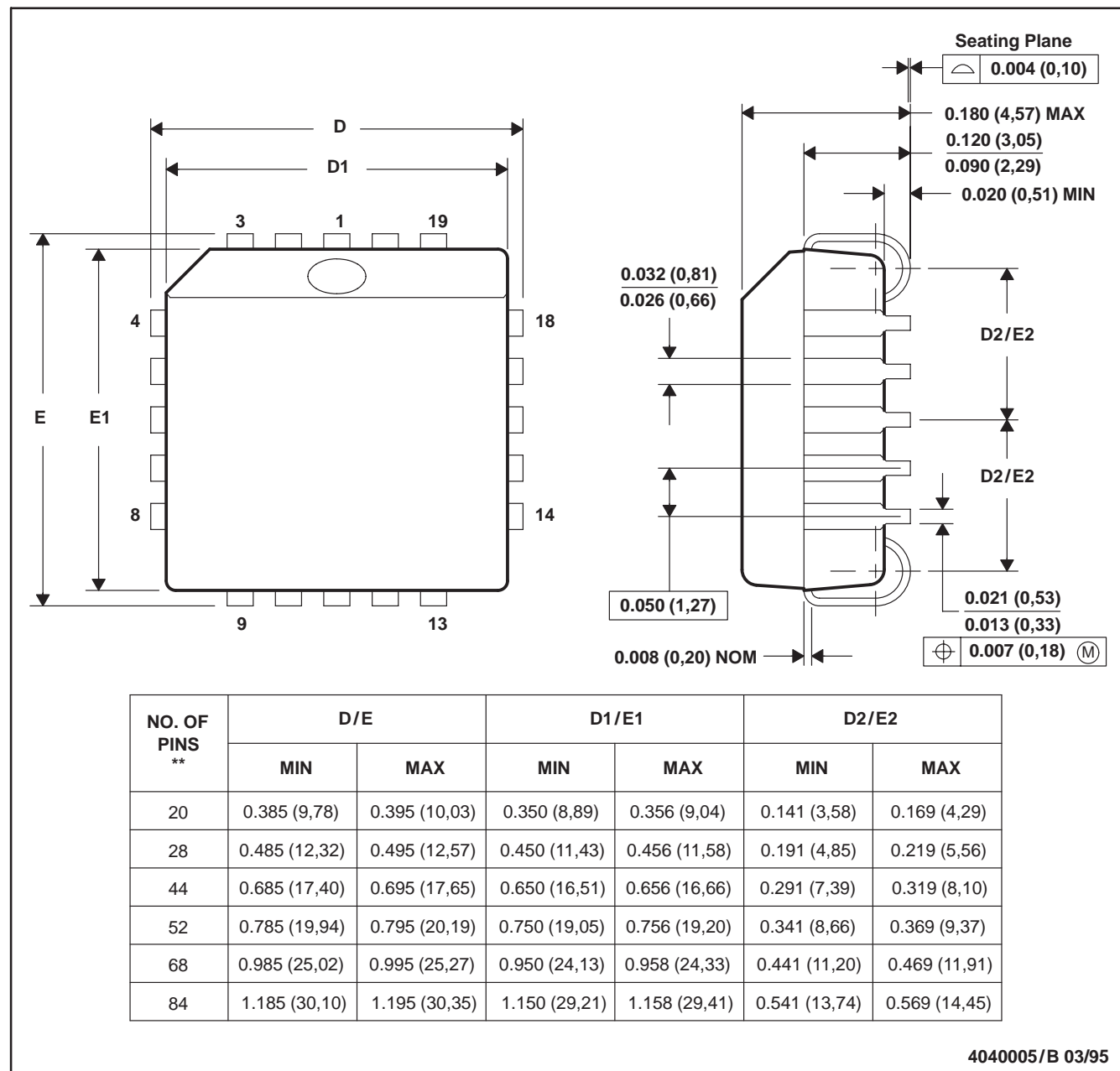


Figure 5

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

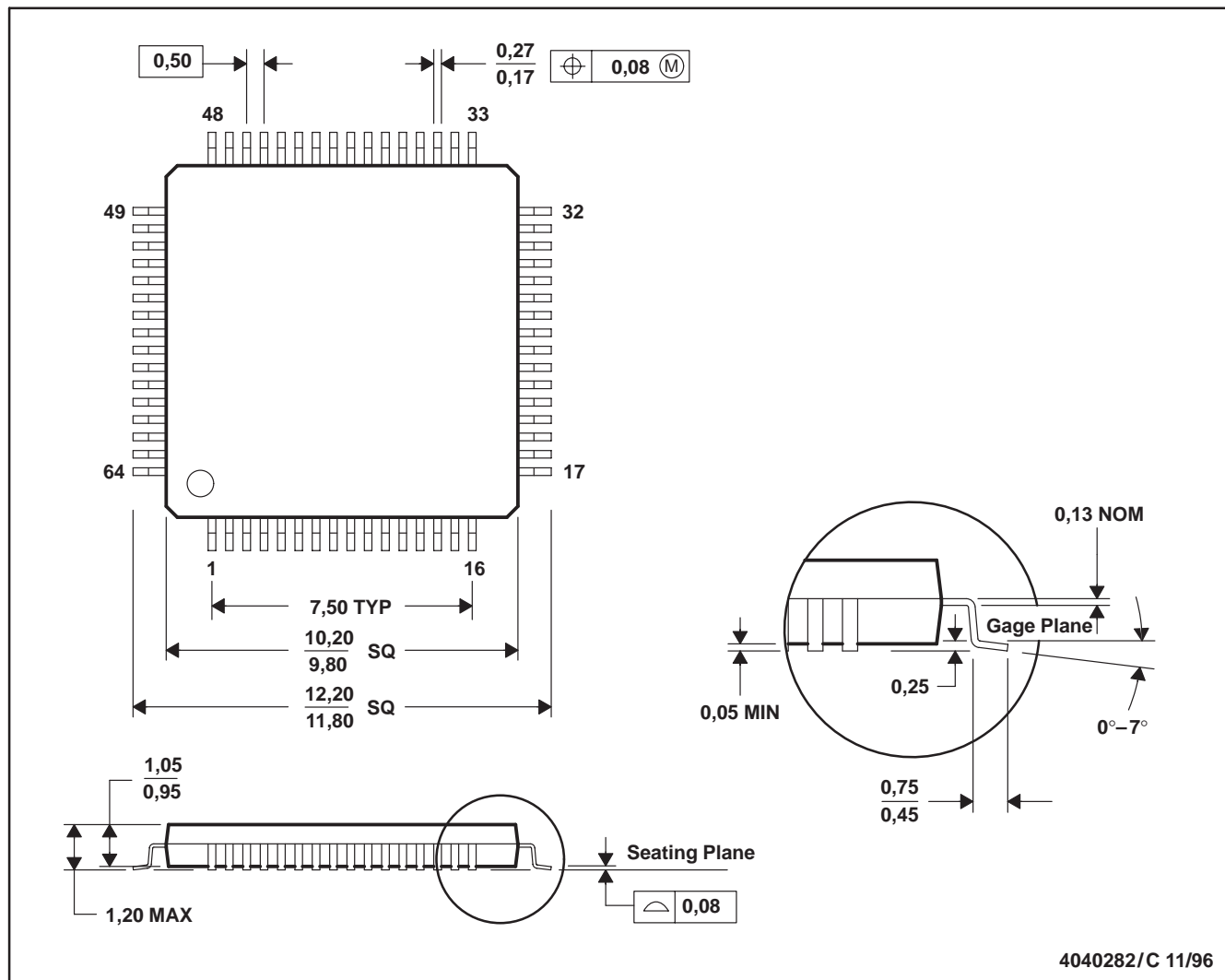
20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-026
 - May also be thermally enhanced plastic with leads connected to the die pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265