

128K x 8 Bit Fast Static Random Access Memory

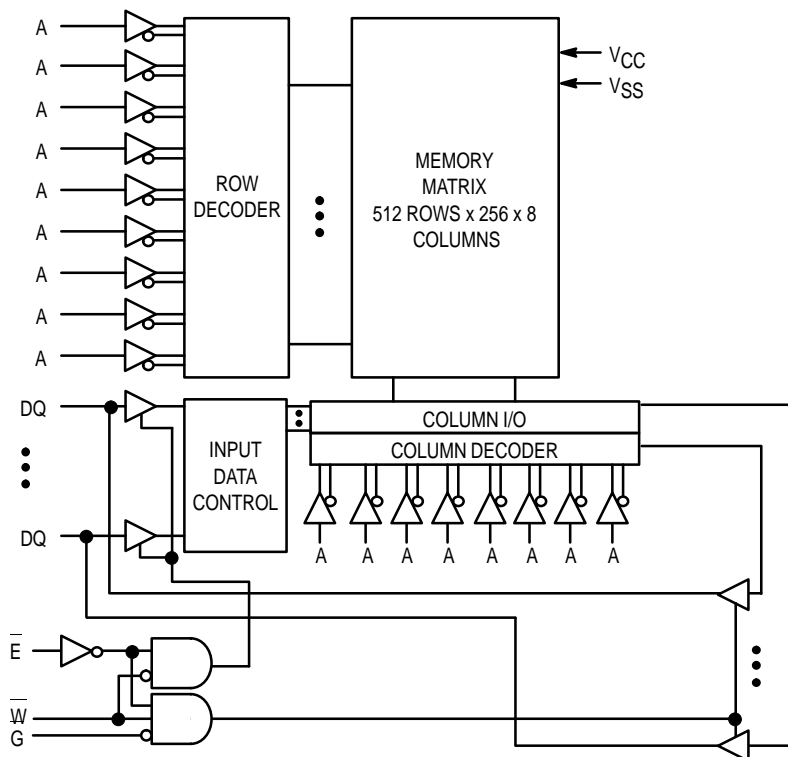
The MCM6726D is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable (\overline{G}) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

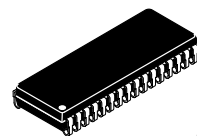
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V \pm 10% Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



MCM6726D



WJ PACKAGE
400 MIL SOJ
CASE 857A-02

PIN ASSIGNMENT

A	1	32	A
A	2	31	A
A	3	30	A
A	4	29	A
\overline{E}	5	28	G
DQ	6	27	DQ
DQ	7	26	DQ
VCC	8	25	VSS
VSS	9	24	VCC
DQ	10	23	DQ
DQ	11	22	DQ
W	12	21	A
A	13	20	A
A	14	19	A
A	15	18	A
A	16	17	A

PIN NAMES

A	Address Input
\overline{E}	Chip Enable
W	Write Enable
G	Output Enable
DQ	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

TRUTH TABLE (X = Don't Care)

E	G	W	Mode	V _{CC} Current	Output	Cycle
H	X	X	Not Selected	I _{SB1} , I _{SB2}	High-Z	—
L	H	H	Output Disabled	I _{CCA}	High-Z	—
L	L	H	Read	I _{CCA}	D _{out}	Read Cycle
L	X	L	Write	I _{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	− 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	− 0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 30	mA
Power Dissipation	P _D	1.2	W
Temperature Under Bias	T _{bias}	− 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.3**	V
Input Low Voltage	V _{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{lkg(I)}	—	± 1.0	μA
Output Leakage Current (E = V _{IH} , V _{out} = 0 to V _{CC})	I _{lkg(O)}	—	± 1.0	μA
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V
Output High Voltage (I _{OH} = − 4.0 mA)	V _{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726D-8	6726D-10	6726D-12	Unit	Notes
AC Active Supply Current (I _{out} = 0 mA) (V _{CC} = max, f = f _{max})	I _{CCA}	195	175	165	mA	1, 2, 3
Active Quiescent Current (E = V _{IL} , V _{CC} = max, f = 0 MHz)	I _{CC2}	100	100	100	mA	
AC Standby Current (E = V _{IH} , V _{CC} = max, f = f _{max})	I _{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V _{CC} = max, f = 0 MHz, E ≥ V _{CC} − 0.2 V, V _{in} ≤ V _{SS} + 0.2 V, or ≥ V _{CC} − 0.2 V)	I _{SB2}	20	20	20	mA	

NOTES:

- Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
- All addresses transition simultaneously low (LSB) and then high (MSB).
- Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C _{in}	—	6	pF
Control Pin Input Capacitance	C _{in}	—	6	pF
Input/Output Capacitance	C _{I/O}	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 2 ns

Output Timing Measurement Reference Level 1.5 V
 Output Load See Figure 1a

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6726D-8		6726D-10		6726D-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t _{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t _{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t _{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t _{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t _{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t _{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t _{EHQZ}	—	4	—	5	—	6	ns	4,5,6
Output Enable High to Output High-Z	t _{GHQZ}	—	4	—	5	—	6	ns	4,5,6

NOTES:

1. W is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected (E = V_{IL}, G = V_{IL}).
8. Addresses valid prior to or coincident with E going low.

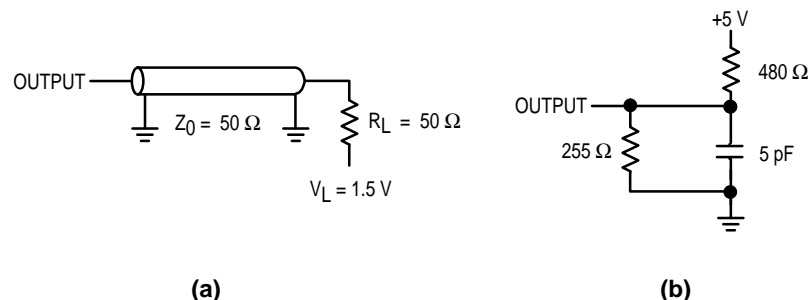
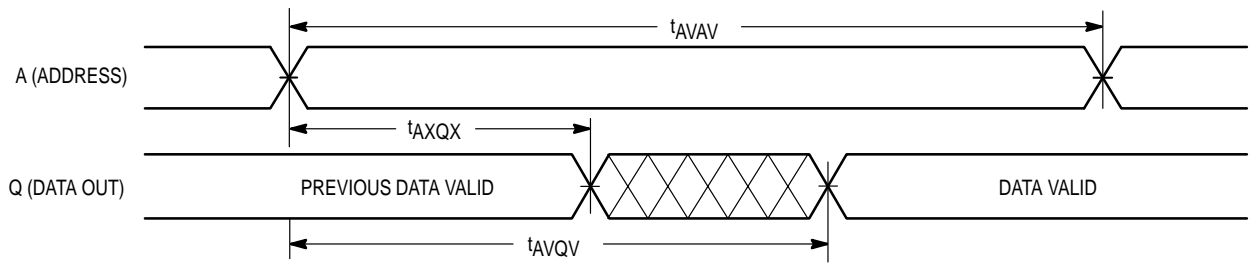


Figure 1. AC TEST LOADS

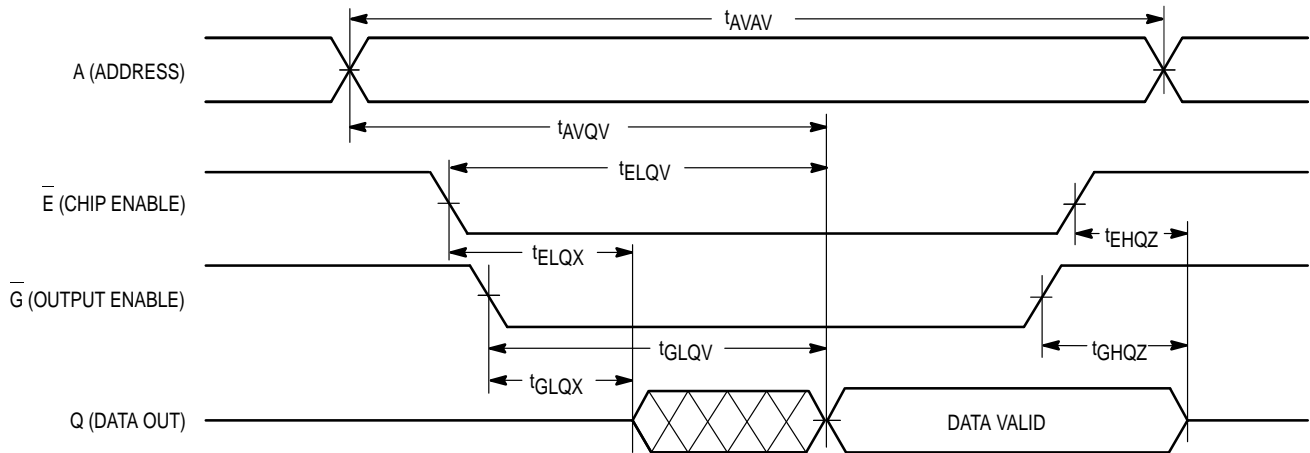
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



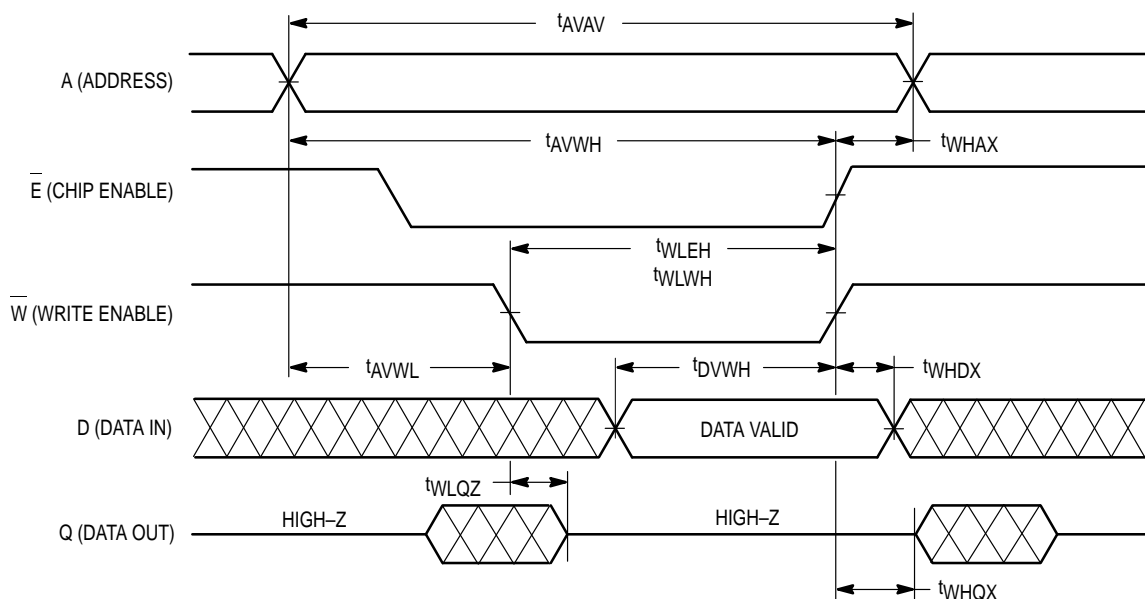
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	6726D-8		6726D-10		6726D-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, G High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, G High	t_{WLWH} , t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	—	4	—	5	—	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$ both for a given device and from device to device.

WRITE CYCLE 1



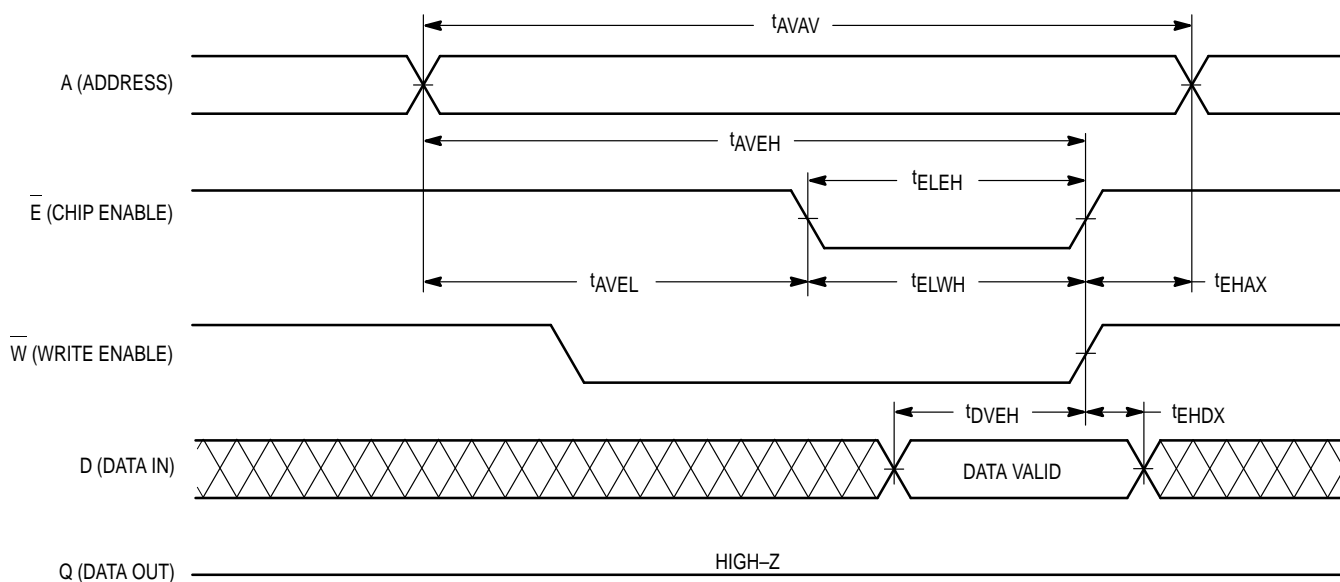
WRITE CYCLE 2 (\overline{E} Controlled, See Notes 1 and 2)

Parameter	Symbol	6726D-8		6726D-10		6726D-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH} , t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If \overline{E} goes low coincident with or after \overline{W} goes low, the output will remain in a high impedance condition.
5. If \overline{E} goes high coincident with or before \overline{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2

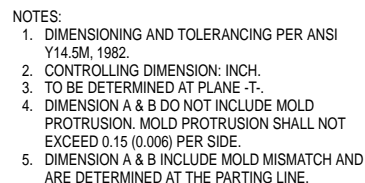


ORDERING INFORMATION (Order by Full Part Number)

MCM 6726D WJ XX X
 Motorola Memory Prefix _____
 Part Number _____
 Shipping Method (R = Tape and Reel, Blank = Rails)
 Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
 Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6726DWJ8 MCM6726DWJ10 MCM6726DWJ12
 MCM6726DWJ8R MCM6726DWJ10R MCM6726DWJ12R

32-LEAD
400 MIL SOJ
CASE 857A-02



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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