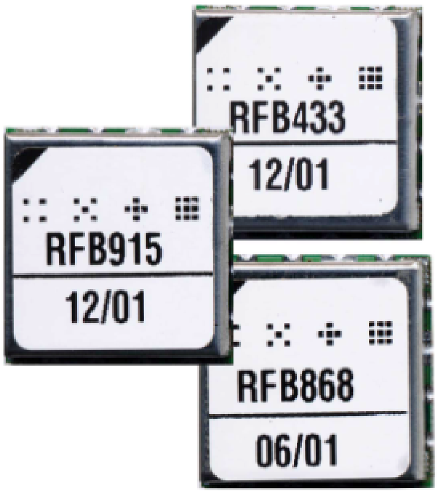
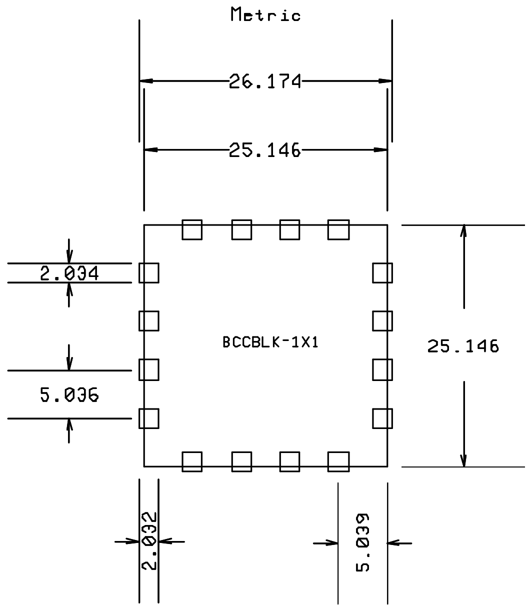
RFB868B, RF Block 868MHz Product Guide v1.4

RFB868B is an 868MHz FHSS transceiver module and measures only one square inch. It's a fully tested and shielded block with all external RF components included. The RFB868B covers the European 868MHz ISM band. RFB868B is pin compatible with RFB433B and RFB915B and allow the user to cover all major markets with one motherboard. It can be utilized in any environment where wireless remote connection is advantageous over cables. The RFB868B is ideal were Ultra low power, low-cost and time to market is one of the major issues. A typical system consists of a microprocessor and a RF Block plus an antenna solution.





Quick reference data:

Parameter	Typ	Unit
Operation frequency	868	MHz
Output power	+10	dBm
Sensitivity	-103	dBm
Data rate	19.2	kbaud/s
Current consumption Rx	<12	mA
Current consumption TX	<50	mA
Power down current	<1	uA

Ordering Information:

Part Number	Temp range	MOQ
RFB868B	-20°C to +75°C	2pcs
Part Number	**Description**	**MOQ**
EVK868	Evaluation kit 868MHz	1 kit

URL:	**www.BlueChip.no**
Mail:	**post@BlueChip.no**

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Electrical Characteristics

Vdd=2.5-3.4V, T=25°C, unless otherwise specified

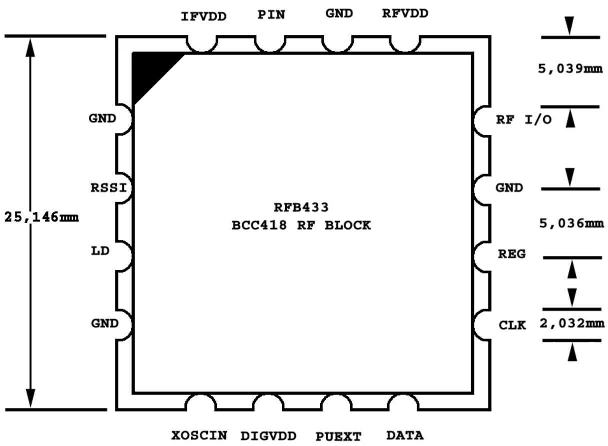
Parameter	Conditions	Min.	Typ.	Max.	Unit
Overall					
Operating frequency		863	868	873	MHz
Supply voltage		2.5	3.0	3.4	V
Power down current			< 1	2	µA
Logic high input, Vih		70%			Vdd
Logic low input, Vil				30%	Vdd
DataIXO, logic high output (Voh)	Ioh=-500µA	Vdd-0.3			V
DataIXO, logic low output (Vol)	Iol= 500µA			0.3	V
LockDet, logic high output (Voh)	Ioh=-100µA	Vdd-0.25			V
LockDet, logic low output (Vol)	Iol= 100µA			0.25	V
Reference frequency			16		MHz
Clock/Data frequency				10	MHz
Clock/Data duty-cycle		25		75	%
Data setup to clock (rising edge)		25			ns
Operating temperature range		–20	25	+75	°C
VCO and PLL section					
PLL lock time			4		ms
Rx – (Tx with PA on) switch time			2		ms
Transmit section	f_{OUT}=868MHz				
Output power	R_{LOAD}=50Ω, Vdd=3.0V		10		dBm
Transmit data rate			19.2		kbauds
Freq. Deviation			30		kHz
Current consumption transmit mode	10 dBm, R_{LOAD}=50Ω		50		mA
Receive section	f_{IN}=868MHz				
Receiver sensitivity	BER=10^{-3}		–103		dBm
Input 1dB compression level			–41		dBm
Input IP3			–31		dBm
RSSI dynamic range			60		dB
RSSI output voltage	Pin = –100dBm		0.7		V
	Pin = –30dBm		2.1		V
Adjacent channel rejection	200kHz channel spacing		45		dB
Blocking immunity (1MHz)			57		dB
Receiver settling time			1		ms
Current consumption receive mode			12		mA

General Description

The transmitter section consists of a PLL frequency synthesizer and a power amplifier. The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual modulus prescaler, programmable frequency dividers and a phase-detector. The VCO is a Colpitts oscillator with internal resonator and varactor. FSK modulation is applied to the VCO. The output power of the power amplifier can be programmed to 8 levels. A lock-detect circuit detects when the PLL is in lock.

In receive mode the PLL synthesizer generates the local oscillator (LO) signal. The N, M and A values that give the LO frequency are stored in the N0, M0 and A0 registers. The receiver is a zero intermediate frequency (IF) type in order to make channel filtering possible with low power integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel include a pre-amplifier, a third order Sallen-Key RC lowpass filter that protects the following gyrator filter from strong adjacent channel signals and finally a limiter. The main channel filter is a gyrator-capacitor implementation of a seven-pole elliptic lowpass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 10kHz, 30kHz, 60kHz and 200kHz. Due to the tolerance of the internal x-tal and selected deviation this filter should be set to 60kHz. The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase of the I and the Q channel signal. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0'). The output of the receiver is available on the DATA pin. A RSSI circuit (receive signal strength indicator) indicates the received signal level. A T/R switch is implemented with 2 pin diodes to give maximum input sensitivity and output power.

A two pin serial interface is used to program the module.



Pin Configuration

Name	Description
GND	Ground plane connection
RSSI	Analog received signal strength indicator output (optional use)
LD	Lock detect output (optional use)
GND	Ground plane connection
XOSCIN	Crystal oscillator input (optional use)
DIGVDD	Digital circuitry power
PUEXT	External power down (0=power down)
DATA	Bi directional RX / TX data

Name	Description
CLK	Control register data clock
REG	Control register data input, programming of RF block
GND	Ground plane connection
RF I/O	50Ω RF input / output
RFVDD	LNA and PA power
GND	Ground plane connection
PIN	TX/RX switch control input
IFVDD	IF power

Programming

A two-line bus is used to program the circuit; the two lines being CLK and REG. The 2-line serial bus interface allows control over the frequency dividers and the selective powering up of Tx, Rx and Synthesizer circuit blocks. After power on the PUEXT should be held low while loading in the control word for the first time. When the control word has been loaded, the PUEXT is brought high for the rest of the power on cycle. The interface consists of an 80-bit programming register. Data is entered on the RegIn line with the most significant bit first. The first bit entered is called p1, the last one p80. The bits in the programming register are arranged as shown in table1.

Table 1: Bit allocation

p1 – p6	p7 – p12	p13 – p24	p25 – p36	p37 – p46	p47 – p56	p57	p58
A1	A0	N1	N0	M1	M0	'0'	Pa2
p59	p60	p61	p62	p63	p64	p65	p66
Pa1	Pa0	Gc	ByLNA	Ref6	Ref5	Ref4	Ref3
p67	p68	p69	p70	p71	p72	p73	p74
Ref2	Ref1	Ref0	Cpmp1	Cpmp0	'1'	'0'	'0'
p75	p76	p77	p78	p79	p80		
'0'	'0'	'0'	'0'	RT	Pu		

Table 2: Bit description

Name	Description
A1	frequency divider A1, 6 bits
A0	frequency divider A0, 6 bits
N1	frequency divider N1, 12 bits
N0	frequency divider N0, 12 bits
M1	frequency divider M1, 10 bits
M0	frequency divider M0, 10 bits
Pa2	gain setting in power amplifier
Pa1	pa2, pa1, pa0 = 0 : lowest output power
Pa0	pa2, pa1, pa0 = 1 : highest output power
Gc	gain control in power amplifier buffer,1=high gain
ByLNA	1 = the Low Noise Amplifier (LNA) is bypassed
Ref6	
Ref5	reference settings in lock detector
Ref4	
Ref3	all 0's: highest reference
Ref2	all 1's: lowest reference
Ref1	
Ref0	
Cpmp1	charge pump setting: Cpmp1=0, Cpmp0=0 : ±125uA
Cpmp0	Cpmp1=0, Cpmp0=1 : ±500uA Cpmp1=1, Cpmp0=0 : controlled by LD (LD) LD=0: ±500uA, LD=1: ±125uA Cpmp1=1, Cpmp0=1 : same as previous in Tx. In Rx the current is ±500µA.
RT	0 = receive mode 1 = transmit mode
Pu	1 = power up, 0 = power down (When Pu=1, power down is controlled by PuExt)

The 80bit control word is first read into a shift-register, and is then loaded into a parallel register by a transition of the REG signal (positive or negative) when the CLK signal is high. The circuit then goes directly into the specified mode (receive, transmit, etc.).

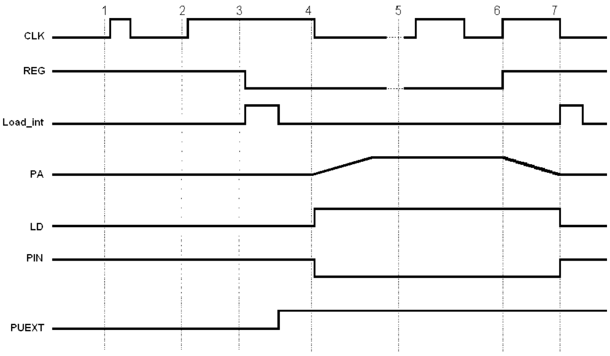


Figure 1: Timing of CLK, REG and the internal Load_int and PA_C signals for the first time after power on.

1: The second last bit is clocked into the first shift register ('1').
2: The last bit is clocked into the first shift register ('1').
3: A transition on the REG signal generates an internal load pulse that loads the control word into the parallel register. The circuit enters the new mode (in this case Tx-mode). The circuit stabilizes in the new mode.
4: The PIN should be brought low when the clock signal goes low. When the clock signal is low the power amplifier (PA) is turned on slowly in order to minimize spurious components on the RF output signal. To be sure the PLL is in lock before the PA is turned on, the PA should be turned on after LD.
The negative transition on the clock signal should come a minimum time of one period of the comparison frequency after the internal load pulse is generated.
5: The power amplifier is fully turned on.
6: A new control word is entered into the first register. A transition on the REG signal when CLK is high will now turn the power amplifier off.
7: When the power amplifier is turned off, an internal load pulse is generated. The PIN should be brought high when the PA is off. New control word is loaded into the parallel register and the circuit enters a new mode (in this case power down mode). CLK must go low after the internal load pulse is generated.

As long as transitions on REG are avoided when CLK is high, a new control word can be clocked into the first register any time without affecting the operation of the transceiver.

The N, M and A values can be calculated from the formula:

$$\frac{f_{XCO}}{M} = \frac{f_{RF}}{64 \cdot N + A}$$

where f_{XCO} is the crystal oscillator frequency and is 16MHz.

Example1: f_{RF} = 869.0MHz

	A1	A0	N1	N0	M1	M0
Tx	3	3	95	95	112	112
Rx	3	3	95	95	112	112
	p57	Pa2	Pa1	Pa0	Gc	ByLNA
Tx	0	1	1	1	1	0
Rx	0	1	1	1	1	0
	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1
Tx	0	0	0	0	0	0
Rx	0	0	0	0	0	0
	Ref0	Cpmp1	Cpmp0	p72	p73	p74
Tx	0	0	1	1	0	0
Rx	0	0	1	1	0	0
	p75	p76	p77	p78	RT	Pu
Tx	0	0	0	0	1	1
Rx	0	0	0	0	0	1

Binary form: (MSB to the left):

```
Tx:     000011 000011 000001011111
        000001011111 0001110000 0001110000
        0111100000000001100000011
Rx:     000011 000011 000001011111
        000001011111 0001110000 0001110000
        0111100000000001100000001
```

Example2: f_{RF} = 868.4MHz

	A1	A0	N1	N0	M1	M0
Tx	49	49	101	101	120	120
Rx	49	49	101	101	120	120
	p57	Pa2	Pa1	Pa0	Gc	ByLNA
Tx	0	1	1	1	1	0
Rx	0	1	1	1	1	0
	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1
Tx	0	0	0	0	0	0
Rx	0	0	0	0	0	0
	Ref0	Cpmp1	Cpmp0	p72	p73	p74
Tx	0	0	1	1	0	0
Rx	0	0	1	1	0	0
	p75	p76	p77	p78	RT	Pu
Tx	0	0	0	0	1	1
Rx	0	0	0	0	0	1

Binary form: (MSB to the left):

```
Tx:     110001 110001 000001100101
        000001100101 0001111000 0001111000
        0111100000000001100000011
Rx:     110001 110001 000001100101
        000001100101 0001111000 0001111000
        0111100000000001100000001
```

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Application notes

DATA

Bi-directional RX / TX data. Modulation is applied to the VCO and therefore the modulation cannot have any DC component. Some kind of coding is needed to ensure that the modulation is DC free, e.g. Manchester code or block code. With Manchester code the bit rate is half the baud rate, but with 3B4B block code the bit rate is ¾ of the baud rate. Connection to a Microcontroller capture/ compare I/O pin allows use of the clock recovery and bit sync routines in the supplied software. The I/O pin should be set as an input for 6ms after programming the RF block in TX mode, prior to starting transmission of data. This gives the fastest set up times for transmit. The 6 ms is for the settling time of the PLL and the P.A. stage ramp up. The I/O line should be set as an input after completion of keying of TX data, prior to loading a new control word in the RF block.

DIGVDD It is recommended that DIGVDD is divided from IFVDD and RFVDD and joined at a common VDD point.

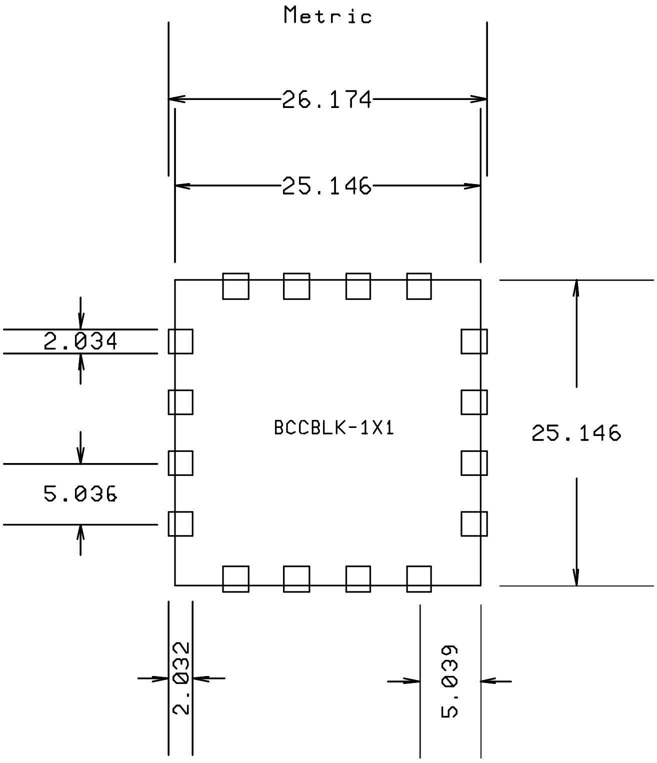
LD The RF Block has a lock detector feature that indicates whether the PLL is in lock or not. A logic high on pin LD means that the PLL is in lock. *See reference manual for BCC918.*

RSSI (Received Signal Strength Indicator) The RSSI provides a DC output voltage proportional to the strength of the RF input signal. Impedance is approximate 50k. *See reference manual for BCC918.*

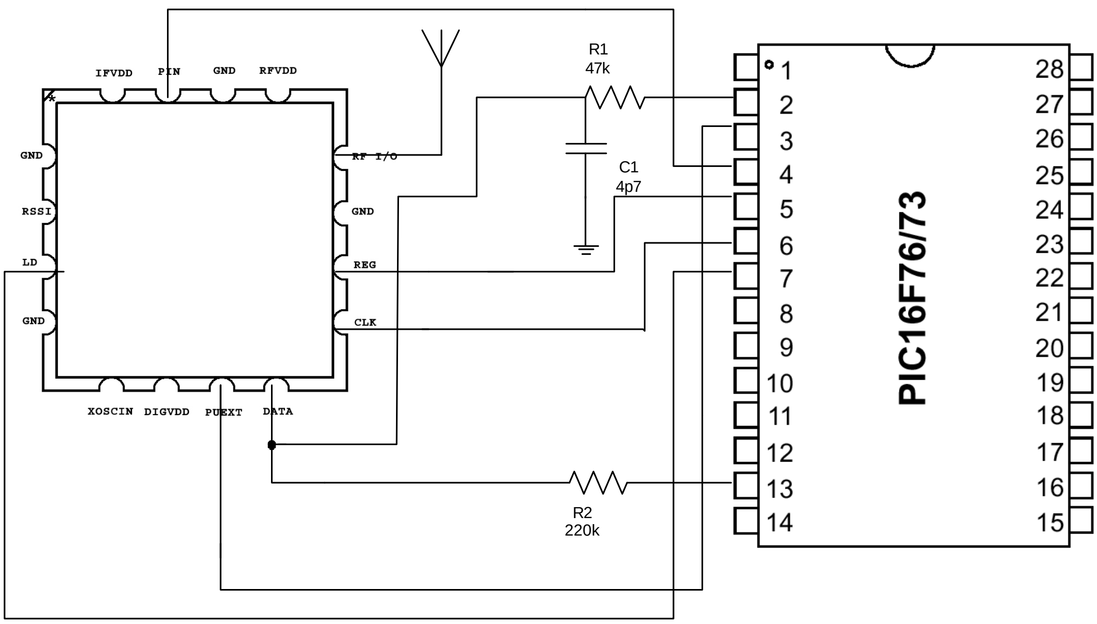
PUEXT The PUEXT pin should be connected to an I/O line.After power on, the pin should be held low while loading in the control word for the first time. An alternative, if no I/O lines are available, is to connect the PUEXT pin to VDD via resistor and a capacitor to GND. After power is applied, a control word should be clocked in during the time the PUEXT pin is at logic 0 levels (30% of VDD). The time constant should be chosen to match the data clock in rate from the Microcontroller. Further loading in of control words can be done in a normal manner.

PCB layout

Keep ground plane areas as large as possible. Keep the track to the RF connector/ antenna as short as possible. The best is a 50 ohm strip line solution. VDD must be "clean" for good performance. If a RS232 converter IC is used , run it on its own voltage regulator as they introduce spikes on VDD. Avoid switch mode power supplies if possible or use a linear regulator after them. For a final type approval of a complete product, there must be detection of a low voltage condition so that the microcontroller places the RF block in standby, otherwise the VCO can get out of lock at below 2.4V and there could be unintentional radiation of RF outside the intended band.



Interfacing to PIC16LF73



Interfacing to microcontrollers operating at higher voltage levels

Standard RF blocks are designed to operate from 2.7V to 3.3V. Some Microcontrollers require higher operating voltages for maximum clock rates.

The circuit below allows interfacing of an RF block with a 3V3 supply to a Microcontroller with a 5V supply. Resistors form a voltage divider for the 5V logic levels from the Microcontroller.

In RX, Q1 detects a logic low or high level via R6 and the inverted signal is converted to 5V levels via R6.

RX_EN is held low during RX and 3 state in TX and standby mode In transmit, R2 together with 2 internal 40k.