

## Features

- High-performance, Low-power AVR<sup>®</sup> 8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Non volatile Program and Data Memories
  - 32K/64K/128K Bytes of In-System Reprogrammable Flash (AT90CAN32/64/128)
    - Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    - Selectable Boot Size: 1K Bytes, 2K Bytes, 4K Bytes or 8K Bytes
    - In-System Programming by On-Chip Boot Program (CAN, UART, ...)
    - True Read-While-Write Operation
  - 1K/2K/4K Bytes EEPROM (Endurance: 100,000 Write/Erase Cycles) (AT90CAN32/64/128)
  - 2K/4K/4K Bytes Internal SRAM (AT90CAN32/64/128)
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Programming Flash (Hardware ISP), EEPROM, Lock & Fuse Bits
  - Extensive On-chip Debug Support
- CAN Controller 2.0A & 2.0B - ISO 16845 Certified <sup>(1)</sup>
  - 15 Full Message Objects with Separate Identifier Tags and Masks
  - Transmit, Receive, Automatic Reply and Frame Buffer Receive Modes
  - 1Mbits/s Maximum Transfer Rate at 8 MHz
  - Time stamping, TTC & Listening Mode (Spying or Autobaud)
- Peripheral Features
  - Programmable Watchdog Timer with On-chip Oscillator
  - 8-bit Synchronous Timer/Counter-0
    - 10-bit Prescaler
    - External Event Counter
    - Output Compare or 8-bit PWM Output
  - 8-bit Asynchronous Timer/Counter-2
    - 10-bit Prescaler
    - External Event Counter
    - Output Compare or 8-Bit PWM Output
    - 32Khz Oscillator for RTC Operation
  - Dual 16-bit Synchronous Timer/Counters-1 & 3
    - 10-bit Prescaler
    - Input Capture with Noise Canceler
    - External Event Counter
    - 3-Output Compare or 16-Bit PWM Output
    - Output Compare Modulation
  - 8-channel, 10-bit SAR ADC
    - 8 Single-ended Channels
    - 7 Differential Channels
    - 2 Differential Channels With Programmable Gain at 1x, 10x, or 200x
  - On-chip Analog Comparator
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USART
  - Master/Slave SPI Serial Interface
    - Programming Flash (Hardware ISP)
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - 8 External Interrupt Sources
  - 5 Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down & Standby
  - Software Selectable Clock Frequency
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-lead QFN
- Operating Voltages: 2.7 - 5.5V
- Operating temperature: Industrial (-40°C to +85°C)
- Maximum Frequency: 8 MHz at 2.7V, 16 MHz at 4.5V

Note: 1. Details on [section 19.4.3 on page 242](#).



**8-bit AVR<sup>®</sup>**  
**Microcontroller**  
**with**  
**32K/64K/128K**  
**Bytes of**  
**ISP Flash**  
**and**  
**CAN Controller**

**AT90CAN32**  
**AT90CAN64**  
**AT90CAN128**

## Summary

Rev. 7679HS-CAN-08/08



## 1. Description

### 1.1 Comparison Between AT90CAN32, AT90CAN64 and AT90CAN128

AT90CAN32, AT90CAN64 and AT90CAN128 are hardware and software compatible. They differ only in memory sizes as shown in [Table 1-1](#).

**Table 1-1.** Memory Size Summary

| Device     | Flash      | EEPROM   | RAM      |
|------------|------------|----------|----------|
| AT90CAN32  | 32K Bytes  | 1K Byte  | 2K Bytes |
| AT90CAN64  | 64K Bytes  | 2K Bytes | 4K Bytes |
| AT90CAN128 | 128K Bytes | 4K Byte  | 4K Bytes |

### 1.2 Part Description

The AT90CAN32/64/128 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90CAN32/64/128 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90CAN32/64/128 provides the following features: 32K/64K/128K bytes of In-System Programmable Flash with Read-While-Write capabilities, 1K/2K/4K bytes EEPROM, 2K/4K/4K bytes SRAM, 53 general purpose I/O lines, 32 general purpose working registers, a CAN controller, Real Time Counter (RTC), four flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented Two-wire Serial Interface, an 8-channel 10-bit ADC with optional differential input stage with programmable gain, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and five software selectable power saving modes.

The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI/CAN ports and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By

combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel AT90CAN32/64/128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

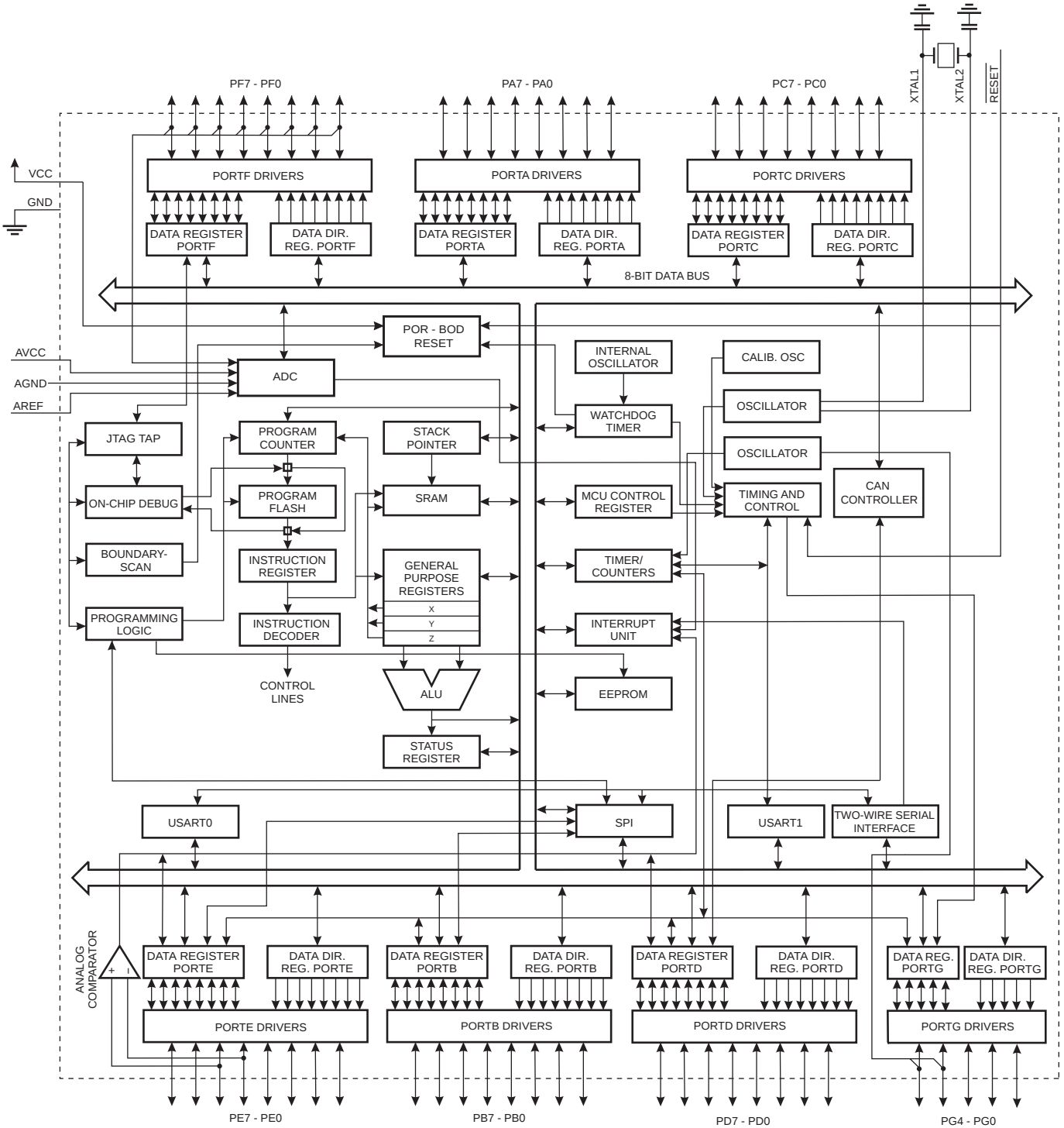
The AT90CAN32/64/128 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

### **1.3 Disclaimer**

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

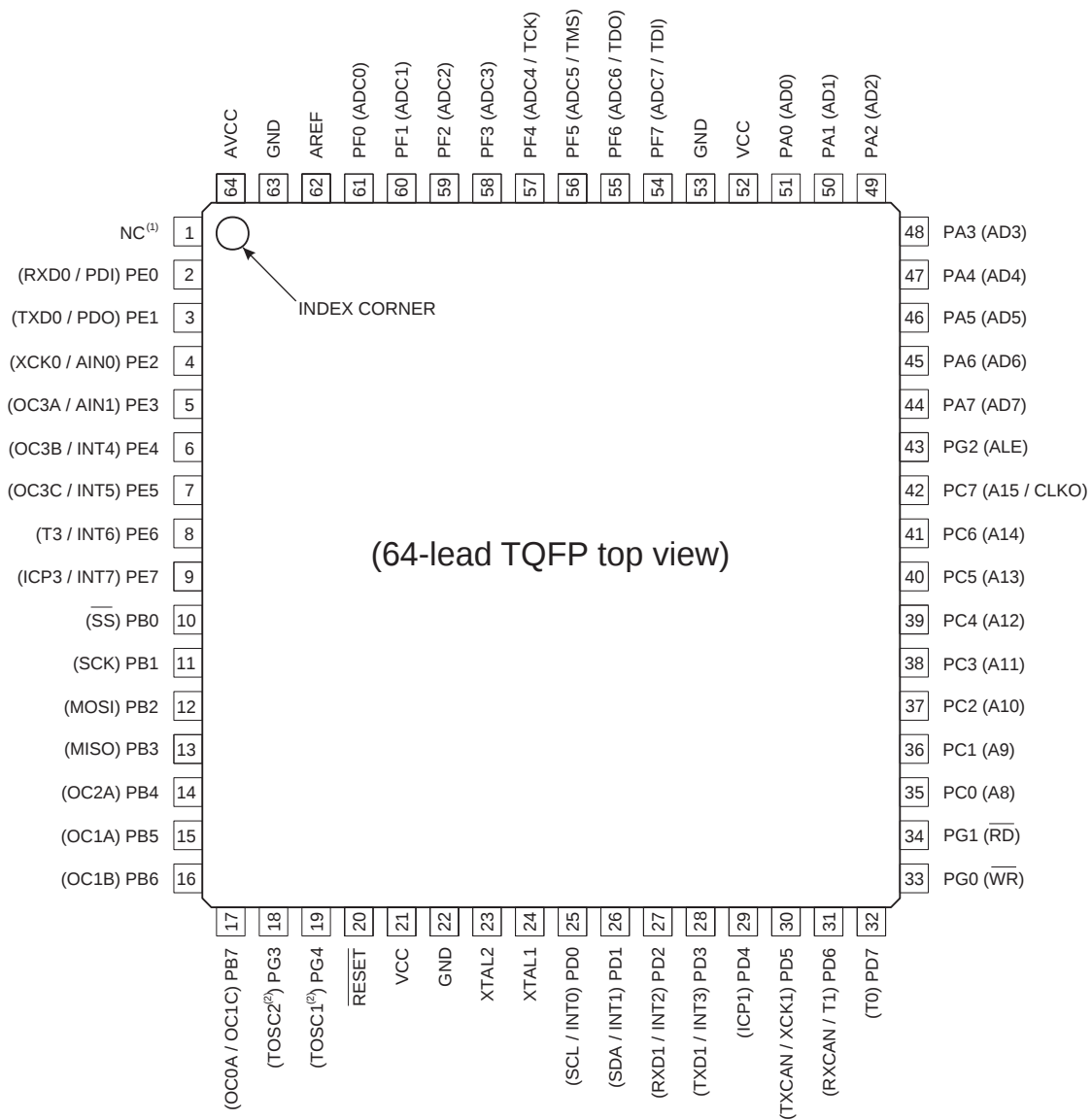
## 1.4 Block Diagram

Figure 1-1. Block Diagram



## 1.5 Pin Configurations

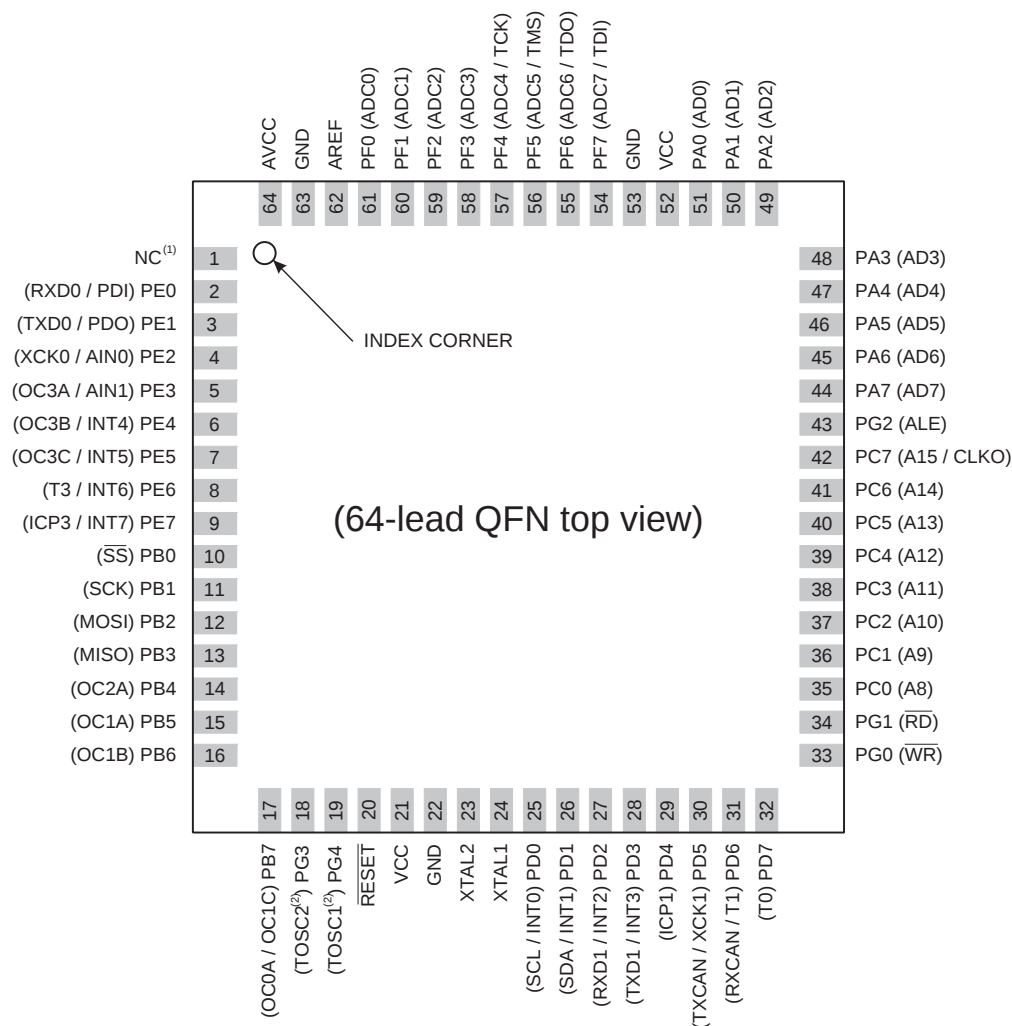
Figure 1-2. Pinout AT90CAN32/64/128 - TQFP



<sup>(1)</sup> NC = Do not connect (May be used in future devices)

<sup>(2)</sup> Timer2 Oscillator

**Figure 1-3.** Pinout AT90CAN32/64/128 - QFN



<sup>(1)</sup> NC = Do not connect (May be used in future devices)

<sup>(2)</sup> Timer2 Oscillator

**Note:** The large center pad underneath the QFN package is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

## 1.6 Pin Descriptions

### 1.6.1 VCC

Digital supply voltage.

### 1.6.2 GND

Ground.

**1.6.3 Port A (PA7..PA0)**

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the AT90CAN32/64/128 as listed on [page 74](#).

**1.6.4 Port B (PB7..PB0)**

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the AT90CAN32/64/128 as listed on [page 76](#).

**1.6.5 Port C (PC7..PC0)**

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the AT90CAN32/64/128 as listed on [page 78](#).

**1.6.6 Port D (PD7..PD0)**

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90CAN32/64/128 as listed on [page 80](#).

**1.6.7 Port E (PE7..PE0)**

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the AT90CAN32/64/128 as listed on [page 83](#).

**1.6.8 Port F (PF7..PF0)**

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port F also serves the functions of the JTAG interface. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

#### 1.6.9 Port G (PG4..PG0)

Port G is a 5-bit I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the AT90CAN32/64/128 as listed on [page 88](#).

#### 1.6.10 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset. The minimum pulse length is given in characteristics. Shorter pulses are not guaranteed to generate a reset. The I/O ports of the AVR are immediately reset to their initial state even if the clock is not running. The clock is needed to reset the rest of the AT90CAN32/64/128.

#### 1.6.11 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

#### 1.6.12 XTAL2

Output from the inverting Oscillator amplifier.

#### 1.6.13 AVCC

AVCC is the supply voltage pin for the A/D Converter on Port F. It should be externally connected to  $V_{CC}$ , even if the ADC is not used. If the ADC is used, it should be connected to  $V_{CC}$  through a low-pass filter.

#### 1.6.14 AREF

This is the analog reference pin for the A/D Converter.

## 2. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

### 3. Register Summary

| Address | Name     | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1   | Bit 0   | Page                     |
|---------|----------|----------|----------|----------|----------|----------|----------|---------|---------|--------------------------|
| (0xFF)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xFE)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xFD)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xFC)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xFB)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xFA)  | CANMSG   | MSG 7    | MSG 6    | MSG 5    | MSG 4    | MSG 3    | MSG 2    | MSG 1   | MSG 0   | <a href="#">page 266</a> |
| (0xF9)  | CANSTMH  | TIMSTM15 | TIMSTM14 | TIMSTM13 | TIMSTM12 | TIMSTM11 | TIMSTM10 | TIMSTM9 | TIMSTM8 | <a href="#">page 266</a> |
| (0xF8)  | CANSTML  | TIMSTM7  | TIMSTM6  | TIMSTM5  | TIMSTM4  | TIMSTM3  | TIMSTM2  | TIMSTM1 | TIMSTM0 | <a href="#">page 266</a> |
| (0xF7)  | CANIDM1  | IDMSK28  | IDMSK27  | IDMSK26  | IDMSK25  | IDMSK24  | IDMSK23  | IDMSK22 | IDMSK21 | <a href="#">page 265</a> |
| (0xF6)  | CANIDM2  | IDMSK20  | IDMSK19  | IDMSK18  | IDMSK17  | IDMSK16  | IDMSK15  | IDMSK14 | IDMSK13 | <a href="#">page 265</a> |
| (0xF5)  | CANIDM3  | IDMSK12  | IDMSK11  | IDMSK10  | IDMSK9   | IDMSK8   | IDMSK7   | IDMSK6  | IDMSK5  | <a href="#">page 265</a> |
| (0xF4)  | CANIDM4  | IDMSK4   | IDMSK3   | IDMSK2   | IDMSK1   | IDMSK0   | RTRMSK   | —       | IDEMSK  | <a href="#">page 265</a> |
| (0xF3)  | CANIDT1  | IDT28    | IDT27    | IDT26    | IDT25    | IDT24    | IDT23    | IDT22   | IDT21   | <a href="#">page 263</a> |
| (0xF2)  | CANIDT2  | IDT20    | IDT19    | IDT18    | IDT17    | IDT16    | IDT15    | IDT14   | IDT13   | <a href="#">page 263</a> |
| (0xF1)  | CANIDT3  | IDT12    | IDT11    | IDT10    | IDT9     | IDT8     | IDT7     | IDT6    | IDT5    | <a href="#">page 263</a> |
| (0xF0)  | CANIDT4  | IDT4     | IDT3     | IDT2     | IDT1     | IDT0     | RTRTAG   | RB1TAG  | RB0TAG  | <a href="#">page 263</a> |
| (0xEF)  | CANCDMOB | CONMOB1  | CONMOB0  | RPLV     | IDE      | DLC3     | DLC2     | DLC1    | DLC0    | <a href="#">page 262</a> |
| (0xEE)  | CANSTMOB | DLCW     | TXOK     | RXOK     | BERR     | SERR     | CERR     | FERR    | AERR    | <a href="#">page 261</a> |
| (0xED)  | CANPAGE  | MOBNB3   | MOBNB2   | MOBNB1   | MOBNB0   | AINC     | INDX2    | INDX1   | INDX0   | <a href="#">page 260</a> |
| (0xEC)  | CANHPMOB | HPMOB3   | HPMOB2   | HPMOB1   | HPMOB0   | CGP3     | CGP2     | CGP1    | CGP0    | <a href="#">page 260</a> |
| (0xEB)  | CANREC   | REC7     | REC6     | REC5     | REC4     | REC3     | REC2     | REC1    | REC0    | <a href="#">page 260</a> |
| (0xEA)  | CANTEC   | TEC7     | TEC6     | TEC5     | TEC4     | TEC3     | TEC2     | TEC1    | TEC0    | <a href="#">page 260</a> |
| (0xE9)  | CANTTCH  | TIMTTC15 | TIMTTC14 | TIMTTC13 | TIMTTC12 | TIMTTC11 | TIMTTC10 | TIMTTC9 | TIMTTC8 | <a href="#">page 260</a> |
| (0xE8)  | CANTTCL  | TIMTTC7  | TIMTTC6  | TIMTTC5  | TIMTTC4  | TIMTTC3  | TIMTTC2  | TIMTTC1 | TIMTTC0 | <a href="#">page 260</a> |
| (0xE7)  | CANTIMH  | CANTIM15 | CANTIM14 | CANTIM13 | CANTIM12 | CANTIM11 | CANTIM10 | CANTIM9 | CANTIM8 | <a href="#">page 259</a> |
| (0xE6)  | CANTIML  | CANTIM7  | CANTIM6  | CANTIM5  | CANTIM4  | CANTIM3  | CANTIM2  | CANTIM1 | CANTIM0 | <a href="#">page 259</a> |
| (0xE5)  | CANTCON  | TPRSC7   | TPRSC6   | TPRSC5   | TPRSC4   | TPRSC3   | TPRSC2   | TPRSC1  | TPRSC0  | <a href="#">page 259</a> |
| (0xE4)  | CANBT3   | —        | PHS22    | PHS21    | PHS20    | PHS12    | PHS11    | PHS10   | SMP     | <a href="#">page 258</a> |
| (0xE3)  | CANBT2   | —        | SJW1     | SJW0     | —        | PRS2     | PRS1     | PRS0    | —       | <a href="#">page 258</a> |
| (0xE2)  | CANBT1   | —        | BRP5     | BRP4     | BRP3     | BRP2     | BRP1     | BRP0    | —       | <a href="#">page 257</a> |
| (0xE1)  | CANSIT1  | —        | SIT14    | SIT13    | SIT12    | SIT11    | SIT10    | SIT9    | SIT8    | <a href="#">page 257</a> |
| (0xE0)  | CANSIT2  | SIT7     | SIT6     | SIT5     | SIT4     | SIT3     | SIT2     | SIT1    | SIT0    | <a href="#">page 257</a> |
| (0xDF)  | CANIE1   | —        | IEMOB14  | IEMOB13  | IEMOB12  | IEMOB11  | IEMOB10  | IEMOB9  | IEMOB8  | <a href="#">page 257</a> |
| (0xDE)  | CANIE2   | IEMOB7   | IEMOB6   | IEMOB5   | IEMOB4   | IEMOB3   | IEMOB2   | IEMOB1  | IEMOB0  | <a href="#">page 257</a> |
| (0xDD)  | CANEN1   | —        | ENMOB14  | ENMOB13  | ENMOB12  | ENMOB11  | ENMOB10  | ENMOB9  | ENMOB8  | <a href="#">page 256</a> |
| (0xDC)  | CANEN2   | ENMOB7   | ENMOB6   | ENMOB5   | ENMOB4   | ENMOB3   | ENMOB2   | ENMOB1  | ENMOB0  | <a href="#">page 256</a> |
| (0xDB)  | CANGIE   | ENIT     | ENBOFF   | ENRX     | ENTX     | ENERR    | ENBX     | ENERG   | ENOVRT  | <a href="#">page 255</a> |
| (0xDA)  | CANGIT   | CANIT    | BOFFIT   | OVRTIM   | BXOK     | SERG     | CERG     | FERG    | AERG    | <a href="#">page 254</a> |
| (0xD9)  | CANGSTA  | —        | OVRG     | —        | TXBSY    | RXBSY    | ENFG     | BOFF    | ERRP    | <a href="#">page 253</a> |
| (0xD8)  | CANGCON  | ABRQ     | OVRQ     | TTC      | SYNTTC   | LISTEN   | TEST     | ENA/STB | SWRES   | <a href="#">page 252</a> |
| (0xD7)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD6)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD5)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD4)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD3)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD2)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD1)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xD0)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xCF)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xCE)  | UDR1     | UDR17    | UDR16    | UDR15    | UDR14    | UDR13    | UDR12    | UDR11   | UDR10   | <a href="#">page 195</a> |
| (0xCD)  | UBRR1H   | —        | —        | —        | —        | UBRR111  | UBRR110  | UBRR19  | UBRR18  | <a href="#">page 199</a> |
| (0xCC)  | UBRR1L   | UBRR17   | UBRR16   | UBRR15   | UBRR14   | UBRR13   | UBRR12   | UBRR11  | UBRR10  | <a href="#">page 199</a> |
| (0xCB)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xCA)  | UCSR1C   | —        | UMSEL1   | UPM11    | UPM10    | USBS1    | UCSZ11   | UCSZ10  | UCPOL1  | <a href="#">page 198</a> |
| (0xC9)  | UCSR1B   | RXCIE1   | TXCIE1   | UDRIE1   | RXEN1    | TXEN1    | UCSZ12   | RXB81   | TXB81   | <a href="#">page 197</a> |
| (0xC8)  | UCSR1A   | RXC1     | TXC1     | UDRE1    | FE1      | DOR1     | UPE1     | U2X1    | MPCM1   | <a href="#">page 195</a> |
| (0xC7)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xC6)  | UDR0     | UDR07    | UDR06    | UDR05    | UDR04    | UDR03    | UDR02    | UDR01   | UDR00   | <a href="#">page 195</a> |
| (0xC5)  | UBRR0H   | —        | —        | —        | —        | UBRR011  | UBRR010  | UBRR09  | UBRR08  | <a href="#">page 199</a> |
| (0xC4)  | UBRR0L   | UBRR07   | UBRR06   | UBRR05   | UBRR04   | UBRR03   | UBRR02   | UBRR01  | UBRR00  | <a href="#">page 199</a> |
| (0xC3)  | Reserved |          |          |          |          |          |          |         |         |                          |
| (0xC2)  | UCSR0C   | —        | UMSEL0   | UPM01    | UPM00    | USBS0    | UCSZ01   | UCSZ00  | UCPOL0  | <a href="#">page 197</a> |
| (0xC1)  | UCSR0B   | RXCIE0   | TXCIE0   | UDRIE0   | RXEN0    | TXEN0    | UCSZ02   | RXB80   | TXB80   | <a href="#">page 196</a> |
| (0xC0)  | UCSR0A   | RXC0     | TXC0     | UDRE0    | FE0      | DOR0     | UPE0     | U2X0    | MPCM0   | <a href="#">page 195</a> |
| (0xBF)  | Reserved |          |          |          |          |          |          |         |         |                          |

| Address | Name     | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1  | Bit 0  | Page                     |
|---------|----------|---------|---------|---------|---------|---------|---------|--------|--------|--------------------------|
| (0xBE)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xBD)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xBC)  | TWCR     | TWINT   | TWEA    | TWSTA   | TWSTO   | TWWC    | TWEN    | –      | TWIE   | <a href="#">page 212</a> |
| (0xBB)  | TWDR     | TWDR7   | TWDR6   | TWDR5   | TWDR4   | TWDR3   | TWDR2   | TWDR1  | TWDR0  | <a href="#">page 214</a> |
| (0xBA)  | TWAR     | TWAR6   | TWAR5   | TWAR4   | TWAR3   | TWAR2   | TWAR1   | TWAR0  | TWGCE  | <a href="#">page 214</a> |
| (0xB9)  | TWSR     | TWS7    | TWS6    | TWS5    | TWS4    | TWS3    | –       | TWPS1  | TWPS0  | <a href="#">page 213</a> |
| (0xB8)  | TWBR     | TWBR7   | TWBR6   | TWBR5   | TWBR4   | TWBR3   | TWBR2   | TWBR1  | TWBR0  | <a href="#">page 212</a> |
| (0xB7)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xB6)  | ASSR     | –       | –       | –       | EXCLK   | AS2     | TCN2UB  | OCR2UB | TCR2UB | <a href="#">page 160</a> |
| (0xB5)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xB4)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xB3)  | OCR2A    | OCR2A7  | OCR2A6  | OCR2A5  | OCR2A4  | OCR2A3  | OCR2A2  | OCR2A1 | OCR2A0 | <a href="#">page 159</a> |
| (0xB2)  | TCNT2    | TCNT27  | TCNT26  | TCNT25  | TCNT24  | TCNT23  | TCNT22  | TCNT21 | TCNT20 | <a href="#">page 159</a> |
| (0xB1)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xB0)  | TCCR2A   | FOC2A   | WGM20   | COM2A1  | COM2A0  | WGM21   | CS22    | CS21   | CS20   | <a href="#">page 164</a> |
| (0xAF)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xAE)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xAD)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xAC)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xAB)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xAA)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA9)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA8)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA7)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA6)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA5)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA4)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA3)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA2)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA1)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0xA0)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x9F)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x9E)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x9D)  | OCR3CH   | OCR3C15 | OCR3C14 | OCR3C13 | OCR3C12 | OCR3C11 | OCR3C10 | OCR3C9 | OCR3C8 | <a href="#">page 141</a> |
| (0x9C)  | OCR3CL   | OCR3C7  | OCR3C6  | OCR3C5  | OCR3C4  | OCR3C3  | OCR3C2  | OCR3C1 | OCR3C0 | <a href="#">page 141</a> |
| (0x9B)  | OCR3BH   | OCR3B15 | OCR3B14 | OCR3B13 | OCR3B12 | OCR3B11 | OCR3B10 | OCR3B9 | OCR3B8 | <a href="#">page 141</a> |
| (0x9A)  | OCR3BL   | OCR3B7  | OCR3B6  | OCR3B5  | OCR3B4  | OCR3B3  | OCR3B2  | OCR3B1 | OCR3B0 | <a href="#">page 141</a> |
| (0x99)  | OCR3AH   | OCR3A15 | OCR3A14 | OCR3A13 | OCR3A12 | OCR3A11 | OCR3A10 | OCR3A9 | OCR3A8 | <a href="#">page 141</a> |
| (0x98)  | OCR3AL   | OCR3A7  | OCR3A6  | OCR3A5  | OCR3A4  | OCR3A3  | OCR3A2  | OCR3A1 | OCR3A0 | <a href="#">page 141</a> |
| (0x97)  | ICR3H    | ICR315  | ICR314  | ICR313  | ICR312  | ICR311  | ICR310  | ICR39  | ICR38  | <a href="#">page 142</a> |
| (0x96)  | ICR3L    | ICR37   | ICR36   | ICR35   | ICR34   | ICR33   | ICR32   | ICR31  | ICR30  | <a href="#">page 142</a> |
| (0x95)  | TCNT3H   | TCNT315 | TCNT314 | TCNT313 | TCNT312 | TCNT311 | TCNT310 | TCNT39 | TCNT38 | <a href="#">page 140</a> |
| (0x94)  | TCNT3L   | TCNT37  | TCNT36  | TCNT35  | TCNT34  | TCNT33  | TCNT32  | TCNT31 | TCNT30 | <a href="#">page 140</a> |
| (0x93)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x92)  | TCCR3C   | FOC3A   | FOC3B   | FOC3C   | –       | –       | –       | –      |        | <a href="#">page 140</a> |
| (0x91)  | TCCR3B   | ICNC3   | ICES3   | –       | WGM33   | WGM32   | CS32    | CS31   | CS30   | <a href="#">page 138</a> |
| (0x90)  | TCCR3A   | COM3A1  | COM3A0  | COM3B1  | COM3B0  | COM3C1  | COM3C0  | WGM31  | WGM30  | <a href="#">page 135</a> |
| (0x8F)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x8E)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x8D)  | OCR1CH   | OCR1C15 | OCR1C14 | OCR1C13 | OCR1C12 | OCR1C11 | OCR1C10 | OCR1C9 | OCR1C8 | <a href="#">page 141</a> |
| (0x8C)  | OCR1CL   | OCR1C7  | OCR1C6  | OCR1C5  | OCR1C4  | OCR1C3  | OCR1C2  | OCR1C1 | OCR1C0 | <a href="#">page 141</a> |
| (0x8B)  | OCR1BH   | OCR1B15 | OCR1B14 | OCR1B13 | OCR1B12 | OCR1B11 | OCR1B10 | OCR1B9 | OCR1B8 | <a href="#">page 141</a> |
| (0x8A)  | OCR1BL   | OCR1B7  | OCR1B6  | OCR1B5  | OCR1B4  | OCR1B3  | OCR1B2  | OCR1B1 | OCR1B0 | <a href="#">page 141</a> |
| (0x89)  | OCR1AH   | OCR1A15 | OCR1A14 | OCR1A13 | OCR1A12 | OCR1A11 | OCR1A10 | OCR1A9 | OCR1A8 | <a href="#">page 141</a> |
| (0x88)  | OCR1AL   | OCR1A7  | OCR1A6  | OCR1A5  | OCR1A4  | OCR1A3  | OCR1A2  | OCR1A1 | OCR1A0 | <a href="#">page 141</a> |
| (0x87)  | ICR1H    | ICR115  | ICR114  | ICR113  | ICR112  | ICR111  | ICR110  | ICR19  | ICR18  | <a href="#">page 142</a> |
| (0x86)  | ICR1L    | ICR17   | ICR16   | ICR15   | ICR14   | ICR13   | ICR12   | ICR11  | ICR10  | <a href="#">page 142</a> |
| (0x85)  | TCNT1H   | TCNT115 | TCNT114 | TCNT113 | TCNT112 | TCNT111 | TCNT110 | TCNT19 | TCNT18 | <a href="#">page 140</a> |
| (0x84)  | TCNT1L   | TCNT17  | TCNT16  | TCNT15  | TCNT14  | TCNT13  | TCNT12  | TCNT11 | TCNT10 | <a href="#">page 140</a> |
| (0x83)  | Reserved |         |         |         |         |         |         |        |        |                          |
| (0x82)  | TCCR1C   | FOC1A   | FOC1B   | FOC1C   | –       | –       | –       | –      | –      | <a href="#">page 139</a> |
| (0x81)  | TCCR1B   | ICNC1   | ICES1   | –       | WGM13   | WGM12   | CS12    | CS11   | CS10   | <a href="#">page 138</a> |
| (0x80)  | TCCR1A   | COM1A1  | COM1A0  | COM1B1  | COM1B0  | COM1C1  | COM1C0  | WGM11  | WGM10  | <a href="#">page 135</a> |
| (0x7F)  | DIDR1    | –       | –       | –       | –       | –       | –       | AIN1D  | AIN0D  | <a href="#">page 272</a> |
| (0x7E)  | DIDR0    | ADC7D   | ADC6D   | ADC5D   | ADC4D   | ADC3D   | ADC2D   | ADC1D  | ADC0D  | <a href="#">page 292</a> |
| (0x7D)  | Reserved |         |         |         |         |         |         |        |        |                          |

| Address     | Name                 | Bit 7       | Bit 6       | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1       | Bit 0       | Page                             |
|-------------|----------------------|-------------|-------------|----------|----------|----------|----------|-------------|-------------|----------------------------------|
| (0x7C)      | ADMUX                | REFS1       | REFS0       | ADLAR    | MUX4     | MUX3     | MUX2     | MUX1        | MUX0        | <a href="#">page 287</a>         |
| (0x7B)      | ADCSRB               | –           | ACME        | –        | –        | –        | ADTS2    | ADTS1       | ADTS0       | <a href="#">page 291, 269</a>    |
| (0x7A)      | ADCSRA               | ADEN        | ADSC        | ADATE    | ADIF     | ADIE     | ADPS2    | ADPS1       | ADPS0       | <a href="#">page 289</a>         |
| (0x79)      | ADCH                 | - / ADC9    | - / ADC8    | - / ADC7 | - / ADC6 | - / ADC5 | - / ADC4 | ADC9 / ADC3 | ADC8 / ADC2 | <a href="#">page 290</a>         |
| (0x78)      | ADCL                 | ADC7 / ADC1 | ADC6 / ADC0 | ADC5 / - | ADC4 / - | ADC3 / - | ADC2 / - | ADC1 / -    | ADC0 / -    | <a href="#">page 290</a>         |
| (0x77)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x76)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x75)      | XMCRB                | XMBK        | –           | –        | –        | –        | XMM2     | XMM1        | XMM0        | <a href="#">page 33</a>          |
| (0x74)      | XMCRA                | SRE         | SRL2        | SRL1     | SRL0     | SRW11    | SRW10    | SRW01       | SRW00       | <a href="#">page 32</a>          |
| (0x73)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x72)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x71)      | TIMSK3               | –           | –           | ICIE3    | –        | OCIE3C   | OCIE3B   | OCIE3A      | TOIE3       | <a href="#">page 142</a>         |
| (0x70)      | TIMSK2               | –           | –           | –        | –        | –        | –        | OCIE2A      | TOIE2       | <a href="#">page 162</a>         |
| (0x6F)      | TIMSK1               | –           | –           | ICIE1    | –        | OCIE1C   | OCIE1B   | OCIE1A      | TOIE1       | <a href="#">page 142</a>         |
| (0x6E)      | TIMSK0               | –           | –           | –        | –        | –        | –        | OCIE0A      | TOIE0       | <a href="#">page 112</a>         |
| (0x6D)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x6C)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x6B)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x6A)      | EICRB                | ISC71       | ISC70       | ISC61    | ISC60    | ISC51    | ISC50    | ISC41       | ISC40       | <a href="#">page 94</a>          |
| (0x69)      | EICRA                | ISC31       | ISC30       | ISC21    | ISC20    | ISC11    | ISC10    | ISC01       | ISC00       | <a href="#">page 93</a>          |
| (0x68)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x67)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x66)      | OSCCAL               | –           | CAL6        | CAL5     | CAL4     | CAL3     | CAL2     | CAL1        | CAL0        | <a href="#">page 42</a>          |
| (0x65)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x64)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x63)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x62)      | Reserved             |             |             |          |          |          |          |             |             |                                  |
| (0x61)      | CLKPR                | CLKPCE      | –           | –        | –        | CLKPS3   | CLKPS2   | CLKPS1      | CLKPS0      | <a href="#">page 44</a>          |
| (0x60)      | WDTCSR               | –           | –           | –        | WDCE     | WDE      | WDP2     | WDP1        | WDP0        | <a href="#">page 58</a>          |
| 0x3F (0x5F) | SREG                 | I           | T           | H        | S        | V        | N        | Z           | C           | <a href="#">page 11</a>          |
| 0x3E (0x5E) | SPH                  | SP15        | SP14        | SP13     | SP12     | SP11     | SP10     | SP9         | SP8         | <a href="#">page 14</a>          |
| 0x3D (0x5D) | SPL                  | SP7         | SP6         | SP5      | SP4      | SP3      | SP2      | SP1         | SP0         | <a href="#">page 14</a>          |
| 0x3C (0x5C) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x3B (0x5B) | RAMPZ <sup>(1)</sup> | –           | –           | –        | –        | –        | –        | –           | RAMPZ0      | <a href="#">page 13</a>          |
| 0x3A (0x5A) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x39 (0x59) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x38 (0x58) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x37 (0x57) | SPMCSR               | SPMIE       | RWWWSB      | –        | RWWWSRE  | BLBSET   | PGWRT    | PGERS       | SPMEN       | <a href="#">page 326</a>         |
| 0x36 (0x56) | Reserved             | –           | –           | –        | –        | –        | –        | –           | –           |                                  |
| 0x35 (0x55) | MCUCR                | JTD         | –           | –        | PUD      | –        | –        | IVSEL       | IVCE        | <a href="#">page 64, 73, 304</a> |
| 0x34 (0x54) | MCUSR                | –           | –           | –        | JTRF     | WDRF     | BORF     | EXTRF       | PORF        | <a href="#">page 56, 304</a>     |
| 0x33 (0x53) | SMCR                 | –           | –           | –        | –        | SM2      | SM1      | SM0         | SE          | <a href="#">page 46</a>          |
| 0x32 (0x52) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x31 (0x51) | OCDR                 | IDRD/OCDR7  | OCDR6       | OCDR5    | OCDR4    | OCDR3    | OCDR2    | OCDR1       | OCDR0       | <a href="#">page 299</a>         |
| 0x30 (0x50) | ACSR                 | ACD         | ACBG        | ACO      | ACI      | ACIE     | ACIC     | ACIS1       | ACIS0       | <a href="#">page 270</a>         |
| 0x2F (0x4F) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x2E (0x4E) | SPDR                 | SPD7        | SPD6        | SPD5     | SPD4     | SPD3     | SPD2     | SPD1        | SPD0        | <a href="#">page 175</a>         |
| 0x2D (0x4D) | SPSR                 | SPIF        | WCOL        | –        | –        | –        | –        | –           | SPI2X       | <a href="#">page 175</a>         |
| 0x2C (0x4C) | SPCR                 | SPIE        | SPE         | DORD     | MSTR     | CPOL     | CPHA     | SPR1        | SPR0        | <a href="#">page 173</a>         |
| 0x2B (0x4B) | GPOR2                | GPOR27      | GPOR26      | GPOR25   | GPOR24   | GPOR23   | GPOR22   | GPOR21      | GPOR20      | <a href="#">page 36</a>          |
| 0x2A (0x4A) | GPOR1                | GPOR17      | GPOR16      | GPOR15   | GPOR14   | GPOR13   | GPOR12   | GPOR11      | GPOR10      | <a href="#">page 36</a>          |
| 0x29 (0x49) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x28 (0x48) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x27 (0x47) | OCR0A                | OCR0A7      | OCR0A6      | OCR0A5   | OCR0A4   | OCR0A3   | OCR0A2   | OCR0A1      | OCR0A0      | <a href="#">page 112</a>         |
| 0x26 (0x46) | TCNT0                | TCNT07      | TCNT06      | TCNT05   | TCNT04   | TCNT03   | TCNT02   | TCNT01      | TCNT00      | <a href="#">page 111</a>         |
| 0x25 (0x45) | Reserved             |             |             |          |          |          |          |             |             |                                  |
| 0x24 (0x44) | TCCR0A               | FOC0A       | WGM00       | COM0A1   | COM0A0   | WGM01    | CS02     | CS01        | CS00        | <a href="#">page 109</a>         |
| 0x23 (0x43) | GTCCR                | TSM         | –           | –        | –        | –        | –        | PSR2        | PSR310      | <a href="#">page 98, 164</a>     |
| 0x22 (0x42) | EEARH <sup>(2)</sup> | –           | –           | –        | –        | EEAR11   | EEAR10   | EEAR9       | EEAR8       | <a href="#">page 22</a>          |
| 0x21 (0x41) | EEARL                | EEAR7       | EEAR6       | EEAR5    | EEAR4    | EEAR3    | EEAR2    | EEAR1       | EEAR0       | <a href="#">page 22</a>          |
| 0x20 (0x40) | EEDR                 | EEDR7       | EEDR6       | EEDR5    | EEDR4    | EEDR3    | EEDR2    | EEDR1       | EEDR0       | <a href="#">page 23</a>          |
| 0x1F (0x3F) | EECR                 | –           | –           | –        | –        | EERIE    | EEMWE    | EEWE        | EERE        | <a href="#">page 23</a>          |
| 0x1E (0x3E) | GPOR0                | GPOR07      | GPOR06      | GPOR05   | GPOR04   | GPOR03   | GPOR02   | GPOR01      | GPOR00      | <a href="#">page 36</a>          |
| 0x1D (0x3D) | EIMSK                | INT7        | INT6        | INT5     | INT4     | INT3     | INT2     | INT1        | INT0        | <a href="#">page 95</a>          |
| 0x1C (0x3C) | EIFR                 | INTF7       | INTF6       | INTF5    | INTF4    | INTF3    | INTF2    | INTF1       | INTF0       | <a href="#">page 95</a>          |
| 0x1B (0x3B) | Reserved             |             |             |          |          |          |          |             |             |                                  |

| Address     | Name     | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Page                     |
|-------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------------------------|
| 0x1A (0x3A) | Reserved |        |        |        |        |        |        |        |        |                          |
| 0x19 (0x39) | Reserved |        |        |        |        |        |        |        |        |                          |
| 0x18 (0x38) | TIFR3    | –      | –      | ICF3   | –      | OCF3C  | OCF3B  | OCF3A  | TOV3   | <a href="#">page 143</a> |
| 0x17 (0x37) | TIFR2    | –      | –      | –      | –      | –      | –      | OCF2A  | TOV2   | <a href="#">page 162</a> |
| 0x16 (0x36) | TIFR1    | –      | –      | ICF1   | –      | OCF1C  | OCF1B  | OCF1A  | TOV1   | <a href="#">page 143</a> |
| 0x15 (0x35) | TIFR0    | –      | –      | –      | –      | –      | –      | OCF0A  | TOV0   | <a href="#">page 112</a> |
| 0x14 (0x34) | PORTG    | –      | –      | –      | PORTG4 | PORTG3 | PORTG2 | PORTG1 | PORTG0 | <a href="#">page 92</a>  |
| 0x13 (0x33) | DDRG     | –      | –      | –      | DDG4   | DDG3   | DDG2   | DDG1   | DDG0   | <a href="#">page 92</a>  |
| 0x12 (0x32) | PING     | –      | –      | –      | PING4  | PING3  | PING2  | PING1  | PING0  | <a href="#">page 92</a>  |
| 0x11 (0x31) | PORTF    | PORTF7 | PORTF6 | PORTF5 | PORTF4 | PORTF3 | PORTF2 | PORTF1 | PORTF0 | <a href="#">page 91</a>  |
| 0x10 (0x30) | DDRF     | DDF7   | DDF6   | DDF5   | DDF4   | DDF3   | DDF2   | DDF1   | DDF0   | <a href="#">page 91</a>  |
| 0x0F (0x2F) | PINF     | PINF7  | PINF6  | PINF5  | PINF4  | PINF3  | PINF2  | PINF1  | PINF0  | <a href="#">page 92</a>  |
| 0x0E (0x2E) | PORTE    | PORTE7 | PORTE6 | PORTE5 | PORTE4 | PORTE3 | PORTE2 | PORTE1 | PORTE0 | <a href="#">page 91</a>  |
| 0x0D (0x2D) | DDRE     | DDE7   | DDE6   | DDE5   | DDE4   | DDE3   | DDE2   | DDE1   | DDE0   | <a href="#">page 91</a>  |
| 0x0C (0x2C) | PINE     | PINE7  | PINE6  | PINE5  | PINE4  | PINE3  | PINE2  | PINE1  | PINE0  | <a href="#">page 91</a>  |
| 0x0B (0x2B) | PORTD    | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | <a href="#">page 91</a>  |
| 0x0A (0x2A) | DDRD     | DDD7   | DDD6   | DDD5   | DDD4   | DDD3   | DDD2   | DDD1   | DDD0   | <a href="#">page 91</a>  |
| 0x09 (0x29) | PIND     | PIND7  | PIND6  | PIND5  | PIND4  | PIND3  | PIND2  | PIND1  | PIND0  | <a href="#">page 91</a>  |
| 0x08 (0x28) | PORTC    | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | <a href="#">page 90</a>  |
| 0x07 (0x27) | DDRC     | DDC7   | DDC6   | DDC5   | DDC4   | DDC3   | DDC2   | DDC1   | DDC0   | <a href="#">page 90</a>  |
| 0x06 (0x26) | PINC     | PINC7  | PINC6  | PINC5  | PINC4  | PINC3  | PINC2  | PINC1  | PINC0  | <a href="#">page 90</a>  |
| 0x05 (0x25) | PORTB    | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | <a href="#">page 90</a>  |
| 0x04 (0x24) | DDRB     | DDB7   | DDB6   | DDB5   | DDB4   | DDB3   | DDB2   | DDB1   | DDB0   | <a href="#">page 90</a>  |
| 0x03 (0x23) | PINB     | PINB7  | PINB6  | PINB5  | PINB4  | PINB3  | PINB2  | PINB1  | PINB0  | <a href="#">page 90</a>  |
| 0x02 (0x22) | PORTA    | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | <a href="#">page 89</a>  |
| 0x01 (0x21) | DDRA     | DDA7   | DDA6   | DDA5   | DDA4   | DDA3   | DDA2   | DDA1   | DDA0   | <a href="#">page 90</a>  |
| 0x00 (0x20) | PINA     | PINA7  | PINA6  | PINA5  | PINA4  | PINA3  | PINA2  | PINA1  | PINA0  | <a href="#">page 90</a>  |

- Notes:
1. Address bits exceeding PCMSB ([Table 25-11 on page 341](#)) are don't care.
  2. Address bits exceeding EEAMSB ([Table 25-12 on page 341](#)) are don't care.
  3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  4. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  5. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  6. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The AT90CAN32/64/128 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 4. Ordering Information

| Ordering Code <sup>(1)</sup> | Speed (MHz) | Power Supply (V) | Package | Operation Range                     | Product Marking |
|------------------------------|-------------|------------------|---------|-------------------------------------|-----------------|
| AT90CAN32-16AI               | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)          | AT90CAN32-16AI  |
| AT90CAN32-16MI               | 16          | 2.7 - 5.5        | Z64-1   | Industrial (-40° to +85°C)          | AT90CAN32-16MI  |
| AT90CAN32-16AU               | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)<br>Green | AT90CAN32-16AU  |
| AT90CAN32-16MU               | 16          | 2.7 - 5.5        | Z64-1   | Industrial (-40° to +85°C)<br>Green | AT90CAN32-16MU  |
| AT90CAN64-16AI               | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)          | AT90CAN64-16AI  |
| AT90CAN64-16MI               | 16          | 2.7 - 5.5        | Z64-2   | Industrial (-40° to +85°C)          | AT90CAN64-16MI  |
| AT90CAN64-16AU               | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)<br>Green | AT90CAN64-16AU  |
| AT90CAN64-16MU               | 16          | 2.7 - 5.5        | Z64-2   | Industrial (-40° to +85°C)<br>Green | AT90CAN64-16MU  |
| AT90CAN128-16AI              | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)          | AT90CAN128-16AI |
| AT90CAN128-16MI              | 16          | 2.7 - 5.5        | Z64-2   | Industrial (-40° to +85°C)          | AT90CAN128-16MI |
| AT90CAN128-16AU              | 16          | 2.7 - 5.5        | A2 64   | Industrial (-40° to +85°C)<br>Green | AT90CAN128-16AU |
| AT90CAN128-16MU              | 16          | 2.7 - 5.5        | Z64-2   | Industrial (-40° to +85°C)<br>Green | AT90CAN128-16MU |

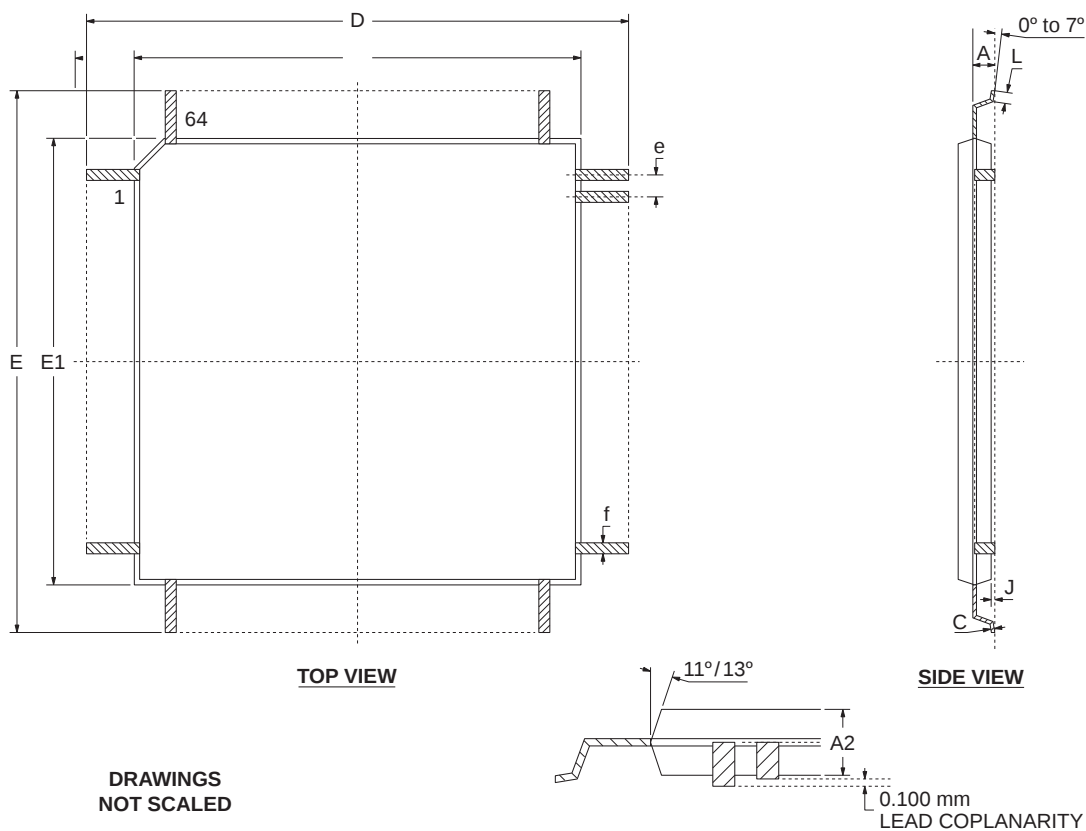
Notes: 1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

## 5. Packaging Information

| Package Type |                                                                             |
|--------------|-----------------------------------------------------------------------------|
| <b>A2 64</b> | 64-Lead, Thin (1.0 mm / 0.03937 in) Plastic Gull Wing Quad Flat Package.    |
| <b>Z64-1</b> | 64-Lead, QFN, Exposed Die Attach Pad D2/E2: 5.4 ± 0.1mm / 0.212 ± 0.004 in. |
| <b>Z64-2</b> | 64-Lead, QFN, Exposed Die Attach Pad D2/E2: 6.0 ± 0.1mm / 0.236 ± 0.004 in. |

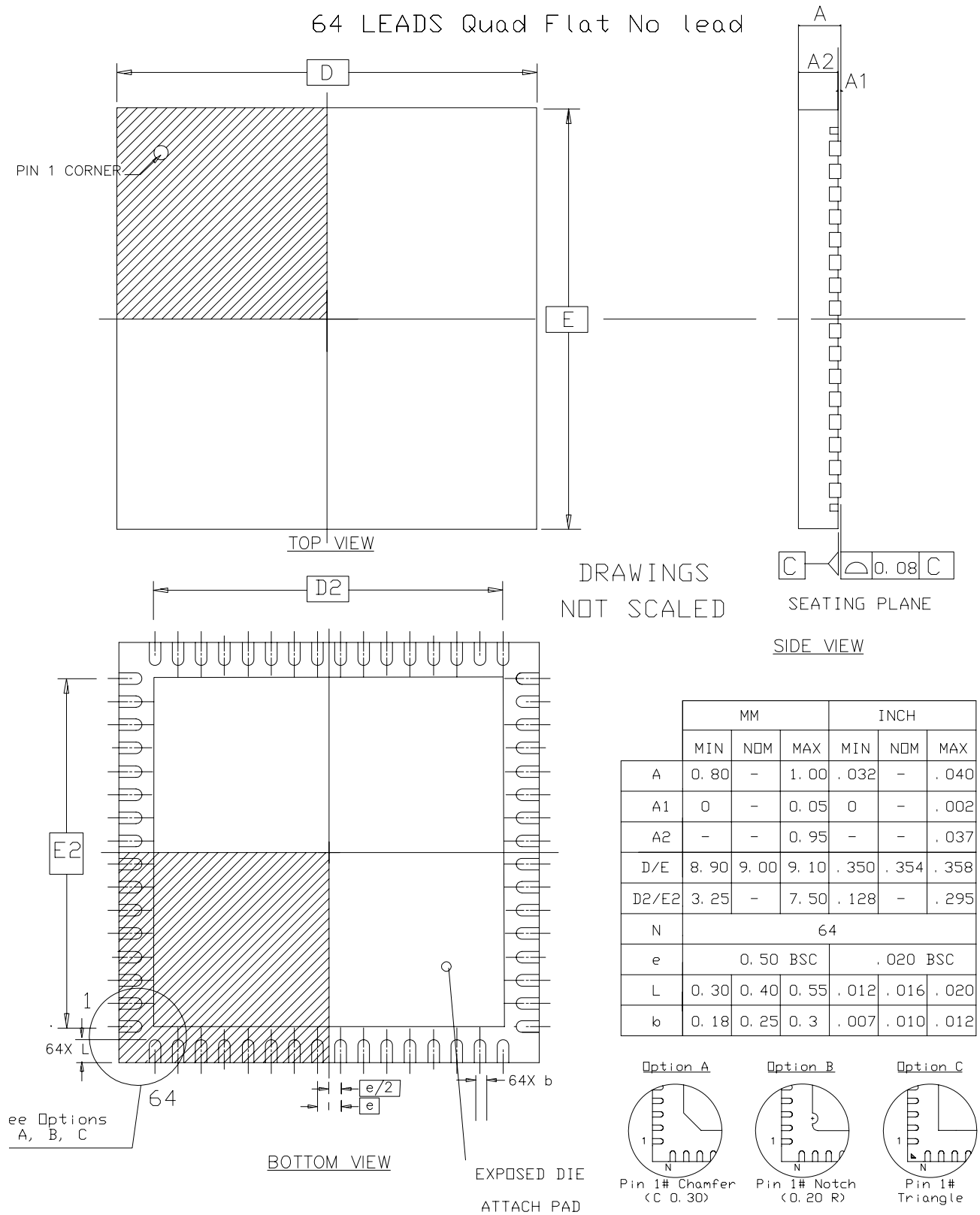
## 5.1 TQFP64

### 64 PINS THIN QUAD FLAT PACK



|    | MM        |      | INCH       |       |
|----|-----------|------|------------|-------|
|    | Min       | Max  | Min        | Max   |
| A  | ----      | 1.20 | ----       | 0.047 |
| A2 | 0.95      | 1.05 | 0.037      | 0.041 |
| C  | 0.09      | 0.20 | 0.004      | 0.008 |
| D  | 16.00 BSC |      | 0.630 BSC  |       |
| D1 | 14.00 BSC |      | 0.551 BSC  |       |
| E  | 16.00 BSC |      | 0.630 BSC  |       |
| E1 | 14.00 BSC |      | 0.551 BSC  |       |
| J  | 0.05      | 0.15 | 0.002      | 0.006 |
| L  | 0.45      | 0.75 | 0.018      | 0.030 |
| e  | 0.80 BSC  |      | 0.0315 BSC |       |
| f  | 0.30      | 0.45 | 0.012      | 0.018 |

## 5.2 QFN64



Compliant JEDEC Standard MO-220 variation VMMD-3

NOTES: QFN STANDARD NOTES

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. DIMENSION *b* APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION *b* SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. MAX. PACKAGE WARPAGE IS 0.05mm.
4. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
5. PIN #1 ID ON TOP WILL BE LASER MARKED.
6. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220.
7. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.  
L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.30 mm
8. THE TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATEI  
THE TERMINAL #1 IDENTIFIER BE EITHER A MOLD OR MARKED FEATURE



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