32K x 16 Static RAM

Features

- **5.0V operation (± 10%)**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— 825 mW (max., 10 ns, "L" version)**
- **Very Low standby power**
  - **— 550 μW (max., "L" version)**
- **Automatic power-down when deselected**
- **Independent Control of Upper and Lower bytes**
- **Available in 44-pin TSOP II and 400-mil SOJ**

Functional Description

The CY7C1020 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_1$ through I/O$_8$), is written into the location specified on the address pins (A$_0$ through A$_{14}$). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_9$ through I/O$_{16}$) is written into the location specified on the address pins (A$_0$ through A$_{14}$).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_1$ to I/O$_8$. If byte high enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_9$ to I/O$_{16}$. See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O$_1$ through I/O$_{16}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1020 is available in standard 44-pin TSOP type II and 400-mil-wide SOJ packages.

Logic Block Diagram

Pin Configuration

SOJ / TSOP II
Top View
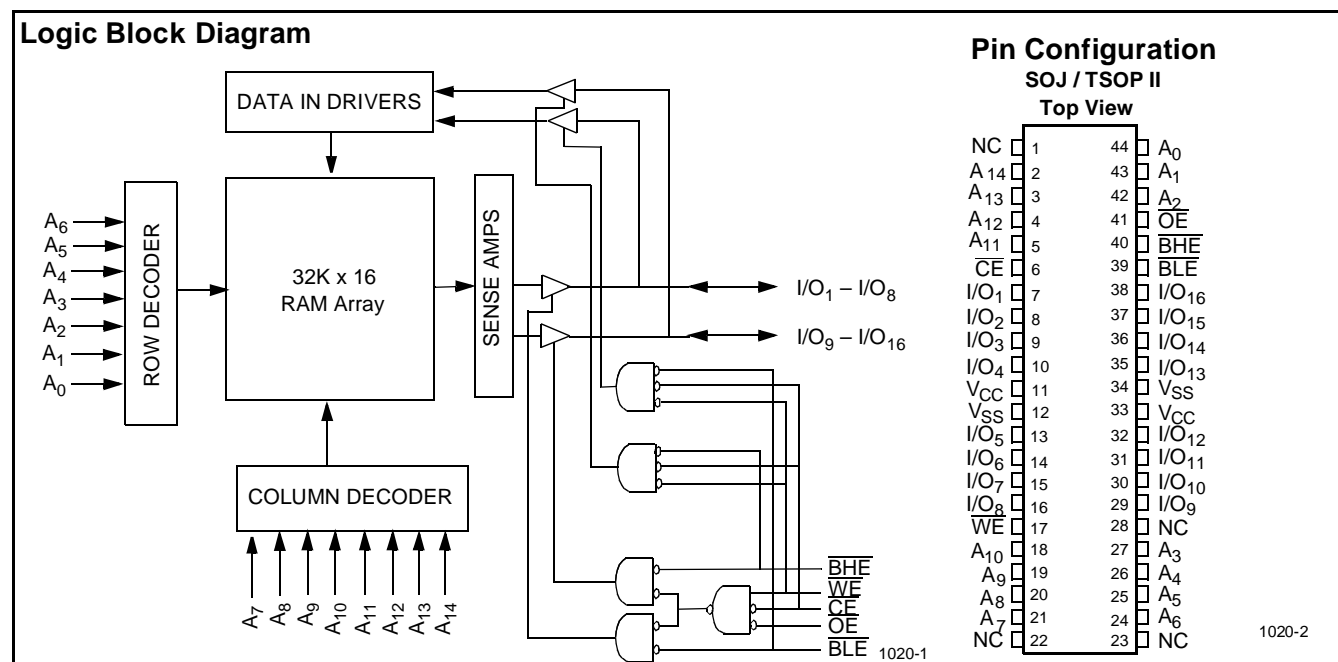
Selection Guide

		7C1020-10	7C1020-12	7C1020-15	7C1020-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)		180	170	160	160
	L	150	140	130	130
Maximum CMOS Standby Current (mA)		3	3	3	3
	L	0.1	0.1	0.1	0.1

Shaded area contains advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with
Power Applied .... $-55°C$ to $+125°C$

Supply Voltage on V_{CC} to Relative GND[1] .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs
in High Z State[1] .... $-0.5V$ to V_{CC} $+0.5V$

DC Input Voltage[1] .... $-0.5V$ to V_{CC} $+0.5V$

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	$0°C$ to $+70°C$	4.5V–5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1020-10		7C1020-12		7C1020-15		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage[1]			-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-1	$+1$	-1	$+1$	-1	$+1$	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		-2	$+2$	-2	$+2$	-2	$+2$	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			180		170		160	mA
			L		150		140		130	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}			20		20		20	mA
			L		10		10		10	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f=0			3		3		3	mA
			L		100		100		100	μA

Shaded area contains advance information.

Notes:
1. V_{IL} (min.) = $-2.0V$ for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C1020-20 Min.	7C1020-20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−1	+1	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−2	+2	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$			160	mA
			L		130	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$			20	mA
			L		10	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq 0.3V$, $f=0$			3	mA
			L		100	μA

Shaded area contains advance information.

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
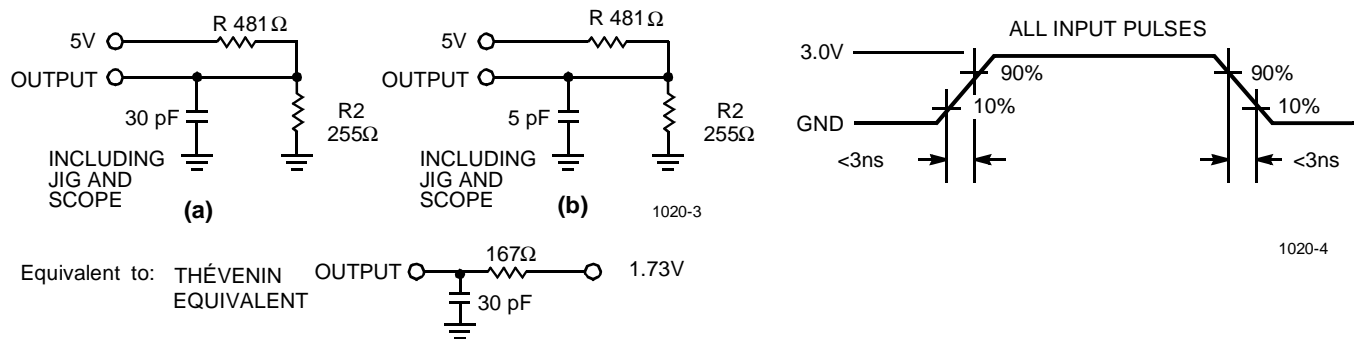
Switching Characteristics[4] Over the Operating Range

Parameter	Description	7C1020-10 Min.	7C1020-10 Max.	7C1020-12 Min.	7C1020-12 Max.	7C1020-15 Min.	7C1020-15 Max.	7C1020-20 Min.	7C1020-20 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		5		6		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		5		6		7		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		12		15		20	ns
t_{DBE}	Byte enable to Data Valid		5		6		7		9	ns
t_{LZBE}	Byte enable to Low Z	0		0		0		0		ns
t_{HZBE}	Byte disable to High Z		5		6		7		9	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	10		12		15		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		12		ns
t_{AW}	Address Set-Up to Write End	7		8		10		12		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		12		ns
t_{SD}	Data Set-Up to Write End	5		6		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		5		6		7		9	ns
t_{BW}	Byte enable to end of write	7		8		9		12		ns

Notes:
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
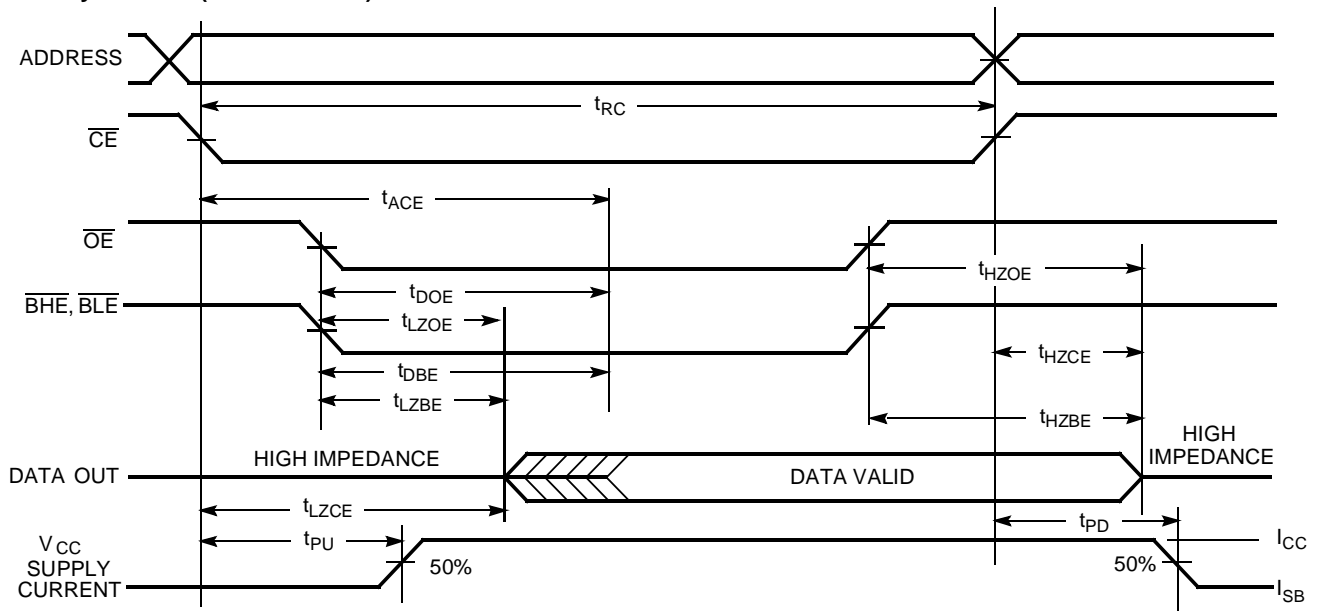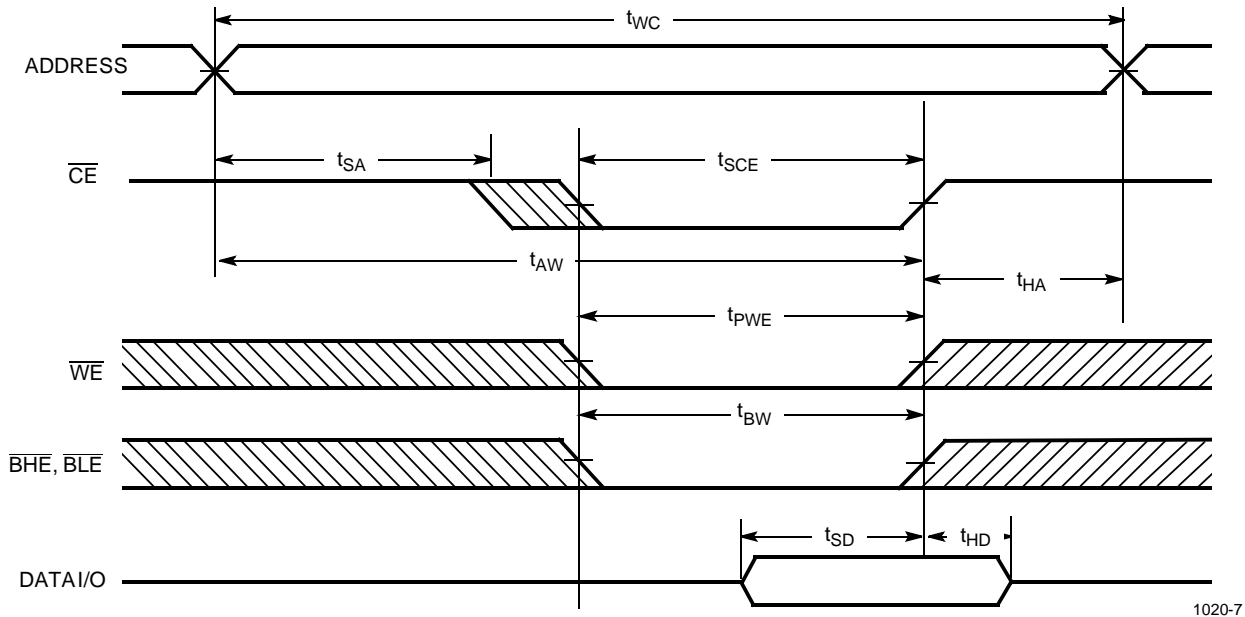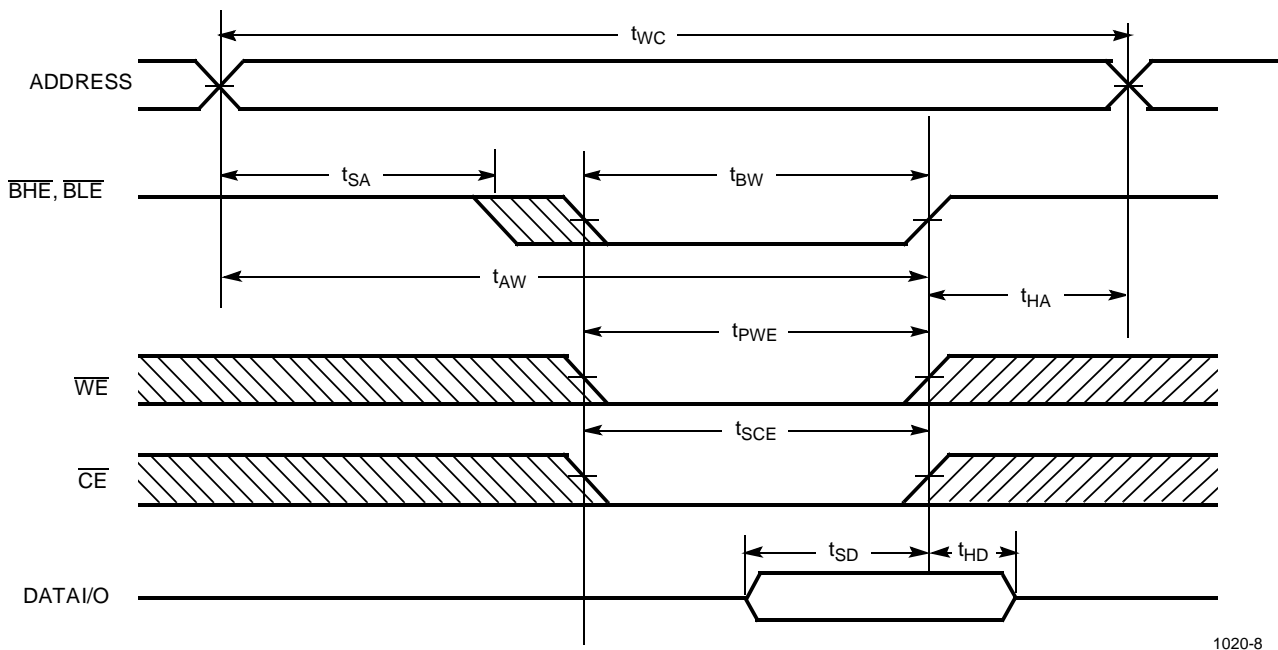
Switching Waveforms

Read Cycle No.1 [8, 9]
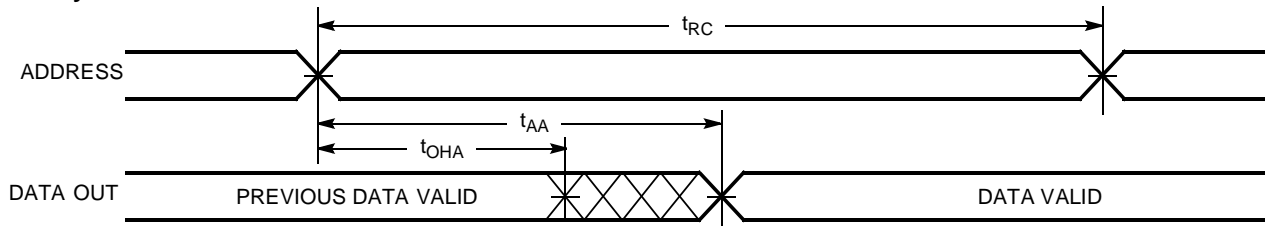
1020-5

Read Cycle No.2 ($\overline{OE}$ Controlled) [9, 10]


1020-6

Notes:
8. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}
9. $\overline{WE}$ is HIGH for read cycle.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled) [11, 12]

1020-7

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

1020-8

Notes:
11. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

8

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)

1020-10
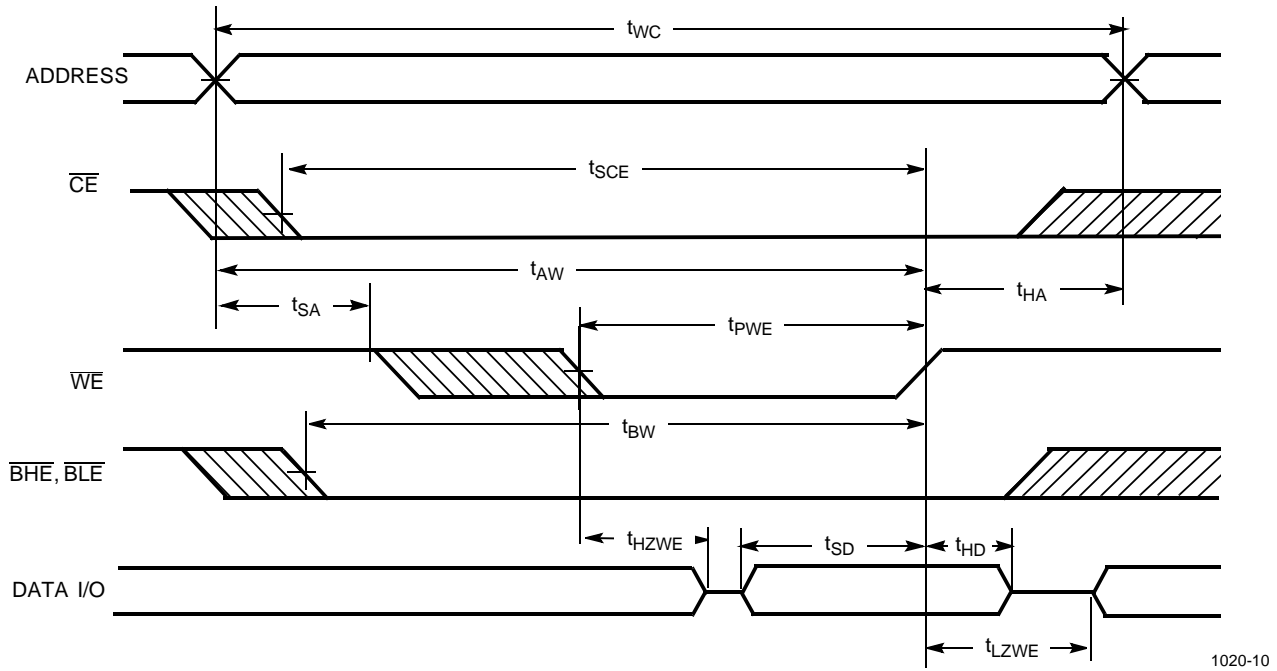
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_1–I/O_8$	$I/O_9–I/O_{16}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1020-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1020-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1020-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-15ZC	Z44	44-Lead TSOP Type II	Commercial
20	CY7C1020-20VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-20VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-20ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-20ZC	Z44	44-Lead TSOP Type II	Commercial

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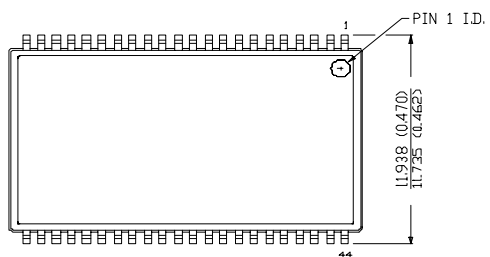
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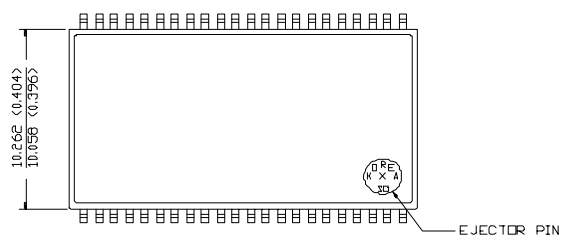
Package Diagrams

44-Lead (400-Mil) Molded SOJ V34
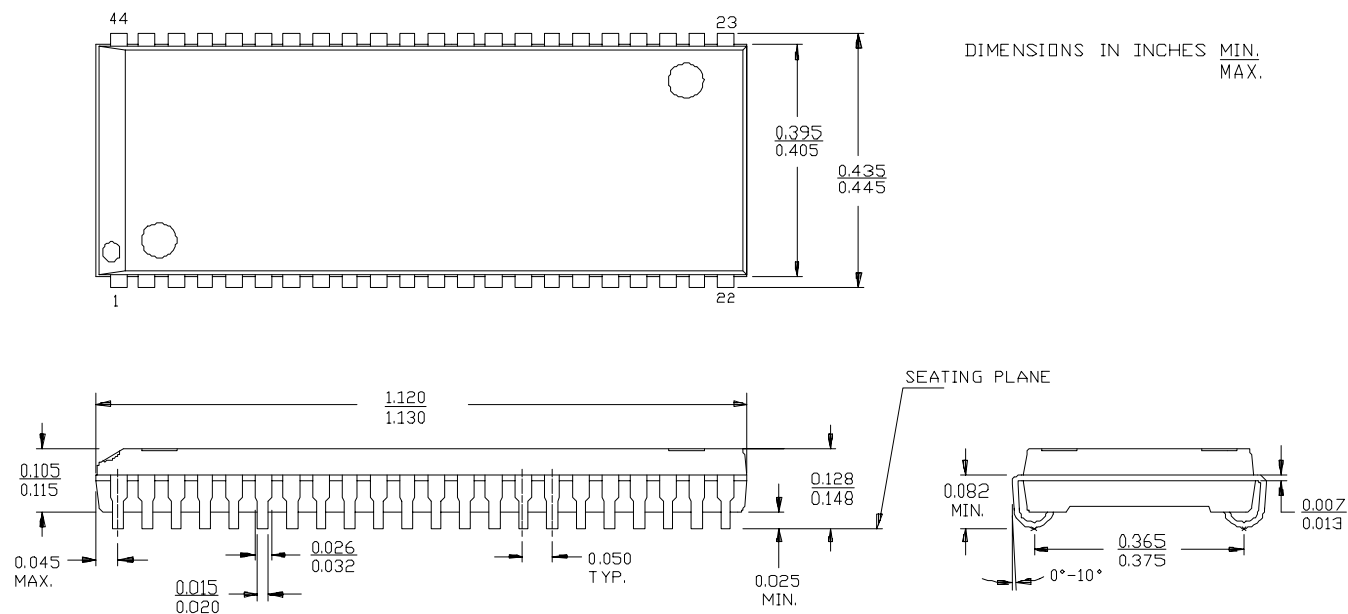
Package Diagrams (continued)

44-Pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX
MIN.
LEAD COPLANARITY 0.004 INCHES.

PIN 1 I.D.

11.938 (0.470)
11.735 (0.462)

TOP VIEW

10.262 (0.404)
10.058 (0.396)

EJECTOR PIN

BOTTOM VIEW

0.800 BSC
(0.0315)

0.400(0.016)
0.300 (0.012)

BASE PLANE

SEATING
PLANE

18.517 (0.729)
18.313 (0.721)

1.194 (0.047)
0.991 (0.039)

0.150 (0.0059)
0.050 (0.0020)

10.262 (0.404)
10.058 (0.396)

0°–5°

0.210 (0.0083)
0.120 (0.0047)

0.597 (0.0235)
0.406 (0.0160)