

M5240P**DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS****DESCRIPTION**

The M5240P is a semiconductor integrated circuit designed as a low-noise Bi-FET operational amplifier which adopts J-FETs in the input stage. The device comes in a 16-pin DIP and contains two circuits for yielding high sound quality, high input impedance, high slew rate and low distortion characteristics. It can be widely used as an operational amplifier in stereo equipment, tape decks, and as preamplifier for digital audio disc players and other similar products, mixer for public announcement or LM, high fidelity VCRs.

FEATURES

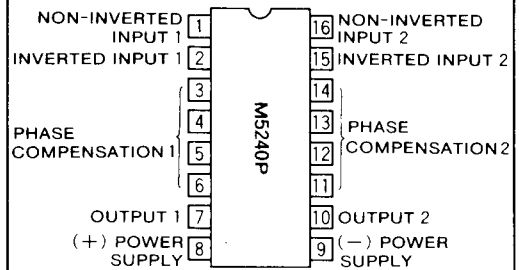
- Low noise $S/N=82\text{dB}(\text{typ.})$
(shorted input, RIAA, IHF-A, PHONO 2.5mVrms)
- High slew rate $SR=40\text{V}/\mu\text{s}(\text{typ.})$
(Variable by externally connected RC due to external phase compensation type)
- High input impedance $R_i=1000\text{M}\Omega(\text{typ.})$
- Low distortion rate $\text{THD}=0.001\%(\text{typ.})$
($f=1\text{kHz}$, RIAA, $V_o=5\text{Vrms}$)
- Large load current and allowable current
..... $I_{LP}=\pm 50\text{mA}$
..... $P_d=1\text{W}$

APPLICATION

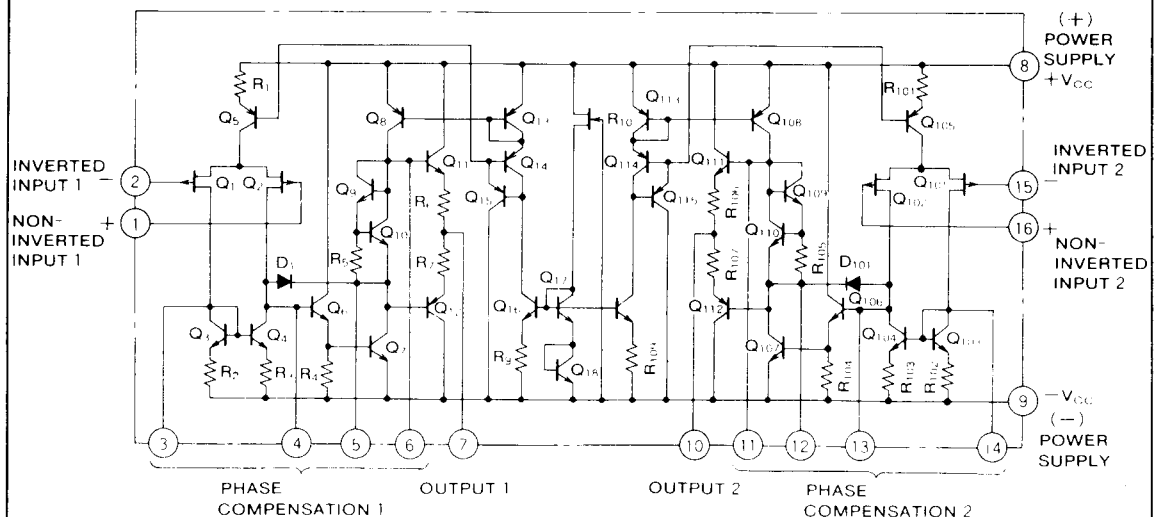
Amplifier in stereo equipment, tape decks and digital audio disc players, mixer.

RECOMMENDED OPERATING CONDITIONS

- Supply voltage range $\pm 5 \sim \pm 15\text{V}$
Rated supply voltage $\pm 15\text{V}$

PIN CONFIGURATION (TOP VIEW)

Outline 16P4

EQUIVALENT CIRCUIT

DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

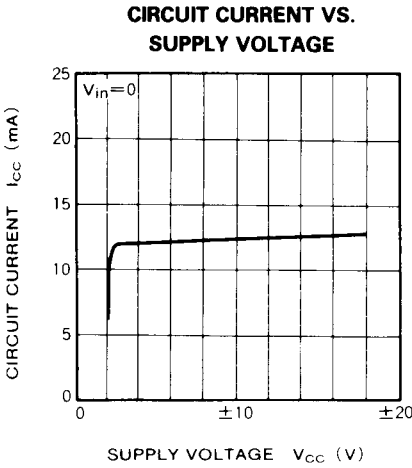
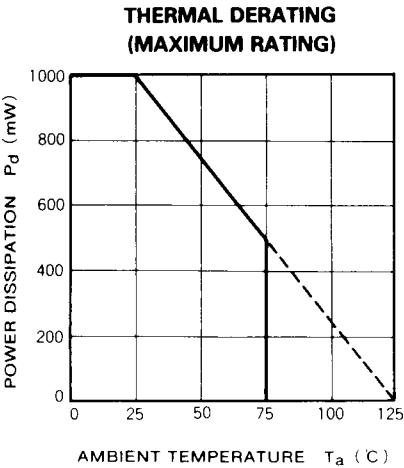
ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		± 18	V
I_{LP}	Load current		± 50	mA
V_{id}	Differential input voltage		± 30	V
V_{ic}	Common input voltage		± 15	V
P_d	Power dissipation		1000	mW
$K\theta$	Thermal derating	$T_a \geq 25^{\circ}\text{C}$	10	mW/ $^{\circ}\text{C}$
T_{opr}	Ambient temperature		$-20 \sim +75$	$^{\circ}\text{C}$
T_{stg}	Storage temperature		$-55 \sim +125$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a=25^{\circ}\text{C}$, $V_{CC}=\pm 15\text{V}$)

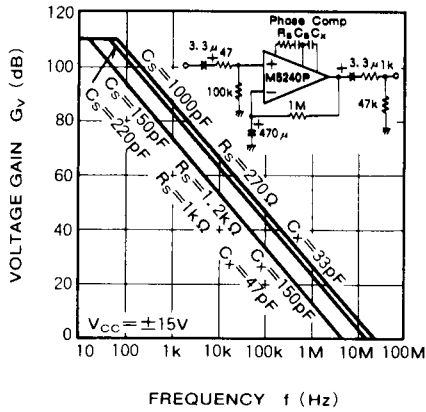
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	$V_{in}=0$		12.0	17.0	mA
V_{IO}	Input offset voltage	$R_s \leq 10\text{k}\Omega$		5.0	15.0	mV
I_{IO}	Input offset current			25	1000	pA
I_{IB}	Input bias current			120	2000	pA
R_{in}	Input resistance			10^3		M Ω
G_{VO}	Open loop voltage gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$		110		dB
V_{OM}	Maximum output voltage	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$	± 12 ± 10	± 14 ± 13		V
V_{CM}	Common input voltage width		± 10	± 12		V
CMRR	Common mode rejection ratio	$R_s \leq 10\text{k}\Omega$	70	76		dB
SVRR	Supply voltage rejection ratio	$R_s \leq 10\text{k}\Omega$		30	150	$\mu\text{V/V}$
P_d	Power dissipation			360	510	mW
SR	Slew rate	$G_v = 16.5\text{dB}$		40		V/ μs
f_T	Gain bandwidth product			18		MHz
e_n	Equivalent input referred noise voltage	$R_s = 100\Omega$, BW = 10Hz $\sim$ 30kHz		3.3		nV/ $\sqrt{\text{Hz}}$
V_{NI}		$R_g = 2.2\text{k}\Omega$, RIAA EQ		1.2	2.5	μVrms
S/N	Signal-to-noise voltage ratio	$R_g = 47\Omega$, RIAA EQ, IHF-A		82		dB

TYPICAL CHARACTERISTICS

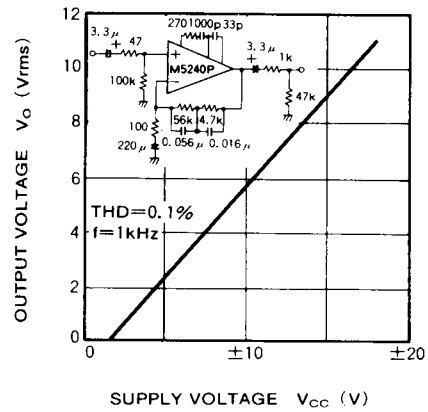


DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

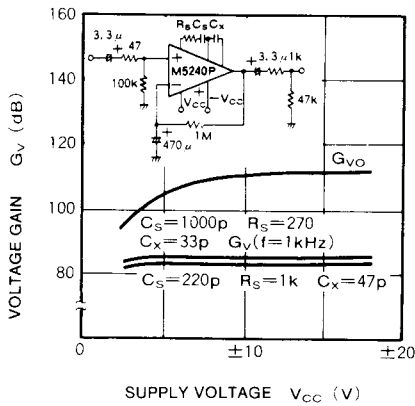
**VOLTAGE GAIN VS.
FREQUENCY RESPONSE**



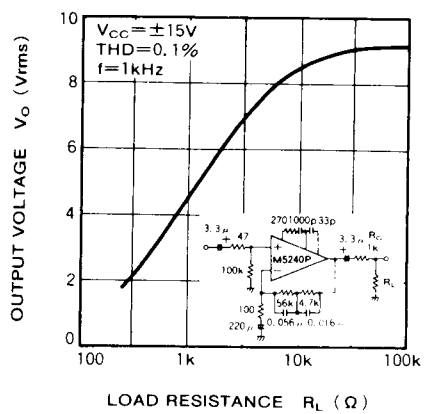
**OUTPUT VOLTAGE VS.
SUPPLY VOLTAGE**



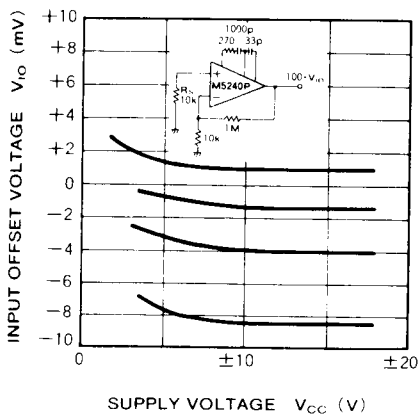
**VOLTAGE GAIN VS.
SUPPLY VOLTAGE**



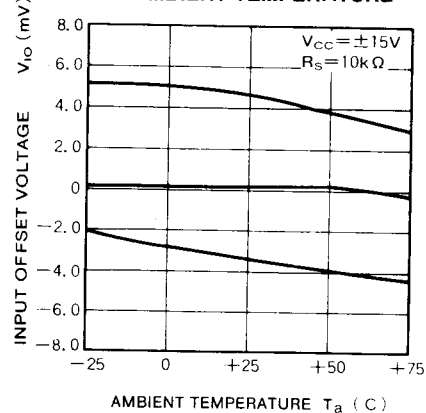
**OUTPUT VOLTAGE VS.
LOAD RESISTANCE**



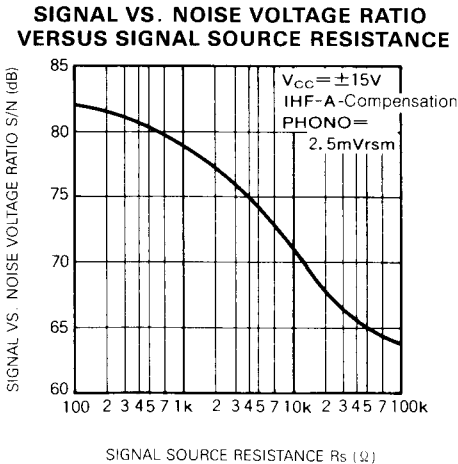
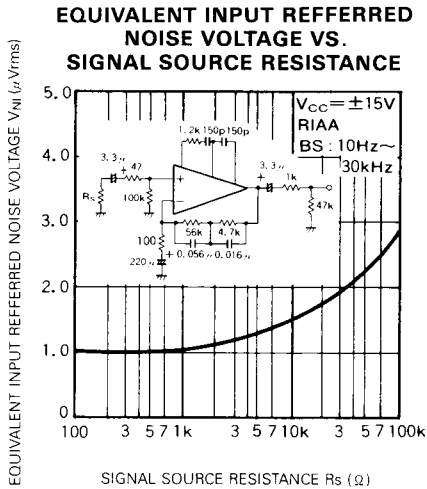
**INPUT OFFSET VOLTAGE
VS. SUPPLY VOLTAGE**



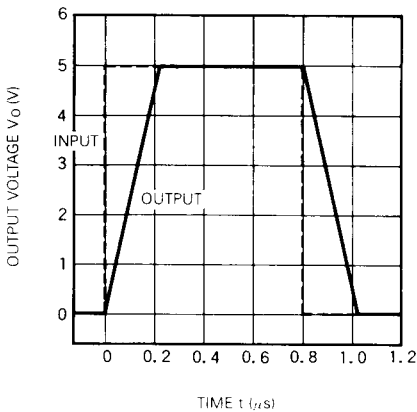
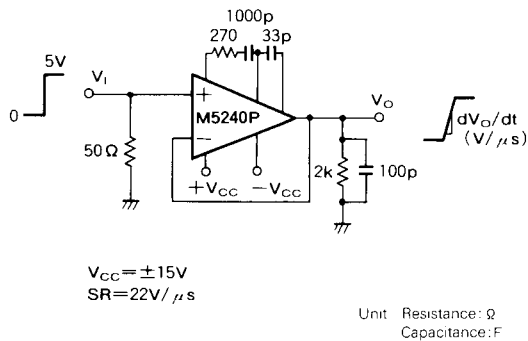
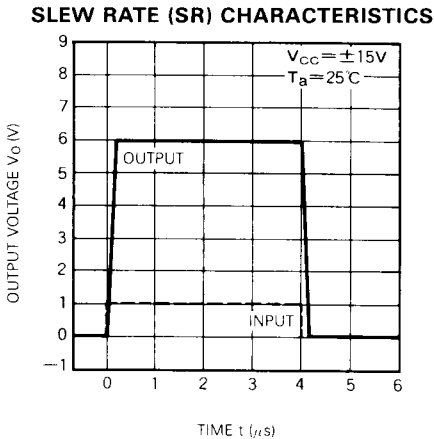
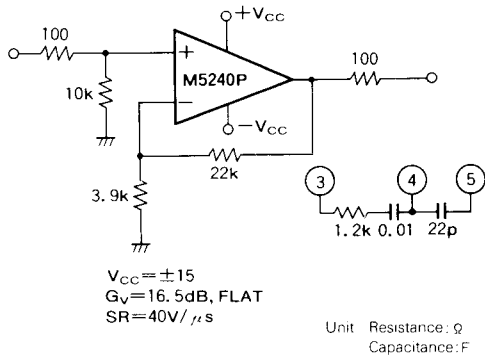
**INPUT OFFSET VOLTAGE VS.
AMBIENT TEMPERATURE**



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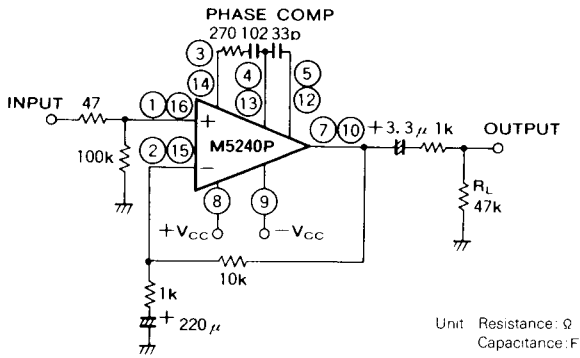


**TYPICAL APPLICATION EXAMPLE
HIGH SLEW RATE FLAT AMP**

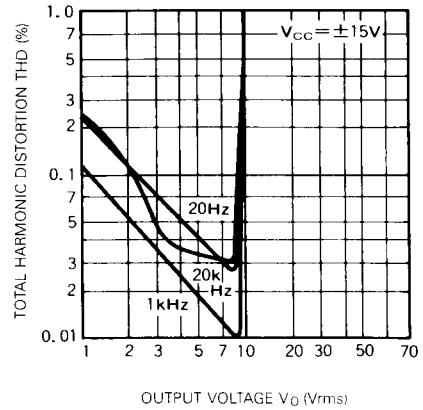


DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

G_v = 20dB FLAT AMP



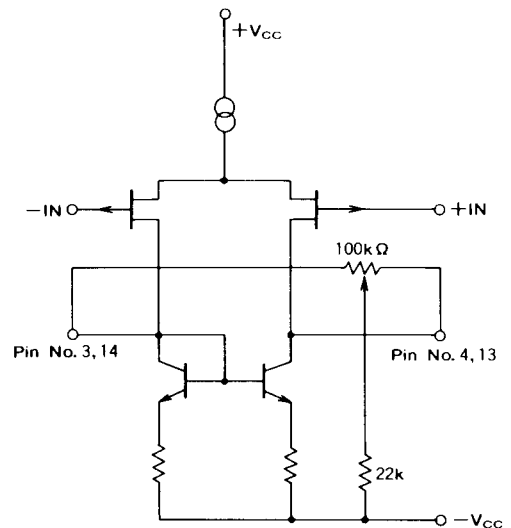
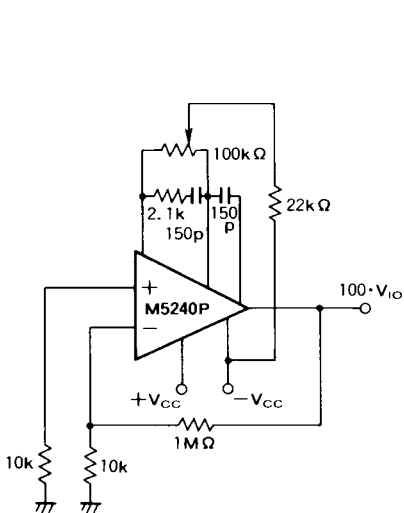
**TOTAL HARMONIC DISTORTION
VS. OUTPUT VOLTAGE**



TYPICAL CHARACTERISTICS

- $V_{CC} = \pm 15V$
- $G_v = 20dB (f = 1kHz)$
- $V_O = 9.5V_{rms} (f = 1kHz, THD = 0.1\%)$
- $THD = 0.01\% (f = 1kHz, V_O = 9V_{rms})$

OFFSET COMPENSATION CIRCUIT



(CIRCUIT FOR EXPLANATION)