VDSL6100i

Integrated VDSL Modem-on-Chip

PEF 22827, Version 1.1

Wireline Communications

Never stop thinking.

Edition 2005-01-30

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VDSL6100i

Revision History:	2005-01-30	Rev. 1.1
Previous Version:	None, First Release	

Page	**Subjects (major changes since last revision)**
	Update of Terminology, Register list and definitions, etc.

Preface

The PEF 22827 is an integrated VDSL modem-on-chip. It combines all the required functionality for standard 4-band VDSL over a twisted pair. This modem-on-chip includes a digital data transceiver supporting Ethernet interface, an analog front end (AFE) handling the VDSL QAM functionality and an internal line driver to provide transmission level to the line.

System functionality complies with ITU-T and ETSI standards for VDSL.

About This Document

This data sheet is organized as follows:

- **Product Overview** on **Page 19**, lists the main features and suggests typical applications.
- **Pin and Signal Descriptions**, starting on **Page 22**, shows the logic symbol and pin layout, lists all pins, and shows pin to signal assignment in different operation modes.
- **Functional Overview**, starting on **Page 55**, describes the functions of the PEF 22827 as a whole, followed by the functions of the digital, analog and line driver blocks, in separate sections. Block diagrams and firmware options are included.
- **Operation – Digital Block**, starting on **Page 81**, describes the operation of the digital block, which controls the analog block. The description includes configuration pins, the system clock, EEPROM, internal RAM management, and the boot process. **Operation – Line Driver** describes the computation of line driver gain and the line driver shut down procedure.
- **Interfaces**, starting on **Page 134**, includes the JTAG interface (boundary scan), management, network and EOC interfaces, and the I^2C interface for EEPROM.
- The **Memory and Register Descriptions – Digital Block** and **Memory and Register Descriptions – Analog Block** sections, starting on **Page 171**, describe memory mapping and registers for the digital and analog blocks, respectively. These sections include lists of registers by address and by type, and links to the detailed description of each register.
- **Electrical Characteristics - Overview**, starting on **Page 266**, specifies maximum ratings, recommended operating conditions, heat dissipation parameters and AC/DC characteristics for the integrated chip first, and then for the digital, analog and line driver blocks.
- **Package Outline** on **Page 290**.

In addition, for convenience, the following sections are included after the last chapter:

- A **Terminology** section – to help you define acronyms and expressions.
- A **References** list – to help you find information not in this data sheet.
- An **Index** – to help you find specific information.

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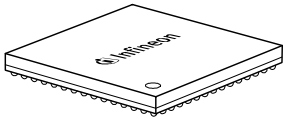
Version 1.1

1 Product Overview



P/PG-LFBGA-225-1

vpa09605

The PEF 22827 modem-on-chip is a single port integrated QAM based VDSL transceiver, whose technology complies fully with all current standards for VDSL - including ITU-T and ETSI.

This IC integrates the following components:

- VDSL digital transceiver in the digital block
- Filterless analog front end (AFE)[1] in the analog block
- Line driver

The VDSL digital transceiver is single port standard compliant QAM based VDSL.

The IC can be operated in Central Office (CO) or in the Customer Premises Equipment (CPE) applications.

The analog front end supports symmetric data rates up to 50 Mbits/s and asymmetric data rates of 40 Mbits/s upstream and 70 Mbits/s downstream.

The adaptive hybrid connected externally to the analog front end helps improve transceiver sensitivity and impedance matching to the line, which in turn contribute to a better data rate and reach performance.

The internal line driver helps implement a simplified design. The line driver consists of two wide-band amplifiers with a wide dynamic range, implementing one differential line driver.

The VDSL6100i internal line driver operates on ±7 V supplies, generating a differential output signal of 22 V_{pp}. The performance of the line driver meets the requirements of the QAM line code. A low Total Harmonic Distortion of -55 dB at 10 MHz (V_{pp}=22 V) into an 112 Ω load and a high slew rate of 1600 V/s are achieved by the current-feedback topology that is used.

[1] It may be necessary to add additional external components to ensure best performance under any line conditions. Refer to the reference design guidelines.

Type	Package
PEF 22827	PG-LFBGA-225-1

The compact design and low foot print of the VDSL6100i make it a preferred solution for the design of a Central Office (CO) or Customer Premises Equipment (CPE).

1.1 Features

Features of the PEF 22827 include:

- Highly integrated QAM VDSL standards compliant Modem-on-Chip
- Filterless AFE[1)]
- 1.3 cm^2 footprint
- ETSI, ANSI and ITU-T compliant high speed VDSL PHY applications
- Support for draft IETF MIBs for VDSL
- Frequency Division Duplexing (FDD)
- Full standards compliance with 2, 3, or 4 bands
- Dual latency support with built-in interleaver memory
- Power Back Off
- Sophisticated Rate Adaptation algorithm when used in CO side
- Embedded crystal oscillator (DCXO) for timing recovery
- Spectral allocation allows noise-free operation with xDSL, ISDN, TCM-ISDN and digital PBX
- Versatile and completely flexible band allocations
- Backward compatibility with Infineon's legacy chip sets

[1)] It may be necessary to add additional external components to ensure best performance under any line conditions. Refer to the reference design guidelines.

1.2 Power

The following are the power characteristics and features:

- Typical power dissipation 0.95 Watt
- Input voltages 1.2, 1.8, 3.3 and ±5
- Fast warm start after power down
- Power Save modes
  - Sleep mode
  - Wake-up

1.3 Typical Applications

The following are typical applications:

- Customer Premises Equipment (CPE)
- DSLAM linecards
- Fiber and broadband wireless extension over copper wire
- Multiple Dwelling/Tenant Units (MDU/MTU) networking
- LAN extensions up to 1,200 meters (4,000 ft.)
- Upgrades of SHDSL and ADSL systems

Figure 1 illustrates one Ethernet over VDSL CPE application. See also the PEF 22827 reference design document for more applications.

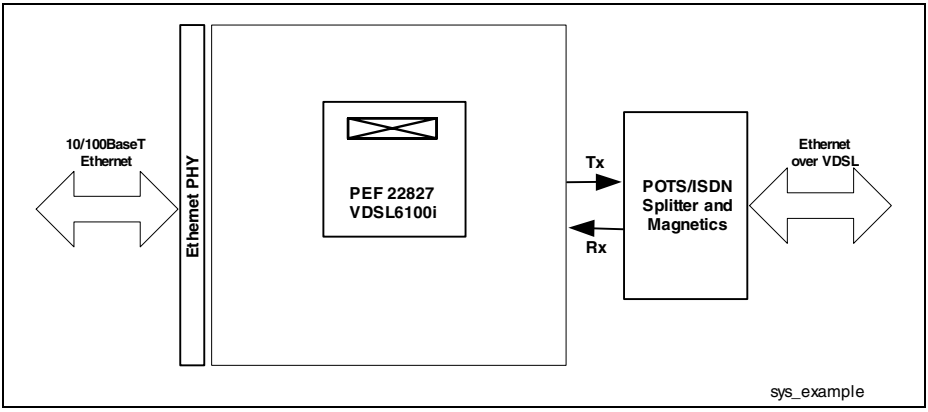


Figure 1 Ethernet over VDSL CPE Application Example

2 Pin and Signal Descriptions

Figure 2 shows the logic symbol of the PEF 22827.

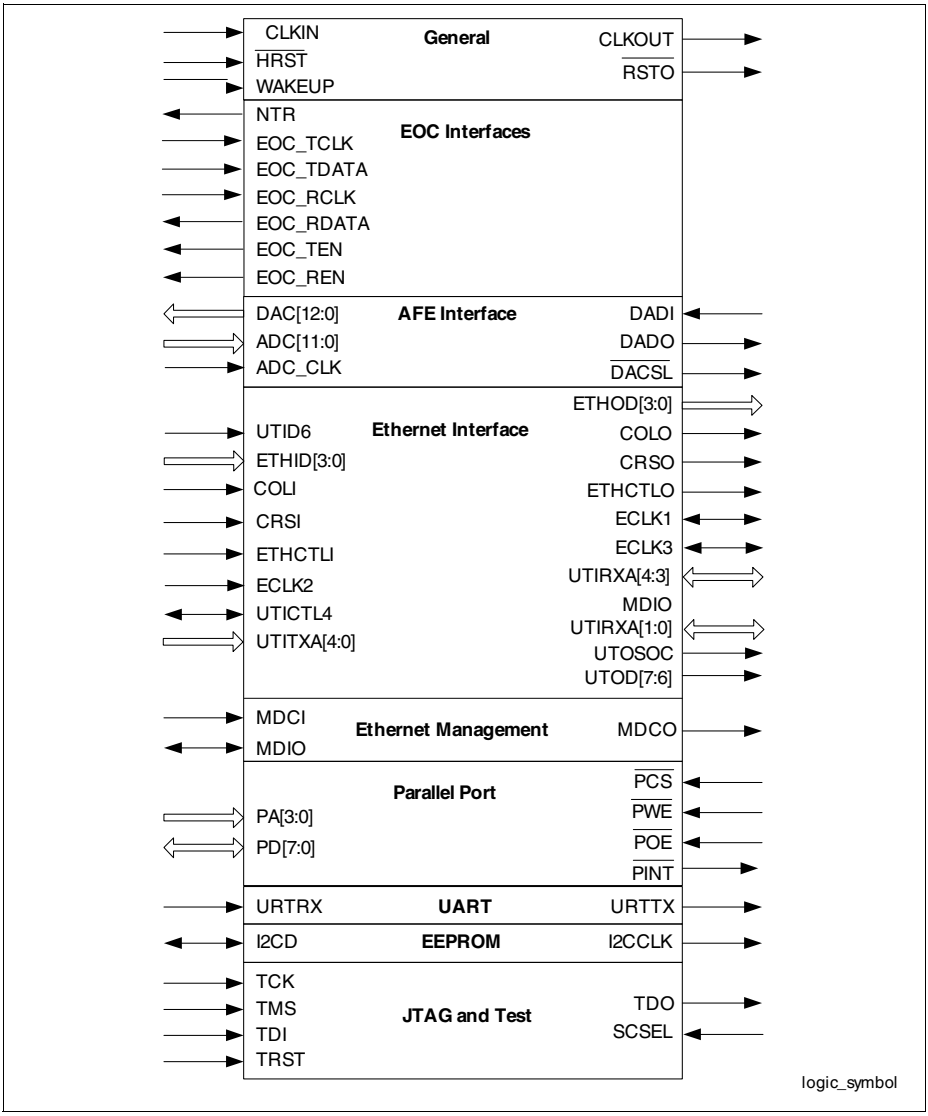


Figure 2 Logic Symbol

2.1 Pin Diagram

Refer to one of the following sections to determine the pin associated with each signal.

- **“Master Pin List” on Page 25** – Includes all pins, arranged by number.
- **“Pin Lists by Function” on Page 39** – Includes all pins, grouped by function.
- **“Pin and Signal Assignment in Different Modes” on Page 49** – Multiplexed pins only, grouped by mode and showing the signals that use each pin in each mode.

Use **Figure 3** to find the pin name corresponding to a pin number.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
1	Res	Res	GPO_A2	GPO_A5	GPO_A4	GPO_A3	VSSA	TEST_P	TX_P	VSSA	RXB_N	RXA_P	VSSR	$\overline{\text{HRST\_A}}$	Res
2	Res	Res	VDDIO_33	GPO_A1	VSSIO_33	GPO_A0	VDDA	TEST_N	TX_N	VDDA	RXA_N	RXB_P	VDDR	TDI_A	$\overline{\text{WAKEUP\_A}}$
3	Res	Res	VDDIO_33	Int	VSSIO_33	Int	VSSIO_33	VSSPLL	VDDT	VSST	TMS_A	TDO_A	SCAN_MODE	XTAL2	XTAL1
4	VSPLUS	Res	Res	Int	Int	Int	VDDIO_33	VDDIO_33	VSSD	CLK_IN	VDDPLL	VSSIO_33	Int	CLKOUT	Int
5	VSPLUS	Res	Res	OUT1	Res	Int	VSSD	Int	VDDD	TST_CLK	CLK_MODE	Int	Int	BOOT_EN	EEPROM_EN
6	VSPLUS	Res	Res	INN1	Res	Int	Int	VDDD	VDDD	VDDD	VDDD	VDDD	Int	Int	Int
7	OUT2	Res	Res	INP1	VSMINUS	Res	Int	Int	Int	Int	Int	Int	VDD_12	Int	NTR
8	INN2	Res	Res	VSMINUS	VSMINUS	PD0	PD1	Int	Int	Int	Int	VDD_12	VSS_12	Int	EOC_TCLK
9	INP2	Res	Res	PD3	PD2	PD4	VDD_33	VSS_12	UTIRXA4	VDD_12	ETHOD0	ETHID3	UTID6	EOC_RCLK	EOC_TDATA
10	Res	Res	Res	PD5	PD6	VDD_12	VDD_33	VSS_12	VSS_12	UTITXA4	VDD_33	ETHID1	CRSI	ECLK2	EOC_RDATA
11	Res	Res	PD7	$\overline{\text{POE}}$	$\overline{\text{PCS}}$	$\overline{\text{PWE}}$	Int	PCM_RCLK	VSS_12	UTITXA3	UTOSOC	UTICTL4	MDCI	ETHID2	COLI
12	Res	Res	PA0	PA2	VDD_12	PA3	TDO_D	PCM_RSIG	PCM_TSIG	UTITXA2	UTIRXA3	ETHCTLO	MDCO	ECLK1	ETHID0
13	VSSPLL12	Res	$\overline{\text{HRST\_D}}$	PA1	$\overline{\text{PINT}}$	Res	TRST	PCM_RDATA	PCM_TDATA	UTITXA0	UTIRXA1	ETHOD2	UTOD7	ETHCTLI	ECLK3
14	VSSPLL12	I2CD	I2CLK	URTTX	URTRX	$\overline{\text{RSTO}}$	TCK	PCM_RSYNC	PCM_TSYNC	EOC_REN	UTIRXA0	ETHOD1	CRSO	UTOD6	VSS_12
15	Res	VDD_PLL_12	VDD_PLL_12	EOC_TEN	$\overline{\text{WAKEUP\_D}}$	TMS_D	TDI_D	SCSEL	Res	UTITXA1	MDIO	VSS_12	ETHOD3	COLO	Res

Res = Reserved. Not connected.
Int = Internal use only. Do not connect.

27PIN_LAYOUT

Figure 3 PEF 22827 Pin Diagram

2.2 Master Pin List

Table 1 lists and describes the pins of the PEF 22827.

Table 1 I/O Signals (page 1 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
A1	Res	NC	-	**Reserved**
A2	Res	NC	-	**Reserved**
A3	Res	NC	-	**Reserved**
A4	VSPLUS	PWR	-	**Positive Supply Voltage** +5 V of Line Driver
A5	VSPLUS	PWR	-	**Positive Supply Voltage** +5 V of Line Driver
A6	VSPLUS	PWR	-	**Positive Supply Voltage** +5 V of Line Driver
A7	OUT2	AO	-	**Output from Amplifier 2** Line Driver
A8	INN2	AI	-	**Negative Input to Amplifier 2** Line Driver
A9	INP2	AI	-	**Positive Input to Amplifier 2** Line Driver
A10	Res	NC	-	**Reserved**
A11	Res	NC	-	**Reserved**
A12	Res	NC	-	**Reserved**
A13	VSS_PLL12	GND	-	**Analog GND for PLL** Digital block, 1.2 V supply
A14	VSS_PLL12	GND	-	**Analog GND for PLL** Digital block, 1.2 V supply
A15	Res	NC	-	**Reserved**
B1	Res	NC	-	**Reserved**
B2	Res	NC	-	**Reserved**
B3	Res	NC	-	**Reserved**
B4	Res	NC	-	**Reserved**
B5	Res	NC	-	**Reserved**
B6	Res	NC	-	**Reserved**

Table 1 I/O Signals (page 2 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
B7	Res	NC	-	**Reserved**
B8	Res	NC	-	**Reserved**
B9	Res	NC	-	**Reserved**
B10	Res	NC	-	**Reserved**
B11	Res	NC	-	**Reserved**
B12	Res	NC	-	**Reserved**
B13	Res	NC	-	**Reserved**
B14	I^2CD	I/O	-	**I^2C Data** Read or write data from or to EEPROM.
B15	VDD_PLL_12	PWR	-	**Analog Supply for PLL** Digital block, 1.2 V supply
C1	GPO_A2	AO	-	**General Purpose Output**
C2	VDDIO_33	PWR	-	**Digital Supply I/O** 3.3 V for analog block
C3	VDDIO_33	PWR	-	**Digital Supply I/O** 3.3 V for analog block
C4	Res	NC	-	**Reserved**
C5	Res	NC	-	**Reserved**
C6	Res	NC	-	**Reserved**
C7	Res	NC	-	**Reserved**
C8	Res	NC	-	**Reserved**
C9	Res	NC	-	**Reserved**
C10	Res	NC	-	**Reserved**
C11	PD7	I/O	-	**Parallel Data Bus** Host interface data bus signal.
C12	PA0	I	-	**Parallel Address Bus** Part of asynchronous address that selects host interface registers.
C13	$\overline{\text{HRST\_D}}$	I	-	**Digital Hard Reset** Hard reset. Activated on transition from low to high and power up.

Table 1 I/O Signals (page 3 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
C14	I^2CCLK	I/O	-	**I^2C Clock** EEPROM clock signal
C15	VDD_PLL_12	PWR	-	**Analog Supply for PLL** Digital block, 1.2 V supply
D1	GPO_A5	AO	-	**General Purpose Output**
D2	GPO_A1	AO	-	**General Purpose Output**
D3	Int	-	-	**Internal** Do not connect.
D4	Int	-	-	**Internal** Do not connect.
D5	OUT1	AO	-	**Output from Amplifier 1** Line Driver
D6	INN1	AI	-	**Negative Input to Amplifier 1**
D7	INP1	AI	-	**Positive Input to Amplifier 1** Line Driver
D8	VSMINUS	PWR	-	**Negative Supply Voltage** –5 V of Line Driver
D9	PD3	I/O	-	**Parallel Data Bus** Host interface data bus.
D10	PD5	I/O	-	**Parallel Data Bus** Host interface data bus.
D11	$\overline{POE}$	I	-	**Parallel Output Enable** Output enable strobe to host interface.
D12	PA2	I	-	**Parallel Address Bus** Part of asynchronous address that selects host interface registers.
D13	PA1	I	-	**Parallel Address Bus** Part of asynchronous address that selects host interface registers.
D14	URTTX	O	-	**UART Transmit Line**
D15	EOC_TEN	O	-	**Configuration, Control and Status** Enables clear channel TX. Configuration input signal during reset.[1)]

Table 1 I/O Signals (page 4 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
E1	GPO_A4	AO	-	**General Purpose Output Pad**
E2	VSSIO_33	GND	-	**GND Digital I/O** Analog and digital blocks, 3.3 V supply
E3	VSSIO_33	GND	-	**GND Digital I/O** Analog and digital blocks, 3.3 V supply
E4	Int	-	-	**Internal** Do not connect.
E5	Res	NC	-	**Reserved**
E6	Res	NC	-	**Reserved**
E7	VSMINUS	PWR	-	**Negative Supply Voltage** –5 V of Line Driver
E8	VSMINUS	PWR	-	**Negative Supply Voltage** –5 V of Line Driver
E9	PD2	I/O	-	**Parallel Data Bus** Host interface data bus.
E10	PD6	I/O	-	**Parallel Data Bus** Host interface data bus signal.
E11	$\overline{\text{PCS}}$	I	-	**Parallel Chip Select** Host interface transceiver selector.
E12	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply
E13	$\overline{\text{PINT}}$	O	OD	**Interrupt Request** Interrupt request from IC to external host.
E14	URTRX	I	-	**UART Reception Line**
E15	$\overline{\text{WAKEUP\_D}}$	I	-	**Wake-up Interrupt Request** Wake the digital transceiver from sleep mode and Loss-of-Power indicator for far-end indication. Connect WAKEUP_D to WAKEUP_A.
F1	GPO_A3	AO	-	**General Purpose Output**
F2	GPO_A0	AO	-	**General Purpose Output**
F3	Int	-	-	**Internal** Do not connect.

Table 1 I/O Signals (page 5 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
F4	Int	-	-	**Internal** Do not connect.
F5	Int	-	-	**Internal** Do not connect.
F6	Int	-	-	**Internal** Do not connect.
F7	Res	NC	-	**Reserved**
F8	PD0	I/O	-	**Parallel Data Bus** Host interface data bus.
F9	PD4	I/O	-	**Parallel Data Bus** Host interface data bus.
F10	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply
F11	$\overline{\text{PWE}}$	I	-	**Parallel Write Enable** Write strobe to the host interface.
F12	PA3	I	-	**Parallel Address Bus** Part of asynchronous address that selects host interface registers.
F13	Res	NC	-	**Reserved**
F14	$\overline{\text{RSTO}}$	O	-	**Digital Hard Reset** Samples reset configuration word. Active low.
F15	TMS_D	I	-	**Digital JTAG Input Control** Tie to 0 in normal mode. For testing only.
G1	VSSA	GND	-	**Analog GND for ADC** Analog block, 1.8 V supply
G2	VDDA	PWR	-	**Analog Supply for ADC** Analog block, 1.8 V supply)
G3	VSSIO_33	GND	-	**GND Digital I/O** Analog and digital blocks, 3.3 V supply
G4	VDDIO_33	PWR	-	**Digital Supply I/O** 3.3 V for analog block
G5	VSSD	GND	-	**Digital GND for Analog Core**

Table 1 I/O Signals (page 6 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
G6	Int	-	-	**Internal** Do not connect.
G7	Int	-	-	**Internal** Do not connect.
G8	PD1	I/O	-	**Parallel Data Bus** Host interface data bus signal.
G9	VDD_33	PWR	-	**Supply Digital I/O** Analog block, 3.3 V supply
G10	VDD_33	PWR	-	**Digital 3.3 V Supply I/O**
G11	Int	-	-	**Internal** Do not connect.
G12	TDO_D	O	-	**Digital JTAG Test Serial Data Output** For testing only.
G13	TRST	I	PU[2)]	**JTAG Test Reset** Tie to 0 in normal mode. For testing only.
G14	TCK	I	-	**JTAG Test Clock** Tie to 0 in normal mode. For testing only.
G15	TDI_D	I	-	**Digital JTAG Test Serial Data Input** Tie to 0 in normal mode. For testing only.
H1	TEST_P	AO	-	**Positive Analog Output** For testing only. Do not connect.
H2	TEST_N	AO	-	**Negative Analog Output** For testing only. Do not connect.
H3	VSSPLL	GND	-	**Analog GND for PLL** Analog block 1.8 V supply
H4	VDDIO_33	PWR	-	**Digital Supply I/O** 3.3 V for analog block
H5	Int	-	-	**Internal** Do not connect.
H6	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply
H7	Int	-	-	**Internal** Do not connect.

Table 1 I/O Signals (page 7 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
H8	Int	-	-	**Internal** Do not connect.
H9	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply
H10	VSS_12	GND	-	**GND Digital Core** Digital block1.2 V supply
H11	PCM_RCLK	I	-	**Configuration, Control and Status** PCM serial clock.[3)] Configuration input signal during reset.[1)]
H12	$\overline{\text{PCM\_RSIG}}$	I	-	**Configuration, Control and Status** Serial signaling input.[3)] Configuration input signal during reset.[1)]
H13	PCM_RDATA	I	-	**Configuration, Control and Status** Serial data input[3)]. Configuration input signal during reset.[1)]
H14	PCM_RSYNC	I	-	**Configuration, Control and Status** Serial synchronization.[3)] Configuration input signal during reset.[1)]
H15	SCSEL	I	-	**Digital Scan Select** Scan chain select. For testing only.
J1	TX_P	AO	-	**Positive Transmission Analog Output** Differential signal.
J2	TX_N	AO	-	**Negative Transmission Analog Output** Differential signal.
J3	VDDT	PWR	-	**Analog Supply for TX-Path** Analog block, 1.8 V supply
J4	VSSD	GND	-	**Digital GND** Analog block, 1.8 V supply
J5	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply
J6	VDDD	PWR	-	**Digital Supply for Analog Block** 1.8 V supply
J7	Int	-	-	**Internal** Do not connect.

Table 1 I/O Signals (page 8 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
J8	Int	-	-	**Internal** Do not connect.
J9	**UTIRXA4**	I/O	-	**Network Interface Input Data**
J10	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply
J11	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply
J12	$\overline{\text{PCM\_TSIG}}$	O	PU[2]	**Configuration, Control and Status** PCM Serial Signaling Interface.[3] Configuration input signal during reset.[1]
J13	PCM_TDATA	O	-	**Configuration, Control and Status** PCM Serial Data.[3] Configuration input signal during reset.[1]
J14	PCM_TSYNC	O	-	**Configuration, Control and Status** PCM Serial Synchronization.[3] Configuration input signal during reset.[1]
J15	Res	NC	-	**Reserved**
K1	VSSA	GND	-	**Analog GND for ADC** Analog block, 1.8 V supply
K2	VDDA	PWR	-	**Analog Supply for ADC** Analog block, 1.8 V supply
K3	VSST	GND	-	**Analog GND for TX-Path** Analog block, 1.8 V supply
K4	CLK_IN	I	-	**External Clock Input**
K5	TST_CLK	AO	-	**Clock Output** For testing only. Do not connect.
K6	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply
K7	Int	-	-	**Internal** Do not connect.
K8	Int	-	-	**Internal** Do not connect.
K9	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply

Table 1 I/O Signals (page 9 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
K10	**UTITXA4**	I	-	**Network Interface Input Data**
K11	**UTITXA3**	I	-	**Network Interface Input Data**
K12	**UTITXA2**	I	-	**Network Interface Input Data**
K13	**UTITXA0**	I	-	**Network Interface Input Data**
K14	EOC_REN	O	PD[4)]	**Configuration, Control and Status** Clear channel reception enable. Configuration input signal during reset.[1)]
K15	**UTITXA1**	I	-	**Network Interface Input Data**
L1	RXB_N	AI	-	**Negative Reception Analog Input B** Differential signal.
L2	RXA_N	AI	-	**Negative Reception Analog Input A** Differential signal.
L3	TMS_A	AI	-	**Analog JTAG Input Control** Tied to 0 in normal mode. For testing only)
L4	VDDPLL	PWR	-	**Analog Supply for PLL** Analog block, 1.8 V supply
L5	CLK_MODE	AI	-	**Analog Clock Source for Signals** Internal via XTAL or external via CLK_IN
L6	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply
L7	Int	-	-	**Internal Use Only** Do not connect.
L8	Int	-	-	**Internal Use Only** Do not connect.
L9	**ETHOD0**	O	-	**Ethernet Network Interface Output Data** Configuration pin during reset.[1)]
	TXD0	O	-	**Ethernet Interface MII MAC - TX Data**
	RXD0	O	-	**Ethernet Interface MII and RMII PHY - RX Data**
	RX	O	-	**Typical and Source Synchronous SMII - Reception Data**
L10	VDD_33	PWR	-	**Supply Digital I/O** Analog block, 3.3 V supply

Table 1 I/O Signals (page 10 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
L11	**UTOSOC**	O	-	**Not Used**
L12	**UTIRXA3**	I/O	-	**Network Interface Input Data**
L13	**UTIRXA1**	I	-	**Not Used**
L14	**UTIRXA0**	I	-	**Not Used**
L15	**MDIO**	I/O	-	**MDIO, Ethernet Interface SMI MAC and PHY – Management Data**
M1	RXA_P	AI	-	**Positive RX Analog Input A** Differential signal.
M2	RXB_P	AI	-	**Positive RX Analog Input B** Differential signal.
M3	TDO_A	AO	-	**Analog JTAG Test Serial Data Out** For testing only.
M4	VSSIO_33	GND	-	**GND Digital I/O** Analog and digital blocks, 3.3 V supply
M5	Int	-	-	**Internal Use Only** Do not connect.
M6	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply
M7	Int	-	-	**Internal Use Only** Do not connect.
M8	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply
M9	**ETHID3**	I	-	**Ethernet Network Interface Data**
	RXD3	I	-	**Ethernet Interface MII MAC - RX Data**
	TXD3	I	-	**Ethernet MII PHY - TX Input Data**
M10	**ETHID1**	I	-	**Ethernet Network Interface Data**
	RXD1	I	-	**Ethernet Interface MII and RMII MAC - RX Data**
	TXD1	I	-	**Ethernet Interface MII and RMII PHY - TX Data**
M11	**UTICTL4**	I	-	**Not Used**

Table 1 I/O Signals (page 11 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
M12	**ETHCTLO**	O	-	**Ethernet Network Interface Control**
	TXEN	O	-	**Ethernet Interface MII and RMII MAC - TX Enable**
	RXDV	O	-	**Ethernet Interface MII and RMII PHY - RX Data Valid**
	RXSYNC	O	-	**Source Synchronous SMII - RX Synchr.**
M13	**ETHOD2**	O	-	**Ethernet Network Interface Data** Configuration pin during hard reset.[1)]
	TXD2	O	-	**Ethernet Interface MII MAC - TX Data**
	RXD2	O	-	**Ethernet Interface MII PHY - RX Data**
M14	**ETHOD1**	O	-	**Network Interface Data** Configuration pin during hard reset.[1)]
	TXD1	O	-	**Ethernet Interface MII MAC - TX Data**
	RXD1	O	-	**Ethernet Interface MII and RMII PHY - RX Data**
M15	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply
N1	VSSR	GND	-	**Analog GND for RX Path** Analog block, 1.8 V supply
N2	VDDR	PWR	-	**Analog Supply for RX-Path** Analog block, 1.8 V supply
N3	SCAN_MODE	AI	-	**Scan Mode for Analog Core** Sets scan testing mode. For testing only.
N4	Int	-	-	**Internal** Do not connect.
N5	Int	-	-	**Internal** Do not connect.
N6	Int	-	-	**Internal** Do not connect.
N7	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply
N8	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply

Table 1 I/O Signals (page 12 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
N9	**UTID6**	I	-	See description of signal using this pin.
	RXSYNC_EN	I	-	**Source Synchronous SMII Mode** Enables RXSYNC signal synchronization
N10	**CRSI**	I	-	**Carrier Sense Input**
	CRS	I	-	**Ethernet MII MAC - Carrier Sense**
N11	**MDCI**	I	-	**MDIO and SMI PHY Input Clock**
	MDC	I		**Management Data Clock**
N12	**MDCO**	O	-	**MDIO and SMI MAC Clock Output** Reset value is 0.
	RXCLK	O	-	**Source Synchronous SMII - RX Clock**
	MDC	O	-	**Management Data Clock**
N13	**UTOD7**	O	-	**Not Used**
N14	**CRSO**	O	-	**Carrier Sense Output**
	CRS	O	-	**Ethernet Interface MII PHY - Carrier Sense**
N15	**ETHOD3**	O	-	**Ethernet Network Interface Output Data** Configuration pin during reset.[1)]
	TXD3	O	-	**Ethernet Interface MII MAC - TX Data**
	RXD3	O	-	**Ethernet Interface MII PHY - RX Data**
P1	$\overline{\text{HRST\_A}}$	AI	-	**Analog Hard Reset**
P2	TDI_A	AI	-	**Analog JTAG Test Serial Data In** Tied to 0 in normal mode. For testing only.
P3	XTAL2	AO	-	**Crystal** Not connected for CLK_MODE (**L5**) = 1.
P4	CLKOUT	O	-	**Clock Output** Reference clock for parallel port and internal use. Provides clock to the host. Termination point must be active.
P5	$\overline{\text{BOOT\_EN}}$	-	PU[2)]	**Boot Link Enable** Configuration pin during hard reset. Do not use during normal operation.[1)]
P6	Int	-	-	**Internal Use Only** Do not connect.

Table 1 I/O Signals (page 13 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
P7	Int	-	-	**Internal Use Only** Do not connect.
P8	Int	-	-	**Internal Use Only** Do not connect.
P9	EOC_RCLK	I	PD[4)]	**Configuration, Control and Status** Clear channel reception clock. Configuration input signal during reset.[1)]
P10	**ECLK2**	I	-	**Network Interface Clock**
	PHYCLK	I	-	**Ethernet Interface MII PHY - MII Source Clock**
P11	**ETHID2**	I	-	**Ethernet Network Interface Data**
	RXD2	I	-	**Ethernet Interface MII MAC - RX Data**
	TXD2	I	-	**Ethernet Interface MII PHY - TX Data**
P12	**ECLK1**	I/O	-	**Network Interface Clock**
	TXCLK	I	-	**Ethernet Interface MII MAC TX Clock**
	RXCLK	O	-	**Ethernet Interface MII PHY - RXClock**
	REFCLK	I	-	**Ethernet Interface RMII MAC and PHY, and Typical SMII - Reference Clock**
	RXCLKREF	I	-	**Source Synchr. SMII - Reference Clock**
P13	**ETHCTLI**	I	-	**Network Interface Control Input**
	RXDV	I	-	**Ethernet Interface MII and RMII MAC - RX Data Valid**
	TXEN	I	-	**Ethernet MII and RMII PHY - TX Enable**
	TXSYNC	O	-	**Typical and Source Synchronous SMII - Transmission Synchronization**
P14	**UTOD6**	O	-	**Configuration Pin During Reset** Reserved after hard reset.[1)]
P15	**COLO**	O	-	**Collision Output** Configuration pin during reset.[1)]
	COL	O	-	**Ethernet Interface MII PHY - Collision Detected**
R1	Res	NC	-	**Reserved**

Table 1 I/O Signals (page 14 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
R2	$\overline{\text{WAKEUP\_A}}$	AO	-	**Analog Wake-up Detection Interrupt** Connect to WAKEUP_D. Internal only.
R3	XTAL1	AI	-	**Crystal** When CLK_MODE (L5) is 1, 0 No divider 1 CLK_IN divided by 2
R4	Int	-	-	**Internal Use Only.** Do not connect.
R5	EEPROM_EN	-	PD[4)]	**EEPROM Enable** Configuration pin during hard reset. Do not use during normal operation.[1)]
R6	Int	-	-	**Internal Use Only** Do not connect.
R7	NTR	I/O	-	**Network Timing Reference** LT receives this 8 kHz clock. NT transmits a sample of this 8 kHz division clock. Can be configured as an independent 8 kHz output clock. Useful for the PCM interface. Configuration pin during hard reset.[1)]
R8	EOC_TCLK	I	-	**Configuration, Control and Status** Clear channel transmit clock (input). Configuration input signal during reset.[1)]
R9	EOC_TDATA	I	PD[4)]	**Configuration, Control and Status** Clear channel transmit data. Configuration input signal during reset.[1)]
R10	EOC_RDATA	O	PU[2)]	**Configuration, Control and Status** Clear channel reception data (output). Configuration input signal during reset.[1)]
R11	**COLI**	I	-	**Collision Input**
	COL	I	-	**Ethernet Interface MII MAC - Collision Detected**

Table 1 I/O Signals (page 15 of 15)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
R12	**ETHID0**	I	-	**Ethernet Network Interface Input Data**
	RXD0	I	-	**Ethernet Interface MII and RMII MAC - RX Data**
	TXD0	I	-	**Ethernet Interface MII and RMII PHY - TX Data**
	TX	I	-	**Typical and Source Synchronous SMII - TX Data**
R13	**ECLK3**	I	-	**Network Interface Clock**
	RXCLK	I	-	**Ethernet Interface MII MAC - RX Clock**
	TXCLK	O	-	**Ethernet Interface MII PHY - TX Clock**
		I	-	**Ethernet Interface Source Synchronous SMII MAC - TX Clock**
R14	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply.
R15	Res		-	**Reserved**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2) Pull Up (PU) buffers are 550 KΩ.

3) In the PCM interface, signals J12, J13, J14, H12, H13, H14 and H11 are bits 6 through 0. When the PCM interface is disabled, signals H11, H12, H13, H14, J12, J13 and J14 are software controlled.

4) Pull Down (PD) buffers are 100 KΩ.

2.3 Pin Lists by Function

The pin lists in this section show all pins in **Figure 3**, grouped as follows:

2.3.1 General Purpose Pins

Table 2 Lists all general purpose pins.

Table 2 General Purpose Signals

Pin or Ball No.	Name	Pin Type	Buffer type	Function
K4	CLK_IN	I	-	**External Clock Input for Analog Signals**
L5	CLK_MODE	AI	-	**Analog Clock Source for Signals** Internal via XTAL or external via CLK_IN.
P4	CLKOUT	O	-	**Clock Output** Reference clock for parallel port and internal use. Provides clock to the host. Termination point must be active.
P1	$\overline{\text{HRST\_A}}$	AI	-	**Analog Hard Reset Input**
C13	$\overline{\text{HRST\_D}}$	I	-	**Digital Hard Reset** Hard reset pin. Activated on transition from low to high. Activate on power up.
F14	$\overline{\text{RSTO}}$	O	-	**Digital Hard Reset** Active on low signal. RSTO is used to sample the reset configuration word.
R2	$\overline{\text{WAKE-UP\_A}}$	AO	-	**Analog Wake-up Detection Interrupt** For analog signals. Connect to WAKEUP_D.
E15	$\overline{\text{WAKEUP\_D}}$	I	-	**Wake-up Interrupt Request** $\overline{\text{WAKEUP\_D}}$ wakes the digital transceiver from sleep mode. Also Loss-of-Power indicator for far-end indication. Connect to Wake-up_A.
R3	XTAL1	AI	-	**Crystal**[1)] When CLK_MODE (L5) = 1, 0 No divider 1 CLK_IN divided by 2
P3	XTAL2	AO	-	**Crystal**[1)] When CLK_MODE (L5) =1, not connected.

1) See the reference design document for the external capacitor connection.

2.3.2 Analog Interface Pins

Table 3 lists all analog interface pins.

Table 3 Analog Interface Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
A7	OUT2	AO	-	**Output of Line Driver Amplifier 2** Line Driver
A8	INN2	AI	-	**Negative Input of Line Driver Amplifier 2** Line Driver
A9	INP2	AI	-	**Positive Input of Line Driver Amplifier 2** Line Driver
D5	OUT1	AO	-	**Output of Line Driver Amplifier 1** Line Driver
D6	INN1	AI	-	**Negative Input of Line Driver Amplifier 1** Line Driver
D7	INP1	AI	-	**Positive Input of Line Driver Amplifier 1** Line Driver
J1	TX_P	AO	-	**Positive TX Analog Output** Differential signal.
J2	TX_N	AO	-	**Negative TX Analog Output** Differential signal.
L1	RXB_N	AI	-	**Negative RX Analog Input B** Differential signal.
L2	RXA_N	AI	-	**Negative RX Analog Input A** Differential signal.
M1	RXA_P	AI	-	**Positive RX Analog Input A** Differential signal.
M2	RXB_P	AI	-	**Positive RX Analog Input B** Differential signal.

2.3.3 Embedded Overhead Channel (EOC) and PCM Pins

Table 4 lists all Embedded Overhead Channel (EOC) and PCM pins.

Table 4 EOC and PCM Pins (page 1 of 2)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function in Normal Mode[1)]
P9	EOC_RCLK	I	PD[2)]	**Clear Channel Reception Clock** Configuration pin during hard reset.[1)]
R10	EOC_RDATA	O	PU[3)]	**EOC Reception Data** See also, **"External Status Signals (LEDs)" on Page 131**. Configuration pin during hard reset.[1)]
K14	EOC_REN	O	PD[2)]	**Clear Channel Reception Enable** Configuration pin during hard reset.[1)]
R8	EOC_TCLK	I	-	**Clear Channel Transmission Clock** Configuration pin during hard reset.[1)]
R9	EOC_TDATA	I	PD[2)]	**EOC Transmission Data** Configuration pin during hard reset.[1)]
D15	EOC_TEN	O	PD[2)]	**Clear Channel Transmission Enable** Configuration pin during hard reset.[1)]
R7	NTR	I/O	-	**Network Timing Reference** LT receives this 8 kHz clock. NT transmits a sample of this 8 kHz division clock. Can be configured as an independent 8 kHz output clock. Useful for the PCM interface. Configuration pin during hard reset.[1)]
H11	PCM_RCLK	I	-	**PCM Reception Clock**[4)] Must be 0 during reset.
H13	PCM_RDATA	I	-	**PCM Reception Serial Data**[4)] Must be 0 during reset.
H12	$\overline{\text{PCM\_RSIG}}$	I	-	**PCM Reception Serial Signaling**[4)] Must be 0 during reset.
H14	PCM_RSYNC	I	-	**PCM Reception Synchronization Signal**[4)] Must be 0 during reset.
J13	PCM_TDATA	O	-	**PCM Transmission Serial Data**[4)] Configuration pin during hard reset.[1)]

Table 4 EOC and PCM Pins (page 2 of 2)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function in Normal Mode[1)]
J12	$\overline{\text{PCM\_TSIG}}$	O	PU[3)]	**PCM Transmission Serial Signaling[4)]** Configuration pin during hard reset.[1)]
J14	PCM_TSYNC	O	-	**PCM Transmission Synchronization Signal[4)]** Configuration pin during hard reset.[1)]

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2) Pull Down (PD) buffers are 100 KΩ.

3) Pull Up (PU) buffers are 550 KΩ.

4) In the PCM interface, signals J12, J13, J14, H12, H13, H14 and H11 are bits 6 through 0. When the PCM interface is disabled, signals H11, H12, H13, H14, J12, J13 and J14 are software controlled.

2.3.4 Ethernet Pins

Table 5 lists dual purpose pins that support Ethernet.

Table 5 Ethernet or Pins (page 1 of 2)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
M9	ETHID3	I	-	**Network Interface Input Data 3**
M10	ETHID1	I	-	**Network Interface Input Data 1**
N9	UTID6	I	-	**Source Synchronous SMII Mode – RXSYNC Signal Synchronization**
N10	CRSI	I	-	**Carrier Sense Input**
R11	COLI	I	-	**Collision Input**
P12	ECLK1	I/O	-	**Network Interface Clock**
P10	ECLK2	I	-	**Network Interface Clock**
R13	ECLK3	I/O	-	**Network Interface Clock**
P11	ETHID2	I	-	**Network Interface Input Data 2**
R12	ETHID0	I	-	**Network Interface Input Data 0**
N11	MDCI	I	-	**MDIO Clock Input**
M11	Res	NC	-	**Reserved**
P13	ETHCTLI	I	-	**Network Interface Control Input**

Table 5 Ethernet or Pins (page 2 of 2)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
N12	MDCO	O	PD[1)]	**MDIO Clock Output**
M12	ETHCTLO	O	PU[2)]	**Network Interface Control Output**
N13	UTOD7	O	-	**Transmission Data Output, High Bit**
P14	UTOD6	O	-	**Transmission Data Output** Configuration pin during hard reset.[3)]
N14	CRSO	O	-	**Carrier Sense Output**
P15	COLO	O	-	**Collision Output** Configuration pin during hard reset.[3)]
L9	ETHOD0	O	-	**Ethernet Network Interface Output Data** Configuration pin during hard reset.[3)]
M14	ETHOD1	O	-	**Ethernet Network Interface Output Data** Configuration pin during hard reset.[3)]
M13	ETHOD2	O	-	**Ethernet Network Interface Output Data** Configuration pin during hard reset.[3)]
N15	ETHOD3	O	-	**Ethernet Network Interface Output Data** Configuration pin during hard reset.[3)]
L13	UTIRXA1	I/O	-	**Network Interface Input Data**
L12	UTIRXA3	I/O	-	**Network Interface Input Data**
J9	UTIRXA4	I/O	-	**Network Interface Input Data**
L15	MDIO	I/O	-	**MDIO Data**
K10	UTITXA4	I	-	**Network Interface Input Data**
K11	UTITXA3	I	-	**Network Interface Input Data**
K12	UTITXA2	I	-	**Network Interface Input Data**
K13	UTITXA0	I	-	**Network Interface Input Data**
K15	UTITXA1	I	-	**Network Interface Input Data**

1) Pull Down (PD) buffers are 100 KΩ.

2) Pull Up (PU) buffers are 550 KΩ.

3) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2.3.5 Parallel Port Pins

Table 6 describes the pins of the parallel port.

Table 6 Parallel Port Pins

Pin	Name	Pin Type	Buffer Type	Function
E13	$\overline{\text{PINT}}$	O	OD	**Parallel Interrupt Request** Interrupt request signal from the transceiver to the external host. $\overline{\text{PINT}}$ is an open drain active on low signal. A pull up should be connected.
C12	PA0	I	-	**Parallel Address Bus** This asynchronous signal selects between the host interface registers.
D13:D12	PA1:PA2	I	-	
F12	PA3	I	-	
D11	$\overline{\text{POE}}$	I	-	**Parallel Output Enable** The output enable strobe to the host interface.
F11	$\overline{\text{PWE}}$	I	-	**Parallel Write Enable** Host interface write strobe signal.
E11	$\overline{\text{PCS}}$	I	-	**Parallel Chip Select** Host interface transceiver selector.
F8	PD0	I/O	-	**Parallel Data Bus** Host interface data bus signals.
G8	PD1	I/O	-	
E9	PD2	I/O	-	
D9	PD3	I/O	-	
F9	PD4	I/O	-	
D10	PD5	I/O	-	
E10	PD6	I/O	-	
C11	PD7	I/O	-	

2.3.6 UART Pins

Table 7 describes pins that connect to the UART line.

Table 7 UART Host and Parallel Port Pins

Pin	Name	Pin Type	Buffer Type	Function
E14	URTRX	I	-	**UART Reception Line**
D14	URTTX	O	-	**UART Transmission Line**

2.3.7 EEPROM Pins

Table 8 describes pins that enable read and write access to the EEPROM.

Table 8 EEPROM Pins

Pin	Name	Pin Type	Pull	Function
B14	I^2CD	I/O	-	**I^2C Data** Used to read or write data to EEPROM. It is open drain and requires a pull-up resistor.
C14	I^2CCLK	I/O	-	**I^2C Clock** Clock signal to EEPROM that is open drain and requires a pull-up resistor.

2.3.8 Test Pins

Table 10 describes JTAG pins. Table 10 describes other test pins.

Table 9 JTAG Pins (page 1 of 2)

Pin	Name	Pin Type	Buffer Type	Function
G14	TCK	I	-	**JTAG Test Clock** For testing only. Tie to 0 in normal mode.
P2	TDI_A	AI	-	**Analog JTAG Test Serial Data In** For testing only. Tie to 0 in normal mode.
G15	TDI_D	I	-	**Digital JTAG Test Serial Data Input** For testing only. Tie to 0 in normal mode.
M3	TDO_A	AO	-	**Analog JTAG Test Serial Data Out** For testing only.

Table 9 JTAG Pins (page 2 of 2)

Pin	Name	Pin Type	Buffer Type	Function
G12	TDO_D	O	-	**Digital JTAG Test Serial Data Output** For testing only.
L3	TMS_A	AI	-	**Analog JTAG Input Control** For testing only. Tie to 0 in normal mode.
F15	TMS_D	I	-	**Digital JTAG Input Control** For testing only. Tie to 0 in normal mode.
G13	TRST	I	PU[1)]	**JTAG Test Reset** For testing only. Tie to 0 in normal mode.

1) Pull Up (PU) buffers are 550 KΩ.

Table 10 Test Pins

Pin	Name	Pin Type	Buffer Type	Function
N3	SCAN_ MODE	AI	-	**Scan Mode for Analog Core** For testing only. Determines scan test mode. Tie to 0 in normal mode.
H15	SCSEL	I	-	**Digital Scan Select** Scan chain select. For testing only.

2.3.9 Voltage Supply and Ground Pins

Table 11 describes voltage supply pins while Table 12 describes ground pins.

Table 11 Voltage Supply Pins (page 1 of 2)

Pin	Name	Pin Type	Buffer Type	Function
E12, F10, K9, M8, N7	VDD_12	PWR	-	**Supply Digital Core** Digital block, 1.2 V supply.
G9, G10, L10	VDD_33	PWR	-	**Supply Digital I/O** Analog block, 3.3 V supply.
B15, C15	VDD_PLL _12	PWR	-	**Analog Supply for PLL** Digital block, 1.2 V supply.
G2, K2	VDDA	PWR	-	**Analog Supply for ADC** Analog block, 1.8 V supply.

Table 11 Voltage Supply Pins (page 2 of 2)

Pin	Name	Pin Type	Buffer Type	Function
H6, J5, J6, K6, L6, M6	VDDD	PWR	-	**Supply Digital Core** Analog block, 1.8 V supply.
C2, C3, G4, H4	VDDIO_33	PWR	-	**Analog Supply I/O** 3.3 V supply.
L4	VDDPLL	PWR	-	**Analog Supply for PLL** Analog block, 1.8 V supply.
N2	VDDR	PWR	-	**Analog Supply for RX Path** Analog block, 1.8 V supply
J3	VDDT	PWR	-	**Analog Supply for TX-Path** Analog block, 1.8 V supply.
D8, E7, E8	VSMINUS	PWR	-	**Negative Supply Voltage** -5 V of Line Driver.
A4, A5, A6	VSPLUS	PWR	-	**Positive Supply Voltage** +5 V of Line Driver.

Table 12 Ground Pins (page 1 of 2)

Pin	Name	Pin Type	Buffer Type	Function
H9, H10, J10, J11, M15, N8, R14	VSS_12	GND	-	**GND Digital Core** Digital block, 1.2 V supply.
A13, A14	VSS_PLL12	GND	-	**Analog GND for PLL** Digital block, 1.2 V supply.
G1, K1	VSSA	GND	-	**Analog GND for ADC** Analog block, 1.8 V supply.
G5, J4	VSSD	GND	-	**Digital GND** Analog block, 1.8 V supply
E2, E3, G3, M4	VSSIO_33	GND	-	**GND Digital I/O** Analog and digital blocks, 3.3 V supply

Table 12 Ground Pins (page 2 of 2)

Pin	Name	Pin Type	Buffer Type	Function
H3	VSSPLL	GND	-	**Analog GND for PLL** Analog block, 1.8 V supply.
N1	VSSR	GND	-	**Analog GND for RX-Path** Analog block, 1.8 V supply.
K3	VSST	GND	-	**Analog Supply for ADC** Analog block, 1.8 V supply.

2.4 Pin and Signal Assignment in Different Modes

The name of the signal using a multiplexed pin depends on the mode of operation. The pin lists in this section show the signal assigned to each of these pins arranged within tables by function, and grouped into tables as follows:

- **Ethernet Interface Modes**
  - **"MII Modes" on Page 50**
  - **"RMII Modes" on Page 51**
  - **"Serial MII Slave Mode" on Page 52**
- **"Ethernet Serial Management Interface Modes" on Page 53**

2.4.1 Ethernet Interface Modes

This section shows the multiplexed pins used for signals in the following Ethernet interface modes:

- Media Independent Interface (MII): MAC – **Table 13** and PHY – **Table 14**
- Reduced Media Independent Interface (RMII): MAC – **Table 15** and PHY – **Table 16**
- Serial MII (SMII) interface: Typical – **Table 17** and Source Synchronous – **Table 18**

Ethernet interface modes include: Media Independent Interface (MII), Reduced Media Independent Interface (RMII) and Serial MII (SMII) modes.

2.4.1.1 MII Modes

Table 13 lists the MII MAC mode pins while Table 14 lists the MII PHY mode pins.

Table 13 MII MAC Mode Pins

Signal Name	Pin Name	Pin #	I/O	Function
COL	COLI	R11	I	**Collision Detected**
CRS	CRSI	N10	I	**Carrier Sense**
RXCLK	ECLK3	R13	I	**Reception Clock**
RXD0	ETHID0	R12	I	**Reception Data Input**
RXD1	ETHID1	M10	I	**Reception Data Input**
RXD2	ETHID2	P11	I	**Reception Data Input**
RXD3	ETHID3	M9	I	**Reception Data Input**
RXDV	ETHCTLI	P13	I	**Received Data Valid**
TXCLK	ECLK1	P12	I	**Transmission Clock**
TXD0	ETHOD0	L9	O	**Transmission Data** Configuration pin during hard reset.[1)]
TXD1	ETHOD1	M14	O	**Transmission Data** Configuration pin during hard reset.[1)]
TXD2	ETHOD2	M13	O	**Transmission Data** Configuration pin during hard reset.[1)]
TXD3	ETHOD3	N15	O	**Transmission Data** Configuration pin during hard reset.[1)]
TXEN	ETHCTLO	M12	O	**Transmission Enable**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

Table 14 MII PHY Mode Pins (page 1 of 2)

Signal Name	Pin Name	Pin #	I/O	Function
COL	COLO	P15	O	**Collision Detected** Configuration pin during hard reset.[1)]
CRS	CRSO	N14	O	**Carrier Sense**
PHYCLK	ECLK2	P10	I	**MII Source Clock**
RXCLK	ECLK1	P12	O	**Reception Clock**

Table 14 MII PHY Mode Pins (page 2 of 2)

Signal Name	Pin Name	Pin #	I/O	Function
RXD0	ETHOD0	L9	O	**Reception Data** Configuration pin during hard reset.[1)]
RXD1	ETHOD1	M14	O	**Reception Data** Configuration pin during hard reset.[1)]
RXD2	ETHOD2	M13	O	**Reception Data** Configuration pin during hard reset.[1)]
RXD3	ETHOD3	N15	O	**Reception Data** Configuration pin during hard reset.[1)]
RXDV	ETHCTLO	M12	O	**Received Data Valid**
TXCLK	ECLK3	R13	O	**Transmission Clock**
TXD0	ETHID0	R12	I	**Transmission Data**
TXD1	ETHID1	M10	I	**Transmission Data**
TXD2	ETHID2	P11	I	**Transmission Data**
TXD3	ETHID3	M9	I	**Transmission Data**
TXEN	ETHCTLI	P13	O	**Transmission Enable**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2.4.1.2 RMII Modes

The Reduced Media Independent Interface (RMII) provides a low pin-count interface for use between Ethernet PHYs and switch ASICs in high port density designs. MII uses 14 pins for data and control per port. RMII uses only six pins per port and one pin per switch ASIC. The interface can be configured to operate as a MAC or PHY device.

Table 15 RMII MAC Mode Pins (page 1 of 2)

Signal Name	Pin Name	Pin #	I/O	Function
REFCLK	ECLK1	P12	I	**Reference Clock**
RXD0	ETHID0	R12	I	**Reception Data Input**
RXD1	ETHID1	M10	I	**Reception Data Input**
RXDV	ETHCTLI	P13	I	**Received Data Valid**
TXD0	ETHOD0	L9	O	**Transmission Data Output** Configuration pin during hard reset.[1)]

Table 15 RMII MAC Mode Pins (page 2 of 2)

Signal Name	Pin Name	Pin #	I/O	Function
TXD1	ETHOD1	M14	O	**Transmission Data Output** Configuration pin during hard reset.[1)]
TXEN	ETHCTLO	M12	O	**Transmission Enable**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

Table 16 RMII PHY Mode Pins

Signal Name	Pin Name	Pin #	I/O	Function
REFCLK	ECLK1	P12	I	**Reference Clock**
RXD0	ETHOD0	L9	O	**Reception Data Output** Configuration pin during hard reset.[1)]
RXD1	ETHOD1	M14	O	**Reception Data Output** Configuration pin during hard reset.[1)]
RXDV	ETHCTLO	M12	O	**Received Data Valid**
TXD0	ETHID0	R12	I	**Transmission Data Input**
TXD1	ETHID1	M10	I	**Transmission Data Input**
TXEN	ETHCTLI	P13	I	**Transmission Enable**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2.4.1.3 Serial MII Slave Mode

Table 17 and **Table 18** shows the Serial MII (SMII) interface. SMII is a low pin count interface, like MII, with 1-bit wide data buses.

The pin descriptions are identical to MII pin descriptions with the following exceptions:

- The LSB of MII data buses TXD0 and RXD0 are used as SMII data buses.
- The TXD3:TXD1 and RXD3:RXD1 buses are not applicable in an SMII configuration.

Table 17 Typical SMII Mode Pins

Signal Name	Pin Name	Pin #	I/O	Description
RX	ETHOD0	L9	O	**Reception Data** Configuration pin during hard reset.[1)]
TX	ETHID0	R12	I	**Transmission Data**
REFCLK	ECLK1	P12	I	**Reference Clock**
TXSYNC	ETHCTLI	P13	I	**Transmission Synchronization**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

Table 18 Source Synchronous SMII Mode Pins

Signal Name	Pin Name	Pin #	I/O	Description
RX	ETHOD0	L9	O	**Reception Data** Configuration pin during hard reset.[1)]
RXCLK	MDCO	N12	O	**Reception Clock**
RXCLKREF	ECLK1	P12	I	**Reference Clock**
RXSYNC	ETHCTLO	M12	O	**Reception Synchronization**
RXSYNC_EN	UTID6	N9		**RXSYNC Synchronization Enable**
TX	ETHID0	R12	I	**Transmission Data**
TXCLK	ECLK3	R13	I	**Transmission Clock**
TXSYNC	ETHCTLI	P13	I	**Transmission Synchronization**

1) Pins that control configuration during hard reset must be pulled up or pushed down with resistors, as required. See **"Configuration Pins During Hard Reset" on Page 81** and reference design document for details.

2.4.2 Ethernet Serial Management Interface Modes

The Serial Management Interface (SMI) is available in all configurations. This section shows multiplexed pins used for signals in the following Serial Management Interface (SMI) modes:

- MAC – **Table 19**
- PHY – **Table 20**

Table 19 Serial Management Interface (SMI) Pins for MAC Modes

Signal Name	Pin Name	Pin #	I/O	Function
MDCO	MDCO	N12	O	**Serial Management Interface Clock**
MDIO	MDIO	L15	I/O	**Serial Management Interface Data**

Table 20 Serial Management Interface (SMI) Pins for PHY Modes

Signal Name	Pin Name	Pin #	I/O	Function
MDCI	MDCI	N11	I	**Serial Management Interface Clock**
MDIO	MDIO	L15	I/O	**Serial Management Interface Data**

3 Functional Overview

This section outlines the functional description of the components in the PEF 22827 and provides information on the JTAG Interface.

3.1 Digital Block - Functional Overview

The digital transceiver performs digital functions for the VDSL modem. These functions have been listed below according to the blocks contained in the main functional block diagram (see figure 4):

- Physical Medium Dependent (PMD) layer functions.
- Physical Medium Specific Transmission Convergence (PMS-TC) functions.
- Transport Protocol Specific Transmission Convergence (TPS-TC) functions .
- Network interface functions.

In the PMC-TC block, the digital functions are carried out by the following blocks:

- QAM Tx Modulator
- QAM Rx Demodulator
- AGC Controller
- Timing Recovery Unit
- Digital and Analog AFE Control Interface

TPS-TC protocol adapts the user application to the VDSL modem format. TPs-TC is implemented using the HDLC byte oriented framing. The interface in this block, includes the *x*MII Interfaces and MII (MAC and PHY).

For details see: **“Functional Description – Digital Block” on Page 58**

3.2 Analog Block - Functional Overview

The analog block performs digital-to-analog conversion (DAC) of the transmission data received from Digital Block. Also, the analog block performs analog-to digital conversion (ADC) of the received data and sends it to the digital block.

For details see, **“Functional Description – Analog Block” on Page 74**

3.3 Line Driver Block - Functional Overview

The new line driver amplifies the signal received from the analog block

For details see, **“Functional Description – Line Driver Block” on Page 80**

3.4 Functional Block Diagram

The block diagram in **Figure 4** shows the major functional blocks of the VDSL6100i Integrated VDSL Modem-on-Chip.

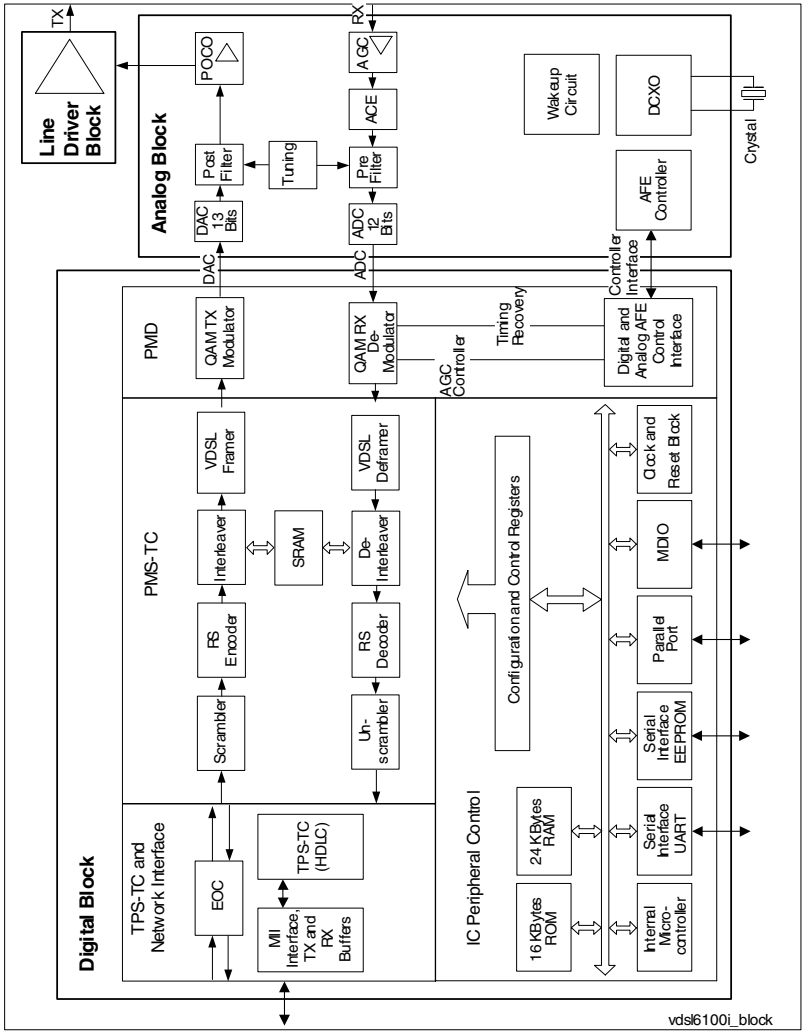


Figure 4 PEF 22827 Functional Block Diagram

3.5 JTAG Interface

The test logic consists of a boundary scan register and other building blocks, and is accessed through a Test Access Port (TAP). The TAP includes the TCK, TMS_A, TMS_D, TDI_A, TDI_D, TDO_A and TDO_D pins.

The Test Clock input pin (TCK) provides the clock for the test logic. The test logic at the Test Data Input (TDI_A and TDI_D) pins receives the serial test instructions and data. The Test Data Output (TDO_A and TDO_D) pins are the serial output pins for test instructions and data from the test logic. The data pins (TDI_A and TDO_D) ensure serial movement of test data through the circuit. See also, **“JTAG Interface (Boundary Scan)” on Page 134**.

The signals received at the Test Mode Select (TMS_A and TMS_D) input pins are decoded by the TAP controller to control test operations.

4 Functional Description – Digital Block

The digital transceiver performs digital functions for the VDSL modem. These functions have been listed below according to the blocks contained in the main functional block diagram (see figure 5):

- Physical Medium Dependent (PMD) layer functions.
- Physical Medium Specific Transmission Convergence (PMS-TC) functions.
- Transport Protocol Specific Transmission Convergence (TPS-TC) functions .
- Network interface functions.

In the PMC-TC block, the digital functions are carried out by the following blocks:

- QAM Tx Modulator
- QAM Rx Demodulator
- AGC Controller
- Timing Recovery Unit
- Digital and Analo AFE Control Interface

TPS-TC protocol adapts the user application to the VDSL modem format. TPs-TC is implemented using the HDLC byte oriented framing. The interface in this block, includes the *x*MII Interfaces and MII (MAC and PHY).

For a complete description of the Management interfaces, see **“JTAG Interface (Boundary Scan)” on Page 134**.

4.1 Functional Block Diagram – Digital Block

Figure 5 shows a detailed functional block diagram of the digital transceiver.

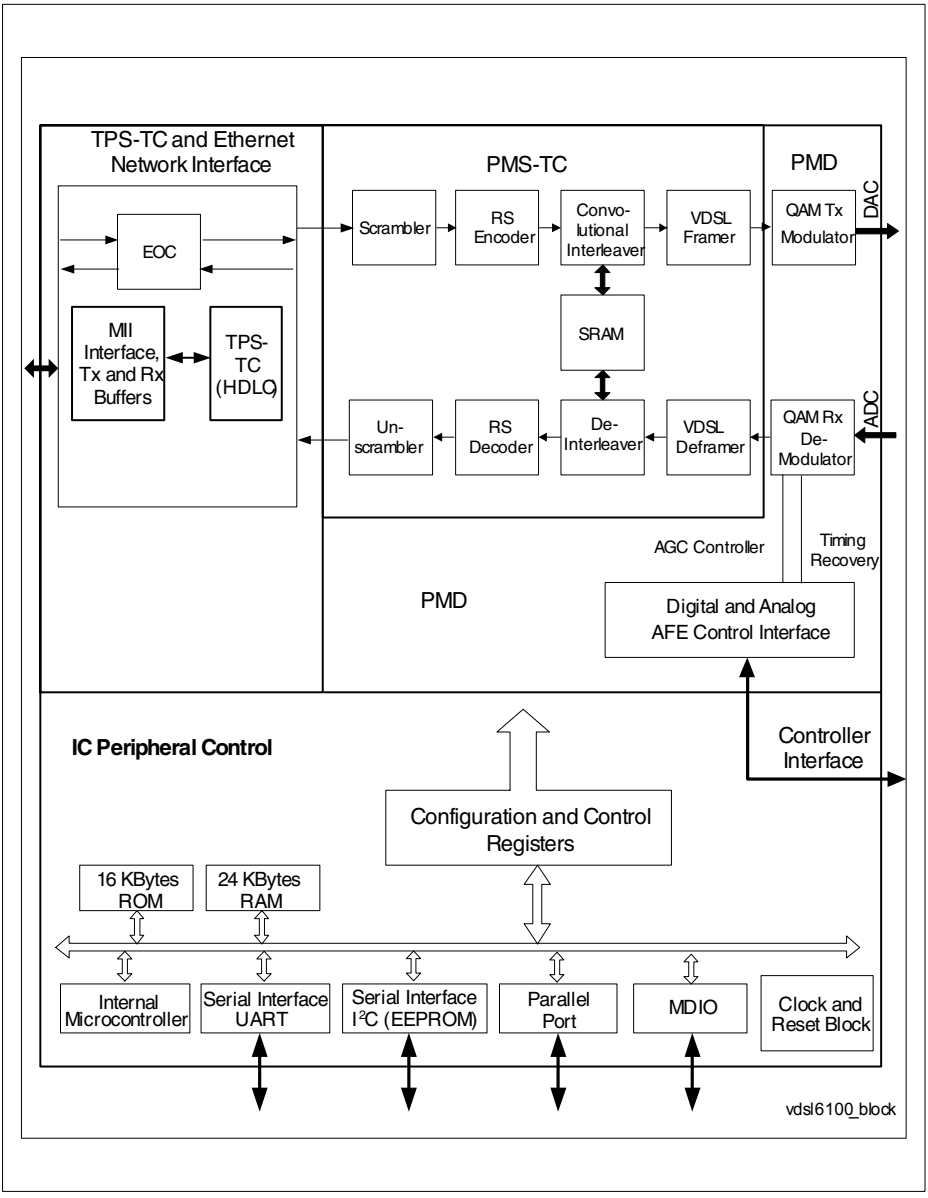


Figure 5 VDSL Digital Transceiver Functional Block Diagram

The detailed functional description of the digital transceiver is organized as shown below:

4.2 Firmware

The digital transceiver contains embedded micro controller and RAM. Firmware is loaded to the RAM during the boot process, immediately after power-on. For details, see **“Management and Control” on Page 72**.

Firmware supports 4-band functionality as described in the standards (see **“Terminology” on Page 292**), without backward compatibility for Infineon First Generation systems.

4.3 Physical Media Dependent (PMD) Layer

The Physical Media Dependent (PMD) layer consist of the Quadrature Amplitude Modulation (QAM) modem core and the interface to the analog block. The QAM modulator and demodulator in the modem core are described below:

4.3.1 QAM Modulator (Transmitter)

The QAM modulator receives two bit streams from the PMS-TC layer. It modulates the bit streams into two carriers, unifies the modulated carriers into one signal and transfers this signal to the DAC (Analog block) over a 13-bit bus at the rate of the 38.88 MHz system clock (25.92 MHz for 3-band applications with lower power consumption).

During transmission, the following processes are performed on both bit streams from the TC layer, in the following order:

1. Bit to symbol mapping. Supported constellations are QAM2 through QAM4096.
2. Interpolation of symbols to DAC sample rate.
3. Upward frequency conversion.
4. PSD shaping.
5. Filtering, including pulse shaping and notch insertion. (See**Table 21** and **Table 22**.)
6. Digital power adjustment.

To configure PMD layer parameters for Standard 4-band firmware, see **“Current and Target STPs” on Page 104**.

Notch filter registers insert a notch into the transmission frequency band. This prevents interference with other systems (amateur radio) that use narrow band transmission in the VDSL frequency band. **Table 21** and **Table 22** show standard values for notch filter registers for 38.88 MHz for different ham radio bands, and their locations in EEPROM.

Note: After changing values in EEPROM, issue a WR 8F00 02 command to apply the new values.

Table 21 ETSI Standard Values for Notch Registers, 38.88 MHz Clock[1)]

Notch Register Name	Ham Bands (MHz)							
	1.81 - 2.0 (DS1)		3.5 - 3.8 (US1)		7.0 - 7.1 (DS2)		10.1 - 10.15 (US2)	
	EEPROM Address - Value		EEPROM Address - Value		EEPROM Address - Value		EEPROM Address - Value	
NTCHA1_L	7816_H	$8C_H$	$781B_H$	CC_H	7820_H	$2B_H$	7825_H	$7A_H$
NTCHA2_L	7817_H	$8A_H$	$781C_H$	85_H	7821_H	$8A_H$	7826_H	$8C_H$
NTCHA_H	7818_H	59_H	$781D_H$	$4A_H$	7822_H	$5D_H$	7827_H	60_H
NTCHB_L	7819_H	$A7_H$	$781E_H$	$9D_H$	7823_H	$7A_H$	7828_H	$A3_H$
NTCHB_H	$781A_H$	04_H	$781F_H$	06_H	7824_H	04_H	7829_H	02_H

1) Based on common reference frequencies and amateur radio bands.

Table 22 ANSI Standard Values for Notch Registers, 38.88 MHz Clock[1)]

Notch Register Name	Ham Bands (MHz)							
	1.81 - 2.0 (DS1)		3.5 - 4 (US1)		7.0 - 7.3 (DS2)		10.1 - 10.15 (US2)	
	EEPROM Address - Value		EEPROM Address - Value		EEPROM Address - Value		EEPROM Address - Value	
NTCHA1_L	7816_H	$8C_H$	$781B_H$	$0D_H$	7820_H	50_H	7825_H	$7A_H$
NTCHA2_L	7817_H	$8A_H$	$781C_H$	08_H	7821_H	52_H	7826_H	$8C_H$
NTCHA_H	7818_H	59_H	$781D_H$	$4B_H$	7822_H	$5D_H$	7827_H	60_H
NTCHB_L	7819_H	$A7_H$	$781E_H$	AD_H	7823_H	26_H	7828_H	$A3_H$
NTCHB_H	$781A_H$	04_H	$781F_H$	07_H	7824_H	05_H	7829_H	02_H

1) Based on common reference frequencies and amateur radio bands.

4.3.2 QAM Demodulator (Receiver)

The QAM demodulator receives a sampled signal from the ADC in the analog block, demodulates the QAM symbols from the two modulated carriers and delivers the two bit streams to the TC layer.

The incoming signal from the analog block is delivered over a 12-bit bus at the rate of the 38.88 MHz system clock for 4-band standard-compliant applications. The incoming signal contains the two modulated received carriers.

The received modulated signal is split into two signals and the following processes are performed on both streams, in the order shown:

1. Digital AGC processing
2. Downward frequency conversion
3. Filtering
4. Decimation
5. Equalization
6. Symbol to bit mapping. Supported constellations are QAM-2 through QAM4096.

Demodulation also includes a timing recovery mechanism and an analog AGC control unit. The timing recovery mechanism in NT modems tracks timing and carrier frequencies. In VDSL, a single tracking mechanism tracks both timing and carrier frequency, which are both derived from the system clock.

The timing recovery mechanism in the digital transceiver tunes the system clock by programming the tuning register in the analog block through a serial control interface.

The digital transceiver also programs the analog AGC in the analog block through the serial control interface.

To configure PMD layer parameters, see **“Current and Target STPs” on Page 104**.

4.4 Physical Medium Specific Transmission Convergence (PMS-TC) Layer

PMS-TC layer is located between the Physical Media Dependent (PMD) and the Transport Protocol Specific Transmission Convergence (TPS-TC) layers. The PMS-TC layer supports transfer of slow and fast data channels, overhead channels and link control information.

To configure PMS-TC layer parameters for standard 4-band firmware, see **“Current and Target STPs” on Page 104**.

4.4.1 Transmission Path Tasks

In the transmission path, the PMS-TC layer does the following:

- **Scrambling**
- **Reed Solomon Encoding**

- Interleaving
- Construction of a Transmission Frame
- Splitting the Transmission Frame into PMD Frames

4.4.1.1 Scrambling

Before Reed Solomon (RS) encoding, a self-synchronizing algorithm scrambles (randomizes) the frame header (without the SYNC word), the payload on the fast channel and the payload on the slow channel, where OC is included in the payload of the slow channel. It scrambles each stream separately, using the algorithm in **Equation (1)**, regardless of the configuration (LT or NT).

$$D_{out}^{n} = D_{in}^{n} \oplus D_{out}^{n-18} \oplus D_{out}^{n-23} \quad (1)$$

4.4.1.2 Reed Solomon Encoding

Reed Solomon encoding adds FEC redundancy bytes to K original data bytes to create a code word with N bytes ($N > K$). The number of FEC (redundancy) bytes is the difference between the number of bytes in the code word and the number of data bytes ($N - K$).

The number of corrected bytes per Reed Solomon code word is half the number of FEC bytes or: $(N - K) / 2$, with truncation to the lower integer.

In the slow stream, the Reed Solomon code word (N,K) is $N = OC + PS + 16$ and $K = OC + PS$, where OC is 3 for the 3-byte operations channel field, PS is the number of payload bytes in the slow stream and 16 is the number of FEC bytes.

In the fast stream, the Reed Solomon code word (N,K) is $N = PF + RF$ and $K = PF$, where PF is the number of payload bytes in the fast stream and RF is the number of bytes in the Reed Solomon code word for the fast stream.

The slow channel and the fast channel are encoded separately. The fast channel encoder can be programmed.

4.4.1.3 Interleaving

Interleaving on the slow stream improves Reed Solomon error correction when there is pulse noise. Reed Solomon codes in the transmission frame of the slow stream are interleaved before transmission by a convolutional interleaver.

The interleaver parameters summarized in **Table 23** are:

- N = Slow Payload (PS) + 19 bytes.
- I = The interleaver block length in bytes. The number of bytes in each interleaver block is $N/8$ or $N/4$. Bytes within the interleaver blocks are numbered from 0 to $I - 1$.
- D = The interleaving depth, in bytes, controls the level of noise protection (erasure correction). $D - 1$ is the number of bytes that separate any two sequential bytes of

the same Reed Solomon code at the output of the interleaver. For all settings, $D - 1$ must be a multiple of the interleaver block length (I), as follows: $D = M * I + 1$, where M is any integer from 0 through 64.

- M = The interleaving depth index. M may be any integer from 0 through 64. If M is 0 there is no interleaving. The value of M for a given transmission profile may not provide erasure correction for more than 500 microseconds.
- E = Erasure correction in bytes. This is the maximum number of corrupted sequential bytes that can be corrected by the Reed Solomon algorithm during interleaving.

Note:

1. *The duration of noise pulses from which the system is protected is $E * .8 / R$, where E is erasure correction in bytes, and R is the bit rate of the transmitted signal.*
2. *A maximum of 24 Kbytes of memory is allocated for upstream and downstream interleaving combined. Before changing interleaver parameters, make sure that downstream plus upstream interleaving together will not require more than 24 Kbytes of memory. See Memory (MEM) in* ***Table 23****.*

Table 23 Interleaver Parameters

Parameter	Value (in Bytes)	Comments
Block Length (I)	N / 8 or N / 4	N = Slow Payload (PS) + 19 bytes
Depth (D)	$M * I + 1$	M is programmable to an integer 0 - 64
Erasure Correction (E)	$(t * I / N) * (M * I + 1)$	t = 8 (RS error correction ability)
End-to-End Delay (DL)	$M * I * (I - 1)$	
Memory (MEM)	$M * I * (I - 1) / 2$	

4.4.1.4 Construction of a Transmission Frame

After interleaving, for both upstream and downstream directions, a transmission frame is constructed that includes all information channels (fast, slow, OC and control). The transmission frame contains 405 bytes, a 5-byte header and a 400-byte payload, as shown in **Figure 6**.

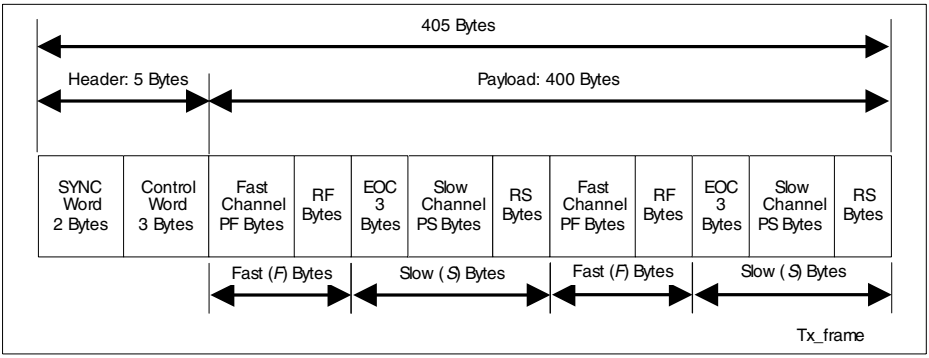


Figure 6 Transmission Frame Format

The payload of each transmission frame includes two fast channel fields and two slow channel fields, which are alternated, as shown in **Figure 6**.

Each fast channel field (F-bytes) transports one Reed Solomon code (RF), with no interleaving. Each slow channel field (S-bytes) transports one Reed Solomon (RS) code that passes through a convolutional interleaver before transmission to the line.

Both F and S are even and depend on the latency set during system configuration. For single latency, F = 0,S = 200. All bytes are transmitted MSB first. The MSB of the first transmitted frame byte corresponds to the beginning of the frame.

The header consists of a 2-byte SYNC word and a 3-byte Control field, as shown in **Table 24**. The Synchronization word contains frame alignment information. The Control field transfers the following delay sensitive synchronization, management and service information:

- Link activation support flags
- Far-end PMD layer defects or failures
- Far-end PMS-TC layer defects or failures
- Far-end TPS-TC layer defects or failures
- VTU-R power loss
- Bits reserved for future applications
- Bits reserved for proprietary purposes
- Header cyclic redundancy check (CRC) bits that enable Control field error detection.

In all header bytes, bit 0 is the MSB. Bit 0 of byte 0 is transmitted first.

Table 24 Transmission Frame Header

Byte	Name	Description	Value
0	SYNC 1	Synchronization word, byte 1.	
1	SYNC 2	Synchronization word, byte 2.	

Table 24 Transmission Frame Header

Byte	Name	Description	Value
2	Control 1	Control and management information, word 1.	Variable
3	Control 2	Control and management information, word 2.	
4	Control 3	Control and management information, word 3.	

The four CRC bits (CRC_1 to CRC_4) are stored in the Control 2 and Control 3 bytes. The CRC_1 bit holds the most significant bit of the remainder and the CRC_4 bit holds the least significant bit of the remainder.

Their combined value is computed as a remainder of the following expression:

$(m_0D^{23} + m_1D^{22} + \ldots + m^{23}) * D^4 / (D^4 + D + 1)$

where:

- The polynomial coefficient m_0 is the most significant bit (bit 0) of the Control 1 byte.
- m_{23} is the least significant bit (bit 7) of the Control 3 byte.
- $m_8, m_{15}, m_{16}, m_{23} = 0$

4.4.1.5 Splitting the Transmission Frame into PMD Frames

Before encoding, the Physical Media Dependent (PMD) framer generates two PMD frames, one for each band, from each transmission frame. This enables compensation for the propagation delay difference between the bands at the receiving end. The splitting procedure is the same for both the upstream and downstream bands.

PMD frames are independent of the band data rate. Each PMD frame consists of 405 bytes: a 2-byte SYNC word and a 403-byte data field. **Figure 7** shows how input transmission frames are mapped into PMD frames for both bands.

The framer maps input frames into two PMD frames to be transmitted by two bands at a data rate of N_1/N_2. Splitting starts from the first SYNC word (frame alignment) byte of an auxiliary input frame (Input Frame 1 in **Figure 7**). The SYNC word bytes from the input frame are inserted into the streams of both bands as their own SYNC word bytes. All SYNC words of subsequent input frames in the current splitting cycle are inverted.

The splitting process is cyclic. Each splitting cycle processes ($N_1 + N_2$) input frames. N_1 frames are mapped into band 1 and N_2 frames are mapped into band 2. For illustration purposes, in **Figure 7**, the first PMD frames of both bands are shown aligned with the SYNC word bytes of Input Frame 1.

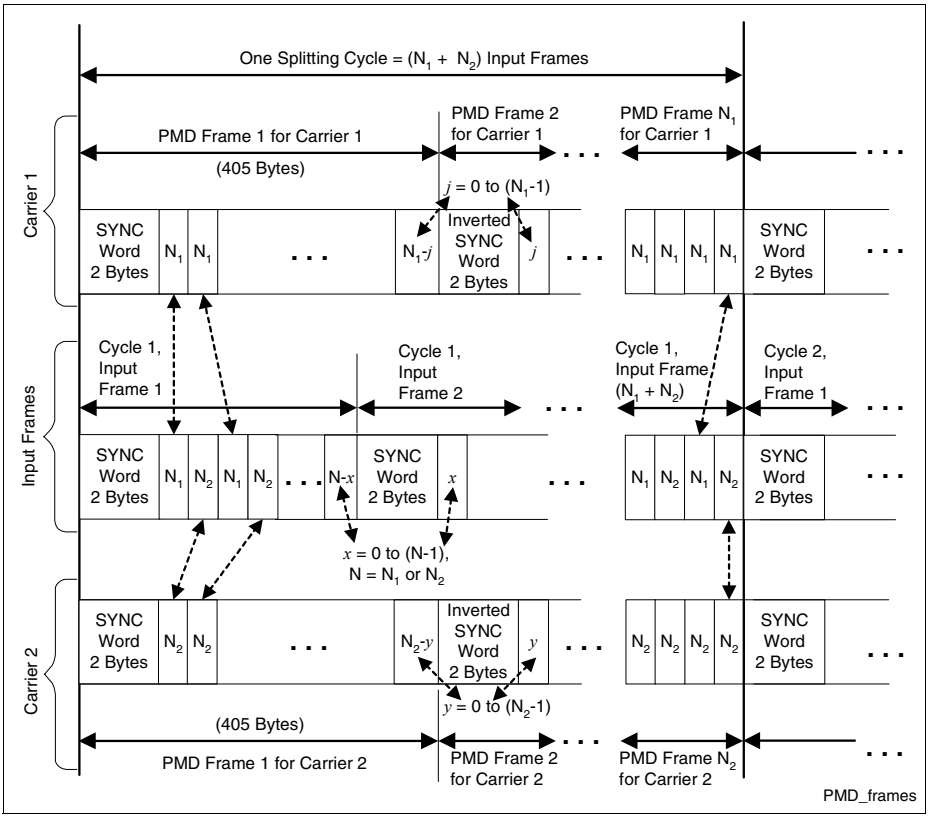


Figure 7 The Frame Splitting Cycle

4.4.2 Reception Path Tasks

In the reception path, the PMS-TC layer performs synchronization on the two PMD frames using a transmission frame delineation algorithm and a state machine that switches states upon detection of events in expected positions.

This state machine has three states, HUNT, PRESYNC and SYNC, which function as shown in **Figure 8** and as described below:

1. HUNT - In this state, the receiver compares bits in the SYNC word, one at a time. When a match is found, the state switches from HUNT to PRESYNC.

2. PRESYNC - In this state, the receiver verifies the match of bits in the SYNC word found during the HUNT and searches for a second consecutive match. If two consecutive matches are found, the state switches from PRESYNC to SYNC. If a second consecutive match is not found, the state returns to HUNT.
3. SYNC - After achieving synchronization, the receiver tracks the SYNC word, frame by frame, until six consecutive frames do not match. This causes the state machine to switch back from the SYNC state to the HUNT state.

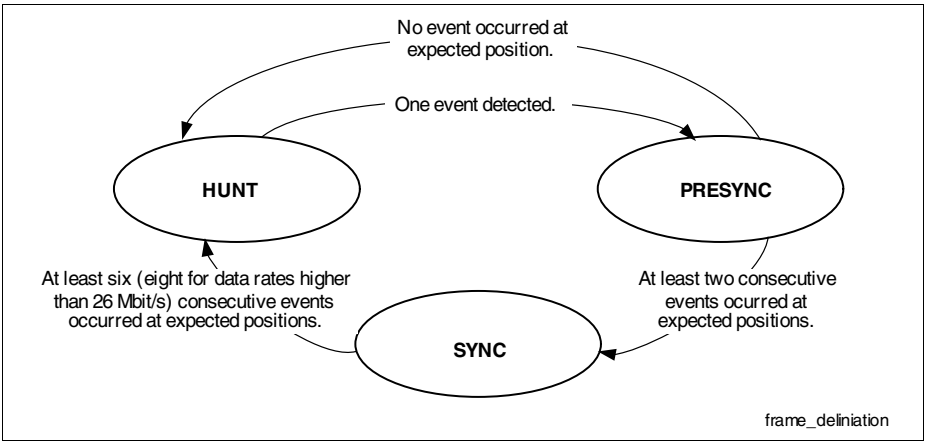


Figure 8 Transmission Frame Delineation State Machine

In the reception path, the PMS-TC layer also does the following:

- **Transmission Frame Construction from PMD Frames**
- **De-interleaving**
- **Reed Solomon Decoding**
- **Unscrambling**
- **Distribution of Data**

4.4.2.1 Transmission Frame Construction from PMD Frames

A single transmission frame is constructed from two PMD frames using a reverse of the process described in **“Splitting the Transmission Frame into PMD Frames” on Page 66**.

4.4.2.2 De-interleaving

The interleaving process described in **“Interleaving” on Page 63** is reversed for the slow stream.

4.4.2.3 Reed Solomon Decoding

Reed Solomon code words are decoded for both fast and slow streams. For more information on Reed Solomon code words, see **“Reed Solomon Encoding” on Page 63**.

4.4.2.4 Unscrambling

After Reed Solomon (RS) decoding, a self-synchronizing algorithm unscrambles the header, the payload on the fast channel and the payload on the slow channel. It unscrambles each stream separately, using following algorithm (the same algorithm that was used for scrambling), regardless of the configuration (LT or NT):

$$D_{out}^{n} = D_{in}^{n} \oplus D_{out}^{n-18} \oplus D_{out}^{n-23}$$

4.4.2.5 Distribution of Data

Information channels (fast, slow, OC and control) are distributed to the relevant modules.

4.5 Ethernet Network Interfaces and the TPS-TC Layer

Packet and data transfer supports Ethernet packets over the slow channel.

The digital transceiver can be configured as a 10 or 100 Mbit/s Ethernet PHY, so that it can interface to a standard 10 or 100 Mbit/s Ethernet MAC, or as a 10 or 100 Mbit/s Ethernet MAC, so that it can interface to a 10 or 100 Mbit/s Ethernet PHY.

The digital transceiver provides the following to support delivery of Ethernet packets:

- Ethernet encapsulation
- Bridging
- 802.3 MAC functionality
- *x*MII Interfaces (MII, RMII, SMII)
- Ethernet MIB support
- Speed and duplex adaptation

4.5.1 Ethernet Encapsulation

With Standard 4-band firmware, HDLC framing is used for encapsulation of Ethernet packets as required by the ITU-T standard G.993.1.

The HDLC block is connected to the slow channel. **Table 25** shows the contents of an HDLC frame.

Table 25 HDLC Frame Contents

Contents	Description
$7E_H$	Opening Flag Sequence
FF_H	Address Field
03_H	Control Field
Data	Information Field
FCS-1	First byte of HDLC_FCS
FCS-2	Second byte of HDLC_FCS
$7E_H$	Closing flag sequence

Data is transported in the information field of the Ethernet packet. This data includes everything from the Ethernet destination address through the Ethernet FCS.

During transmission, if a byte in the Ethernet packet is equal to $7E_H$ (the flag sequence) or $7D_H$ (the Control escape) the following occurs:

- $7E_H$ is replaced by two bytes containing the following sequence: $7D_H$ plus $5E_H$
- $7D_H$ is replaced by two bytes containing the following sequence: $7D_H$ plus $5D_H$

During reception, if a sequence of two bytes in the data contains $7D_H$ and $5E_H$ or $5D_H$, the following occurs:

- The $7D_H$ plus $5E_H$ sequence is replaced by one byte containing the value $7E_H$.
- The $7D_H$ plus $5D_H$ sequence is replaced by one byte containing the value $7D_H$.

4.5.2 Bridging

The following bridging mechanisms are provided:

- Packet buffers and a flow control mechanism between the ends of the VDSL channel, prevent loss of packets. Packet buffers (8 Kbyte transmission buffer and 16 Kbyte reception buffer) are located between the MII interface and the encapsulation block.
- Address filtering includes 32 unicast addresses, self learning for source addresses and automatic aging.
- Erroneous packets are discarded.

For details, see **“Network Interfaces” on Page 124**.

4.5.3 MAC Functions

The digital transceiver supports 802.3 MAC layer operation, regardless of the PHY or MAX configuration. In full duplex mode, it generates and accepts flow control frames . In half duplex mode, it supports back pressure and power back off (PBO) schemes.

For details, see **“Network Interfaces” on Page 124**.

4.5.4 MII Interface and Configuration

When configured as an Ethernet MAC, the digital transceiver can be connected to an Ethernet PHY through MII or RMII interfaces. In this case, the Serial Management Interface (SMI) provides access to the attached Ethernet PHY registers.

When configured as Ethernet PHY, the digital transceiver can be connected to an Ethernet MAC through MII, RMII or SMII interfaces. In this case, the digital transceiver contains an SMI interface and registers that allow any MAC or switch to control the digital transceiver through the interface.

MAC or PHY configuration only affects the MII interface when the clock direction is as expected.

For details, see **“Network Interfaces” on Page 124**.

4.5.5 MIB Support

Status registers and counters are provided to support Management Information Base (MIB) functionality.

For details, see **“Network Interfaces” on Page 124**.

4.5.6 Speed and Duplex Mode Adaptation

When configured as a MAC, the digital transceiver adapts speed and duplex mode by polling the attached Ethernet PHY. In PHY mode, the digital transceiver acts like an Ethernet PHY by supporting full standard SMI control and emulating auto negotiation.

4.5.7 Embedded Overhead Channel (EOC)

The digital transceiver supports an Embedded Overhead Channel (EOC) as specified in ETSI, ANSI and ITU standards.

The EOC provides a clear channel between the LT and NT for the exchange of system management data and traffic control. Data exchanged includes system-related primitives, performance parameters, test parameters and configuration and maintenance commands.

For a complete list, see the appropriate table in **Reference [2] on page 291**.

EOC traffic uses dedicated pins as described in **Table 4 "EOC and PCM Pins" on Page 42**.

The PMS-TC multiplexes external EOC traffic into the internal VOC stream. A special VOC opcode (FC_H) is used to carry the EOC data to the remote side (either NT or LT). There it is extracted from the PMS-TC frame and transmitted on the EOC pins to an external management entity.

4.6 Management and Control

In the digital transceiver, management and control are implemented by the following:

- Internal micro controller
- Management interfaces
- Configuration pins
- EEPROM
- JTAG

4.6.1 Internal Micro Controller

An 8-bit internal micro controller is used to control the processes in the digital transceiver. It establishes a user registers mechanism which the user can configure and control the digital transceiver.

The internal micro controller is connected to internal ROM (16 Kbytes) and internal RAM (24 Kbytes). ROM contains the kernel for carrying out the task of boot processing and management interface control. RAM contains the rest of the code, for the task of controlling the internal processes and user register management.

Firmware for the RAM can be loaded automatically from an EEPROM, or directly from the parallel UART or MDIO management interface.

Firmware is loaded to the RAM during the boot process immediately after power-on. At the conclusion of the boot process the digital transceiver enters normal operation mode.

4.6.2 User Registers

User registers enable the user to configure and control the digital transceiver. Some are accessible during the boot process, and all are accessible at the conclusion of the boot process. For more information, see **“The Boot Loop” on Page 99**.

4.6.3 Management Interfaces

The following management interfaces enable loading of firmware during the boot process and access to user registers:

- 8-bit Parallel Interface
- Serial Interface (UART)
- MDIO Serial Interface

Note: Use only one interface at a time.

See also, **“Management Interfaces” on Page 135**.

4.6.4 Configuration Pins

Several pins function as configuration pins in addition to their normal tasks. After power is turned ON, and before these pins assume their normal function, the value of the pins is sampled to determine the configuration.

Make sure that these pins are pulled down or up, as required, to define the required configuration. See also, **"Configuration Pins During Hard Reset" on Page 81**.

4.6.5 EEPROM

The digital transceiver can be connected directly to an EEPROM device through a standard serial I^2C interface. The digital transceiver supports both 32-Kbyte and 64-Kbyte EEPROMs.

The EEPROM holds firmware to be downloaded to RAM, and other initialization parameters. An EEPROM is usually included in NT systems in which a host processor is not used. In LT systems that have a host processor on board, the EEPROM is not required because firmware and other configuration parameters can be programmed from the host. See also, **"EEPROM" on Page 83**.

4.6.6 JTAG Interface

The test logic consists of a boundary scan register and other building blocks, and is accessed through a Test Access Port (TAP). The TAP includes the TCK, TMS_A, TMS_D, TDI_A, TDI_D, TDO_A and TDO_D pins.

The Test Clock input pin (TCK) provides the clock for the test logic. The test logic at the Test Data Input (TDI_A and TDI_D) pins receives the serial test instructions and data. The Test Data Output (TDO_A and TDO_D) pins are the serial output pins for test instructions and data from the test logic. The data pins (TDI_A and TDO_D) ensure serial movement of test data through the circuit. See **"JTAG Interface (Boundary Scan)" on Page 134**.

The signals received at the Test Mode Select (TMS_A and TMS_D) input pins are decoded by the TAP controller to control test operations.

5 Functional Description – Analog Block

The Analog Block of the PEF 22827 provides a filterless VDSL AFE (Analog Front End)[1], which is programmable under system control and modifiable through management commands. The AFE is connected to the External Adaptive Hybrid, which eliminates the requirement for transmission and receive filters.

The filterless AFE satisfies diverse requirements:

- Support for different band-plans
- Support for different PSDs with a single chip-set
- Support for different line throughputs

5.1 Classical AFE

The Infineon filterless AFE differs from a classical AFE. A classical AFE includes predefined fixed filters and a hybrid, which attenuate the echo noise to a minimum in order not to limit the SNR. Generally, echo noise has two sources:

- Echo signal in the transmission bands. This portion of the echo is attenuated by the hybrid and by the receive filter.
- Echo side-lobes, out-of-transmission-band (in-receive-band), generated by the non-linearity of the line-driver and analog circuitry. This portion of the echo is attenuated by the transmission filter and by the hybrid.

A classical AFE includes the following elements:

- Analog chip: Mainly converts analog signals to digital, and digital to analog. The chip includes ADC and DAC blocks.
- Internal Line driver: Drives the transmit signal according to specific PSD masks.
- Transmit and receive filters: Defined according to the band plan. Their main purpose is to overcome echo noise in the DSL modem. Echo noise is an inherent element in any DSL modem. Echo noise decreases the SNR (Signal to Noise Ratio) and thus limits the overall performance of a modem. Receive and transmit filters are passive and pre-defined. Such filters can not be used in regions that support a different band plan.
- Hybrid: Converts a single-pair loop into dual-pair circuitry, and vise versa. The hybrid should be perfectly matched to the line to avoid reflections of the transmission signal into the receive path (echo signal). Passive hybrids are matched to a pre-defined line impedance. However, line impedance varies from region to region, and within a region, due to bridge taps. Consequently, matching is not perfect and permits the presence of echo noise.

[1] It may be necessary to add additional external components to ensure best performance under any line conditions. Refer to the reference design guidelines.

5.2 Filterless AFE

The filterless AFE[1)] has no transmission and reception filters. Echo noise is eliminated by connecting to an External Adaptive Hybrid that automatically matches any line impedance and efficiently removes echo noise.

5.3 Functional Block Diagram – Analog Block

The Analog Block performs DAC on data received from the digital transceiver for transmission, and provides reconstruction filtering (through a Post Filter) and signal conditioning (through a Power Controller). The reception signal is amplified by the Automatic Gain Controller (AGC) and passed through an Analog Channel Equalizer (ACE). After anti-alias filtering (PREFI) the signal is converted to digital form. A control interface accesses registers. A digitally controlled crystal oscillator (DCXO) provides clock generation and timing recovery.

Figure 9 illustrates the major Analog Blocks. All analog signals are fully differential to reduce noise coupling.

1) It may be necessary to add additional external components to ensure best performance under any line conditions. Refer to the reference design guidelines.

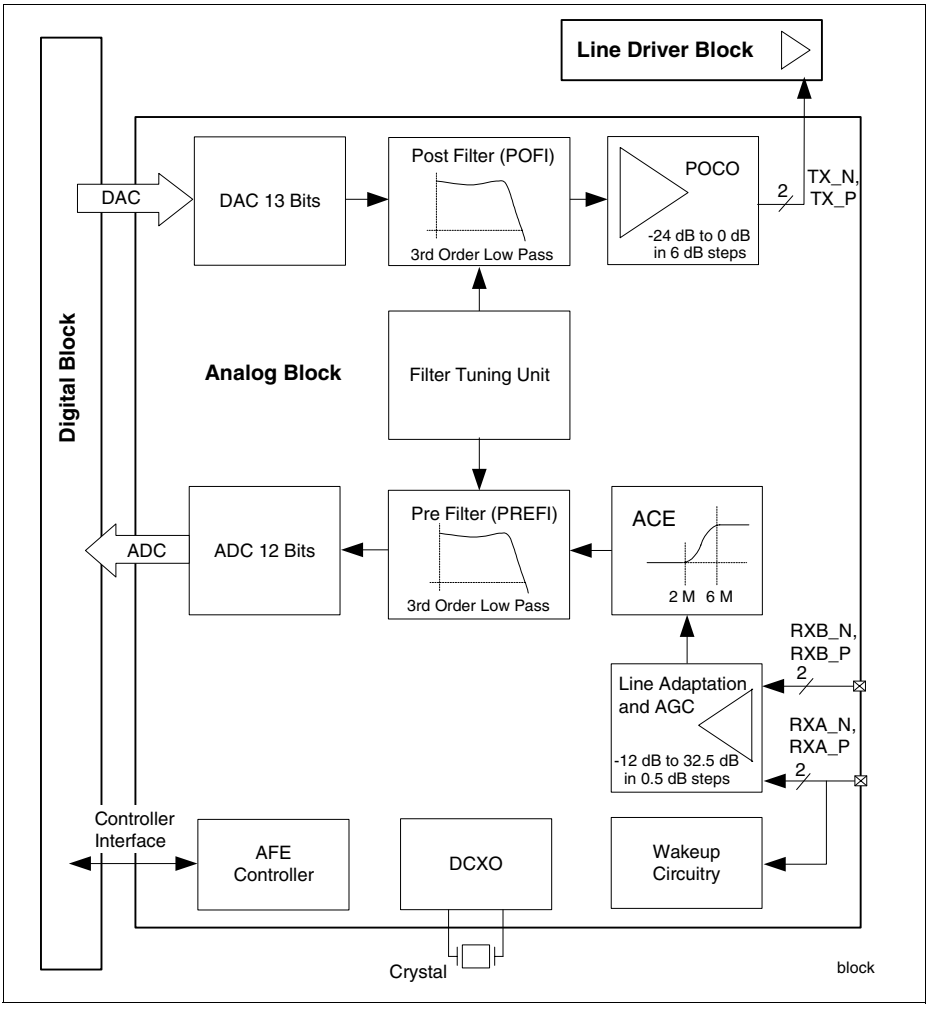


Figure 9 Functional Block Diagram - Analog Block

5.4 Filter Tuning Unit

PEF 22827 has a built-in filter tuning unit (**Figure 10**) to manage PREFI and POFI tuning. The filter mode depends on the crystal frequencies, available frequency bands, and available bit rates.

The digital block controls filter tuning in the AFE with the **FC_TUNE** ($0C_H$), **WAK_PLL_TUN_RF** ($0D_H$) and **XTAL_TUN_PAR** ($0F_H$) registers, as described here.

The tuning cycle for pre-filter and post-filter parameter adjustment is set by the digital block software.

A 0 to 1 transition of **TUNE_START** (bit 1 of the **FC_TUNE** register at $0C_H$) triggers a tuning cycle. The filter tuning unit measures the current filter time constant of a reference circuit (analog tuning measurement circuit) and adjusts the analog filter parameters accordingly. When the tuning process is finished, **TUNE_READY** (bit 5 of the **WAK_PLL_TUN_RF** register at $0D_H$) is set to 1.

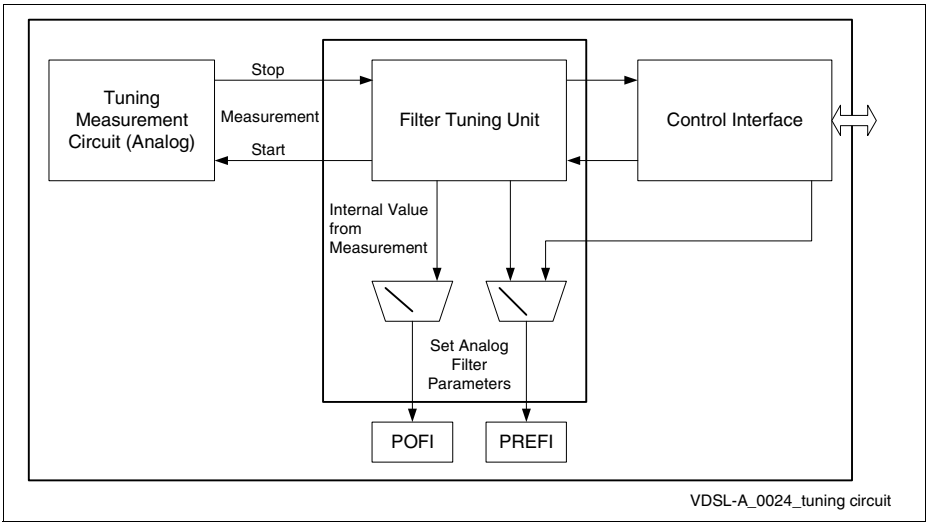


Figure 10 Filter Tuning Unit Functional Block Diagram

5.5 Transmission Path

The transmission path of the Analog Block includes a Digital-to-Analog Converter (DAC), a Post Filter (POFI) and a Power Controller (POCO). **Figure 9** illustrates the transmission path.

5.5.1 Digital-to-Analog Converter (DAC)

The DAC has a resolution of 13 bits (11 $bits_{eff}$) and an analog bandwidth of 12 MHz.

5.5.2 Post Tuning Filter (POFI)

The Post Tuning Filter (POFI) is a third order Chebyshev filter with a programmable corner frequency. See **“Corner Frequency and Tuning” on Page 261** for a complete description about programming the corner frequency. No external filter is required.

5.5.3 Power Controller

In order to comply with required PSD masks, a power control unit optimizes the transmission power. Furthermore, the digital transceiver’s PBO algorithm controls the power for different loop lengths. See **“Power Control” on Page 258** for a complete description about power control gain programming.

In the upstream direction, a VDSL modem located near the cabinet causes strong far end crosstalk (FEXT). In this case the power control unit and PBO mechanism may be used to reduce power in small increments. Power management functionality enables the modem to optimize power for balanced performance between the upstream and downstream transmissions while reducing FEXT between systems.

5.6 Receive Path

The receive path of the Analog Block includes an Automatic Gain Control (AGC) unit, a Prefilter (PREFI) and an Analog to Digital Converter (ADC) unit.

5.6.1 Automatic Gain Control (AGC)

The signal power at the ADC input depends on the transmission line length. The AGC adapts the signal to the ADC range. The digital transceiver’s internal processor controls the AGC circuit. The dynamic range of the AGC is from -12 to 32.5 dB in increments of 0.5 dB. See **“ACE, Measurement Buffer and AGC Mode” on Page 257** for detailed information about programming the AGC register.

5.6.2 Analog Channel Equalizer

The transmission channel attenuates higher frequencies more than lower frequencies. The analog channel equalizer raises the higher transmission frequencies to compensate for the receive signal.

5.6.3 Pre-Tuning Filter

The PREFI performs anti-aliasing for the modem and has the same characteristics as the post filter (POFI). See **“Post Tuning Filter (POFI)” on Page 78**.

5.6.4 Analog-to-Digital Converter (ADC)

The ADC has a resolution of 12 bits and an analog bandwidth of 12 MHz.

5.7 Clock Generation

When the VDSL system operates in *LT Mode* (master mode), either the internal crystal (DCXO) or an external clock can generate the master clock. If an external clock is used to generate the master clock, the external clock is connected instead of the crystal. In *NT mode* (Slave Mode) the clock frequency is derived from the receive signal.

On the LT side, the clock frequency is fixed. On the NT side the clock frequency is controlled by the DCXO within a timing recovery loop. The clock can be tuned in a range of ±120 ppm in increments of < 5 ppm.

The accuracy of the externally connected crystal or the external clock is ±50 ppm, as specified in the ETSI and ANSI standards. Depending on the desired system configuration, frequencies between 25 MHz and 38.88 MHz are possible. (See **“Operating Range – Analog Block” on Page 281**.)

5.8 Reset

All digital circuits are reset to zero or to their default state with the $\overline{\text{RESET}}$ signal. $\overline{\text{RESET}}$ is active low and has a circuit that prevents glitches. $\overline{\text{RESET}}$ should remain low for a minimum of 200 ns to generate a reset.

6 Functional Description – Line Driver Block

This section shows the block diagram of the internal line driver and describes Power Down mode.

6.1 Functional Block Diagram – Line Driver

The functional block diagram of line driver, located in the PEF 22827, is shown in Figure 11. The drivers AMP1 and AMP2 are implemented as current-feedback amplifiers. Main advantages of this topology are a high slew rate and the possibility to vary gain and bandwidth independently.

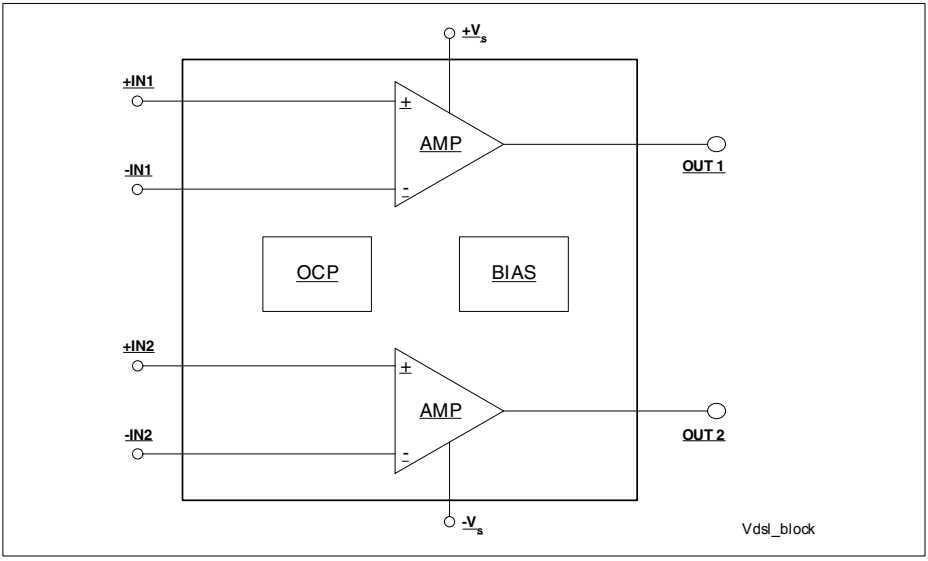


Figure 11 Functional Block Diagram

6.2 Power Down Mode

Use the PD pin to switch the line driver to a Power Down mode.

Table 26 Operating Mode Selection

Mode	V_{PD} (referred to $-V_S$)
Active Mode (ACT)[1)]	$V_{PD} < 0.7$ V
Power Down Mode (PDM)	$V_{PD} > 1.6$ V

1) If the PD pin is left floating, its input resistance pulls the pin down and the Active Mode is selected.

7 Operation – Digital Block

This chapter describes the digital block operations. The operations of the analog block are controlled in the digital block. Line driver block operations are described in **"Operation – Line Driver" on Page 132**.

Digital block operations are described below:

7.1 Configuration Pins During Hard Reset

Some pins are used as configuration pins, in addition to their normal tasks. During hard reset (until the $\overline{\text{RSTO}}$ signal becomes inactive high) these pins are configured as input pins. At the rising edge of $\overline{\text{RSTO}}$, these pins are sampled and used for configuration purposes. Immediately after reset, these pins assume their normal operation. During reset, the user must ensure that these pins are defined appropriately to produce the required configuration.

Table 27 lists the configuration pins and their settings. All pins must be pulled up or pushed down with resistors.

Table 27 Configuration Pins (page 1 of 2)

Normal Pin Name	Pin #	Configuration Pin Name	Settings for Configuration
PCM_TSYNC	J14	Reserved	Must be 0 during reset.
$\overline{\text{PCM\_TSIG}}$	J12	Reserved	Must be 1 during reset.
PCM_TDATA	J13	Reserved	Must be 1 during reset.
UTOD6	P14	Reserved	0_B SAR disabled. (Ethernet mode) 1_B SAR enabled.
EOC_TEN	D15	NT	0_B Work at LT side. 1_B Work at NT side.
EOC_TCLK	R8	EOC_TCLK	0_B No synthesized impedance. Standard VDSL mask used to determine PSD levels. 1_B Synthesized impedance. Firmware may boost PSD to levels defined by standard ADSL mask.

Table 27 Configuration Pins (page 2 of 2)

Normal Pin Name	Pin #	Configuration Pin Name	Settings for Configuration
EOC_TDATA EOC_RCLK EOC_RDATA EOC_REN	R9(MSB) P9 R10 K14(LSB)	DATA_IF	Data interface pins R9 (MSB),P9, R10 and K14 (LSB), in that order. Unused values are reserved. 0100_B MII MAC. 0101_B RMII MAC. 0110_B Typical SMII PHY. 1000_B TC layer parallel. 1100_B MII PHY. 1101_B RMII PHY. 1110_B Source Synchronous SMII PHY.
NTR	R7	CLKIN_FRQ	Frequency of CLKIN: 0_B 25.92 MHz 1_B 38.88 MHz (Standard)
COLO ETHOD3: ETHOD0	P15 N15, M13, M14, L9	PHY_ADD	PHY address for MDIO. Address pins P15 (MSB), N15, M13, M14, L9 (LSB), in that order.
EE_EN	R5	EEPROM_EN	0_B EEPROM is disabled. 1_B EEPROM is enabled.

7.2 System Clock

A crystal with the required typical frequency must be connected to the analog chip. An internal mechanism in the AFE provides capacitor switching that fine tunes the oscillation frequency along with the Digital Control Crystal Oscillator (DCXO). See **Figure 12**.

The analog chip exports the system clock to the digital transceiver through the CLKIN input signal. In NT systems, the digital transceiver tunes the frequency of the DCXO, through the serial AFE control interface, according to its timing recovery mechanism, which tracks the frequency and phase of the received signal.

In LT systems the frequency of the system clock is fixed; the digital chip programs the DCXO to a fixed value.

For standard compliant systems, connect a 38.88 MHz crystal to the AFE. For 3-band applications with lower power consumption applications, use a 25.92 MHz crystal. Configure the CLKIN_FRQ configuration pin accordingly.

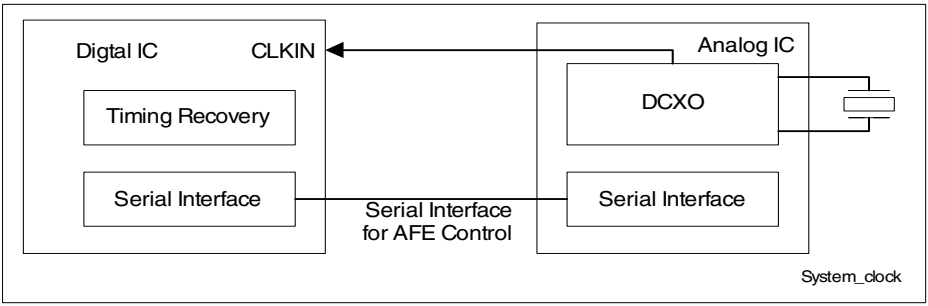


Figure 12 System Clock Generation

7.3 EEPROM

A 32-Kbyte or a 64-Kbyte EEPROM is supported. The 32-Kbyte EEPROM can hold one firmware version, with its parameters zone. The 64-Kbyte EEPROM can hold two firmware versions and a separate parameters zone for each.

Note: During firmware download with a 64-Kbyte EEPROM, it is recommended to download firmware to the currently inactive firmware bank. Then, after download finishes successfully, activate the downloaded firmware.

7.3.1 EEPROM Structure

The EEPROM includes the following zones (as shown in **Figure 13**) are described below:

- Header - See **"The EEPROM Header" on Page 84**.
- Two firmware banks - See **"Firmware Banks in EEPROM" on Page 85**.
- Two parameters zones, one dedicated for each firmware bank - See **"The Parameters Zones in EEPROM" on Page 85**.
- Reserved zones that are for internal use only.
- Spare zones that are not used and are available to the user. See **"Spare Zones" on Page 96**.

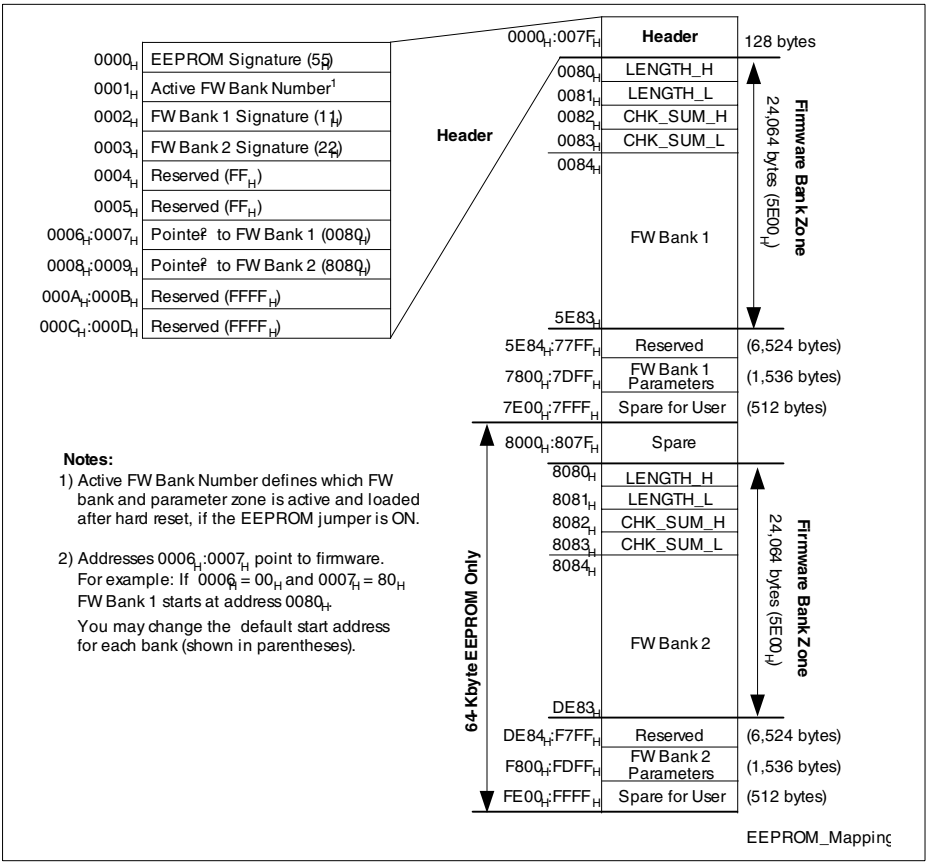


Figure 13 EEPROM Data Structure

7.3.1.1 The EEPROM Header

The EEPROM header holds the following information about the content of the EEPROM:

- EEPROM Signature (0000_H) - This field must be equal to 55_H to enable download from the EEPROM. When this field is not equal to 55_H, firmware is not downloaded from the EEPROM and configuration parameters are not updated from it.
- Active FW Bank Number (0001_H) - This field specifies the bank from which to download firmware. In a 64-Kbyte EEPROM, this field may have a value of 1_H or 2_H. In a 32-Kbyte EEPROM this field may have a value of 1_H only.

- FW Bank x Signature (0002_H for bank 1 and 0003_H for bank 2) - The bank is not used unless this field indicates that it is valid. Values of 11_H (FW Bank 1) and 22_H (FW Bank 2) indicate valid banks.
- Pointer to FW Bank 1 (0006_H:0007_H) or 2 (0008_H:0009_H) - The 2-byte pointer for each bank points to the address where the corresponding firmware bank begins. **Figure 13** shows the default address for the start of each bank.

7.3.1.2 Firmware Banks in EEPROM

Addresses 0080_H through $5E83_H$ (and 8080_H through $DE83_H$ for a 64-Kbyte EEPROM) are dedicated to firmware banks. Each area can hold one bank.

A firmware bank is a data block that contains:

- The code to be downloaded to RAM
- Two bytes that specify the length of the bank
- Two bytes that specify check sum of the bank (2's complement algorithm)

The maximum size of a firmware bank is $5E00_H$ or $24{,}064_D$ bytes.

7.3.1.3 The Parameters Zones in EEPROM

Two parameters zones (7800_H:$7DFF_H$ and $F800_H$:$FDFF_H$) are dedicated for storage of registers, STP parameters and profiles for Firmware Banks 1 and 2, respectively.

Note: Addresses in the parameters zone for Firmware Bank 2 are offset from the corresponding addresses in the parameters zone for Firmware Bank 1 by 8000_H.

The parameters zones are divided as follows (adresses for Firmware Bank 1 parameters shown first, followed by addresses for Firmware Bank 2 parameters):

- Parameter Signatures (7800_H, $F800_H$) - A value of 55_H is required to indicate valid parameter values. If any parameter value is not valid, clear the register containing the corresponding parameters signature to 00_H.
- STP signatures (7801_H, $F801_H$) - A value of 55_H is required to indicate a valid STP signature.
- Registers in the following groups:
  (See **Table 28 "Register Parameter Mapping in EEPROM" on Page 86**.)
  - 7802_H:7829_H, $F802_H$:$F829_H$ - Link mode, MII control and notch filter coefficient registers.
  - $7AD0_H$:$7AD4_H$, $FAD0_H$:$FAD4_H$ - PBO registers. See also, **"Power Back Off (PBO)" on Page 115**.
  - $7ADA_H$:$7B09_H$, $FADA_H$:$FB09_H$ - Rate Adaptive process registers. See also **"The Rate Adaptive Process" on Page 117**.
- WS_STP parameters (7861_H:$787F_H$, $F861_H$:$F87F_H$) - See **Table 29 "WS_STP Parameter Mapping in EEPROM" on page 89**.

- DF_STP1 (7880_H:$789E_H$, $F880_H$:$F89E_H$) and DF_STP2 parameters ($789F_H$:$78BD_H$, $F89F_H$:$F8BD_H$) - See **Table 30 "DF_STP1 and DF_STP2 Parameter Mapping in EEPROM" on page 92**.

Table 28 Register Parameter Mapping in EEPROM (page 1 of 4)

Address (Hex)		Parameter or Register Name	Description
Bank 1	**Bank 2**		
7802	F802	LINK_MODE	Link operation mode 1 (**$8F02_H$**)
7805	F805	MIICNTL	MII control (**$8D40_H$**)
7806	F806	BPCNTL1	MII back pressure control, register 1 (**$8D41_H$**)
7807	F807	BPCNTL2	MII back pressure control, register 2 (**$8D42_H$**)
7808	F808	BPCNTL3	MII back pressure control, register 3 (**$8D43_H$**)
7809	F809	FLOWCTL	Flow control (**$8D44_H$**)
780A	F80A	SRCADD	Pause packet source address (**$8D45_H$**)
780B	F80B	ADDTCTL	Address table control (**$8D46_H$**)
780C	F80C	AGTIMER	Aging timer (**$8D47_H$**)
780E	F80E	VP_INF_L	Vendor PHY SMI status information, L (**$8D4E_H$**)
780F	F80F	VP_INF_H	Vendor PHY SMI status information, H (**$8D4F_H$**)
7812	F812	PSDADJ	Adjust PSD output from board (**$8F0C_H$**)
7813	F813	ATTADJ	Adjust attenuation input to board (**$8F0D_H$**)
7814	F814	MAIN_MODE[3:0]	Bits 3:0 of MAIN_MODE at **$8F01_H$**
7816	F816	NTCHA1_L_DS1	Low byte of downstream notch filter coefficient NTCHA1 for 160 m (1.81 MHz - 2.0 MHz) LT operation on band 1.
7817	F817	NTCHA2_L_DS1	Low byte of downstream notch filter coefficient NTCHA2 for 160 m (1.81 MHz - 2.0 MHz) LT operation on band 1.
7818	F818	NTCHA_H_DS1	High four bits of downstream notch filter coefficients NTCHA1 and NTCHA2 for 160 m (1.81 MHz - 2.0 MHz) LT operation on band 1.
7819	F819	NTCHB_L_DS1	Low byte of downstream notch filter coefficient NTCHB for 160 m (1.81 MHz - 2.0 MHz) LT operation on band 1.
781A	F81A	NTCHB_H_DS1	Low byte of downstream notch filter coefficient NTCHA1 for 160 m (1.81 MHz - 2.0 MHz) LT operation on band 1.

Table 28 Register Parameter Mapping in EEPROM (page 2 of 4)

Address (Hex)		Parameter or Register Name	Description
Bank 1	Bank 2		
781B	F81B	NTCHA1_L_US1	Low byte of upstream notch filter coefficient NTCHA1 for 80 m (3.5 MHz - 3.8 MHz) NT operation on band 1.
781C	F81C	NTCHA2_L_US1	Low byte of upstream notch filter coefficient NTCHA2 for 80 m (3.5 MHz - 3.8 MHz) NT operation on band 1.
781D	F81D	NTCHA_H_US1	High four bits of upstream notch filter coefficients NTCHA1 and NTCHA2 for 80 m (3.5 MHz - 3.8 MHz) NT operation on band 1.
781E	F81E	NTCHB_L_US1	Low byte of upstream notch filter coefficient NTCHB for 80 m (3.5 MHz - 3.8 MHz) NT operation on band 1.
781F	F81F	NTCHB_H_US1	Low byte of upstream notch filter coefficient NTCHA1 for 80 m (3.5 MHz - 3.8 MHz) NT operation on band 1.
7820	F820	NTCHA1_L_DS2	Low byte of downstream notch filter coefficient NTCHA1 for 40 m (7.0 MHz - 7.1 MHz) LT operation on band 2.
7821	F821	NTCHA2_L_DS2	Low byte of downstream notch filter coefficient NTCHA2 for 40 m (7.0 MHz - 7.1 MHz) LT operation on band 2.
7822	F822	NTCHA_H_DS2	High four bits of downstream notch filter coefficients NTCHA1 and NTCHA2 for 40 m (7.0 MHz - 7.1 MHz) LT operation on band 2.
7823	F823	NTCHB_L_DS2	Low byte of downstream notch filter coefficient NTCHB for 40 m (7.0 MHz - 7.1 MHz) LT operation on band 2.
7824	F824	NTCHB_H_DS2	Low byte of downstream notch filter coefficient NTCHA1 for 40 m (7.0 MHz - 7.1 MHz) LT operation on band 2.
7825	F825	NTCHA1_L_US2	Low byte of upstream notch filter coefficient NTCHA1 for 30 m (10.1 MHz - 10.15 MHz) NT operation on band 2.

Table 28 Register Parameter Mapping in EEPROM (page 3 of 4)

Address (Hex)		Parameter or Register Name	Description
Bank 1	Bank 2		
7826	F826	NTCHA2_L_US2	Low byte of upstream notch filter coefficient NTCHA2 for 30 m (10.1 MHz - 10.15 MHz) NT operation on band 2.
7827	F827	NTCHA_H_US2	High four bits of upstream notch filter coefficients NTCHA1 and NTCHA2 for 30 m (10.1 MHz - 10.15 MHz) NT operation on band 2.
7828	F828	NTCHB_L_US2	Low byte of upstream notch filter coefficient NTCHB for 30 m (10.1 MHz - 10.15 MHz) NT operation on band 2.
7829	F829	NTCHB_H_US2	Low byte of upstream notch filter coefficient NTCHA1 for 30 m (10.1 MHz - 10.15 MHz) NT operation on band 2.
7AD0	FAD0	**PBO_K**	PBO K constant ($5B00_H$)
7AD1	FAD1	**PBO_US1D**	PBO US1 Distance ($5B01_H$)
7AD2	FAD2	**PBO_US2D**	PBO US2 Distance ($5B02_H$)
7AD3	FAD3	**PBO_MAXPSD**	PBO Maximum PSD ($5B03_H$)
7AD4	FAD4	**PBO_MINPSD**	PBO Minimum PSD ($5B04_H$)
7ADA	FADA	**RA_COMMAND**	Rate Adaptive Command ($5B10_H$)
7ADB	FADB	**RA_MN_MRG_D1**	RA Minimum Noise Margin for D1 ($5B11_H$)
7ADC	FADC	**RA_MN_MRG_D2**	RA Minimum Noise Margin for D2 ($5B12_H$)
7ADD	FADD	**RA_MN_MRG_U1**	RA Minimum Noise Margin for U1 ($5B13_H$)
7ADE	FADE	**RA_MN_MRG_U2**	RA Minimum Noise Margin for U2 ($5B14_H$)
7AE3: 7AE4	FAE3: FAE4	**RA_MX_RATE_DS**	RA Maximum Downstream Rate ($5B19_H$:$5B1A_H$)
7AE5: 7AE6	FAE5: FAE6	**RA_MX_RATE_US**	RA Maximum Upstream Rate ($5B1B_H$:$5B1C_H$)
7AE7: 7AE8	FAE7: FAE8	**RA_CF_D1**	RA Center Frequency (CF) for D1 ($5B1D_H$:$5B1E_H$)
7AE9: 7AEA	FAE9: FAEA	**RA_CF_D2**	RA Center Frequency (CF) for D2 ($5B1F_H$:$5B20_H$)
7AEB: 7AEC	FAEB: FAEC	**RA_CF_U1**	RA Center Frequency (CF) for U1 ($5B21_H$:$5B22_H$)

Table 28 Register Parameter Mapping in EEPROM (page 4 of 4)

Address (Hex)		Parameter or Register Name	Description
Bank 1	Bank 2		
7AED: 7AEE	FAED: FAEE	RA_CF_U2	RA Center Frequency (CF) for U2 ($5B23_H$:$5B24_H$)
7AEF	FAEF	RA_SR_D1	RA Symbol Rate (SR) for D1 ($5B25_H$)
7AF0	FAF0	RA_SR_D2	RA Symbol Rate (SR) for D2 ($5B26_H$)
7AF1	FAF1	RA_SR_U1	RA Symbol Rate (SR) for U1 ($5B27_H$)
7AF2	FAF2	RA_SR_U2	RA Symbol Rate (SR) for U2 ($5B28_H$)
7AF3	FAF3	RA_PSD_D1	RA Power Spectral Density (PSD) for D1 ($5B29_H$)
7AF4	FAF4	RA_PSD_D2	RA Power Spectral Density (PSD) for D2 ($5B2A_H$)
7AF5	FAF5	RA_PSD_U1	RA Power Spectral Density (PSD) for U1 ($5B2B_H$)
7AF6	FAF6	RA_PSD_U2	RA Power Spectral Density (PSD) for U2 ($5B2C_H$)
7AF7	FAF7	RA_PSD_MASK	RA Power Spectral Density (PSD) mask ($5B2D_H$)
7AF8	FAF8	RA_PSD_MAX	RA Power Spectral Density (PSD) max ($5B2E_H$)
7AF9	FAF9	RA_INTR_DS	Interleaver delay on the DS channel ($5B2F_H$)
7AFA	FAFA	RA_INTR_US	Interleaver delay on the US channel ($5B30_H$)

Table 29 WS_STP Parameter Mapping in EEPROM (page 1 of 3)

Address (Hex)		Parameter	Description
Bank 1	Bank 2		
7861	F861	CENTER_FREQ_DS1	2 bytes, MSB first. First downstream center frequency equals this value * 33.75 kHz
7863	F863	CENTER_FREQ_DS2	2 bytes, MSB first. Second downstream center frequency equals this value * 33.75 kHz
7865	F865	CENTER_FREQ_US1	2 bytes, MSB first. First upstream Center Frequency equals this value * 33.75 kHz
7867	F867	CENTER_FREQ_US2	2 bytes, MSB first. Second upstream center frequency equals this value * 33.75 kHz
7869	F869	CONSTELATION_DS1	This value is a power of 2 to define the first downstream QAM. QAM = $2^{CONSTELATION\_DS1}$

Table 29 WS_STP Parameter Mapping in EEPROM (page 2 of 3)

Address (Hex)		Parameter	Description
Bank 1	**Bank 2**		
786A	F86A	CONSTELATION_DS2	This value is a power of 2 to define the second downstream QAM. QAM = $2^{CONSTELATION\_DS2}$
786B	F86B	CONSTELATION_US1	This value is a power of 2 to define the first upstream QAM. QAM = $2^{CONSTELATION\_US1}$
786C	F86C	CONSTELATION_US2	This value is a power of 2 to define the second upstream QAM. QAM = $2^{CONSTELATION\_US2}$
786D	F86D	SYMBOL_RATE_DS1	First downstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
786E	F86E	SYMBOL_RATE_DS2	Second downstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
786F	F86F	SYMBOL_RATE_US1	First upstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
7870	F870	SYMBOL_RATE_US2	Second upstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
7871	F871	PSD_LEVEL_DS1	First linear downstream PSD level.
7872	F872	PSD_LEVEL_DS2	Second linear downstream PSD level.
7873	F873	PSD_LEVEL_US1	First linear upstream PSD level.
7874	F874	PSD_LEVEL_US2	Second linear upstream PSD level.
7875	F875	PSD_MASK	Notch control for a direction and carrier. One notch per band supported, with bits 7:4 reserved and: Bit 3: notch on US2 at the NT, 10.1 - 10.15 MHz. Bit 2: notch on DS2 at the LT, 7.0 - 7.1 MHz. Bit 1: notch on US1 at the NT, 3.5 - 3.8 MHz. Bit 0: notch on DS1 at the LT, 1.81 - 2.0 MHz.
7876	F876	Reserved	Reserved
7877	F877	INTERLEAVER_M_DS	Range 0:64. 0 = Interleaver OFF downstream.
7878	F878	INTERLEAVER_M_US	Range 0:64. 0 = Interleaver OFF upstream.

Table 29 WS_STP Parameter Mapping in EEPROM (page 3 of 3)

Address (Hex)		Parameter	Description
Bank 1	**Bank 2**		
7879	F879	INTERLEAVER_I	Denominator for calculating interleaver block length, where: Bit 1 is for upstream, and 0 = 4, 1= 8 Bit 0 is for downstream, and 0 = 4, 1= 8 See **"Interleaving" on Page 63** for details.
787A	F87A	FAST_SIZE_DS	Length of downstream fast channel, in bytes.
787B	F87B	FAST_SIZE_US	Length of upstream fast channel, in bytes.
787C	F87C	FFEC_SIZE_LT	Bits 7:4 specify upstream reception FFEC. Bits 3:0 specify upstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
787D	F87D	FFEC_SIZE_NT	For Bits 7:4 specify downstream reception FFEC. Bits 3:0 specify downstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
787E	F87E	SFEC_SIZE_LT	Bits 7:4 specify upstream reception SFEC. Bits 3:0 specify upstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
787F	F87F	SFEC_SIZE_NT	Bits 7:4 specify downstream reception SFEC. Bits 3:0 specify downstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*

In Table 29, (1) indicates the parameter zone for Firmware Bank 1 and (2) indicates the parameter zone for Firmware Bank 2.

Table 30 DF_STP1 and DF_STP2 Parameter Mapping in EEPROM (page 1 of 3)

Address (Hex) [1]		Parameter	Description
DF_STP1	**DF_STP2**		
7880_H (1) $F880_H$ (2)	$789F_H$ (1) $F89F_H$ (2)	CENTER_FREQ_DS1	2 bytes, MSB first. First downstream center frequency equals this value ∗ 33.75 kHz
7882_H (1) $F882_H$ (2)	$78A1_H$ (1) $F8A1_H$ (2)	CENTER_FREQ_DS2	2 bytes, MSB first. Second downstream center frequency equals this value ∗ 33.75 kHz
7884_H (1) $F884_H$ (2)	$78A3_H$ (1) $F8A3_H$ (2)	CENTER_FREQ_US1	2 bytes, MSB first. First upstream Center Frequency equals this value ∗ 33.75 kHz
7886_H (1) $F886_H$ (2)	$78A5_H$ (1) $F8A5_H$ (2)	CENTER_FREQ_US2	2 bytes, MSB first. Second upstream center frequency equals this value ∗ 33.75 kHz
7888_H (1) $F888_H$ (2)	$78A7_H$ (1) $F8A7_H$ (2)	CONSTELATION_DS1	This value is a power of 2 to define the first downstream QAM. QAM = $2^{CONSTELATION\_DS1}$
7889_H (1) $F889_H$ (2)	$78A8_H$ (1) $F8A8_H$ (2)	CONSTELATION_DS2	This value is a power of 2 to define the second downstream QAM. QAM = $2^{CONSTELATION\_DS2}$
$788A_H$ (1) $F88A_H$ (2)	$78A9_H$ (1) $F8A9_H$ (2)	CONSTELATION_US1	This value is a power of 2 to define the first upstream QAM. QAM = $2^{CONSTELATION\_US1}$
$788B_H$ (1) $F88B_H$ (2)	$78AA_H$ (1) $F8AA_H$ (2)	CONSTELATION_US2	This value is a power of 2 to define the second upstream QAM. QAM = $2^{CONSTELATION\_US2}$
$788C_H$ (1) $F88C_H$ (2)	$78AB_H$ (1) $F8AB_H$ (2)	SYMBOL_RATE_DS1	First downstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
$788D_H$ (1) $F88D_H$ (2)	$78AC_H$ (1) $F8AC_H$ (2)	SYMBOL_RATE_DS2	Second downstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
$788E_H$ (1) $F88E_H$ (2)	$78AD_H$ (1) $F8AD_H$ (2)	SYMBOL_RATE_US1	First upstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.
$788F_H$ (1) $F88F_H$ (2)	$78AE_H$ (1) $F8AE_H$ (2)	SYMBOL_RATE_US2	Second upstream symbol rate = this value ∗ 67.5 kHz. 0 = disabled.

Table 30 DF_STP1 and DF_STP2 Parameter Mapping in EEPROM (page 2 of 3)

Address (Hex) [1]		Parameter	Description
DF_STP1	**DF_STP2**		
7890_H (1) $F890_H$ (2)	$78AF_H$ (1) $F8AF_H$ (2)	PSD_LEVEL_DS1	First linear downstream PSD level.
7891_H (1) $F891_H$ (2)	$78B0_H$ (1) $F8B0_H$ (2)	PSD_LEVEL_DS2	Second linear downstream PSD level.
7892_H (1) $F892_H$ (2)	$78B1_H$ (1) $F8B1_H$ (2)	PSD_LEVEL_US1	First linear upstream PSD level.
7893_H (1) $F893_H$ (2)	78B2 (1) $F8B2_H$ (2)	PSD_LEVEL_US2	Second linear upstream PSD level.
7894_H (1) $F894_H$ (2)	$78B3_H$ (1) $F8B3_H$ (2)	PSD_MASK	Notch control for a direction and carrier. One notch per band supported, with bits 7:4 reserved and: Bit 3: notch on US2 at the NT, 10.1 - 10.15 MHz. Bit 2: notch on DS2 at the LT, 7.0 - 7.1 MHz. Bit 1: notch on US1 at the NT, 3.5 - 3.8 MHz. Bit 0: notch on DS1 at the LT, 1.81 - 2.0 MHz.
7895_H (1) $F895_H$ (2)	$78B4_H$ (1) $F8B4_H$ (2)	Reserved	Reserved
7896_H (1) $F896_H$ (2)	$78B5_H$ (1) $F8B5_H$ (2)	INTERLEAVER_M_DS	Range 0:64. 0 = Interleaver OFF.
7897_H (1) $F897_H$ (2)	7897_H (1) $F897_H$ (2)	INTERLEAVER_M_US	Range 0:64. 0 = Interleaver OFF.
7898_H (1) $F898_H$ (2)	$78B7_H$ (1) $F8B7_H$ (2)	INTERLEAVER_I	Denominator for calculating interleaver block length, where: Bit 1 is for upstream, and 0 = 4, 1= 8 Bit 0 is for downstream, and 0 = 4, 1= 8 See **“Interleaving” on Page 63** for details.
7899_H (1) 7899_H (2)	$78B8_H$ (1) $78B8_H$ (2)	FAST_SIZE_DS	Length of DS fast channel, in bytes.
$789A_H$ (1) $789A_H$ (2)	$78B9_H$ (1) $78B9_H$ (2)	FAST_SIZE_US	Length of US fast channel, in bytes.

Table 30 DF_STP1 and DF_STP2 Parameter Mapping in EEPROM (page 3 of 3)

Address (Hex) [1]		Parameter	Description
DF_STP1	DF_STP2		
$789B_H$ (1) $789B_H$ (2)	$78BA_H$ (1) $78BA_H$ (2)	FFEC_SIZE_LT	Bits 7:4 specify US reception FFEC. Bits 3:0 specify US transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
$789C_H$ (1) $789C_H$ (2)	$78BB_H$ (1) $78BB_H$ (2)	FFEC_SIZE_NT	Bits 7:4 specify DS reception FFEC. Bits 3:0 specify DS transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
$789D_H$ (1) $789D_H$ (2)	$78BC_H$ (1) $78BC_H$ (2)	SFEC_SIZE_LT	Bits 7:4 specify US reception SFEC. Bits 3:0 specify US transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
$789E_H$ (1) $789E_H$ (2)	$78BD_H$ (1) $78BD_H$ (2)	SFEC_SIZE_NT	Bits 7:4 specify DS reception SFEC. Bits 3:0 specify DS transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*

[1] (1) indicates the parameter zone for Firmware Bank 1 and (2) the parameter zone for Firmware Bank 2.

Table 31 provides the values of DF_STP1.

Table 31 DF_STP1 Parameter Values in EEPROM

Parameter	Value
CENTER_FREQ_DS1	0038_H
CENTER_FREQ_DS2	$00CC_H$
CENTER_FREQ_US1	0084_H
CENTER_FREQ_US2	0138_H
CONSTELATION_DS1	02_H
CONSTELATION_DS2	02_H
CONSTELATION_US1	02_H
CONSTELATION_US2	02_H
SYMBOL_RATE_DS1	$0A_H$
SYMBOL_RATE_DS2	00_H
SYMBOL_RATE_US1	$0B_H$
SYMBOL_RATE_US2	00_H
PSD_LEVEL_DS1	$A0_H$
PSD_LEVEL_DS2	$A0_H$
PSD_LEVEL_US1	$A0_H$
PSD_LEVEL_US2	$A0_H$
PSD_MASK	00_H
INTERLEAVER_M_DS	00_H
INTERLEAVER_M_US	00_H
INTERLEAVER_I	03_H
FAST_SIZE_DS	00_H
FAST_SIZE_US	00_H
FFEC_SIZE_LT	88_H
FFEC_SIZE_NT	88_H
SFEC_SIZE_LT	88_H
SFEC_SIZE_NT	88_H

Table 32 provides the values of DF_STP2.

Table 32 DF_STP2 Parameter Values in EEPROM

Parameter	Value
CENTER_FREQ_DS1	$000D_H$
CENTER_FREQ_DS2	0000_H
CENTER_FREQ_US1	0001_H
CENTER_FREQ_US2	0000_H
CONSTELATION_DS1	02_H
CONSTELATION_DS2	02_H
CONSTELATION_US1	02_H
CONSTELATION_US2	02_H
SYMBOL_RATE_DS1	04_H
SYMBOL_RATE_DS2	00_H
SYMBOL_RATE_US1	01_H
SYMBOL_RATE_US2	00_H
PSD_LEVEL_DS1	$C9_H$
PSD_LEVEL_DS2	$A0_H$
PSD_LEVEL_US1	$A0_H$
PSD_LEVEL_US2	$A0_H$
PSD_MASK	00_H
INTERLEAVER_M_DS	00_H
INTERLEAVER_M_US	00_H
INTERLEAVER_I	03_H
FAST_SIZE_DS	00_H
FAST_SIZE_US	00_H
FFEC_SIZE_LT	88_H
FFEC_SIZE_NT	88_H
SFEC_SIZE_LT	88_H
SFEC_SIZE_NT	88_H

7.3.1.4 Spare Zones

Spare zones are not used by the digital transceiver, and can be used for private purposes. In a 32-Kbyte EEPROM, the spare zone is at $7F00_H$:$7FFF_H$. In a 64-Kbyte EEPROM, there is an additional spare zone at $FF00_H$:$FFFF_H$.

7.3.2 Accessing EEPROM

Access EEPROM for read and write operations through a set of user registers.

After firmware is loaded to EEPROM, if the write protect pin of the EEPROM is connected correctly to the digital transceiver, the EEPROM is automatically write protected. For connection instructions and to enable or disable this mechanism, refer to the Reference Design and the API documents.

7.3.2.1 Writing to EEPROM

To write to the EEPROM, disable EEPROM write protection and do the following:

1. Write the EEPROM address into the EEP_ADDR register from $5F70_H$ through $5F71_H$.
2. Write the number of data bytes to write into the EEP_LENGTH register at $5F72_H$. The maximum length is 128 bytes for a 64-Kbyte EEPROM, and 64 bytes for 32-Kbyte EEPROM.
3. Load the data into the EEP_DATA register, from address $5F74_H$ through $5FF3_H$.
4. Write the checksum byte into the EEP_CHKSUM register at $5F73_H$. The value of the checksum should be the 2's complement of the arithmetic sum of EEP_ADDR, EEP_LENGTH and the written EEP_DATA data.
5. Write the appropriate value into the EEP_COMMAND register at $5FF6_H$. See **"EEP_COMMAND" on Page 213**.
6. Poll the EEP_COMMAND register until it shows 00_H (no operation), which indicates that the write operation is finished and the EEP_STATUS register is valid.
7. Read the EEP_STATUS register at $5FF7_H$. The value of EEP_STATUS shows if the operation succeeded or failed, and the reason for failure. See **"EEP_STATUS" on Page 213** for a description of all possible EEP_STATUS values.

7.3.2.2 Reading from EEPROM

To read from the EEPROM, carry out the following steps:

1. Write the EEPROM address into the EEP_ADDR register from $5F70_H$ through $5F71_H$.
2. Write the number of data bytes to read into the EEP_LENGTH register at $5F72_H$. The maximum length is 128 bytes for a 64-Kbyte EEPROM, and 64 bytes for 32-Kbyte EEPROM.
3. Write 04_H to the EEP_COMMAND register at $5FF6_H$.
4. Poll the EEP_COMMAND register until it shows 00_H (no operation), which indicates that the read operation is finished and the EEP_STATUS register is valid.
5. Read the EEP_STATUS register at $5FF7_H$. The value of EEP_STATUS shows if the operation succeeded or failed, and the reason for failure. See **"EEP_STATUS" on Page 213** for a description of all possible EEP_STATUS values.
6. If the operation succeeded, read data from the **EEP_DATA** register, starting from address $5F74_H$.

7.4 Internal RAM Management

The internal micro controller is connected to an internal 24-Kbyte RAM, which holds both code and data. This RAM is mapped to addresses 2000_H through $7FFF_H$, with code stored in the following addresses:

- 2000_H:$5AFF_H$
- 6000_H:$7DFF_H$

Data is stored in addresses:

- $5B00_H$:$5FFF_H$
- $7E00_H$:$7FFF_H$

Full read and write access to both code and data in the RAM is enabled during the boot loop (see **"The Boot Loop" on Page 99**). During normal operation, read and write operation are valid in data segments only. Write access to code is denied.

A checksum mechanism automatically calculates the checksum for a specified area in RAM. This mechanism can be used to verify that firmware was downloaded correctly. It can be used during the boot loop or during normal operation.

The checksum mechanism is activated through user registers. To check a specific area in RAM, do the following:

1. Write the requested start address into the **RAM_ADDR** register from $5F67_H$ through $5F68_H$.
2. Write the size (number of bytes) in the block to check to the **RAM_LENGTH** register from $5F69_H$ through $5F6A_H$.
3. Write the expected checksum value to the **RAM_CHKSUM** register from $5F6B_H$ through $5F6C_H$. The value of the expected checksum should be the 2's complement of the arithmetic sum of all the bytes in the block.
4. Write 02_H (run checksum process) or 03_H (run checksum process, and if successful go to normal operation) to the **RAM_CMD_STS** register at $5F6D_H$. See **"RAM_ADDR" on Page 208** for a description of all possible values.
5. Poll the **RAM_CMD_STS** register until its value is 00_H (expected checksum was correct) or 01_H (expected checksum not correct).

7.5 The Boot Process

After hard reset, the digital transceiver automatically starts the boot process in which firmware is downloaded to RAM from EEPROM, provided that the firmware exists in EEPROM and is valid.

If there is no valid firmware in EEPROM, the digital transceiver enters the boot loop. During the boot loop, firmware may be downloaded to RAM through one of the management interfaces or from the remote modem (from the LT to the NT). See **"The Boot Loop" on Page 99**.

7.5.1 Firmware Download from EEPROM

Firmware download takes up to three seconds. After it is finishes, the digital transceiver does one of the following:

- If firmware download was successful, normal operation begins.
- If firmware download is not successful, the digital transceiver enters a boot loop within a few milliseconds. During the loop the user can manually download firmware to RAM or write data to the EEPROM.

To determine whether or not firmware download succeeded, read the **FW_DLOAD** register ($5F6F_H$).

- If the FW_DLOAD register is set to 01_H, firmware download succeeded and normal operation has begun.
- If this register is cleared to 00_H, firmware download failed and the digital transceiver is in a boot loop.

Firmware download from EEPROM fails in the following cases:

- The EEPROM is not enabled; that is, the EEPROM_EN configuration pin is not set to 1. See **Table 27 “Configuration Pins” on Page 81**.
- The EEPROM is not valid; that is, the EEPROM Valid field in the EEPROM is not 55_H.
- There is no valid FW bank in the EEPROM.
- The checksum content of the valid FW bank is not correct.
- There is an electrical problem in the EEPROM or in the I^2C lines.

See **“EEPROM Structure” on Page 83** for more information about these problems.

7.5.2 The Boot Loop

The boot loop enables firmware download to the RAM through the parallel interface or the MDIO interface, or from the remote modem. During the boot loop, you can also load the EEPROM. This allows system vendors to write content to the EEPROM on the board, after board assembly.

The digital transceiver exits from the boot loop and enters normal operation as soon as the firmware is loaded and the **FW_DLOAD** register at $5F6F_H$ is set to 01_H.

During the boot loop, only the following user registers are supported:

- **“Version Status Registers” on Page 205**: addresses $5F62_H$:$5F65_H$
- **“RAM Check Registers” on Page 208**: addresses $5F67_H$:$5F6D_H$.
- **“Firmware Control Register” on Page 210**: address $5F6F_H$.
- **“EEPROM Control Registers” on Page 211**: addresses $5F70_H$:$5FF7_H$.

7.5.2.1 Download Using Local Interfaces

To download firmware using parallel or MDIO management interfaces, write the code to RAM at addresses 2000_H through $7DFF_H$.

After download ends, start normal operation by setting the FW_DLOAD register at $5F6F_H$ to 01_H. To verify the checksum of the code before starting normal operation mode, see **“Internal RAM Management” on Page 98**.

7.6 Application Management

As soon as firmware is loaded and activated, normal operation starts and the appropriate features become available. This section describes the features available.

The memory map for registers is described in **“Memory and Register Descriptions – Digital Block” on Page 171**. For detailed descriptions of registers, see **“Detailed Register Descriptions – Digital Block” on Page 185**.

Two link environments are supported:

- Standard compliant
- Boot - used to download firmware to the remote NT.

To select a link environment, set one of the values listed for the MAIN_MODE field (bits 2:0) of the **MAIN_MODE** register ($8F01_H$). See **Page 186** for details.

7.6.1 Standard Compliant Links

A standard compliant environment supports the following links:

- Default link - A default link is established after a cold start. Its parameters are as defined in the standard and listed in **Table 33**.

Table 33 Default Link Parameters in Standard Compliant Environment

Parameter	1 Downstream	2 Downstream	1 Upstream	2 Upstream
Symbol rate	675 kbaud	0	742.5 kbaud	0
Constellation	4	-	4	-
Center Frequency	1.350 MHz	-	4.455 MHz	-
Interleaver	Disabled			
Frame format	Single Latency			

- Alternate default links - Infineon VDSL supports two additional default profiles (DF_STP1 and DF_STP2), in addition to the primary one (DF_STP0), to enable the modem to overcome critical bridge taps and interference. Initially, the LT or NT tries to establish a link using the primary default, DF_STP0. If this link fails, the modem automatically switches to the next DF_STP. The STP that enables establishment of the link becomes the new DF_STP. See also, **“DF_STP1 and DF_STP2 Parameter Mapping in EEPROM” on Page 92** and **“Current and Target STPs” on Page 104**.
- Target Link - A target link is established for transmission of data. It is defined by setting the target profile to the desired value in the LT.

7.6.2 Management of Standard Compliant Links

Link management is performed in two layers, LT and NT, as shown in **Figure 14**.

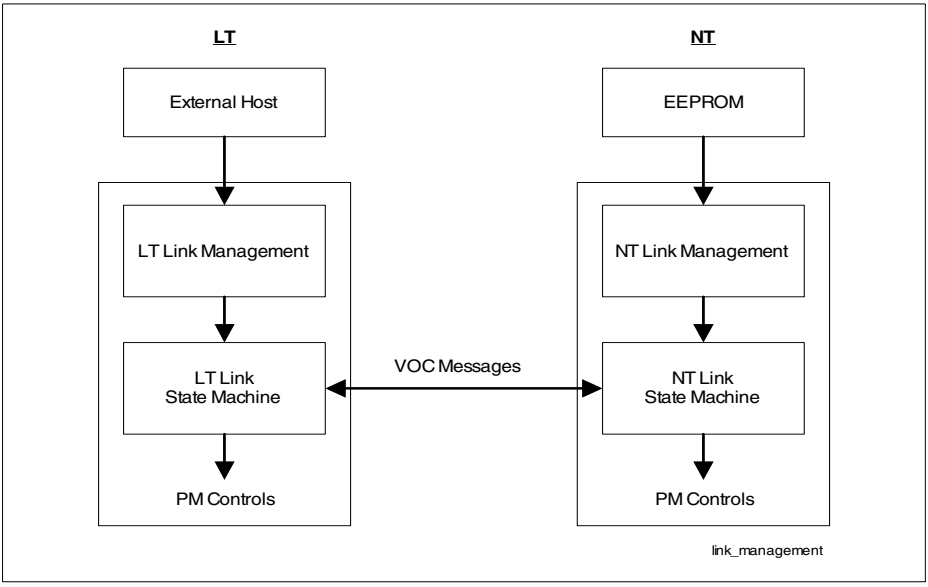


Figure 14 Link Management at the LT and the NT

The Link State Machine supports inter-operability by providing services and mechanisms specified in the Standard. The Link State Machine provides:

- Cold and warm starts
- Transfer to and from an idle link
- Standard Sets of Transmission Parameters (STPs) for links used by the state machine (CR_STP, DF_STP0, DF_STP1, DF_STP2, WS_STP, WR_STP). Upon transition to the Steady State, the current STP (CR_STP) always contains the transmission parameters that were current in the previous state. **Figure 15** shows different states that may precede the Steady State.

Note: To reload the CR_STP from the WS_STP when a warm link is active, a transition to warm start must be set on the LT side only, using the **MAIN_MODE** *register.*

To do this, first clear the **MAIN_MODE** *register (bits 2:0 to 000) on the LT side, to enter 'no operation' mode. Then, set the* **MAIN_MODE** *register (bits 2:0) to 011 or 001, to trigger a new warm start.*

- Power back off mechanism

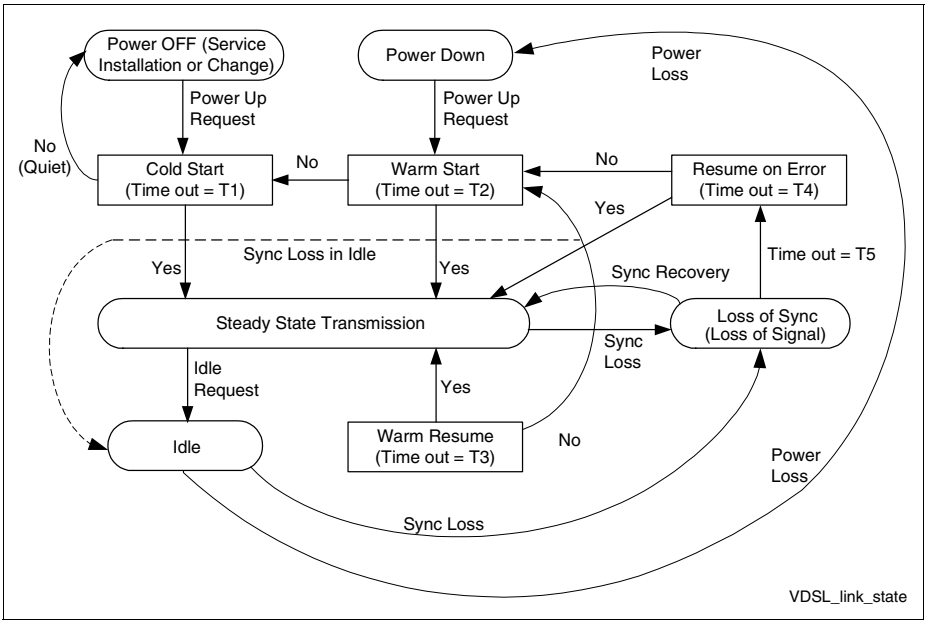


Figure 15 VDSL Transmission Profile Link State Machine

The Link State Machine is shown in **Figure 16** and described in detail in the "*VTU-x State Machine*" sections of the ETSI Standard, where *x* indicates O (LT) or R (NT). See **Reference [2] on page 291**.

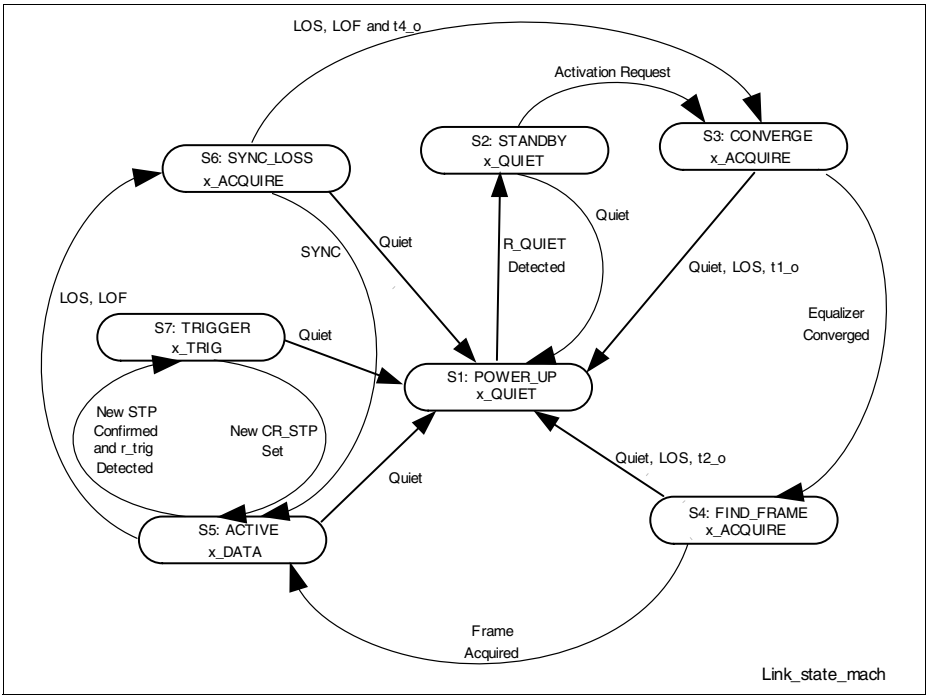


Figure 16 The Link State Machine

The LT link management layer controls and configures the Link State Machine and establishes the target link requested by the user. It also controls the Link State Machines at both the NT and LT throughout this process. The Link State Machine at the NT acts as a slave and is controlled through the VOC channel.

The NT link management layer sets basic configuration capabilities of the Link State Machine. Dynamic control tasks are not needed at the NT, because the NT acts as a slave during link establishment.

The NT link management layer also holds transmission profiles used by the Link State Machine. Transmission profiles are sets of predefined link profiles. Each profile consists of a profile name and link parameters (for example, carrier frequencies, constellations and symbol rates). Transmission profiles simplify the programming of the STPs, because the LT only needs to name the profile instead of specifying a complete set of link parameters. Transmission profiles are kept in the EEPROM and can be changed by the user. The data structure of the transmission profiles in the EEPROM is described in **“EEPROM” on Page 83**.

7.6.3 Configuration of Standard Compliant Links

Fields in the MAIN_CTL, MAIN_MODE and LINK_MODE registers control and configure links. For more information on these fields, see detailed descriptions in:

- **"MAIN_CTL" on Page 186**
- **"MAIN_MODE" on Page 186**
- **"LINK_MODE" on Page 187**.

The fields and bits that control and configure links are:

- MAIN_MODE (bits 2:0 in the MAIN_MODE register at **$8F01_H$**) selects one of the link environments described in **"Application Management" on Page 100**. Selection of a standard compliant link establishes a target link.
  - At the LT, this field can also be used to establish a default link or a reduced link.
  - At the NT, this field cannot be changed and is always set to standard link activation.
- INITIATOR (bit 0 in LINK_MODE at **$8F02_H$**) determines whether the modem initiates a link by transmitting a signal to the channel, or waits for the other side to initiate a link.
- PBO_EN (bit 3 in LINK_MODE at **$8F02_H$**) enables power back off. This bit is relevant for the NT only.
- IDLE (bit 4 in LINK_MODE at **$8F02_H$**) is set to 1 to establish an idle link. When this bit is cleared to 0, a target link is established. This bit is supported in the LT only.

Note: The recommended option is to enable the wake-up mechanism at both sides and to set the NT as initiator. When this is done, the modem at the LT can wait quietly in the DSLAM with very low power consumption. Once the NT is connected, it transmits a WAKEUP signal and the link is established.

If the wake-up mechanism is not enabled, it is advisable to set the LT as the initiator. In this case, the LT constantly transmits a VDSL signal, which enables the NT to tune its power back off mechanism when it is connected.

7.6.4 Current and Target STPs

The current STP (CR_STP) is the set of parameters that describes the currently active link. A warm start STP (WS_STP) contains the parameters used during a warm start. **Table 34** shows the address to read for each parameter in the current or warm start STP.

A default STP contains a set of parameters that is used to establish a link for the first time. Three default STPs support the most popular world connection standards. Two (DF_STP1 and DF_STP2) are customizable. If a link is not established using DF_STP0, after the timeout period, the system will try with the next default STP, DF_STP1. If that fails, after the timeout period, DF_STP2 is used. Once a link is established, the successful STP is the first used in case of a link failure.

Table 35 shows the address to read for each parameter in the customizable default STPs.

7.6.4.1 Modifying STPs

A target STP is the set of transmission parameters that describes the requested link. The following registers enable access to target STP parameters:

- **"VOC_CNTL" on Page 189**
- **"VOC_OC" on Page 190**
- **"VOC_DAT" on Page 190**

To change a parameter in a target STP, do the following:

1. Write the opcode of the parameter to the VOC_OC (**$8F05_H$**) register. For detailed descriptions of opcode parameters and related data fields see **Table 68 "Link Control" on Page 192**.
2. Write the new value of the parameter to the VOC_DAT (**$8F06_H$:$8F07_H$**) register.
3. Write 40_H to the VOC_CNTL (**$8F04_H$**) register.
4. Read VOC_OC to verify that the operation:
   – If it contains the same opcode that was sent, read bits 11:0 of VOC_DAT for the requested parameters.
   – If it contains 00_H, there is a communication error.
   – If it contains $F0_H$ (Unable to Comply VOC), the remote modem cannot comply with the request.

7.6.4.2 Copying STPs

To copy an entire STP from RAM into EEPROM for use as a new default STP and write valid signatures to the appropriate addresses in the EEPROM, see **DF_STP1 and DF_STP2 Parameter Mapping in EEPROM**.

7.6.4.3 STP Mapping

This section shows the mapping of parameters in the current STP (CR_STP), the warm start STP (WS_STP) in **Table 34** and the two customizable default STPs (DF_STP1 and DF_STP2) in **Table 35**.

Table 34 Current and Warm Start STP Mapping (page 1 of 3)

Address (Hex)		Parameter	Description
CR_STP	WS_STP		
5E11	5E30	CENTER_FREQ_DS1	2 bytes, MSB first. First downstream center frequency equals this value * 33.75 kHz
5E13	5E32	CENTER_FREQ_DS2	2 bytes, MSB first. Second downstream center frequency equals this value * 33.75 kHz
5E15	5E34	CENTER_FREQ_US1	2 bytes, MSB first. First upstream Center Frequency equals this value * 33.75 kHz
5E17	5E36	CENTER_FREQ_US2	2 bytes, MSB first. Second upstream center frequency equals this value * 33.75 kHz
5E19	5E38	CONSTELATION_DS1	This value is a power of 2 to define the first downstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5E1A	5E39	CONSTELATION_DS2	This value is a power of 2 to define the second downstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5E1B	5E3A	CONSTELATION_US1	This value is a power of 2 to define the first upstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5E1C	5E3B	CONSTELATION_US2	This value is a power of 2 to define the second upstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5E1D	5E3C	SYMBOL_RATE_DS1	First downstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5E1E	5E3D	SYMBOL_RATE_DS2	Second downstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5E1F	5E3E	SYMBOL_RATE_US1	First upstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5E20	5E3F	SYMBOL_RATE_US2	Second upstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5E21	5E40	PSD_LEVEL_DS1	First linear downstream PSD level.
5E22	5E41	PSD_LEVEL_DS2	Second linear downstream PSD level.

Table 34 Current and Warm Start STP Mapping (page 2 of 3)

Address (Hex)		Parameter	Description
CR_STP	WS_STP		
5E23	5E42	PSD_LEVEL_US1	First linear upstream PSD level.
5E24	5E43	PSD_LEVEL_US2	Second linear upstream PSD level.
5E25	5E44	PSD_MASK	Notch control for a direction and carrier. One notch per band supported, with bits 7:4 reserved and: Bit 3: notch on US2 at the NT, 10.1 - 10.15 MHz. Bit 2: notch on DS2 at the LT, 7.0 - 7.1 MHz. Bit 1: notch on US1 at the NT, 3.5 - 3.8 MHz. Bit 0: notch on DS1 at the LT, 1.81 - 2.0 MHz.
5E26	5E45	Reserved	Reserved
5E27	5E46	INTERLEAVER_M_DS	Range 0:64. 0 = Interleaver OFF.
5E28	5E47	INTERLEAVER_M_US	Range 0:64. 0 = Interleaver OFF.
5E29	5E48	INTERLEAVER_I	Denominator for calculating interleaver block length, where: Bit 1 is for upstream, and 0 = 4, 1= 8 Bit 0 is for downstream, and 0 = 4, 1= 8 See **“Interleaving” on Page 63** for details.
5E2A	5E49	FAST_SIZE_DS	Length of downstream fast channel, in bytes.
5E2B	5E4A	FAST_SIZE_US	Length of upstream fast channel, in bytes.
5E2C	5E4B	FFEC_SIZE_LT	Bits 7:4 specify upstream reception FFEC. Bits 3:0 specify upstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*

Table 34 Current and Warm Start STP Mapping (page 3 of 3)

Address (Hex)		Parameter	Description
CR_STP	**WS_STP**		
5E2D	5E4C	FFEC_SIZE_NT	For Bits 7:4 specify downstream reception FEC. Bits 3:0 specify downstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
5E2E	5E4D	SFEC_SIZE_LT	Bits 7:4 specify upstream reception SFEC. Bits 3:0 specify upstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
5E2F	5E4E	SFEC_SIZE_NT	Bits 7:4 specify downstream reception SFEC. Bits 3:0 specify downstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*

Table 35 Default STP Mapping (page 1 of 4)

Address (Hex)		Parameter	Description
DF_STP1	**DF_STP2**		
5ECB	5EEA	CENTER_FREQ_DS1	2 bytes, MSB first. First downstream center frequency equals this value * 33.75 kHz
5ECD	5EEC	CENTER_FREQ_DS2	2 bytes, MSB first. Second downstream center frequency equals this value * 33.75 kHz

Table 35 Default STP Mapping (page 2 of 4)

Address (Hex)		Parameter	Description
DF_STP1	**DF_STP2**		
5ECF	5EEE	CENTER_FREQ_US1	2 bytes, MSB first. First upstream Center Frequency equals this value * 33.75 kHz
5ED1	5EF0	CENTER_FREQ_US2	2 bytes, MSB first. Second upstream center frequency equals this value * 33.75 kHz
5ED3	5EF2	CONSTELATION_DS1	This value is a power of 2 to define the first downstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5ED4	5EF3	CONSTELATION_DS2	This value is a power of 2 to define the second downstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5ED5	5EF4	CONSTELATION_US1	This value is a power of 2 to define the first upstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5ED6	5EF5	CONSTELATION_US2	This value is a power of 2 to define the second upstream QAM. QAM = $2^{CONSTELATION\_DS1}$
5ED7	5EF6	SYMBOL_RATE_DS1	First downstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5ED8	5EF7	SYMBOL_RATE_DS2	Second downstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5ED9	5EF8	SYMBOL_RATE_US1	First upstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5EDA	5EF9	SYMBOL_RATE_US2	Second upstream symbol rate = this value * 67.5 kHz. 0 = disabled.
5EDB	5EFA	PSD_LEVEL_DS1	First linear downstream PSD level.
5EDC	5EFB	PSD_LEVEL_DS2	Second linear downstream PSD level.
5EDD	5EFC	PSD_LEVEL_US1	First linear upstream PSD level.
5EDE	5EFD	PSD_LEVEL_US2	Second linear upstream PSD level.

Table 35 Default STP Mapping (page 3 of 4)

Address (Hex)		Parameter	Description
DF_STP1	**DF_STP2**		
5EDF	5EFE	PSD_MASK	Notch control for a direction and carrier. One notch per band supported, with bits 7:4 reserved and: Bit 3: notch on US2 at the NT, 10.1 - 10.15 MHz. Bit 2: notch on DS2 at the LT, 7.0 - 7.1 MHz. Bit 1: notch on US1 at the NT, 3.5 - 3.8 MHz. Bit 0: notch on DS1 at the LT, 1.81 - 2.0 MHz.
5EE0	5EFF	Reserved	Reserved
5EE1	5F00	INTERLEAVER_M_DS	Range 0:64. 0 = Interleaver OFF.
5EE2	5F01	INTERLEAVER_M_US	Range 0:64. 0 = Interleaver OFF.
5EE3	5F02	INTERLEAVER_I	Denominator for calculating interleaver block length, where: Bit 1 is for upstream, and 0 = 4, 1= 8 Bit 0 is for downstream, and 0 = 4, 1= 8 See **“Interleaving” on Page 63** for details.
5EE4	5F03	FAST_SIZE_DS	Length of downstream fast channel, in bytes.
5EE5	5F04	FAST_SIZE_US	Length of upstream fast channel, in bytes.
5EE6	5F05	FFEC_SIZE_LT	Bits 7:4 specify upstream reception FFEC. Bits 3:0 specify upstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information*

Table 35 Default STP Mapping (page 4 of 4)

Address (Hex)		Parameter	Description
DF_STP1	DF_STP2		
5EE7	5F06	FFEC_SIZE_NT	For Bits 7:4 specify downstream reception FEC. Bits 3:0 specify downstream transmission FFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
5EE8	5F07	SFEC_SIZE_LT	Bits 7:4 specify upstream reception SFEC. Bits 3:0 specify upstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*
5EE9	5F08	SFEC_SIZE_NT	Bits 7:4 specify downstream reception SFEC. Bits 3:0 specify downstream transmission SFEC. *Note: To receive real FFEC/SFEC values, multiply this setting by 2. See page 111 for additional information.*

7.6.4.4 Setting the Gross Bit Rate

Upstream and downstream gross bit rates (bits in the air) are defined by the constellations and symbol rates, as follows:

$$BitRate = SymbolRate1 * Log_2(Constellation1) + SymbolRate2 * Log_2(Constellation2)$$

where, 1 and 2 correspond to bands 1 and 2 of the upstream or downstream signal, and where the symbol rate is a multiple of 67.5 Kbps.

When setting bit rates, ensure that the following is always true:

$$SymbolRate1 * Log(Constellation1) / [SymbolRate2 * Log(Constellation2)] = N_1 / N_2$$

where, $N_1 + N_2 + 64 \leq 200$ and $N_1 \geq 1$

Note: If this relation is not maintained, the target link is not established. The default link is established instead, and the PROFILE_ERR bit in the GEN_STATUS2 register ($8F10_H$) is asserted.

7.6.4.5 Net Throughput

The structure of the transmission frame before it is split into two bands is shown in **Figure 17**. See **"Construction of a Transmission Frame" on Page 64** for more information about transmission frame fields.

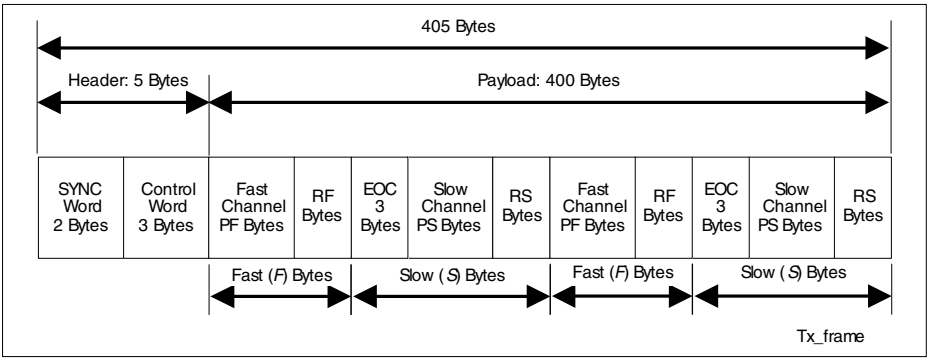


Figure 17 Transmission Frame Format

The number of fast channel bytes (F) in each field is set in the FRAME parameter (see **Table 68 "Link Control" on Page 192**) and S is the number of slow channel bytes in each field, where:

$$S = 200 - F$$

and F must conform with the following:

$F \leq 180$ and $F =$ a multiple of 4 bytes

In the fast channel, RF bytes are allocated for FEC. Supported values for RF are 0, 2, 4, 8 and 16. The value is specified in the FRAME parameter (see **Table 68**).

Fast channel throughput is defined as:

$$\text{FastThroughput} = \text{BitRate} * (F - RF) * 2 / 405$$

In the slow channel, three bytes are allocated for the operation channel, and RS bytes are allocated for FEC. Only a value of 16 is supported for RS.

Slow channel throughput is defined as:

$$\text{SlowThroughput} = \text{BitRate} * (200 - F - RS - 3) * 2 / 405$$

7.6.4.6 Setting the Interleaver

The interleaver is configured by setting the I and M fields in the INTERLV parameter (see **Table 68 "Link Control" on Page 192**), where:

- I is the interleaver block length. Supported values are S / 4 and S / 8.
- M is the interleaver depth index.

The following interleaver characteristics are derived for the slow channel from I and M:

- Interleaver depth (D) = $M * I + 1$
- End-to-end delay (DL) =
  - in bytes, $DL_B = M * I * (I - 1)$
  - in bits, $DL_b = 8 * M * I * (I - 1)$
  - in µsec, $DL_t = 8 * M * I * (I - 1)$ / *Rate*
- Interleaver memory size (MEM) = $M * I * (I - 1)$ / *2*
- Noise protection, which is Erasure Correction:
  - in bytes, $E_B = [t * I / S] * (M * I + 1)$
  - in µsec, $E_t = E * 8 / Rate$

For more information on the interleaver, see **"Interleaving" on Page 63**.

7.6.4.7 Calculating Interleaver Protection

Table 36 shows how to calculate protection provided by the interleaver for 21.6 Mbit/s downstream operation, with S / 8. See also, **"Interleaving" on Page 63**.

Table 36 Protection Calculation Parameters for 21.6 Bit Rate, DS, S/8

Parameter	Parameter Values			
Fast Channel Bytes (F), multiple of 8	0	96	0	96
Slow Channel Bytes (S) 200 – F	200	104	200	104
Slow Bit Rate in Mbit/s	21.6	11.232	21.6	11.232
Interleaver Depth Index M	27	27	54	54
Interleaver Block in Bytes (I) S / 8	25	13	25	13
Memory Allocation (MEM) in Bytes[1)]	8,100	2,106	16,200	4,212
Total Memory for Interleaver and De-interleaver in Bytes	16,200	4,212	32,400	8,424
Delay in µs (DL)	6,000	3,000	12,000	6,000
Erased Bytes (E_B)	676	352	1351	703
Protection Time in µs (E_t)	250.3704	250.7123	500.3704	500.7123

1) Upstream memory allocation plus downstream memory allocation may not exceed 24 KB.

Table 37 shows how to calculate protection provided by the interleaver for 21.6 Mbit/s downstream operation, with S / 4. See also, "Interleaving" on Page 63.

Table 37 Protection Calculation Parameters, 21.6 Bit Rate, DS, S/4

Parameter	Parameter Values			
Fast Channel Bytes (F), must be a multiple of 4	0	4	0	4
Slow Channel Bytes (S) 200 – F	200	196	200	196
Slow Bit Rate in Mbit/s	21.6	21.168	21.6	21.168
Interleaver Depth Index M	7	7	14	14
Interleaver Block in Bytes (I) S / 4	50	49	50	49
Memory Allocation (MEM) in Bytes[1)]	8,575	8,232	17,150	16,464
Total Memory for Interleaver and De-interleaver in Bytes	17,150	16,464	34,300	32,928
Delay in µs (DL)	6,351.85	6,222.22	12,703.70	12,444.44
Erased Bytes (E_B)	702	688	1402	1374
Protection Time in µs (E_t)	260	260.0151	519.2593	519.2744

1) Upstream memory allocation plus downstream memory allocation may not exceed 24 KB.

Table 38 shows how to calculate protection provided by the interleaver for 9.99 Mbit/s upstream operation, with S / 8. See also, "Interleaving" on Page 63.

Table 38 Protection Calculation Parameters, 9.99 Bit Rate, Upstream, S/8
(page 1 of 2)

Parameter	Parameter Values			
Fast Channel Bytes (F), must be a multiple of 8	0	96	0	96
Slow Channel Bytes (S) 200 – F	200	104	200	104
Slow Bit Rate in Mbit/s	9.99	5.1948	9.99	5.1948
Interleaver Depth Index M	13	13	25	25
Interleaver Block in Bytes (I) S / 8	25	13	25	13
Memory Allocation (MEM) in Bytes[1)]	3,900	1,014	7,500	1,950
Total Memory for Interleaver and De-interleaver in Bytes	7,800	2,028	15,000	3,900
Delay in µs (DL)	6,246.25	3,123.12	12,012.01	6,006.01

Table 38 Protection Calculation Parameters, 9.99 Bit Rate, Upstream, S/8 (page 2 of 2)

Parameter	Parameter Values			
Erased Bytes (E_B)	326	170	626	326
Protection Time in µs (E_t)	261.0611	261.8003	501.3013	502.0405

1) Upstream memory allocation plus downstream memory allocation may not exceed 24 KB.

Table 39 shows how to calculate the protection provided by the interleaver for 9.99 Mbit/s upstream operation, with S / 4. See also, **"Interleaving" on Page 63**.

Table 39 Protection Calculation Parameters, 9.99 Bit Rate, Upstream, S/4

Parameter	Parameter Values			
Fast Channel Bytes (F), must be a multiple of 4	0	4	0	4
Slow Channel Bytes (S) 200 – F	200	196	200	196
Slow Bit Rate in Mbit/s	9.99	9.7902	9.99	9.7902
Interleaver Depth Index M	3	3	6	6
Interleaver Block in Bytes (I) S / 4	50	49	50	49
Memory Allocation (MEM) in Bytes[1)]	3,675	3,528	7,350	7,056
Total Memory for Interleaver and De-interleaver in Bytes	7,350	7,056	14,700	14,112
Delay in µs (DL)	5,885.89	5,765.77	11,771.77	11,531.53
Erased Bytes (E_B)	302	296	602	590
Protection Time in µs (E_t)	241.8418	241.8745	482.0821	482.1148

1) Upstream memory allocation plus downstream memory allocation may not exceed 24 KB.

7.6.5 Power Back Off (PBO)

Upstream Power Back Off (PBO) ensures that all NT modems are received by the LT with the same power, as if they were located at the maximum reach. The PBO algorithm converts measured downstream attenuation into required upstream Power Spectral Density (PSD) levels.

The line attenuation can be modeled after the ETSI recommendation as follows according to the formula

$$A = Kd\sqrt{f} \quad (2)$$

where:

- A= Attenuation in dB
- K= Wire type constant as measured by [dB / km / $(Hz)^{0.5}$]
- d= line length in km
- f= frequency in Hz

Upstream power back off is applied separately, to both upstream bands. The system estimates the electrical distance between the NT and LT from the physical line length and the attenuation characteristics of the downstream signal. It uses this estimated electrical distance to attenuate transmitted signals on the upstream bands, so that each is received in the LT as though it were generated from the maximum reach.

When PBO is enabled, (PBO_EN, bit 3 in the LINK_MODE register at $8F02_H$ is set to 1), firmware implements the upstream power back off algorithm, based on the profile parameters and the maximum reach parameter, which are specified in the PBO registers.

The digital transmitter hardware uses programmable shaping filters to adjust non-flat Power Spectral Density (PSD) separately for each band.

See also **“Power Back Off Registers (PBO)” on Page 235**.

7.6.6 Performance Monitoring for Standard Compliant Links

Link performance is monitored using the following registers:

- **“VOC_CNTL” on Page 189** ($8F04_H$)
- **“VOC_OC” on Page 190** ($8F05_H$)
- **“VOC_DAT” on Page 190** ($8F06_H$:$8F07_H$)
- **“GEN_STATUS2” on Page 198** ($8F10_H$)

To get performance information about the local receiver, do the following:

1. Write the opcode of the parameter to the **VOC_CNTL** register. For detailed descriptions of opcodes and related data fields see **Table 69 “Link Performance Parameters” on Page 193**.
2. If necessary, in VOC_DAT, write the number of the band (CARRIER_NUM) to read. All other fields are ignored.
3. Write 10_H to the VOC_CNTL register.
4. Read bits 11:0 of VOC_DAT for the requested parameters.

To get performance information about the remote receiver, do the following:

1. Write the opcode of the parameter to the VOC_OC register. For detailed descriptions of opcodes and related data fields see **Table 69 “Link Performance Parameters” on Page 193**.
2. If necessary, in VOC_DAT, write the number of the band (CARRIER_NUM) to read. All other fields are ignored.
3. Write 40_H to the VOC_CNTL register.
4. Read VOC_OC.
   – If it contains the same opcode that was sent, read bits 11:0 of VOC_DAT for the requested parameters.
   – If it contains 00_H, there is a communication error.
   – If it contains $F0_H$ (Unable to Comply VOC), the remote modem cannot comply with the request

To monitor transmission of VOC messages at the remote modem, read the GEN_STATUS2 register. If CF (bit 2) is set to 1, the operation succeeded and the information can be read from bits 11:0 of the VOC_DAT register. If UTCF (bit 3) is set to 1, the operation failed.

7.6.7 The Rate Adaptive Process

The Rate Adaptive (RA) process enables a modem pair (LT and NT) to optimize their link configurations based on the line conditions.

This section includes the following sections:

- **The Rate Adaptive Loop**
- **Configuring the RA Process**
- **Executing the RA Process**
- **Polling the Status of the RA Process**
- **Selecting an RA Scanning Band Plan**
- **Running the RA Process with PBO in Changing Conditions**
- **Running the RA Process with Long Reach VDSL**

7.6.7.1 The Rate Adaptive Loop

During RA execution, the RA algorithm selects the profile with the highest rate that meets user requirements and is within the permitted band plan. In addition, the RA algorithm can monitor the selected optimal link.

The Rate Adaptive algorithm has two main states, as shown in **Figure 18** and described below:

- **“Achieving the Optimal Link” on Page 118**
- **“Monitoring the Optimal Link” on Page 119**

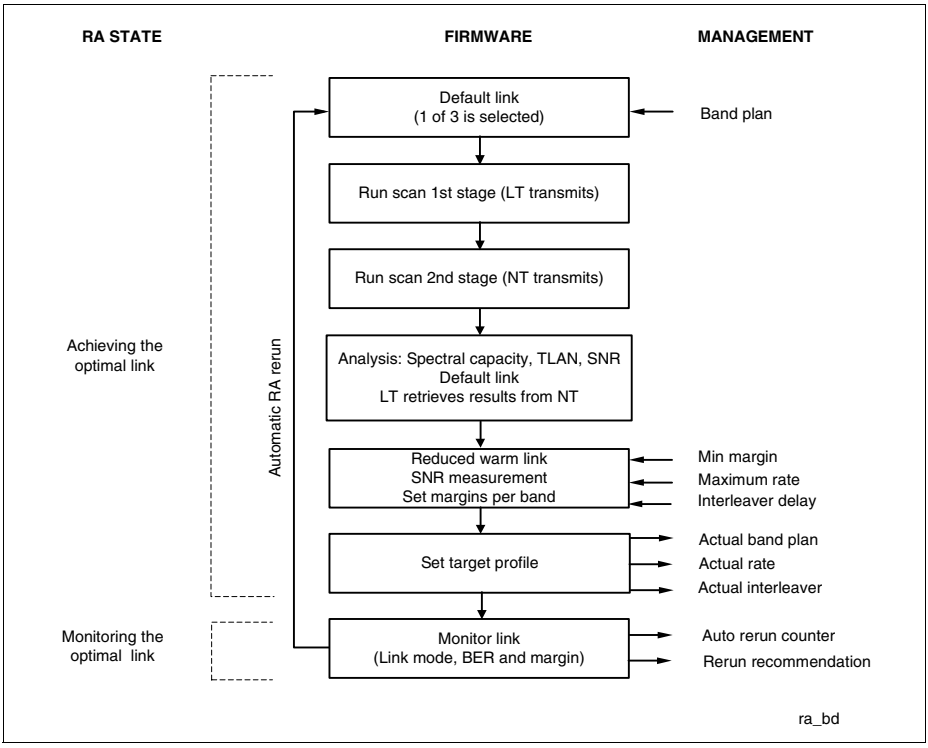


Figure 18 RA Simplified Flow Diagram

Achieving the Optimal Link

In this state, the RA algorithm takes the following parameters into account:

- Modem limitations
- Noise profile including self FEXT and alien noise
- Permitted band plan, including notch
- Abnormal spectrum distortion (for example, wide notch caused by multiple bridge taps)
- Rate limitations

To achieve the optimal link, the RA algorithm does the following:

1. Scans the spectrum in compliance with the band plan limits and power back off laws.
2. Analyzes the scanned data to detect the following sources of interference:
   – Bridge taps
   – NEXT
   – FEXT

3. Computes a raw estimate of the received SNR for each band.
4. Loads a reduced profile to measure the actual SNR.
5. Sets the optimal profile based on the actual SNR and the following parameters:
   – Minimum margin
   – TLAN
   – Maximum rate
   – Interleaver delay

Monitoring the Optimal Link

Although monitoring is not mandatory, it helps management to track the link status and recovers the link if failure occurs. The monitor runs on both LT and NT. See **Figure 19** for details.

During monitoring, firmware monitors link mode, BER and margin. If the link becomes inadequate, firmware automatically reruns the RA algorithm.

If margin goes above or below defined thresholds, firmware recommends running the RA algorithm again to set a new link configuration that is optimized for the new current SNR. Management then decides whether or not to run the RA algorithm again.

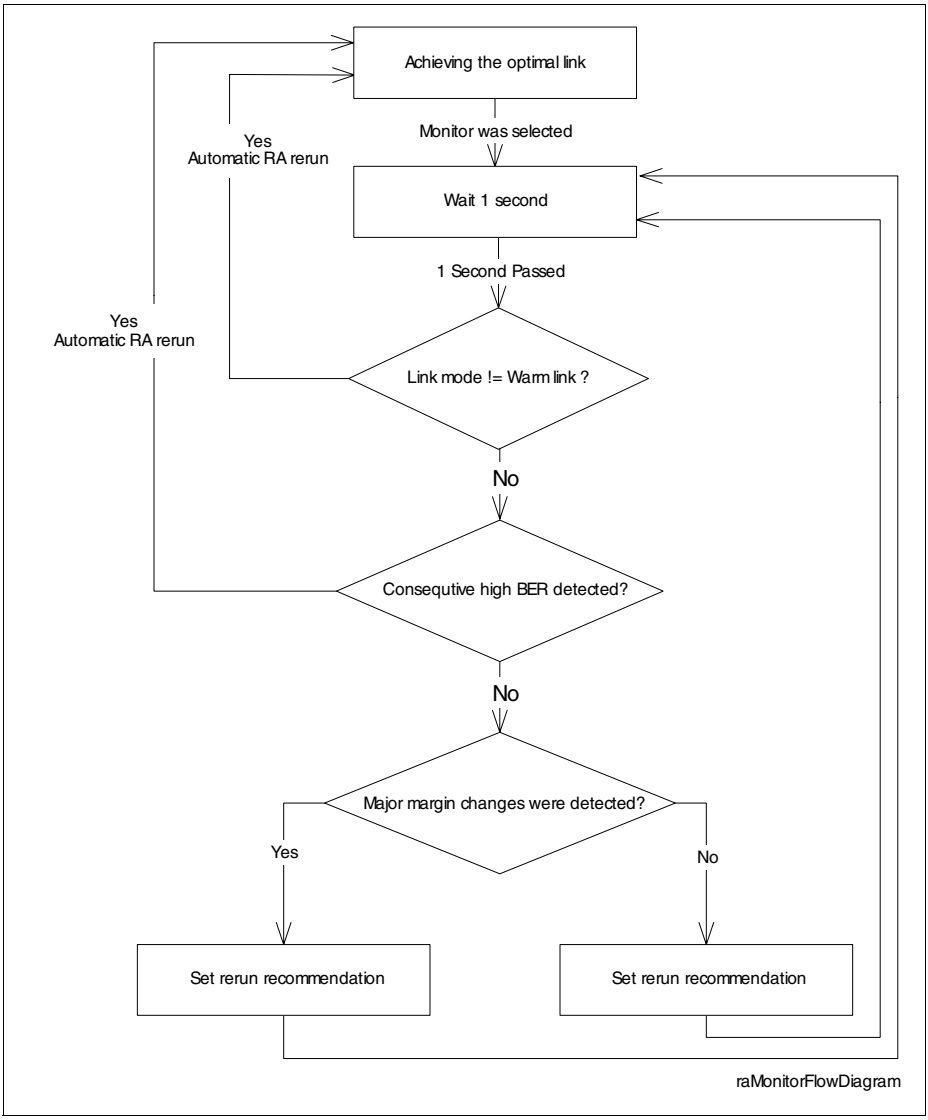


Figure 19 RA Monitor Flow Diagram

7.6.7.2 Configuring the RA Process

The following registers are required for configuring the Rate Adaptive (RA) process:

- Noise margin registers (LT only)
  - **RA_MN_MRG_D1**
  - **RA_MN_MRG_D2**
  - **RA_MN_MRG_U0** (when configuring LR)
  - **RA_MN_MRG_U1**
  - **RA_MN_MRG_U2**
- Maximum bit rate registers (LT only)
  - **RA_MX_RATE_DS**
  - **RA_MX_RATE_US**
- RA scan profile registers (LT and NT)
  - RA center frequency registers: **RA_CF_D1**, **RA_CF_D2**, **RA_CF_U1**, **RA_CF_U2**
  - Symbol rate registers: **RA_SR_D1**, **RA_SR_D2**, **RA_SR_U1**, **RA_SR_U2**
  - PSD level registers: **RA_PSD_D1**, **RA_PSD_D2**, **RA_PSD_U1**, **RA_PSD_U2**
  - PSD mask register: **RA_PSD_MASK**
  - PSD maximum level (while using the first downstream band only): **RA_PSD_MAX**
- Interleaver delay registers (LT only)
  - **RA_INTR_DS**
  - **RA_INTR_US**

7.6.7.3 Executing the RA Process

Use the **RA_COMMAND** register at the LT for execution. For implementation information, refer to the Application Note.

7.6.7.4 Polling the Status of the RA Process

At the LT only, verify the RA status by polling the **RA_ANAL** and **RA_RDY** bits in the **RA_STATUS** register at address $5B40_H$.

Note: For more information on RA, please see the Application Note on the RA process.

7.6.7.5 Selecting an RA Scanning Band Plan

The RA scan profile used by the RA algorithm is configurable. Management can choose any band plan in the range 0.138 MHz - 12.0 MHz, including the upstream 0 band for Long Reach VDSL (LR-VDSL), provided that the following two statements are true:

- Symbol rate (SR) values for both bands are even numbers.
- The result of the low frequency on band 2 minus the low frequency on band 1 is a multiple of 4, where the low frequency on each band is center frequency minus

symbol rate, or:
$((F_{LOW\_BAND2} - F_{LOW\_BAND1}) \bmod 4) = 0$ where, $F_{LOW\_BANDx} = CF_{BANDx} - SR_{BANDx}$
If Long Range is enabled, the RA process may automatically choose to use US0 (0.25-0.138).

7.6.7.6 Running the RA Process with PBO in Changing Conditions

The Power Back Off (PBO) mechanism computes transmission power at the NT (CPE) for each upstream carrier, according to line conditions. PBO may be activated whenever a link is established, if the RA process is not active.

To ensure consistent results, the RA process freezes the PBO mechanism and uses only the first set of PBO results. Whenever distances are changed, it may be necessary to unfreeze the PBO mechanism before running the RA process again.

To ensure new PBO computation do the following:

1. Disable RA at the CPE. (Clear bit **RA_EN** to 0_B.)
2. Deactivate and reactivate the link.

7.6.7.7 Running the RA Process with Long Reach VDSL

The RA process automatically implements Long Reach VDSL (LR-VDSL) mode (if it is enabled on both ends) to support operation at distances greater than 1300 m.

To enable automatic implementation of LR-VDSL by the RA process, do the following:

1. **Enable Long Reach at the Remote Modem** - At the NT, activate the LR_EN bit (set bit 7 of the **LINK_MODE** register to 1 at the EEPROM, address $8F02_H$ or $F802_H$, depending on the bank used). Set this bit at the NT only once, after the first firmware download, if upstream channel 0 filters and long reach capabiilty are both present. Never turn it off. Downloading new firmware using the API preserves the previous value.
2. **Disable DF_STP0** - Set the **DF0_SKIP** bit (bit 5 in the **LINK_MODE** register at $8F02_H$) to 1 in both the LT and the NT. When long reach VDSL is enabled, it is recommended to use DF0_SKIP mode. DF_STP0 is the standard short range default STP. In DF0_SKIP mode, only DF_STP1 and DF_STP2 are the alternating STPs.
3. **Use DF_STP2 Values** - At both the LT and the NT, replace the values of the DF_STP1 parameters with the default values for the DF_STP2 parameters (long reach support) shown in **Table 32 on page 96**. For descriptions of DF_STP1 and DF_STP2 parameters, see also **Table 30 on page 92**.
4. **Enable Long Reach at the Local Modem** - At the LT, activate the LR_EN bit (set bit 7 of the **LINK_MODE** register at $8F02_H$ to 1).

For more information refer to the application notes that describe the Rate Adaptive process and Long Reach VDSL (LR-VDSL) mode.

To implement Long Reach VDSL without running the RA process, see, **"Implementing Long Reach VDSL Manually" on Page 123**.

7.6.8 Implementing Long Reach VDSL Manually

LR-VDSL operation mode operates only on one upstream band. On this band, only the constellation can be configured via the relevant STP (CR_STP or WS_STP). All other parameters are fixed by firmware and cannot be modified.

The Rate Adaptive process can automatically implement Long Reach VDSL (LR-VDSL) mode to support operation at distances greater than 1,300 m, as described in , **"Running the RA Process with Long Reach VDSL" on Page 122**.

To manually implement LR-VDSL mode without running the RA process, do the following:

1. **Set the Frequency** - Make sure the crystal frequency at the LT is 25.92 MHz.
2. **Enable Long Reach at Both LT and NT** - Make sure that in both the LT and the NT, the LR_EN bit (bit 7 of the **LINK_MODE** register) is set to 1. It is recomended that in the NT, LR_EN bit is always set to 1.
3. **Set STP Values** - Send VOCs to set Upstream 1 (US1), with both Center Frequency (CF) and Symbol Rate (SR) parameters in the approriate STP to 1.
   It is recommended to replace the values of the DF_STP1 parameters with the default values for the DF_STP2 parameters (long reach support) shown in **Table 32 on page 96**. For descriptions of DF_STP1 and DF_STP2 parameters, see also **Table 30 on page 92**.

For more information refer to the application notes that describe the Rate Adaptive process and Long Reach VDSL (LR-VDSL) mode.

7.6.9 Accessing the Remote Transceiver

Registers in the remote NT can be accessed from the LT using the following registers:

- **"VOC_CNTL" on Page 189** ($8F04_H$)
- **"VOC_OC" on Page 190** ($8F05_H$)
- **"VOC_DAT" on Page 190** ($8F06_H$:$8F07_H$)
- **"GEN_STATUS2" on Page 198** ($8F10_H$)

To read a byte from the remote NT, do the following at the LT:

1. Write the address of the remote register to read, into the VOC_DAT register.
2. Write 93_H to the VOC_OC register. For detailed descriptions of opcodes and related data fields see **Table 70 "Access to Remote Registers" on Page 194**.
3. Write 40_H to the VOC_CNTL register.
4. Read VOC_OC, and wait for it to change from 00_H to opcode 93_H.
5. Read the GEN_STATUS2 register. If the CF (bit 2) is set to 1, the operation succeeded and the low byte of the VOC_DAT register contains the information read, where the low byte is at address $8F07_H$. If UTCF (bit 3) is set to 1, the operation failed.

To write a byte to the remote NT, do the following at the LT:

1. Write the address of the remote register to which to write, into the VOC_DAT register.
2. Write 94_H to the VOC_OC register. For detailed descriptions of opcodes and related data fields see **Table 70 "Access to Remote Registers" on Page 194**.
3. Write 40_H to the VOC_CNTL register.
4. Read VOC_OC, and wait for it to change from 00_H to opcode 94_H.
5. Read the GEN_STATUS2 register. If CF (bit 2) is set to 1, the operation succeeded and the address was delivered. If UTCF (bit 3) is set to 1, the operation failed.
6. Write the requested data into the low byte of the VOC_DAT register, where the low byte is at address $8F07_H$.
7. Write $E3_H$ to the VOC_OC register.
8. Write 40_H to VOC_CNTL register.
9. Read VOC_OC, and wait for it to change from 00_H to opcode $E3_H$.
10. Read the GEN_STATUS2 register. If CF (bit 2) is set to 1, the operation succeeded. If UTCF (bit 3) is set to 1, the operation failed.

7.6.10 Network Interfaces

Network interfaces serve as the main data path between the IC and the outside world. Data received on these interfaces is output and transmitted over the VDSL line.

For more information, see **"Network Interfaces" on Page 156**.

7.6.10.1 Ethernet Packet Transfer

In the Ethernet network environment, the digital transceiver can be configured as an Ethernet MAC or as a PHY, as described in **"Configuration Pins" on Page 81**.

When it is configured as a PHY, it is managed through the Serial Management Interface (SMI) and SMI registers. SMI registers include the standard registers defined in IEEE 802.3 and proprietary registers that enable access to internal memory and support extended proprietary features. For more information about SMI **"MII Serial Management Interface (SMI)" on Page 142.**

When it is configured as a MAC, it controls the 10/100Base-TX Ethernet PHY through the SMI. In this case, it acts as a master of the SMI.

Management of the network interface includes the following:

- MII configuration - setting the speed and duplex mode of the MII interface
- Back pressure and flow control management
- Address filtering management
- Back signaling management

7.6.10.1.1 MII Configuration for a PHY-MAC Scenario

In a PHY-MAC scenario, the SMI registers of the remote 10/100Base-TX PHY are not changed by the remote MAC. Local SMI registers are not affected by the remote 10/100Base-TX PHY. **Table 40** describes the behavior of the local SMI registers.

Table 40 SMI Register Behavior (page 1 of 2)

SMI Register and Address (Hex)	Behavior
00 (BMCR)	Unless otherwise indicated, bits behave as described in **"Detailed Description of SMI Registers" on Page 146**. • Bit 15 (RESET) - Local effect as in register description. • Bit 14 (LPBK) - Local effect as in register description. • Bit 13 (SPEED) - If ANEGEN is cleared, the speed indicated by this bit is considered the actual speed. • Bit 12 (ANEGEN) - Disables or enables local automatic negotiation process. • Bit 10 (ISOLATE) - Local effect as in register description. • Bit 9 (RESANEG) - Restarts local automatic negotiation. • Bit 8 (DUPLEX) - In ANEGEN is cleared, the duplex mode indicated by this bit is considered the duplex mode. • Bit 7 (COL) - Local effect as in register description. • BIT 0 (RESET_DISABLE) - Local effect as in register description.
01 (BMSR)	Unless otherwise indicated, bits behave as described in **"Detailed Description of SMI Registers" on Page 146**. • Bits 14:11 All set to 1 to indicate that all options are supported. • Bit 6 (MFPS) - Local effect as in register description. • Bit 5 (ANEG_STATUS) - Status of local automatic negotiation. • Bit 4 (REMOTE_ERR) - Always 0. No remote fault detection. • Bit 3 (ANEGABILITY) - Always 1. Local automatic negotiation is supported. • Bit 2 (LINK_STATUS) - Status of the VDSL link. • Bit 1 (JABBER) - Always 0. Jabber detection is not available. • BIT 0 (EXTEND) - Local effect as in register description.
02:03 (OUI)	Organizationally Unique Identifier
04 (ANAR)	When local automatic negotiation is activated, the ANAR register is copied to the ANLPAR register.
05 (ANLPAR)	
10 (IADDSR)	Internal Address Space
11 (OPCDR)	Opcode Register - Command and status bits.

Table 40 SMI Register Behavior (page 2 of 2)

SMI Register and Address (Hex)	Behavior
12 (RSLTR)	Result Register - Data from last read operation.

In the remote side, MII configuration for speed and duplex parameters in the digital transceiver is automatic, according to the status of the SMI registers in the remote 10/100Base-TX PHY as follows:

1. If the ANEGEN bit (bit 12) in the BMCR register of the 10/100Base-TX is asserted, then the speed and duplex parameters are derived from the ANAR and ANLPAR registers of the 10/100Base-TX PHY.
2. Otherwise, these parameters are derived from the SPEED (bit 13) and DUPLEX (bit 8) bits in the BMCR register of the 10/100Base-TX PHY.

In the local side, MII configuration for speed and duplex parameters in the digital transceiver is automatic, according to the status of the local SMI registers as follows:

1. If the ANEGEN bit (bit 12) in the local BMCR register is asserted, then the speed and duplex parameters are derived from the local ANAR and ANLPAR registers.
2. Otherwise, these parameters are derived from the SPEED (bit 13) and DUPLEX (bit 8) bits in the BMCR register.

7.6.10.1.2 MII Configuration for a MAC-MAC Scenario

Figure 20 illustrates a MAC-MAC scenario.

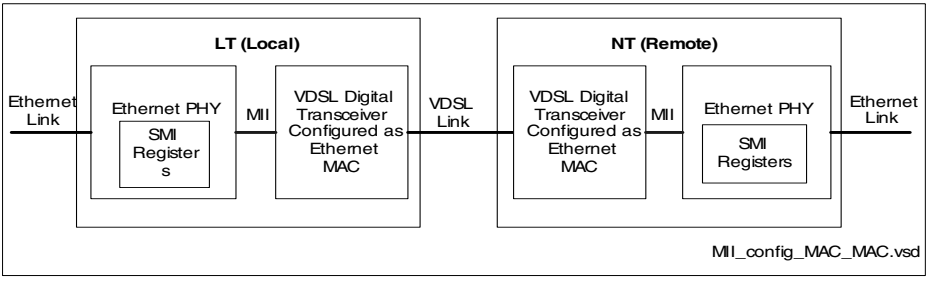


Figure 20 MAC-MAC Scenario

In a MAC-MAC scenario, the MII speed and duplex parameters of the digital transceivers at the ends are configured automatically according to the status of the attached 10/100Base-TX PHY, as follows:

1. If the ANEGEN bit (bit 12) in the BMCR register of the attached PHY is asserted, then the speed and duplex parameters are derived from the ANAR and ANLPAR registers of the attached PHY.

2. If the ANEGEN bit (bit 12) is cleared, these parameters are derived from the SPEED (bit 13) and DUPLEX (bit 8) bits in the BMCR register of the attached PHY.

7.6.10.1.3 MII Configuration for a PHY-PHY Scenario

Figure 21 illustrates a PHY-PHY scenario.

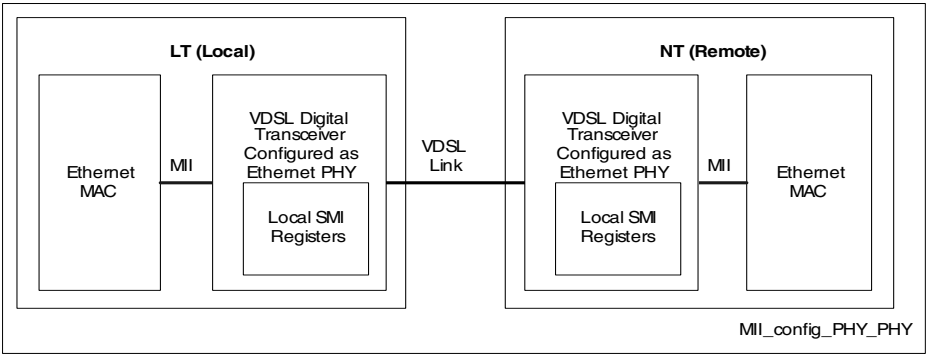


Figure 21 PHY-PHY Scenario

In devices on both sides, MII speed and duplex parameters of the digital transceiver are configured automatically according to the status of the SMI registers as follows:

1. If the ANEGEN bit (bit 12) in the BMCR register is asserted, then the speed and duplex parameters are derived from the ANAR and ANLPAR registers.
2. Otherwise, these parameters are derived from the SPEED (bit 13) and DUPLEX (bit 8) bits in the BMCR register.

7.6.10.1.4 802.3 MAC Flow Control

In the Ethernet interface, flow control keeps internal buffers from overflowing as follows:

- In half duplex operation, back pressure is used with signaling between both ends of the link to implement flow control.
- In full duplex operation, 802.3*x* flow control is used together with signaling between both ends of the link in full duplex operation.

Flow control is identical in MAC and PHY interface modes.

Reception Buffer Flow Control - Half Duplex Mode

In low rate modes, the reception buffer may fill faster than the data flow over the VDSL link. When the free space in the buffer reaches the appropriate threshold, the Ethernet interface in half duplex generates back pressure, other transmitters on the Ethernet segment stop trying to transmit and no more messages are added to the reception

buffer. The Ethernet interface stops applying back pressure when the free space in the reception buffer reaches the appropriate threshold.

The Ethernet interface starts generating back pressure after a legal inter-packet gap (IPG). If there are packets to transmit, they are transmitted without applying the back off algorithm. If a collision occurs, only the minimum IPG (9.6 µs) is inserted before retransmission. If packets are received over the VDSL link after the transmission buffer is emptied, they may be appended to the continuous preamble or another IPG may be inserted before they are transmitted.

If the reception buffer becomes full, the Ethernet generates a collision by transmitting a jamming pattern. This collision is detected by the transmitter of the current packet and the transmitter retransmits the packet at a later time. This prevents loss of data.

802.3*x* Flow Control - Full Duplex mode

In full duplex mode, the Ethernet interface implements IEEE 802.3*x* flow control, if it is enabled. The Ethernet interface must notify the other side (PHY or MAC) that flow control is enabled.

Flow control prevents forwarding of a packet to the link when it is enabled and a received packet meets the following conditions:

- It is received without errors.
- Its destination address (DA) is either of the following:
  - 01-80-C2-00-00-01
  - The programmed source address (SA)
- Its type is 88-08.
- Its MAC control opcode is 01.

When flow control is disabled, the decision to forward or discard a packet is determined by the appropriate register setting.

A pause packet parameter specifies how long transmission of a new packet is prevented. Whenever the reception buffer exceeds a programmable upper flow control threshold, a pause packet is sent with a parameter of $FFFF_H$. After a time period equal to $FFFF_H * 128$ bits, a pause disable packet is transmitted. When the reception buffer falls below a lower flow control threshold, a pause packet with a parameter of 0_H is sent.

Transmission Buffer Flow Control

The transmission buffer may fill faster than it is emptied, when traffic on the Ethernet segment slows access to less than the VDSL link rate. When the number of free bytes in the FIFO drops below a programed threshold, the Ethernet interface signals the remote Ethernet interface to stop transmitting data over the VDSL link.

When this happens, the remote Ethernet interface reception buffers may become full. The back pressure algorithm may be implemented locally, to prevent overflow.

Adjustable Back Off Algorithm

Ethernet transmitter activity is increased by resetting the collision counter for a packet after less than the standard 16 retries. This resets the exponential back off algorithm, thereby allowing insertion of shorter IPGs than are possible using the algorithm specified by the IEEE 802.3 standard.

Packets are not discarded and retransmission is continued indefinitely.

The number of retries can be set to 16, 8, 4 and 2. If back pressure is enabled, the algorithm is limited to one retry, with a minimum back off of one IPG, regardless of the number of retries programmed.

7.6.10.1.5 Bridging Control

The Ethernet interface learns the MAC address of attached Ethernet devices in real time. It searches for the source address of an incoming packet in the address table. If it is not found, the Ethernet interface waits until the end of the packet to verify that it is has no errors, and updates the address table. The address table can be used to filter addresses of packets whose source and destination are on the same side of a link.

The Ethernet interface forwards an incoming packet from the Ethernet link to the digital transceiver link according to the destination address as follows:

- If the destination address is Unicast and the address is in the address table, the packet is discarded.
- If the destination address is Unicast and the address is not in the address table, the packet is forwarded to the digital transceiver link
- If the destination address is a broadcast address, the packet is forwarded on the digital transceiver link.

If an address recognition cycle fails because more than 32 addresses entered the address table, the packet is treated as unknown and forwarded to the digital transceiver link.

When an address moves from one side of the link to the other, the Ethernet interface detects the change and updates its address table accordingly.

Aging can be fully automatic or triggered by the micro controller. The micro controller can ask for invalidation of address table entries.

The Ethernet interface keeps a record of the relative age of an address by setting a bit in the address table whenever it receives a packet. The Ethernet interface scans the address table during programmable time intervals and resets this bit. If, in an interval, the bit remained clear, this station did not transmit any packet in this period, and the address is removed from the table.

The embedded controller can be programmed to trigger aging.

The micro controller can read up to 32 entries in the address table. It reads the source address through a protocol and an address counter points to an entry in the table. The counter is incremented on each read and can be reset to point to the first address.

7.6.10.1.6 Ethernet Management Information Base (MIB) Support

Simple Network Management Protocol (SNMP) is used for network management and to monitor network device performance.

Remote Network Monitoring (RMON) provides standard information to monitor, analyze, and troubleshoot a group of distributed local area networks (LANs) and network devices from a remote site. RMON defines the information that any network monitoring system can provide. It is an extension of SNMP, specified as part of the Management Information Base (MIB) in RFC 1757.

Although the digital transceiver transparently transfers Ethernet packets across VDSL media, it does not fully implement standard MAC functionality. Ethernet statistics it gathers are a subset of standard RMON MIB Ethernet statistics, and include only implemented functionality. All counters are 32 bits wide, and are cleared after they are read.

7.6.10.1.7 Loop Back Options

The digital transceiver supports the following loop back options (illustrated in **Figure 22**):

- Local loop back returns data from the Ethernet Interface input pins to the Ethernet Interface output pins through the local device. In this case, no data is transmitted over the VDSL line during local loop back.
- Remote loop back returns data through the remote device, over the VDSL link. In this case, the data path includes the full data paths in the local device and in the remote device.

The type of loop back is set by the **LB** field (bits 7:6) in the **MAIN_MODE** register at **$8F01_H$**.

To operate in local loop back mode, do the following in the local LT:

1. Set the **LB** bits in the **MAIN_MODE** register to 01_B.
2. Force the **SPEED** (bit 13 in the **BMCR** SMI register at address 00_H) to 10 Mbit/s (0) or 100 Mbit/s (1).
3. Force the **DUPLEX** (bit 8) in the **BMCR** SMI register to Full Duplex mode (1).

For remote loop back, configure the remote NT as follows:

1. Set the **LB** bits in the **MAIN_MODE** register to 10_B.
2. If the remote NT is configured as an MII MAC, reconfigure it as an RMII MAC to prevent differing transmission and reception clocks during loop back.

For test purposes, remote loop back can be activated from the local LT device using the VOC message channel. See **“Accessing the Remote Transceiver” on Page 123**.

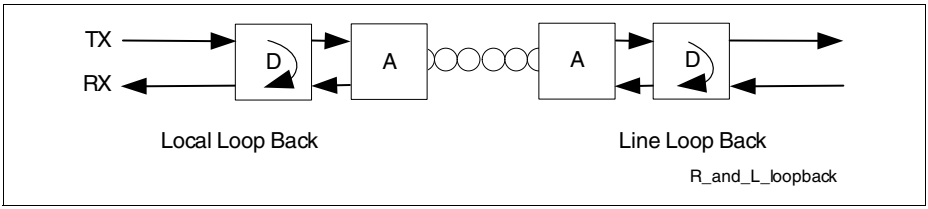


Figure 22 Remote Loop Back and Local Loop Back

7.6.11 The Dying Gasp Mechanism

To monitor voltage drops in the DSLAM at the NT end, do the following:

1. Connect the external voltage drop sensing signal to the **WAKEUP_D** pin at the NT end. When this signal is asserted, a dying gasp indication is sent to the LT end.
2. At the LT end, poll bit 7 of the **GEN_STATUS2** (**8F10$_H$**) register. After it is read, this bit is cleared to 0.

7.6.12 External Status Signals (LEDs)

When the EOC interface is disabled (default), LEDs on its pins and signals show the status of the link, RS errors and network activity. These LEDS are driven on the EOC_RDATA, EOC_REN and EOC_TEN pins, respectively (see **Table 27 “Configuration Pins” on Page 81**.

- Link Status - Set to high (ON) when a VDSL link is established, otherwise it is set to low (OFF). This indication is driven on the EOC_RDATA pin.
- RS Error - Set to high (ON) for a period of 25 ms each time uncorrectable frames are detected by the RS mechanism. This indication is driven on the EOC_REN pin.
- Network activity - Set to high (ON) for a period of 25 ms each time Ethernet packets accumulate in the TPS-TC layer buffers. This indication is driven on the EOC_TEN pin.

To enable LEDs, disable the EOC interface by clearing the EOC_EN bit (bit 2 of the LINK_MODE register at **8F02$_H$**) to 0.

8 Operation – Line Driver

This section describes the following:

- **Calculating Line Driver Gain in a VDSL Application**

8.1 Calculating Line Driver Gain in a VDSL Application

To achieve typical power of 10 dBm for VDSL on the line, you must determine the insertion loss of the hybrid and the transmitter filter (see **Figure 23**). To match the power impedance of the transmission filter, insert additional resistors in each part of the transmitted signal. The resistors R_1 + R_2 must equal the internal impedance of the transmission filter. Thus, 3 dB power is dissipated at these resistors. Another 3 dB is dissipated due to the hybrid implementation loss L_{impl}.

Transmission power at the line driver output pins is calculated as follows:

$$Pout[dBm] = 10dBm + 3dBm + L_{imp1} + L_{ins1} + L_{ins2} \quad [dBm]$$

$$Pout[dBm] = 10dBm + 6dBm + 0,5dBm + 0,5dBm = 17dBm$$

where:

- P_{out} : Transmit power at the line driver output pins.
- L_{ins1}: Insertion loss transmit filter (dependent on the filter device, typ. 0.5 dB)
- L_{ins2}: Insertion loss hybrid (dependent on the hybrid device, typ. 0.5 dB)

The necessary rms voltage $V_{L,rms}$ at the line driver output pins is calculated as follows:

$$V_{rms} = \sqrt{Pout[W] \times (R_1 + R_2 + R_e)} \quad [V]$$

$$V_{rms} = \sqrt{50mW \times (80\Omega)} = 2V \quad [Vrms]$$

with :

$$(R_1 + R_2 + R_e) = 20\Omega + 20\Omega + 40\Omega = 80\Omega \quad [\Omega]$$

$$Pout[W] = 1mW \times 10^{\left(\frac{Pout[dBm]}{10}\right)} \quad [W]$$

$$Pout[W] = 1mW \times 10^{\left(\frac{17}{10}\right)} = 50mW \quad [W]$$

A crest factor (CF) of 3.5 for single carrier VDSL must also be considered. Calculate peak-to-peak voltage $V_{L,p-p}$ at the line driver output to achieve the required transmission power as follows:

$$V_{L,p-p} = 2 \times CF \times V_{rms} \quad [V]$$

$$V_{L,p-p} = 2 \times 3,5 \times 2V = 14V \quad [V]$$

The gain of the line driver circuitry has to be adjusted accordingly to achieve $V_{L,p-p}$.The output peak-to-peak voltage of the PEB 22811 is 4 V. Thus, the maximum voltage swing V_{in} at the line driver's input is 4 V. In order to achive the desired output voltage of 14 V ($V_{L,p-p}$), the gain has to be set to G = 3.5.

The gain of the line driver is determined by resistors R_F and R_G as follows:

$$G = 1 + \frac{R_F}{R_G}$$

With R_F= 850 R and R_Q= 2 * R_G = 2 * 340 R = 680 R, the desired gain of 3.5 can be adjusted.

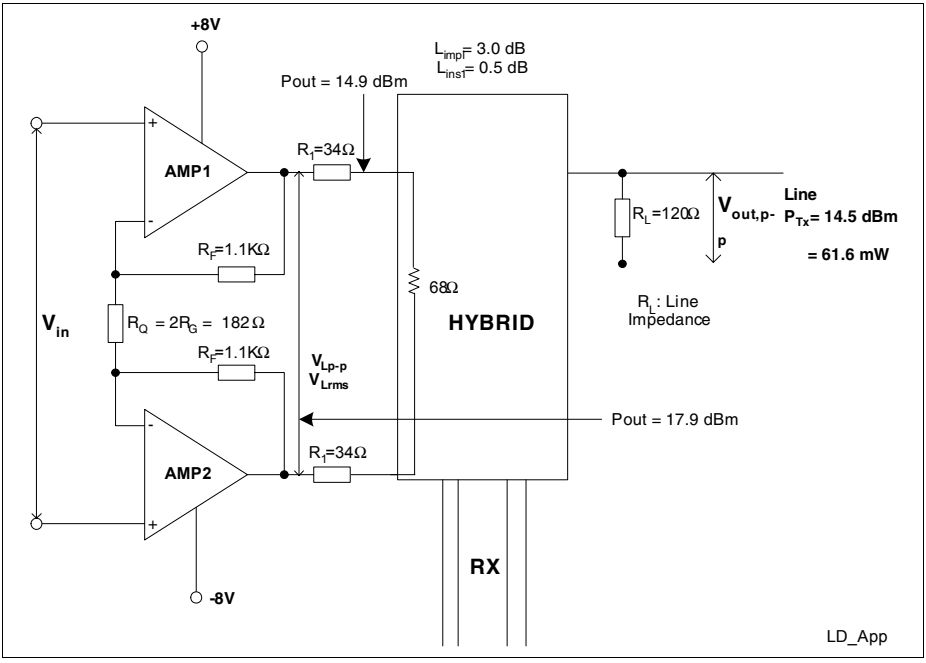


Figure 23 VDSL Line Driver Application

9 Interfaces

This chapter describes the following interfaces:

9.1 JTAG Interface (Boundary Scan)

Boundary Scan is implemented according to the IEEE 1149.1 standard. **Table 41** shows the signals used for this purpose.

Table 41 Boundary Scan Interface

Symbol	Name	Function
TRST	Test Reset	TAP Controller with instruction, bypass and identification register
TCK	Test Clock	
TMS_D	Digital Test Mode Select	
TMS_A	Analog Test Mode Select	
TDI_D	Digital Test Data IN	Boundary scan chain
TDI_A	Analog Test Data IN	
TDO_D	Digital Test Data Out	
TDO_A	Analog Test Data Out	

The Test Clock input pin (TCK) provides the clock for the test logic. Serial test instructions and data are received by the test logic on Test Data Input (TDI_D for digital and TDI_A for analog). Test Data Output (TDO_D for digital and TDO_A for analog) is the serial output for test instructions and data from the test logic.

The data pins (TDI_D, TDO_D, TDI_A and TDO_A) ensure serial movement of test data through the digital or analog circuit. The signal received at the Test Mode Select (TMS_D for digital and TMS_A for analog) input pin is decoded by the internal TAP controller to control test operations.

To perform a boundary test of the entire integrated circuit, connect the Digital and Analog Blocks externally. Do one of the following:

- Connect TDI_A to TDO_D
- Connect TDO_A to TDI_D

To select a test mode, serially load one of the 3-bit instruction codes shown in **Table 42** into the JTAG instruction register via the TDI (TDI_D or TDI_A) pin, least significant byte first.

Table 42 Boundary Scan Test Mode Selection

3-bit Instruction Code	Test Mode Selected
000	EXTEST (external testing)
001	INTEST (internal testing)
010	SAMPLE/PRELOAD (snapshot testing)
011	IDCODE (reading ID code)
100	CLAMP
101	HIGHZ
111	BYPASS (bypass operation)
others	For test purposes

See **"JTAG Interface" on Page 267** for the AC characteristics of the JTAG interface signals.

Note: A standard `.bsdl` file that describes the JTAG pins is available from Infineon.

9.2 Management Interfaces

Management interfaces include:

- **"Serial Host Interface" on Page 135**
- **"Parallel Host Interface" on Page 136**
- **"MII Serial Management Interface (SMI)" on Page 142**

9.2.1 Serial Host Interface

The serial UART port can be used to access internal registers. The UART rate is 19200 baud.

The serial port commands (listed in **Table 43**) use an ASCII based protocol as follows:

- The address may have up to four characters.
- The next field may be up to two characters.
- A command line has the following form: `opcode address parameter <Enter>`
- All values are in hexadecimal notation.
- The opcode is always followed by an address field.
- A space character separates fields.
- An `<Enter>` character ends the input command.

- For the WR, OR and ND opcodes the parameter is the data used for the operation. For example: To write $A4_H$ to address $8C0B_H$, send the string:
  `WR 8C0B A4 <Enter>`
- The parameter is optional for the RD opcode. If used, it specifies the number of consecutive bytes to read. The default value of 1 is not needed. For example: To read four bytes, starting at address $8C0B_H$, send the string: `RD 8C0B 4 <Enter>`

Table 43 Serial Port Commands

Opcode	Address	Parameter	Notes
WR	address	Data	Write data to RAM at specified address
RD	address	Number of Bytes (optional)	Read data from RAM at specified address
OR	address	Data	OR data with data address
ND	address	Data	AND the data with data address
RDE	address	Number of Bytes (optional)	Read data from EEPROM at specified address
WRE	address	Data	Write data from EEPROM at specified address
PR	address	Buffer Size in Bytes	After the PR (program size) is entered: • The modem acknowledges with A. • Buffer content is copied into RAM. • The modem indicates that copy is finished by issuing O.

9.2.2 Parallel Host Interface

The parallel port enables the external host to read and write to the registers. It is an asynchronous port that enables the host to perform read or write cycles of up to four bytes in each cycle. The 64-Kbyte internal memory space can be accessed indirectly. The user writes the internal address to the address registers, the type of access to the command register and, for a write operation, the data to the data registers.

The parallel port has the following features:

- Asynchronous read and write access
- 120 ns for the fastest cycle
- 15-pin interface, plus one interrupt pin

9.2.2.1 Parallel Port Signals

Signals to the parallel port include address, data, chip select and read write strobes. **Figure 24** and **Figure 25** illustrate the timing of these signals in typical read and write

cycles, respectively. For detailed timing diagrams of read and write cycles, see **"Parallel Host Interface" on Page 271**.

Table 44 Parallel Port Signals

Name	Input/Output	Comment
PA3:PA0	Input	Parallel port address - See **Table 45**.
PD7:PD0	Input/Output	Parallel Data
$\overline{PCS}$	Input	Parallel Chip Select - Must be 0 for parallel port read or write operations.
$\overline{PWE}$	Input	Parallel port Write Enable - Data is latched when $\overline{PWE}$ is asserted (0). Valid only when $\overline{PCS}$ is also asserted (0).
$\overline{POE}$	Input	Parallel port Output Enable - Data is latched when $\overline{POE}$ is asserted (0). Valid only when $\overline{PCS}$ is also asserted (0).
$\overline{PINT}$	Output	Interrupt Request - Open drain output signal.

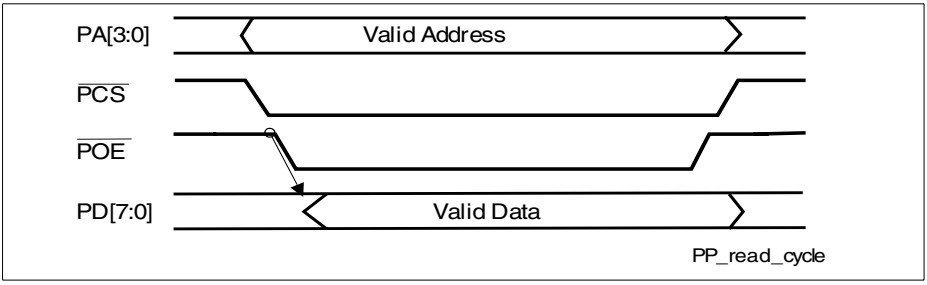


Figure 24 Typical Parallel Port Read Cycle

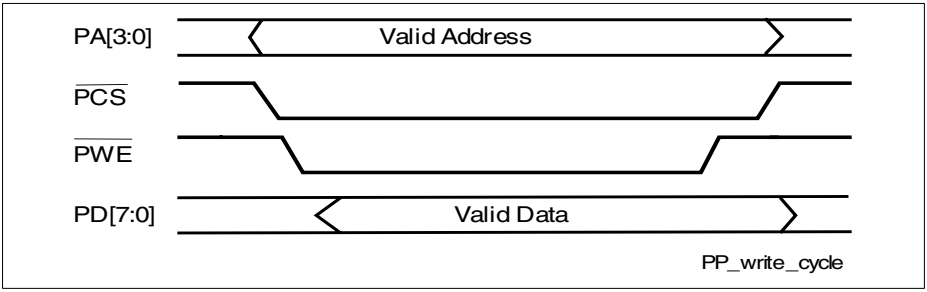


Figure 25 Typical Parallel Port Write Cycle

9.2.2.2 Parallel Port Registers

Table 45 shows the memory mapping of the parallel port registers and indicates the page on which its detailed description begins.

Table 45 Parallel Port Registers

Address (Hex)	Short Name	Long Name	Access	Pg
00	CMD	Host command for operation control	rw	138
01	CNT	Number of bytes to transfer counter	rw	139
02:03	ADDR	Address	rw	139
04:07	DAT	Data bytes, LSB to MSB	rw	139
08	INTR	Interrupt status	r	140
09	MASK	Interrupt mask	rw	140
0F	HIID	Host Interface (parallel port) ID	r	141

Host Command Register (CMD)

The CMD register controls the operation of the parallel port. Setting bit 1 (WR) starts the write operation, while setting bit 0 (RD) starts the read operation.

Before each read or write operation, the data (DAT at 04_H:07_H), address (ADDR at 02_H:03_H) and count (CNT at 01_H) registers must be set.

CMD
Host Command Register (00_H) Reset Value: 00_H

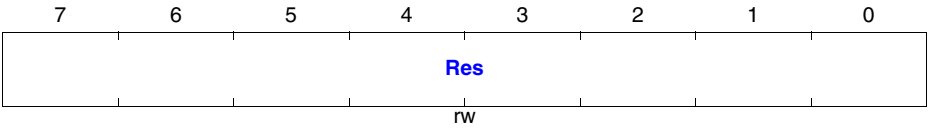
7	6	5	4	3	2	1	0
Res						WR	RD
rw						rw	rw

Field	Bits	Type	Description
Res	7:2	rw	Reserved.
WR	1	rw	Trigger for write operation. 0 No operation. 1 Start write operation.
RD	0	rw	Trigger for read operation. 0 No operation. 1 Start read operation.

Byte Counter Register (CNT)

The byte counter (**CNT**) register contains the number of bytes to be transferred to or from the parallel port. The content of **CNT** should not be set to 0.

CNT
Byte Counter Register **(01_H)** **Reset Value: 00_H**

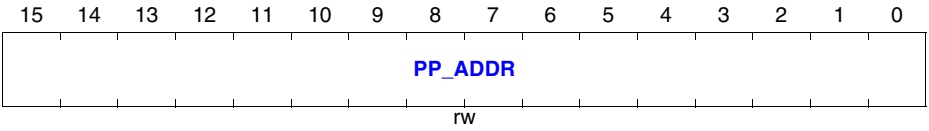


Field	Bits	Type	Description
BYTE_COUNT	7:0	rw	Byte count to transfer to or from parallel port.

Address Register (ADDR)

The 16-bit **ADDR** register contains the internal address of the parallel port.

ADDR
Address Register **(02_H:03_H)** **Reset Value: 00_H**

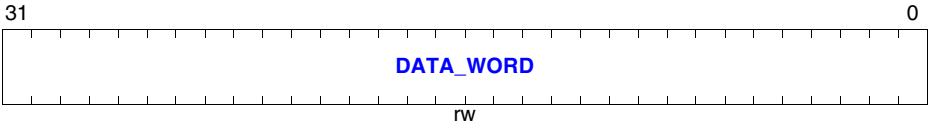


Field	Bits	Type	Description
PP_ADDR	15:0	rw	Internal address of the parallel port.

Data Word Register (DAT)

The 32-bit **DAT** register contains the data word.

DAT
Data Word Register **(04_H:07_H)** **Reset Value: 00_H**

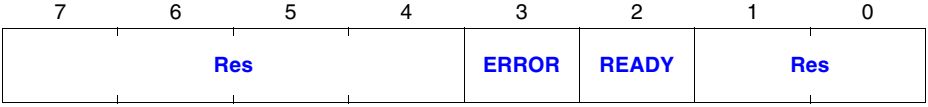


Field	Bits	Type	Description
DATA_WORD	31:0	rw	Data word of the parallel port.

Interrupt Request Register (INTR)

The **INTR** register indicates the cause of an interrupt on the $\overline{\text{PINT}}$ signal. This register can also be polled while the interrupt is masked by the MASK register ($09_{H)}$.

INTR
Interrupt Request Register (08_H) Reset Value: 04_H

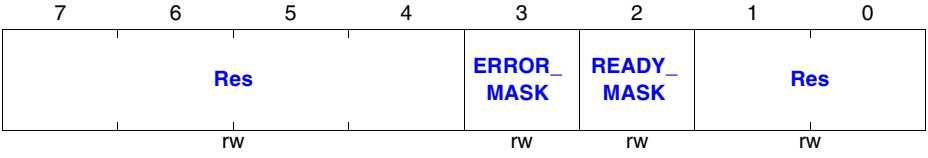


Field	Bits	Type	Description
Res	7:4	rw	Reserved.
ERROR	3	sc	Flag indicating an attempt to access the parallel port when it was busy, before the READY bit (bit 0) was set to 1. Cleared on read. 0 No access error. 1 Access error. Attempt to access parallel port when it was busy.
READY	2	sc	Flag indicating the parallel port is ready for a new command. Cleared on read. 0 Parallel port is not ready. 1 Parallel port is ready for a new command.
Res	1:0	rw	Reserved

Interrupt Mask Request Register (MASK)

The **MASK** register masks the causes of an interrupt on the $\overline{\text{PINT}}$ signal.

MASK
Interrupt Mask Request Register (09_H) Reset Value: 00_H

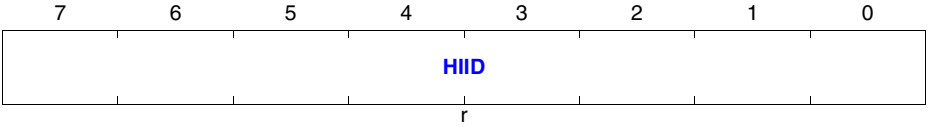


Field	Bits	Type	Description
Res	7:4	rw	Reserved.
ERROR_MASK	3	rw	Control generation of $\overline{\text{PINT}}$ signal on error. 0 No signal generated by error. 1 Error generates $\overline{\text{PINT}}$ signal.
READY_MASK	2	rw	Control generation of $\overline{\text{PINT}}$ signal by ready condition. 0 No signal generated by ready condition. 1 Ready condition generates $\overline{\text{PINT}}$ signal.
Res	1:0	rw	Reserved

Host Interface ID (HIID)

The **HIID** register specifies the ID of the parallel port (host interface).

HIID
Host Interface ID **(0F$_H$)** **Reset Value: 11$_H$**



Field	Bits	Type	Description
HIID	7:0	r	ID of the parallel port.

9.2.2.3 Indirect Read Cycle

To execute a read cycle, the host must first verify that the CMD register (at 00$_H$) is equal to 00$_H$. Next, the host loads the internal address into the 16-bit ADDR register (at 02$_H$:03$_H$). The number of bytes to be read should be set in the CNT register (at 01$_H$). Finally, the read cycle is triggered by setting the RD bit (bit 0) in the CMD register.

When the internal operation is finished, the embedded controller updates the 32-bit DAT register (at 04$_H$:07$_H$) with the requested data. The number of bytes read is added to the ADDR register and subtracted from the CNT register.

The embedded controller then clears the CMD register to 0. After the host polls the CMD register to confirm that it is cleared to 00$_H$, it can read data from the DAT register.

Data is loaded to the DAT register one byte at a time, LSB first, regardless of the internal address from which the bytes are read. Up to four bytes are fetched in each read cycle, even if the CNT register specifies more than four. To invoke a new read cycle that fetches up to four more bytes of data, the host must set the RD bit in the CMD register again. This process continues until CNT reaches zero.

9.2.2.4 Write Cycle

To execute a single write cycle, the host should first verify that the CMD register (at 00_H) is cleared to 0. Next the host should set the 16-bit ADDR register (at 02_H:03_H) with the internal address and load up to four bytes of data to be written into the 32-bit DAT register (at 04_H:07_H). The CNT register (at 01_H) must specify the number of bytes to be written. The write cycle is triggered by setting the WR bit (bit 1) in the CMD register.

When a write cycle begins, data is written from the DAT register, one byte at a time, LSB first, regardless of the internal address to which bytes are written.

When the internal operation is finished, the embedded controller adds the number of bytes written (up to four) to the ADDR register and subtracts the same number from the CNT register.

The embedded controller then clears the CMD register to 0.

Even if the CNT register specifies more than four bytes, only four bytes are written in each write cycle. To invoke a new write cycle and write up to four more bytes of data, the host must first poll the CMD register until it is cleared to 00_H, indicating that the command was completed. The host must then update the DAT register and set the WR bit of the CMD register. This process continues until CNT reaches zero.

9.2.3 MII Serial Management Interface (SMI)

The section describes the standard MII Serial Management Interface (SMI).

When the digital transceiver is configured as an Ethernet PHY, the SMI acts as a slave and may be used by many PHY devices. In this case, it contains standard (IEEE 802.3) and proprietary SMI registers that enable basic control functions of Ethernet PHY and access to internal memory space through the SMI interface.

When the digital transceiver is configured as an Ethernet MAC, a single PHY device may be connected to this port and controlled through it. In this case, internal memory space is not accessible through this interface.

Table 46 and **Table 47** show the signals that support SMI and their functions.

Table 46 SMI Signals in MAC Interface Mode

Signal	Direction	Function
MDCO	OUT	MII Serial Management Data Clock generated digital transceiver when it is configured as a MAC device. • This signal is not synchronized with other network interface clocks. • Minimum MDC high/low values is 160 ns. • Minimum MDC period is 400 ns.
MDIO	IN/OUT	MII Serial Management Data Input/Output • Bidirectional, tristate signal • Requires an external pull-up resistor • Synchronized with the MDC signal

Table 47 SMI Signals in PHY Interface Mode

Signal	Direction	Function
MDCI	IN	MII Serial Management Data Clock - Generated by the MAC device. • This signal does not have to be synchronized with RX_CLK or TX_CLK. • Minimum MDCI high/low values is 160 ns. • Minimum MDCI period is 400 ns.
MDIO	IN/OUT	MII Serial Management Data Input/Output • Bidirectional, tristate signal. • Requires an external pull-up resistor. • Synchronized with the MDC signal.

9.2.3.1 SMI Frame Structure

The structure of the Serial Management Interface (SMI) frames is shown in **Table 48**.

Table 48 MII Management Serial Interface Frame Structure

Preamble	SFD	OP	PHY Address	Register Address	Turnaround	Data	Idle
1…1	01	10 = read 01 = write	AAAAA	RRRRR	TT	DDDD DDDD DDDD DDDD	Z

Serial Management Interface frames contain the following fields (see also **Table 48**):

- **Preamble** - A string of at least 32 consecutive **ones** (1) on MDIO, optional.
- **SFD** - Start of Frame Delimiter.
- **OP** - Opcode.
- **PHY Address -** Defined by configuration pins as described in **"Configuration Pins During Hard Reset" on Page 81**.
- **Register Address** - Register to be read from or written to.
- **Turnaround -** Idle time that enables the MDIO driver to switch from the MAC to the PHY for register reads. The MAC drives 10 during this time for writes, or ZZ for reads. During turnaround, no device should drive MDIO. The PHY begins driving 0 on the second bit of the turnaround period.
- **Data -** 16-bit write or read data, as determined by the opcode.
- **Idle -** The MAC and the PHY put MDIO in tristate during transfer of this bit, and the pull-up resistor pulls it to a logical **1.**

9.2.3.2 SMI Registers (PHY Mode)

SMI registers include the following:

- Standard registers (addresses 00_H through 05_H) include the SMI standard registers described in the IEEE 802.3 standard to support basic control and status, PHY identifier and automatic negotiation operations.
- Internal memory access registers (addresses 10_H through 12_H) enable an external host to access registers in internal memory space.
- Extended PHY capabilities registers (addresses 13_H through 14_H) support proprietary PHY capabilities.

Table 49 shows memory mapping and the location of detailed descriptions of the SMI registers in PHY mode. For detailed descriptions of each register, see the page indicated in the table, in the "**Detailed Description of SMI Registers**" section.

Table 49 Serial Management Interface (SMI) Registers (PHY Mode) (page 1 of 2)

SMI Address	Mnemonic	Register Description	Pg
00_H	**BMCR**	16-bit Basic Mode Control	**146**
01_H	**BMSR**	16-bit Basic Mode Status	**148**
02_H:03_H	**OUI**	32-bit Organizationally Unique Identifier	**149**
04_H	**ANAR**	Automatic Negotiation Advertisement	**150**
05_H	**ANLPAR**	Automatic Negotiation Link Partner Ability	**151**
08_H:$0F_H$	-	Not implemented	-
10_H	**IADDSR**	Internal Address Space	**152**
11_H	**OPCDR**	Opcode	**153**

Table 49 Serial Management Interface (SMI) Registers (PHY Mode) (page 2 of 2)

SMI Address	Mnemonic	Register Description	Pg
12_H	RSLTR	Result	154
13_H:$1F_H$		Reserved	-

9.2.3.3 Accessing Internal Memory Space through the SMI

The Serial Management Interface (SMI) uses three 16-bit proprietary OEM registers in the SMI address space to gain access to the internal address space. The function of each OEM register is:

- Address pointer into the internal address space
- Opcode/status register
- Result register

A write transaction into an internal register is performed as follows:

1. The host writes the internal address into the internal address register.
2. The host writes eight bits of data into bits 15:8 of the OPCDR register (at 11_H), setting the Write opcode register bit to **1**.
3. The SMI asserts the BUSY status bit (bit 7) in the OPCDR register.
4. When the write operation into the internal register is complete, the SMI clears the BUSY status bit.

Note: The user must verify that a new write transaction does not override an old write or read command. To avoid overriding commands, poll the BUSY status bit to verify that it is cleared before any new transaction with the internal registers.

The sequence of operations of a read transaction from an internal register is:

1. The host writes the internal address into the address register.
2. The host sets the Read opcode register bit to 1.
3. The SMI asserts the BUSY status bit.
4. The host polls the opcode register to check the Busy status bit. Once the Busy status bit is clear, the requested data in the Result register is valid.

9.2.3.4 SMI Registers (MAC Mode)

The 16-bit internal registers provide access to the MII SMI register set of the attached Ethernet PHY. Access to these registers triggers the appropriate access process through the MII SMI access registers. This simplifies access of a host to the standard MII SMI register set.

Table 50 shows memory mapping and the location of detailed descriptions of the SMI registers in MAC mode. For detailed descriptions of each register, see the page indicated in the **Detailed Description of SMI Registers** section.

Table 50 Serial Management Interface (SMI) Registers (MAC Mode)

SMI Address	Mnemonic	Register Description	Page
00_H	BMCR	16-bit Basic Mode Control	146
01_H	BMSR	16-bit Basic Mode Status	148
02_H:03_H	OUI	32-bit Organizationally Unique Identifier	149
04_H	ANAR	Automatic Negotiation Advertisement	150
05_H	ANLPAR	Automatic Negotiation Link Partner Ability	151

9.2.4 Detailed Description of SMI Registers

This section describes the SMI registers in detail.

Basic Mode Control Register (BMCR)

The 16-bit **BMCR** register sets parameters for the basic operation of the serial management interface (SMI).

An external host can access this register, via the SMI interface at the Standard compliant SMI address of 00_H.

BMCR
Basic Mode Control Register (00_H) Reset Value: 1000_H

15	14	13	12	11	10	9	8
RESET	LPBK	SPEED	ANEGEN	Res	ISOLATE	RESANEG	DUPLEX
sc	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
COL	Res						RESET_ DISABLE
rw	rw						rw

Field	Bits	Type	Description
RESET	15	w	Trigger soft reset of all SMI registers. This bit is automatically cleared after the action is complete. 0 No reset, normal operation. 1 If **RESET_DISABLE** (bit 0) is cleared to 0, all SMI registers assume their default values.

Field	Bits	Type	Description
LPBK	14		Enable echo loop back in which data is echoed back on the Ethernet interface pins without intervention by logic. 0 Disable echo loop back. 1 Enable echo loop back.
SPEED	13		Speed specification bit. 0 10 Mbit/s 1 100 Mbit/s
ANEGEN	12		Automatic negotiation (ANEG) enable bit. 0 Disable ANEG procedure. 1 Enable ANEG procedure.
Res	11		Reserved.
ISOLATE	10		Isolate the PHY from the Ethernet interface. In this state, a high impedance is applied to all Ethernet pins except MDIO and MDC. 0 No isolation. IC responds to normal management. 1 Isolate PHY.
RESANEG	9		Restart the automatic negotiation (ANEG) procedure. 0 Do not start ANEG. 1 Restart ANEG.
DUPLEX	8		Set duplex mode. 0 Half duplex mode. 1 Full duplex mode.
COL	7		Enable or disable collision test. 0 Collision test disabled. 1 Collision test enabled.
Res	6:1		Reserved.
RESET_DISABLE	0		Enable or disable the effect of the **RESET** bit (bit 15) on SMI registers. 0 Effect of **RESET** bit disabled. 1 Effect of **RESET** bit enabled.

Basic Mode Status Register (BMSR)

The 16-bit **BMSR** register contains the status of basic operation of the serial management interface (SMI).

An external host can access this register, via the SMI interface at the Standard compliant SMI address of 01_H.

BMSR
Basic Mode Status Register **(01_H)** **Reset Value: 7849_H**

15	14	13	12	11	10	9	8
Res	100F	100H	10F	10H		Res	
r	r	r	r	r		r	

7	6	5	4	3	2	1	0
Res	MFPS	ANEG_ STATUS	REMOTE_ ERR	ANEG ABILITY	LINK_ STATUS	JABBER	EXTEND
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Res	15	r	Reserved.
100F	14	r	Ethernet interface support flag for 100 Mbit/s full duplex operation. 0 100 Mbit/s full duplex operation not supported. 1 100 Mbit/s full duplex operation supported.
100H	13	r	Ethernet interface support flag for 100 Mbit/s half duplex operation. 0 100 Mbit/s half duplex operation not supported. 1 100 Mbit/s half duplex operation supported.
10F	12	r	Ethernet interface support flag for 100 Mbit/s full duplex operation. 0 10 Mbit/s full duplex operation not supported. 1 10 Mbit/s full duplex operation supported.
10H	11	r	Ethernet interface support flag for 100 Mbit/s full duplex operation. 0 10 Mbit/s half duplex operation not supported. 1 10 Mbit/s half duplex operation supported.
Res	10:7	r	Reserved.
MFPS	6	r	Management frames preamble suppression. This bit is always 1 to indicate that the PHY accepts management frames when the preamble is suppressed.
ANEG_STATUS	5	r	Automatic negotiation procedure status flag. 0 Automatic negotiation procedure is not complete. 1 Automatic negotiation procedure is complete.

Field	Bits	Type	Description
REMOTE_ER R	4	r	Remote fault indicator. 0 No remote fault condition detected. 1 Remote fault condition detected.
ANEGABILITY	3	r	Automatic negotiation ability indicator. 0 PHY is not able to perform automatic negotiation. 1 PHY is able to perform automatic negotiation.
LINK_STATUS	2	r	Link status flag. This bit holds the status of the VDSL link. In MAC mode, this bit indicates an Ethernet link. In PHY mode, this bit indicates a VDSL link. 0 Link is down. 1 Link is up.
JABBER	1	r	Jabber detection flag. 0 No jabber condition detected. 1 Jabber condition detected.
EXTEND	0	r	Always 1 to indicate that the PHY supports an extended register set.

Organizationally Unique Identifier (OUI) Register (OUI)

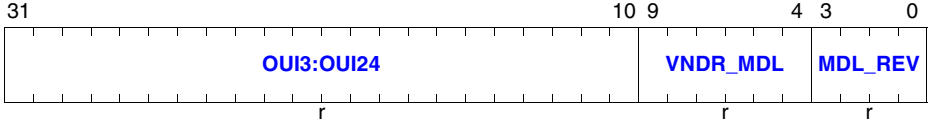
This 32-bit PHY identifier register holds a unique identifier for the digital transceiver consisting of 22 of the 24 bits of the Organizationally Unique Identifier (OUI), the vendor model number (six bits) and the model revision number (four bits). The two most significant bits of the OUI are ignored. The IEEE standard calls these bits 1 and 2.

A PHY may return a value of zero in each of the 32 bits of the PHY identifier if desired. The PHY identifier supports network management.

The OUI assigned to Infineon by the IEEE is 00 0319_H.

An external host can access this register, via the SMI interface at the Standard compliant SMI address of 02_H:03_H

OUI
Organizationally Unique Identifier (OUI) Register (02_H:03_H) **Reset Value: 000C 6421_H**



Field	Bits	Type	Description
OUI3:OUI24	31:10	r	22 least significant bits of the OUI register. MSB to LSB. 00 0000 0000 0011 0001 1001
VNDR_MDL	9:4	r	Vendor model number. MSB to LSB. 00 0010
MDL_REV	3:0	r	Model revision number. MSB to LSB. Incremented for all major device changes. 0001

Automatic Negotiation Advertisement Register (ANAR)

The 16-bit automatic negotiation advertisement register (**ANAR**) controls announcement of the flow control ability and Carrier Sense Multiple Access-Collision Detected (CSMA-CD) support.

An external host can access this register, via the SMI interface at the Standard compliant SMI address of 04_H.

ANAR
Automatic Negotiation Advertisement Register
(04_H) **Reset Value: $05E1_H$**

15	14	13	12	11	10	9	8
Res					FDFC	Res	100FD
		rw			rw	rw	rw

7	6	5	4	3	2	1	0
100HD	10FD	10HD	SELECTOR				
rw	rw	rw			rw		

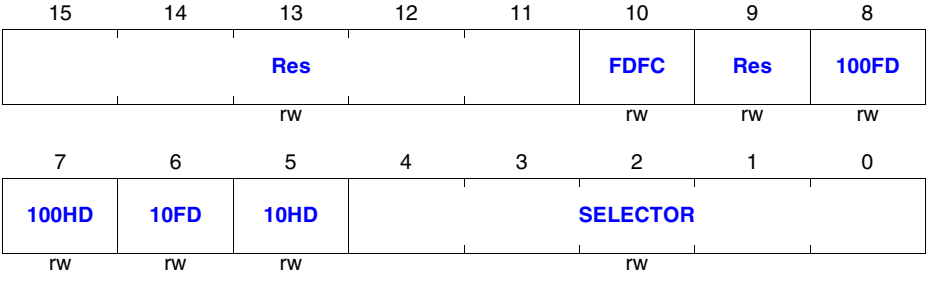
Field	Bits	Type	Description
Res	15:11	rw	Reserved.
FDFC	10	rw	Full duplex with flow control ability advertisement control. 0 Do not advertise. 1 Advertise full duplex mode with flow control ability.
Res	9	rw	Reserved
100FD	8	rw	100 Mbit/s full duplex mode advertisement control. 0 Do not advertise 100 Mbit/s full duplex mode. 1 Advertise 100 Mbit/s full duplex mode.

Field	Bits	Type	Description
100HD	7	rw	100 Mbit/s half duplex mode advertisement control. 0 Do not advertise 100 Mbit/s half duplex mode. 1 Advertise 100 Mbit/s half duplex mode.
10FD	6	rw	10 Mbit/s full duplex mode advertisement control. 0 Do not advertise 10 Mbit/s full duplex mode. 1 Advertise 10 Mbit/s full duplex mode.
10HD	5	rw	10 Mbit/s half duplex mode advertisement control. 0 Do not advertise 10 Mbit/s half duplex mode. 1 Advertise 10 Mbit/s half duplex mode.
SELECTOR	4:0	rw	Carrier Sense Multiple Access-Collision Detection support. 0 0001IEEE 802.3 CSMA-CD supported.

Automatic Negotiation Link Partner Advertisement Register (ANLPAR)

The 16-bit automatic negotiation link partner advertisement register (**ANLPAR**) controls announcement of the flow control ability and Carrier Sense Multiple Access-Collision Detected (CSMA-CD) support for the link partner.

ANLPAR
Automatic Negotiation Link Partner Advertisement Register
(05_H) **Reset Value: 0021_H**



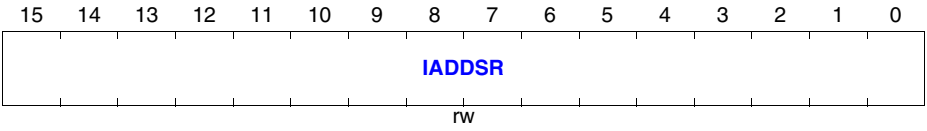
Field	Bits	Type	Description
Res	15:11	rw	Reserved.
FDFC	10	rw	Full duplex mode with flow control ability advertisement control. 0 Do not advertise. 1 Advertise full duplex mode with flow control ability.

Field	Bits	Type	Description
Res	9	rw	Reserved
100FD	8	rw	100 Mbit/s full duplex mode advertisement control. 0 Do not advertise 100 Mbit/s full duplex mode. 1 Advertise 100 Mbit/s full duplex mode.
100HD	7	rw	100 Mbit/s half duplex mode advertisement control. 0 Do not advertise 100 Mbit/s half duplex mode. 1 Advertise 100 Mbit/s half duplex mode.
10FD	6	rw	10 Mbit/s full duplex mode advertisement control. 0 Do not advertise 10 Mbit/s full duplex mode. 1 Advertise 10 Mbit/s full duplex mode.
10HD	5	rw	10 Mbit/s half duplex mode advertisement control. 0 Do not advertise 10 Mbit/s half duplex mode. 1 Advertise 10 Mbit/s half duplex mode.
SELECTOR	4:0	rw	Carrier Sense Multiple Access-Collision Detection support. 0 0001IEEE 802.3 CSMA-CD supported.

Internal Address Space Register (IADDSR)

The external host writes to the 16-bit **IADDSR** register the pointer to the internal address that the next read or write command will access. The contents remain unchanged until the next external host access.

IADDSR
Internal Address Space Register **(10_H)** **Reset Value: 0000_H**

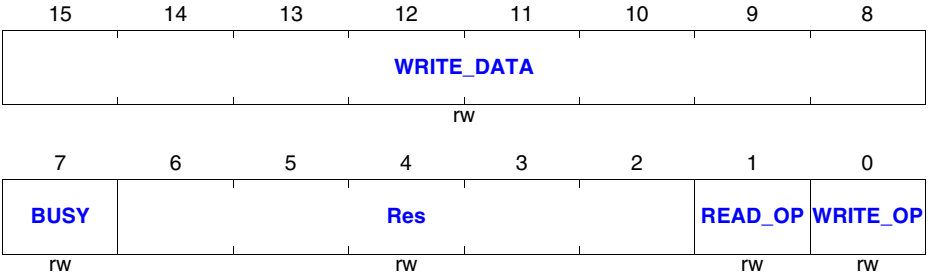


Field	Bits	Type	Description
IADDSR	15:0	rw	Pointer to next address accessed for write or read.

Opcode Register (OPCDR)

The 16-bit opcode register controls read and write operations to and from internal registers, and contains the data to write.

OPCDR
Opcode Register **(11_H)** **Reset Value: 0000_H**

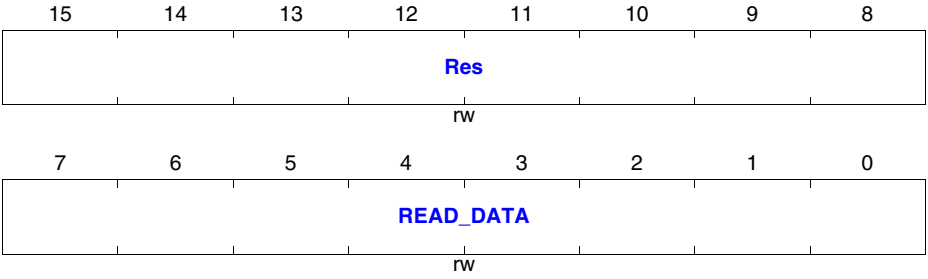


Field	Bits	Type	Description
WRITE_DATA	15:8	rw	Data to write to the internal register.
BUSY	7	rw	Read or write operation status indicator. For a read operation, indicates validity of **RSLTR** (12_H)register contents. 0 Not busy. Transaction complete. 1 Busy. Set to 1 after write.
Res	6:2	rw	Reserved
READ_OP	1	rw	Control read to specified internal register. 0 No operation. 1 Read the specified register into **RSLTR** (12H). Content is available when the **BUSY** bit (bit 7) is 0.
WRITE_OP	0	rw	Control write to specified internal register. 0 No operation. 1 Write the data that is in **WRITE_DATA** (bits 15:8).

Result Register (RSLTR)

Bits 15:8 of the 16-bit result register contains the last data read from the internal register specified by **IADDSR** (10_H). The data is available whenever the **BUSY** bit (bit 7) in the **OPCDR** register (11_H) is 0.

RSLTR
Result Register **(12_H)** **Reset Value: 0000_H**

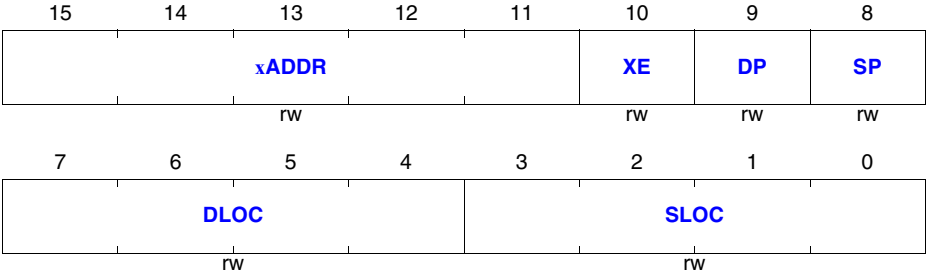


Field	Bits	Type	Description
Res	15:8	rw	Reserved
READ_DATA	7:0	rw	Data read from the internal register.

Status of Proprietary Information Register (SPR_PTR)

This 16-bit register contains information about where to find the actual speed and duplex parameters in the remote Ethernet PHY.

SPR_PTR
Status of Proprietary Information Register(13_H) **Reset Value: 0000_H**



Field	Bits	Type	Description
xADDR	15:11	rw	Address of register x, which contains the actual speed and duplex mode settings in the remote 10/100Base-TX PHY.

Field	Bits	Type	Description
XE	10	rw	Existence indicator for actual speed and duplex bits in the remote 10/100Base-TX PHY. 0 They do not exist. 1 They exist.
DP	9	rw	Duplex setting polarity. 0 Duplex setting polarity is normal. (1 is full duplex.) 1 Duplex setting polarity is negated. (1 is half duplex.)
SP	8	rw	Speed setting polarity. 0 Speed setting polarity is normal. (1 is 100 Mbit/s.) 1 Speed setting polarity is negated. (1 is 10 Mbit/s.)
DLOC	7:4	rw	Duplex bit location in register x, where 0 is the LSB.
SLOC	3:0	rw	Speed bit location in register x, where 0 is the LSB.

Status of Proprietary Information Register (SPR)

This 16-bit register contains the status of proprietary information.

SPR
Status of Proprietary Information Register(14_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8
RS	RD	VLINK	VFAIL	Res	CHKDONE	Res	Res
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
SP	DP	RMAC	Res				
rw	rw	rw			rw		

Field	Bits	Type	Description
RS	15	rw	Remote speed from register x. 0 10 Mbit/s. 1 100 Mbit/s.
RD	14	rw	Remote duplex mode setting from register x. 0 Half duplex. 1 Full duplex.

Field	Bits	Type	Description
VLINK	13		VDSL link status. 0 No link. 1 Link is active.
VFAIL	12	rw	VDSL failure sticky bit. 0 No VDSL failure. 1 VDSL failure since last clear.
Res	11	rw	Reserved.
CHKDONE	10:9	rw	Boot status. 0 No indication. 1 Boot check finished.
Res	8	rw	Reserved.
SP	7	rw	Local speed. 0 10 Mbit/s. 1 100 Mbit/s.)
DP	6	rw	Local duplex setting. 0 Half duplex. 1 Full duplex.
RMAC	5	rw	Remote configuration. 0 PHY. 1 MAC.
Res	4:0	rw	Reserved.

9.3 Network Interfaces

Network interfaces serve as the main data path between the IC and the outside world. Data received on these interfaces is output and transmitted over the VDSL line.

The following network interfaces are supported:

- **“MII Interface” on Page 156**
- **“xMII Interfaces” on Page 160**

9.3.1 MII Interface

In the Media Independent Interface (MII), the digital transceiver can be configured to act as a MAC or as a PHY.

9.3.1.1 MAC Configuration with MII Interface

Configuration as a MAC uses a Media Independent Interface (MII) to interface to an Ethernet PHY unit. This is common in CPE units in which the digital transceiver

interfaces between the VDSL link using the AFE, and the local Ethernet link using an Ethernet PHY. This MII interface is compatible with the IEEE 802.3 standard.

Figure 26 shows the block diagram when the digital transceiver is configured as a MAC and uses MII to interface to a PHY unit.

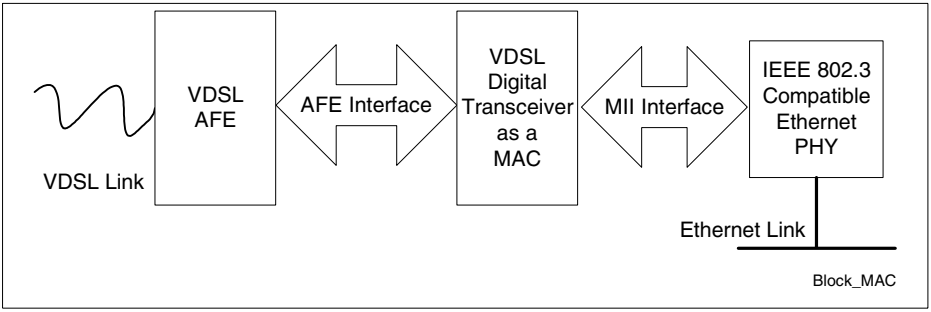


Figure 26 Block Diagram of a MAC Configuration with MII Interface to a MAC

Figure 27 shows the names of the signals used for the MII interface connection between the MAC and the PHY, with the corresponding MII signal and the direction of each. For mapping of these pins and signals, see **Table 2.4 "Pin and Signal Assignment in Different Modes" on Page 49**.

For more functional descriptions of the corresponding MII signals, see IEEE Standard 802.3. For AC characteristics of the MII signals, see **“MII Interface” on Page 274**.

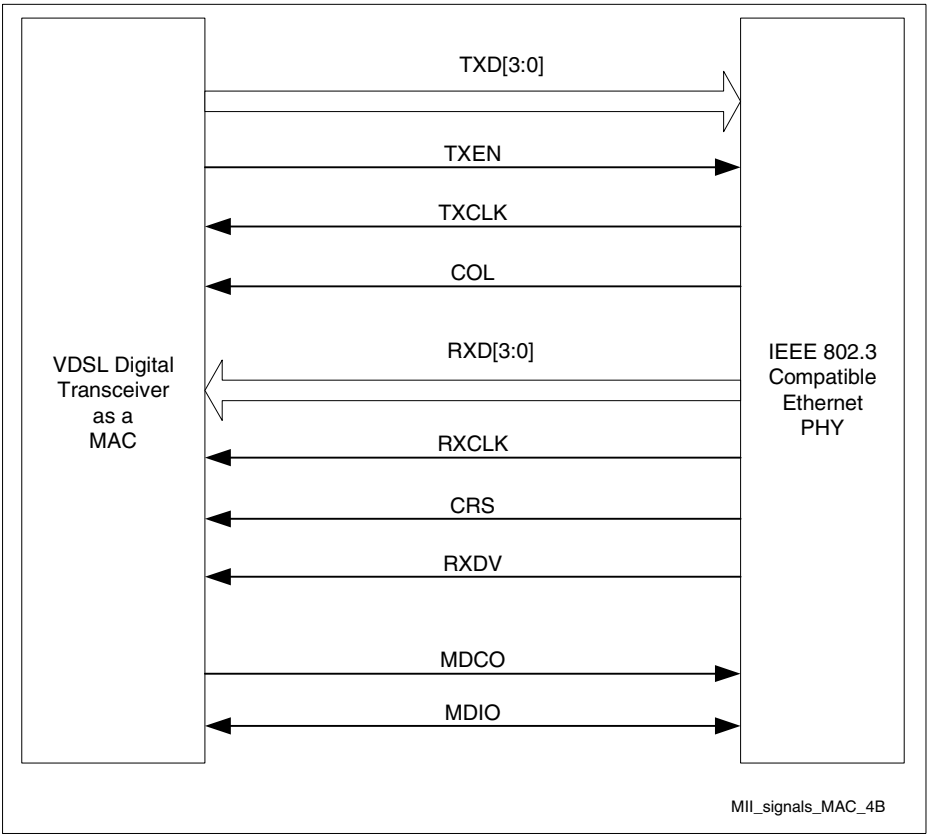


Figure 27 Signals for a MAC Configuration with MII Interface to a PHY

9.3.1.2 PHY Configuration with MII Interface

Configuration as a PHY uses a Media Independent Interface (MII) to interface to a MAC is common in switch applications in which the digital transceiver interfaces between the VDSL link using the AFE and the Ethernet MAC implemented by the switch itself. The digital transceiver acts as a standard Ethernet PHY and can connect directly to the standard MII interface of a switch. This MII interface is compatible with the IEEE 802.3 standard.

Figure 28 shows the block diagram when the digital transceiver is configured as a PHY and uses MII to interface to a MAC unit.

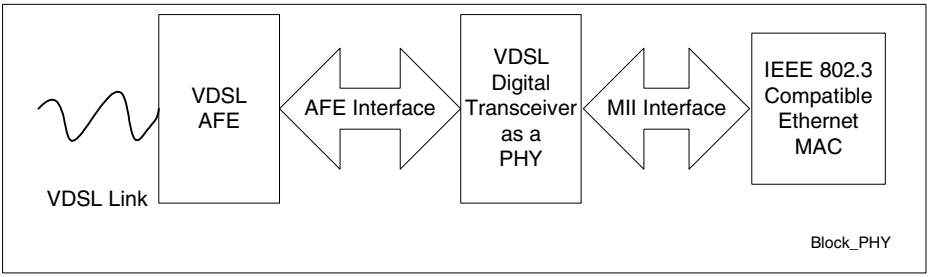


Figure 28 Block Diagram of PHY Configuration with MII Interface to a MAC

Figure 29 shows the names of the signals used for the MII interface between the PHY and the MAC, with the corresponding MII signal and the direction for each. It also shows the external 25 MHz source clock required for correct operation that must be connected to the UTID7 pin (PHYCLK signal).

For mapping of these pins and signals, see **Table 2.4 "Pin and Signal Assignment in Different Modes" on Page 49**.

For functional descriptions of the corresponding MII signals, see IEEE Standard 802.3. **“MII Interface” on Page 274** specifies the AC characteristics of these signals.

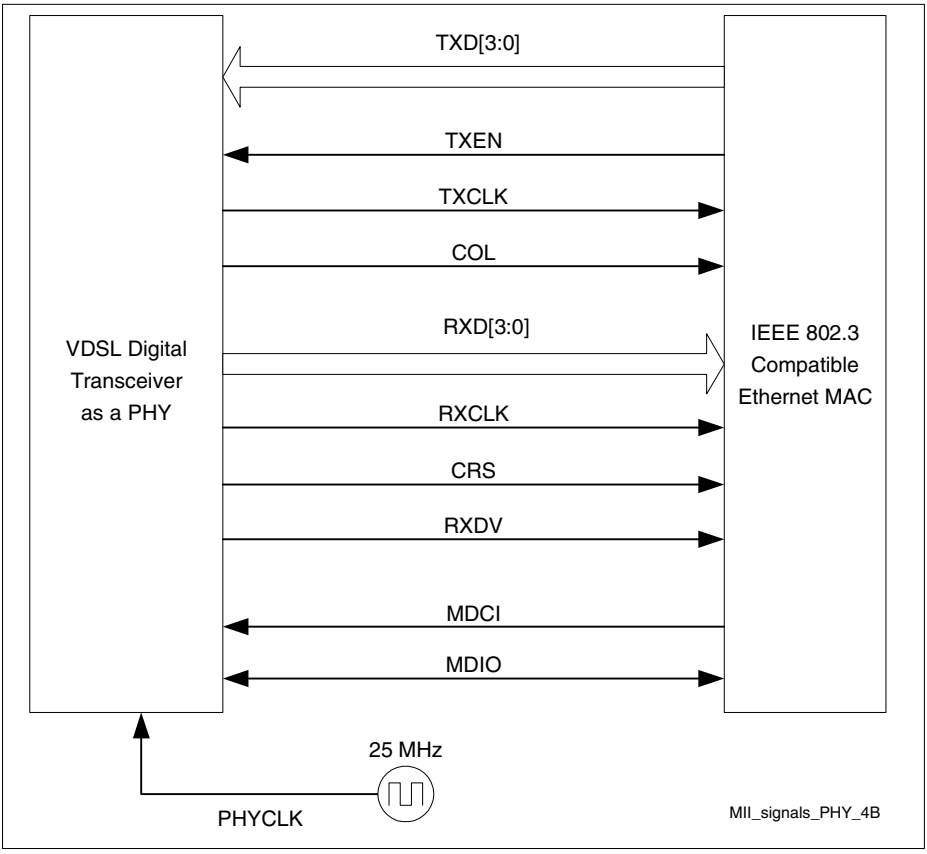


Figure 29 Signals for PHY Configuration with MII Interface to a MAC

9.3.2 *x*MII Interfaces

This section describes the different kinds of Media Independent Interface (MII) supported.

9.3.2.1 MII Interface to a PHY in a MAC Configuration

A digital transceiver configured as a MAC that uses MII to interface to a PHY is common in CPE units in which the digital transceiver interfaces between the VDSL link using the AFE, and the local Ethernet link using an Ethernet PHY. This MII interface is compatible with the IEEE 802.3 standard.

Figure 30 shows the block diagram when the digital transceiver is configured as a MAC and uses MII to interface to a PHY unit.

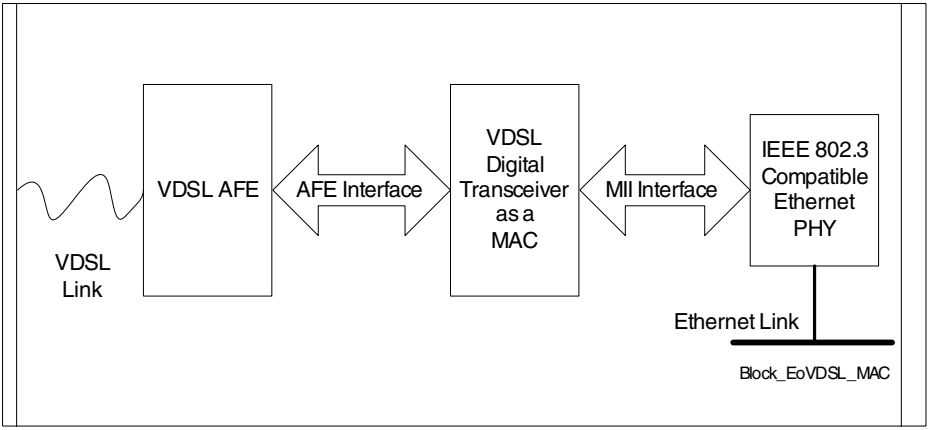


Figure 30 Block Diagram of MAC Configuration with MII Interface to a PHY

Figure 31 shows the names of the pins (in parentheses) used for the MII interface between the MAC and the PHY, with the corresponding MII signal and the direction for each. For mapping for these pins and signals, see **Table 13 "MII MAC Mode Pins" on Page 50** and **Table 19 "Serial Management Interface (SMI) Pins for MAC Modes" on Page 54**.

For functional descriptions of the corresponding MII signals, see IEEE Standard 802.3. **"MII Interface" on Page 274** specifies the AC characteristics of these signals.

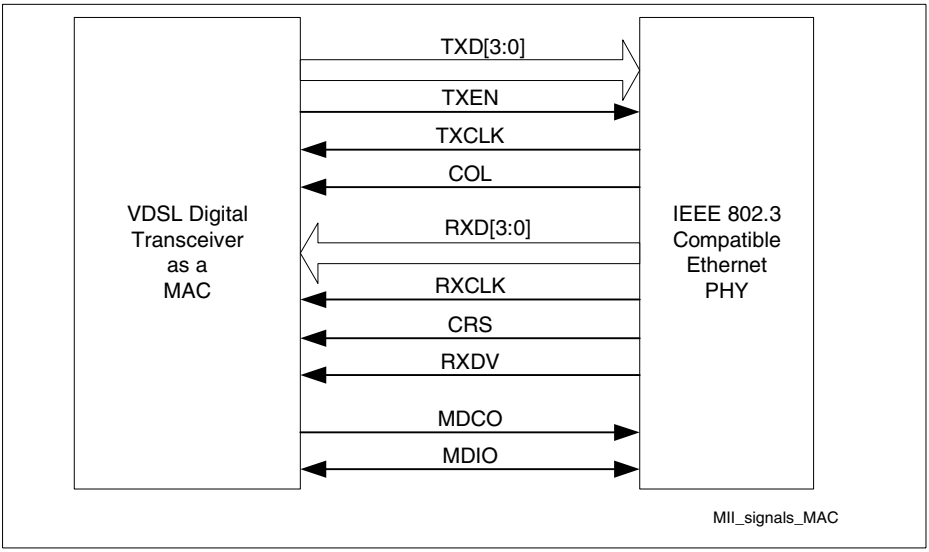


Figure 31 Signals for MAC Configuration with MII Interface to a PHY

9.3.2.2 MII Interface to a MAC in a PHY Configuration

A digital transceiver configured as a PHY that uses a Media Independent Interface (MII) to interface to a MAC is common in switch applications in which the digital transceiver interfaces between the VDSL link using the AFE and the Ethernet MAC implemented by the switch itself. The digital transceiver acts as a standard Ethernet PHY and can connect directly to the standard MII interface of a switch. This MII interface is compatible with the IEEE 802.3 standard.

Figure 30 shows the block diagram when the digital transceiver is configured as a PHY and uses MII to interface to a MAC unit.

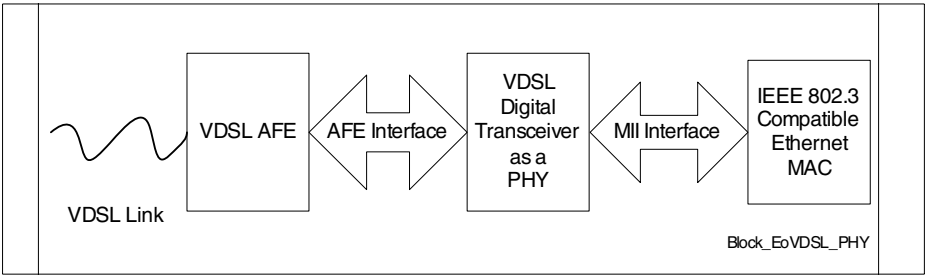


Figure 32 Block Diagram of PHY Configuration with MII Interface to a MAC

Figure 33 shows the names of the pins (in parentheses) used for the MII interface between the PHY and the MAC, with the corresponding MII signal and the direction for each. It also shows the external 25 MHz source clock required for correct operation that must be connected to the ECLK2 pin (PHYCLK signal).

For mapping for these pins and signals, see **Table 14 "MII PHY Mode Pins" on Page 50** and **Table 20 "Serial Management Interface (SMI) Pins for PHY Modes" on Page 54**.

For functional descriptions of the corresponding MII signals, see reference **[9]**. **"MII Interface" on Page 274** specifies the AC characteristics of these signals.

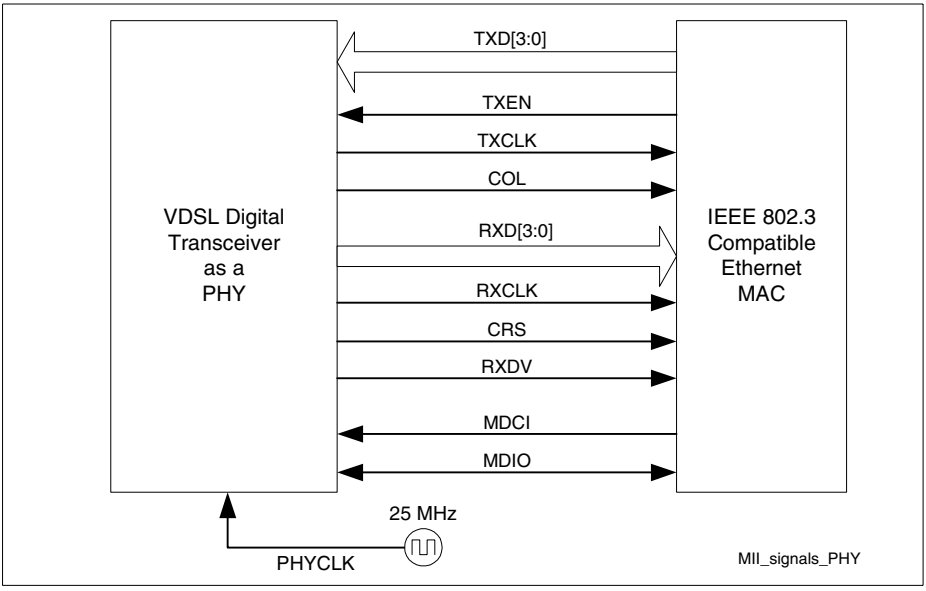


Figure 33 Signals for PHY Configuration with MII Interface to a MAC

9.3.2.3 RMII Interface to a PHY in a MAC Configuration

A digital transceiver configured as a MAC that uses a Reduced Media Independent Interface (RMII) to interface to a PHY provides a low pin count interface between Ethernet PHYs and switch ASICs in high port density designs. RMII uses only six pins for data and control per port plus one pin per switch ASIC, compared with MII, which uses 14 pins per port.

This RMII interface is compatible with that described in reference **[12]**. For functional descriptions of the RMII signals, see that document.

The block diagram of the digital transceiver when it is configured as a MAC and uses RMII to interface to a PHY is the same as for MII, as shown in **Figure 31, Signals for MAC Configuration with MII Interface to a PHY, on page 162**.

Figure 34 shows the names of the pins (in parentheses) used for the RMII interface between the MAC and the PHY, with the corresponding RMII signal and the direction for each. It also shows the external 50 MHz source clock required for correct operation that must be connected to the REFCLK signal on pin ECLK1 (pin 60).

For mapping for these pins and signals, see **Table 15 "RMII MAC Mode Pins" on Page 51** and **Table 19 "Serial Management Interface (SMI) Pins for MAC Modes" on Page 54**. **"RMII Interface" on Page 274** specifies the AC characteristics of these signals.

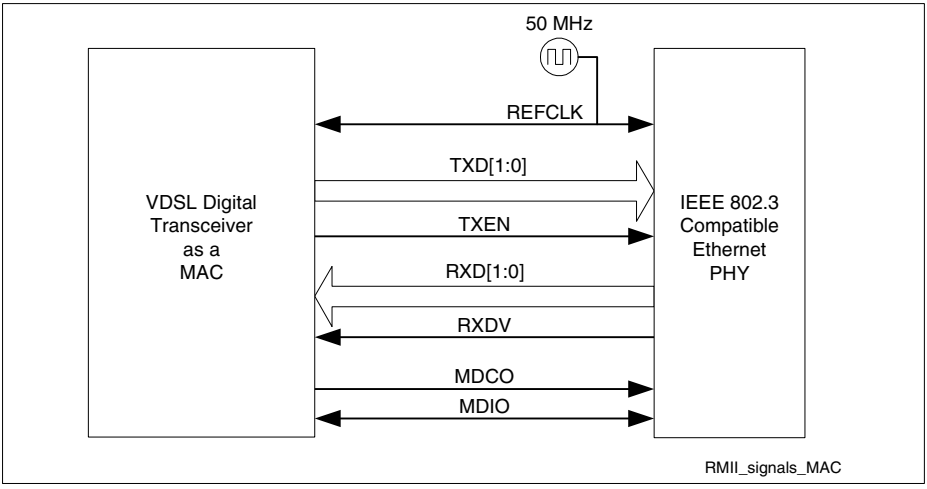


Figure 34 Signals for MAC Configuration with RMII Interface to a PHY

9.3.2.4 RMII Interface to a MAC in a PHY Configuration

A digital transceiver configured as a PHY that uses a Reduced Media Independent Interface (RMII) to interface to a MAC provides a low pin count interface between Ethernet PHYs and switch ASICs in high port density designs. RMII uses only six pins for data and control per port plus one pin per switch ASIC, compared with MII, which uses 14 pins per port.

This RMII interface is compatible with that described in For detailed functional descriptions of the RMII signals, see that document.

The block diagram of the digital transceiver when it is configured as a PHY and uses RMII to interface to a MAC is the same as for MII, as shown in **Figure 32, Block Diagram of PHY Configuration with MII Interface to a MAC, on page 162**.

Figure 35 shows the names of the pins (in parentheses) used for the RMII interface between the PHY and the MAC, with the corresponding RMII signal and the direction for each. It also shows the external 50 MHz source clock required for correct operation that must be connected to the REFCLK signal on pin ECLK1 (pin 60).

For mapping for these pins and signals, see Table 16 "RMII PHY Mode Pins" on Page 52 and Table 20 "Serial Management Interface (SMI) Pins for PHY Modes" on Page 54. “RMII Interface” on Page 274 specifies the AC characteristics of these signals.

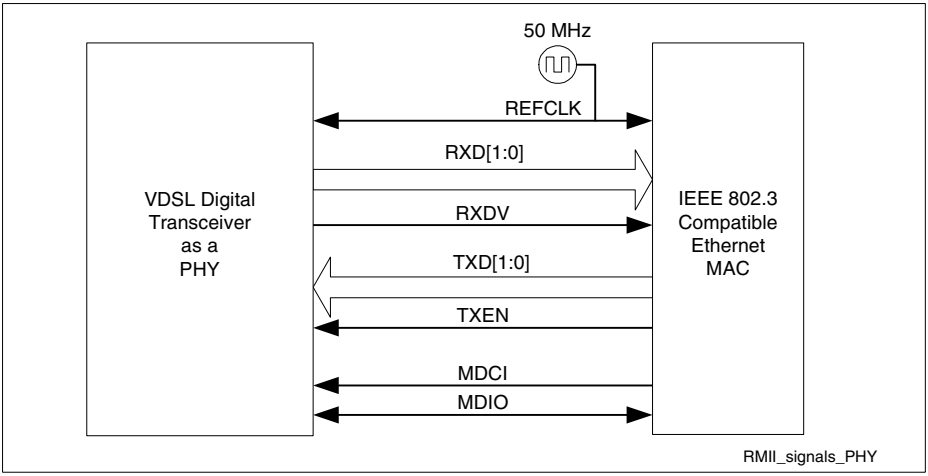


Figure 35 Signals for PHY Configuration with RMII Interface to a MAC

9.3.2.5 Typical SMII Interface

A digital transceiver that is configured as a PHY with a Serial Media Independent Interface (SMII) to interface to a MAC provides an MII interface that uses a 1-bit wide data bus and only four signals, including clock and Serial Management Interface signals. Only PHY connection with this interface is supported.

This SMII interface is compatible with that described in Reference [10]. For detailed functional descriptions of the SMII signals, see that document.

The block diagram when the digital transceiver is configured as a PHY and uses SMII to interface to a MAC is the same as for MII, as shown in Figure 32, Block Diagram of PHY Configuration with MII Interface to a MAC, on page 162.

SMII signals differ from MII signals in the use of the TXD and RXD buses. In SMII, only the LSB (bit 0) of each bus is used. The remaining bits that are used in the MII interface, are ignored in the SMII interface.

Figure 36 shows the names of the pins (in parentheses) used for a typical SMII interface between the PHY and the MAC, with the corresponding SMII signal and the direction for each. It also shows the external 125 MHz source clock required for correct operation that must be connected to the REFCLK signal on pin ECLK1 (pin P12).

For mapping for these pins and signals, see **Table 18 "Source Synchronous SMII Mode Pins" on Page 53** and **Table 20 "Serial Management Interface (SMI) Pins for PHY Modes" on Page 54**. **"Serial MII Interface, Typical Mode" on Page 275** specifies the AC characteristics of these signals.

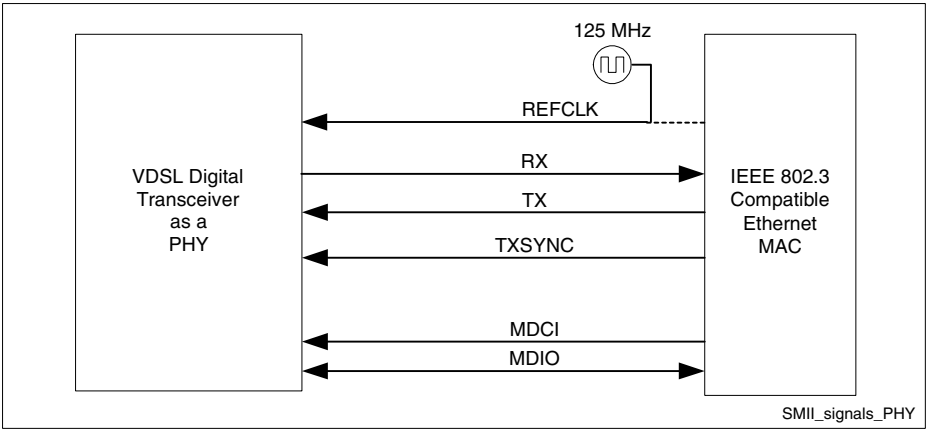


Figure 36 Signals for a Typical SMII Interface

9.3.2.6 Source Synchronous SMII Interface

A digital transceiver that is configured as a PHY with a source synchronous Serial Media Independent Interface (SMII) to interface to a MAC provides an MII interface that uses a 1-byte wide data bus and eight signals, including clock and Serial Management Interface signals. Only PHY connection with this interface is supported.

This source synchronous SMII interface is compatible with that described in reference **[10]**. For detailed functional descriptions of the source synchronous SMII signals, see that document.

The block diagram when the digital transceiver is configured as a PHY and uses source synchronous SMII to interface to a MAC is the same as for MII, as shown in **Figure 32, Block Diagram of PHY Configuration with MII Interface to a MAC, on page 162**.

Source synchronous SMII signals differ from MII signals in the use of the TXD and RXD buses. In source synchronous SMII, only the LSB (bit 0) of each bus is used. The remaining bits that are used in the MII interface, are ignored in the source synchronous SMII interface.

Figure 37 shows the names of the pins (in parentheses) used for the source synchronous SMII interface between the PHY and the MAC, with the corresponding source synchronous SMII signal and the direction for each. It also shows the external 125 MHz source clock required for correct operation that must be connected to the ECLK1 pin (RXCLKREF signal).

For mapping for these pins and signals, see **Table 18 "Source Synchronous SMII Mode Pins" on Page 53** and **Table 20 "Serial Management Interface (SMI) Pins for PHY Modes" on Page 54**. **"Serial MII Interface, Typical Mode" on Page 275** specifies the AC characteristics of these signals.

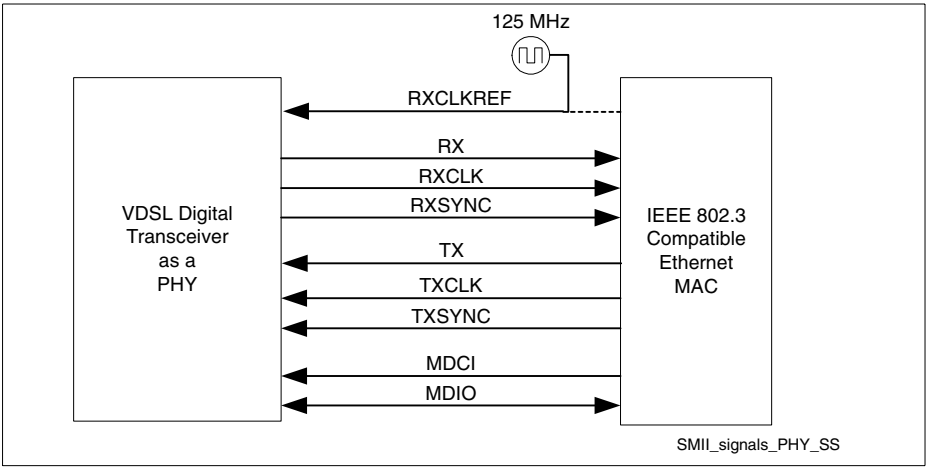


Figure 37 Signals for a Source Synchronous SMII Interface

9.4 EOC Interface

Figure 38 shows a block diagram of the signals used for the EOC interface, **Table 51** describes them and **Figure 39** shows their timing. See also, **Table 4 "EOC and PCM Pins" on Page 42**.

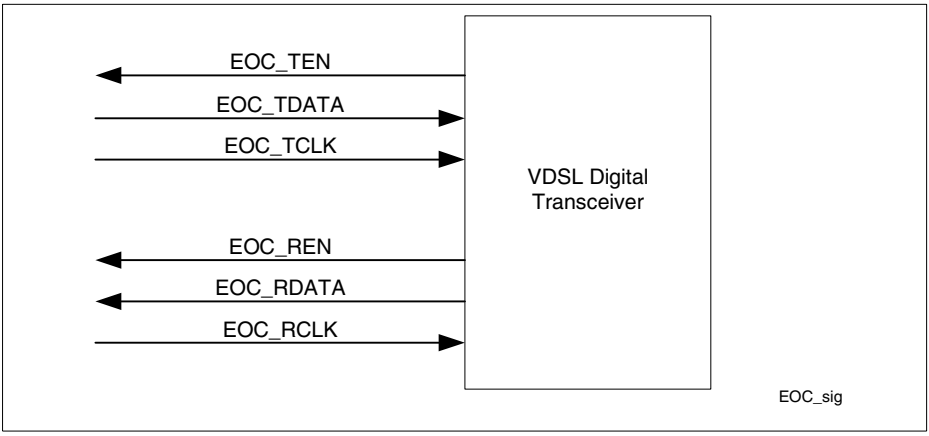


Figure 38 EOC Interface Signals

Table 51 EOC Signals

Signal	I/O	Description	Timing[1)]
EOC_TDATA	I	Data In (two bytes per frame)	Sample on EOC_TCLK falling edge
EOC_RDATA	O	Data Out (two bytes per frame); valid while EOC_REN is asserted	Driven on EOC_RCLK rising edge
EOC_TCLK	I	Transmission clock	
EOC_RCLK	I	Reception clock	
EOC_TEN	O	Asserted when OPCODE = IDLE and the VDSL is able to receive the next bit	Driven on EOC_TCLK rising edge
EOC_REN	O	Asserted when OPCODE = IDLE and the VDSL is able to transmit the next bit	Driven on EOC_RCLK rising edge

1) *The maximum clock frequency of the EOC_TCLK and EOC_RCLK signals is CLKIN/4. For example, a 38 MHz clock is equal to 9 MHz.*

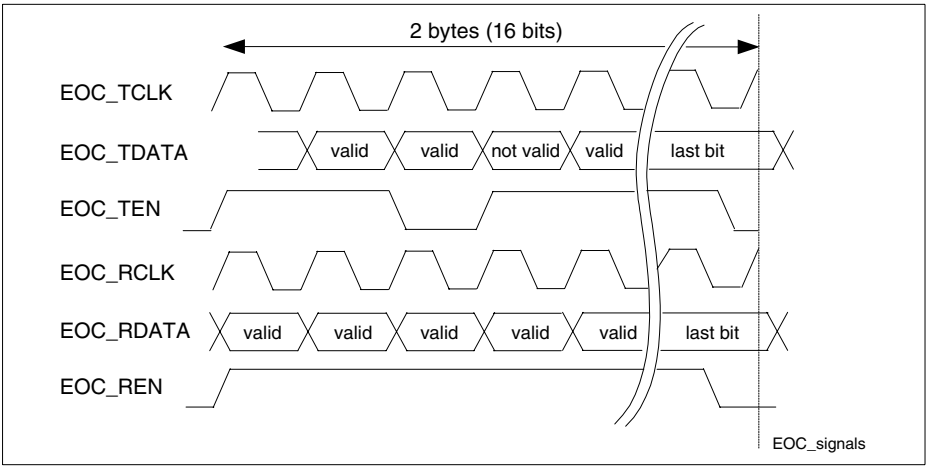


Figure 39 EOC Signals Timing Diagram

9.5 I²C Interface for EEPROM

Connection to the EEPROM is implemented with a standard I²C interface, using the I2CCLK and I2CD pins. The internal 8051 microprocessor emulates the EEPROM I²C interface. Due to the internal program, the E2CLK has no consistent clock cycle, however it conforms to the I²C protocol. The digital transceiver supports I²C connection to a 32-Kbit or a 64-Kbit EEPROM.

The I²C interface is a bidirectional, two-wire bus and data transmission protocol. The digital transceiver acts as the master on this bus, and the EEPROM is the slave.

The digital transceiver initiates read and write transactions by generating a start condition, in which I²CD changes from high to low while I²CCLK is high. Then it sends several bytes serially (MSB first) on the I2CD line, changing the I2CD signal value only while I²CCLK is low.

After each byte sent (and received on a read access), the digital transceiver expects a low bit on the I²CD line, driven by the EEPROM to acknowledge the read or write transaction for the byte.

After the read or write transaction is done, the digital transceiver generates a stop condition, in which I²CD changes from low to high while I²CCLK is high.

Figure 40 illustrates a typical read or write transaction.

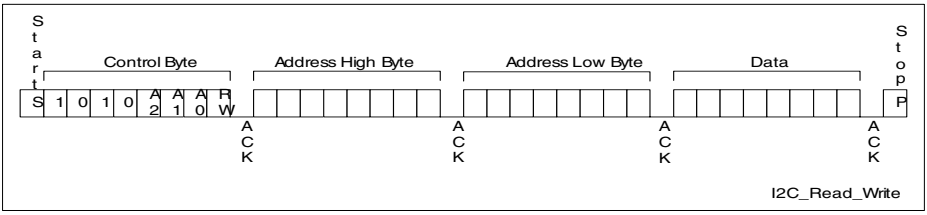


Figure 40 I²C Read or Write Transaction

The control byte identifies the slave IC, which is accessed by the master (the digital transceiver). The digital transceiver writes $A0_H$ for a write access and $A1_H$ for a read access (bits A2:A0] are 0). EEPROM pins A2, A1 and A0 must be connected to GND to enable the EEPROM to respond as a slave to the digital transceiver.

For a write cycle, data bits are driven by the digital transceiver. For a read cycles, these bits are driven by the EEPROM.

See **“EEPROM Interface” on Page 279** for detailed AC characteristics of the I²C signals.

10 Memory and Register Descriptions – Digital Block

This section describes the registers that are dedicated to digital operations. The overview includes lists of the registers with their offset addresses. Detailed descriptions of each follow, beginning on **Page 185**.

10.1 Register Overview – Digital Block

Table 52 lists all the registers in one table. The "**Register Lists by Type – Digital Block**" section starting on **Page 177** organizes the registers into groups and lists them by type.

Table 52 lists all the registers of the digital transceiver.

Table 52 Register List (page 1 of 7)

Offset Address	Short Name	Long Name	Pg
Main Control Registers			
$8F00_H$	**MAIN_CTL**	Main control	**186**
$8F01_H$	**MAIN_MODE**	Main operation mode	**186**
$8F02_H$	**LINK_MODE**	Link operation mode	**187**
$8F04_H$	**VOC_CNTL**	VOC control	**189**
$8F05_H$	**VOC_OC**	VOC message opcode to send	**190**
$8F06_H$:$8F07_H$	**VOC_DAT**	VOC data to send, MSB to LSB	**190**
$8F0C_H$	**PSDADJ**	Adjust PSD output from board	**195**
$8F0D_H$	**ATTADJ**	Adjust attenuation input to board	**196**
Main Status Registers			
$8F0F_H$	**GEN_STATUS1**	General status register 1	**197**
$8F10_H$	**GEN_STATUS2**	General status register 2	**198**
$8F11_H$	**GEN_STATUS3**	General status register 3	**199**
$8F12_H$	**CONFIG_STS1**	Configuration pins status 1	**199**
$8F13_H$	**CONFIG_STS2**	Configuration pins status 2	**200**
$8F14_H$	**SNR_BAND1**	SNR for first received band	**201**
$8F15_H$	**SNR_BAND2**	SNR for second received band	**201**
8D37	**R_FR_LOS_CNT**	Remote loss of frame error counter	**202**
$8D38_H$	**FAIL_CNT**	Channel failures counter	**202**

Table 52 Register List (page 2 of 7)

Offset Address	Short Name	Long Name	Pg
$8D3F_H$	L_FR_LOS_CNT	Local loss of frame error counter	203
$7F11_H$	SNR_BER	SNR margin and BER overflow status	204
$7F18_H$	SNR_MAX	SNR maximum	205
$7F19_H$	SNR_MIN	SNR minimum	205
STPs			
$5E11_H$:$5E2F_H$	CR_STP	Current set of parameters, STP	106
$5E30_H$:$5E4E_H$	WS_STP	Warm start set of parameters, STP	106
$5ECB_H$:$5EE9_H$	DF_STP1	Default STP1 set of parameters	108
$5EEA_H$:$5F08_H$	DF_STP2	Default STP2 set of parameters	108
Notch Filters Registers			
$5DBD_H$	NTCHA1_L (DS1)	Notch filter coefficient registers for DS1	249
$5DBE_H$	NTCHA2_L (DS1)		250
$5DBF_H$	NTCHA_H (DS1)		251
$5DC0_H$	NTCHB_L (DS1)		252
$5DC1_H$	NTCHB_H (DS1)		253
$5DC2_H$	NTCHA1_L (US1)	Notch filter coefficient registers for US1	249
$5DC3_H$	NTCHA2_L (US1)		250
$5DC4_H$	NTCHA_H (US1)		251
$5DC5_H$	NTCHB_L (US1)		252
$5DC6_H$	NTCHB_H (US1)		253
$5DC7_H$	NTCHA1_L (DS2)	Notch filter coefficient registers for DS2	249
$5DC8_H$	NTCHA2_L (DS2)		250
$5DC9_H$	NTCHA_H (DS2)		251
$5DCA_H$	NTCHB_L (DS2)		252
$5DCB_H$	NTCHB_H (DS2)		253

Table 52 Register List (page 3 of 7)

Offset Address	Short Name	Long Name	Pg
$5DCC_H$	**NTCHA1_L** (US2)	Notch filter coefficient registers for US2	**249**
$5DCD_H$	**NTCHA2_L** (US2)		**250**
$5DCE_H$	**NTCHA_H** (US2)		**251**
$5DCF_H$	**NTCHB_L** (US2)		**252**
$5DD0_H$	**NTCHB_H** (US2)		**253**
Version Status Registers			
$5F62_H$	**HW_VER_FIELD**	Hardware version register	**206**
$5F63_H$	**ROM_VER_FIELD**	ROM firmware version	**206**
$5F64_H$	**FW_VER_FIELD**	Application version	**207**
$5F65_H$	**FW_REL_FIELD**	Application release	**207**
$5F66_H$	**FW_BLD_FIELD**	Application build	**208**
RAM Check Registers			
$5F67_H$:5 $F68_H$	**RAM_ADDR**	Start address, MSB to LSB	**208**
$5F69_H$:5 $F6A_H$	**RAM_LENGTH**	RAM length, MSB to LSB	**209**
$5F6B_H$: $5F6C_H$	**RAM_CHKSUM**	Expected CHKSUM, MSB to LSB	**209**
$5F6D_H$	**RAM_CMD_STS**	Command or status field	**210**
Firmware Control Register			
5F6F	**FW_DLOAD**	Firmware Control register	**210**
EEPROM Control Registers			
$5F70_H$:5 $F71_H$	**EEP_ADDR**	Start address to read or write in EEPROM, MSB to LSB	**211**
$5F72_H$	**EEP_LENGTH**	Page length to write in EEPROM	**211**
$5F73_H$	**EEP_CHKSUM**	CHKSUM for EEPROM	**212**
$5F74_H$:5 $FF3_H$	**EEP_DATA**	Data for EEPROM, MSB to LSB	**212**
$5FF6_H$	**EEP_COMMAND**	EEPROM handler command field	**213**
$5FF7_H$	**EEP_STATUS**	EEPROM handler status field	**213**
Analog Front End (AFE) Registers			

Table 52 Register List (page 4 of 7)

Offset Address	Short Name	Long Name	Pg
$8C60_H$	ADC	ADC Operation Parameters	256
$8C62_H$	DAC	DAC Control	256
$8C63_H$	PREFI_POFI	PREFI and POFI Power Down	257
$8C64_H$	ACE_MBUF_AGC	ACE, Measurement Buffer and AGC Mode	258
8C65	POCO	Power Control	259
8C66	AGC	Value for AGC Gain Calculation	260
8C67	ALOOP_BIAS	Analog Loop and Bias Control	260
8C68	DCXO	Digital Crystal Frequency	261
8C6C	FC_TUNE	Corner Frequency and Tuning	261
8C6D	WAK_PLL_TUN_RF	Wake-up, PLL, Tuning and RFS Status	263
8C6F	XTAL_TUN_PAR	Clock, Test, Crystal and Tuning Parameters	263
8C72	PLL_PAR	PLL Parameters	264
8C79	GPO_PADS	General Purpose Output Pad Parameters	265
MDIO Master Interface Registers			
$8CB0_H$	MII_PHY	Physical address of slave MII	214
$8CB1_H$	MII_REG	Register address in slave	215
$8CB3_H$: $8CB2_H$	MII_D	Data to/from slave MII, MSB-LSB	215
$8CB4_H$	MII_CMD	MII command	216
MII Status Registers (Counters)			
$8CE0_H$	MII_SALE	SNMP alignment errors count-LSB	217
$8CE1_H$	MII_SSCF	SNMP single collision frames-LSB	217
$8CE2_H$	MII_SMCF	SNMP multiple collision frames-LSB	218
$8CE3_H$	MII_SDT	SNMP deferred transmissions-LSB	218
$8CE4_H$	MII_SLC	SNMP late collisions counter-LSB	219
$8CE5_H$	MII_SEC	LSB of excessive collisions counter	219
$8CE6_H$	MII_SRE	LSB of reception errors counter	220
$8CE7_H$	MII_SCSE	LSB of carrier sense errors counter	220

Table 52 Register List (page 5 of 7)

Offset Address	Short Name	Long Name	Pg
$8CE8_H$	MII_SFTL	LSB of frames too long counter	221
$8CE9_H$	MII_SFCS	LSB of FCS errors counter	221
$8CEA_H$	MII_SOTO	Bytes transmitted OK counter, LSB	222
$8CEB_H$	MII_SORO	LSB of bytes received OK counter	222
$8CEC_H$	MII_BCAST	Broadcast frames received, LSB	223
$8CED_H$	RXPAUS	Reception pause packets, LSB	223
$8CEE_H$	TXPAUS	Transmission pause packets, LSB	224
$8CEF_H$	TXBCNT	LSB of transmitted frames counter	224
$8CF0_H$	RXBCNT	LSB of received frames counter	225
$8CF3_H$: $8CF1_H$	MII_CNTR_MSB	Current MII status counter, 3 MSBs	225
MII Control Registers			
$8D40_H$	MIICNTL	MII control	226
$8D41_H$	BPCNTL1	MII back pressure control register 1	227
$8D42_H$	BPCNTL2	MII back pressure control register 2	228
$8D43_H$	BPCNTL3	MII back pressure control register 3	229
$8D44_H$	FLOWCTL	Flow control	230
$8D45_H$	SRCADD	Pause packet source address	231
$8D46_H$	ADDTCTL	Address table control	232
$8D47_H$	AGTIMER	Aging timer	233
$8D4D_H$: $8D48_H$	PFSRC	Current source address, MSB-LSB	233
MII Vendor Specific Registers			
$8D4E_H$	VP_INF_L	Vendor PHY SMI Status Register, L	234
$8D4F_H$	VP_INF_H	Vendor PHY SMI Status Register, H	235
PBO and PSD Registers			
$5B00_H$	PBO_K	PBO K constant	236
$5B01_H$	PBO_US1D	PBO US1 Distance	236
$5B02_H$	PBO_US2D	PBO US2 Distance	237
$5B03_H$	PBO_MAXPSD	PBO Maximum PSD	237

Table 52 Register List (page 6 of 7)

Offset Address	Short Name	Long Name	Pg
$5B04_H$	PBO_MINPSD	PBO Minimum PSD	238
Rate Adaptive Process Registers			
$5B10_H$	RA_COMMAND	Rate Adaptive Command	239
$5B11_H$	RA_MN_MRG_D1	RA Minimum Noise Margin for D1	239
$5B12_H$	RA_MN_MRG_D2	RA Minimum Noise Margin for D2	240
$5B13_H$	RA_MN_MRG_U1	RA Minimum Noise Margin for U1	240
$5B14_H$	RA_MN_MRG_U2	RA Minimum Noise Margin for U2	240
$5B19_H$:5 $B1A_H$	RA_MX_RATE_DS	RA Maximum Downstream Rate	240
$5B1B_H$: $5B1C_H$	RA_MX_RATE_US	RA Maximum Upstream Rate	241
$5B1D_H$: $5B1E_H$	RA_CF_D1	RA Center Frequency (CF) for D1	242
$5B1F_H$: $5B20_H$	RA_CF_D2	RA Center Frequency (CF) for D2	242
$5B21_H$:5 $B22_H$	RA_CF_U1	RA Center Frequency (CF) for U1	242
$5B23_H$:5 $B24_H$	RA_CF_U2	RA Center Frequency (CF) for U2	242
$5B25_H$	RA_SR_D1	RA Symbol Rate (SR) for D1	242
$5B26_H$	RA_SR_D2	RA Symbol Rate (SR) for D2	242
$5B27_H$	RA_SR_U1	RA Symbol Rate (SR) for U1	243
$5B28_H$	RA_SR_U2	RA Symbol Rate (SR) for U2	243
$5B29_H$	RA_PSD_D1	RA Power Spectral Density (PSD) for D1	243
$5B2A_H$	RA_PSD_D2	RA Power Spectral Density (PSD) for D2	243
$5B2B_H$	RA_PSD_U1	RA Power Spectral Density (PSD) for U1	243
$5B2C_H$	RA_PSD_U2	RA Power Spectral Density (PSD) for U2	243
$5B2D_H$	RA_PSD_MASK	RA Power Spectral Density (PSD) Mask	244
$5B2E_H$	RA_PSD_MAX	RA Power Spectral Density (PSD) Max	245
$5B2F_H$	RA_INTR_DS	RA Interleaver Delay, DS Register	245
$5B30_H$	RA_INTR_US	RA Interleaver Delay, US Register	245

Table 52 Register List (page 7 of 7)

Offset Address	Short Name	Long Name	Pg
$5B31_H$	RA_MN_MRG_U0	RA Process Minimum Noise Margin for U0	246
$5B32_H$	RA_TLAN_PSD_DS1_MAX	RX_TLAN_PSD Maximum Level on DS1	246
$5B40_H$	RA_STATUS	RA Process Status	247
$5B41_H$	RA_RESTRT_CNT	RA Process Rerun Counter	247
$5B42_H$	RA_RSLT_D1	D1 Band Use as a Result of RA Process	248
$5B43_H$	RA_RSLT_D2	D2 Band Use as a Result of RA Process	249
$5B44_H$	RA_RSLT_U1	U1 Band Use as a Result of RA Process	249
$5B45_H$	RA_RSLT_U2	U2 Band Use as a Result of RA Process	249

10.2 Register Lists by Type – Digital Block

This section lists registers grouped by type, as follows:

- Version status registers - **Table 53** on **Page 177**.
- A firmware control register - **Table 54** on **Page 178**.
- EEPROM control registers - **Table 55** on **Page 178**.
- RAM check registers - **Table 56** on **Page 178**.
- Main control registers - **Table 58** on **Page 179**.
- Main status registers - **Table 59** on **Page 179**.
- STPs - **Table 60** on **Page 180**.
- Notch filter registers - **Table 61** on **Page 180**.
- MII control registers - **Table 62** on **Page 181**.
- MII vendor specific registers - **Table 63** on **Page 181**.
- MDIO master interface registers - **Table 64** on **Page 181**.
- MII status registers - **Table 65** on **Page 182**.
- Power Back Off (PBO) and PSD registers - **Table 66** on **Page 182**.
- Rate Adaptive (RA) Process registers - **Table 67** on **Page 183**.

Table 53 Version Status Registers

Offset Address	Short Name	Long Name	Pg
$5F62_H$	HW_VER_FIELD	Hardware version register	206
$5F63_H$	ROM_VER_FIELD	ROM firmware version	206
$5F64_H$	FW_VER_FIELD	Application version	207
$5F65_H$	FW_REL_FIELD	Application release	207
$5F66_H$	FW_BLD_FIELD	Application build	208

Table 54 Firmware Control Register

Offset Address	Short Name	Long Name	Pg
$5F6F_H$	FW_DLOAD	Firmware Control register	210

Table 55 EEPROM Control Registers

Offset Address	Short Name	Long Name	Pg
$5F70_H$:$5F71_H$	EEP_ADDR	Start address of page to read or write in EEPROM, MSB to LSB	211
$5F72_H$	EEP_LENGTH	Page length to save or read in EEPROM	211
$5F73_H$	EEP_CHKSUM	CHKSUM for EEPROM	212
$5F74_H$:$5FF3_H$	EEP_DATA	Data to save or read in EEPROM, MSB to LSB	212
$5FF6_H$	EEP_COMMAND	Command field for EEPROM handler	213
$5FF7_H$	EEP_STATUS	Status field from EEPROM handler	213

Table 56 RAM Check Registers

Offset Address	Short Name	Long Name	Pg
$5F67_H$:$5F68_H$	RAM_ADDR	Start address, MSB to LSB	208
$5F69_H$:$5F6A_H$	RAM_LENGTH	RAM length, MSB to LSB	209
$5F6B_H$:$5F6C_H$	RAM_CHKSUM	Expected CHKSUM, MSB to LSB	209
$5F6D_H$	RAM_CMD_STS	Command or status field	210

Table 57 Analog Front End (AFE) Registers (page 1 of 2)

Offset Address	Short Name	Long Name	Pg
$8C60_H$	ADC	ADC Operation Parameters	256
$8C62_H$	DAC	DAC Control	256
$8C63_H$	PREFI_POFI	PREFI and POFI Power Down	257
$8C64_H$	ACE_MBUF_AGC	ACE, Measurement Buffer and AGC Mode	258
8C65	POCO	Power Control	259
8C66	AGC	Value for AGC Gain Calculation	260
8C67	ALOOP_BIAS	Analog Loop and Bias Control	260

Table 57 Analog Front End (AFE) Registers (page 2 of 2)

Offset Address	Short Name	Long Name	Pg
8C68	DCXO	Digital Crystal Frequency	261
8C6C	FC_TUNE	Corner Frequency and Tuning	261
8C6D	WAK_PLL_TUN_RF	Wake-up, PLL, Tuning and RFS Status	263
8C6F	XTAL_TUN_PAR	Clock, Test, Crystal and Tuning Parameters	263
8C72	PLL_PAR	PLL Parameters	264

Table 58 Main Control Registers

Offset Address	Short Name	Long Name	Pg
$8F00_H$	MAIN_CTL	Main control	186
$8F01_H$	MAIN_MODE	Main operation mode	186
$8F02_H$	LINK_MODE	Link operation mode	187
$8F04_H$	VOC_CNTL	VOC control	189
$8F05_H$	VOC_OC	VOC message opcode to send	190
$8F06_H$:$8F07_H$	VOC_DAT	VOC data to send, MSB to LSB.	190
$8F0C_H$	PSDADJ	Adjust PSD output from board	195
$8F0D_H$	ATTADJ	Adjust attenuation input to board	196

Table 59 Main Status Registers (page 1 of 2)

Offset Address	Short Name	Long Name	Pg
$8F0F_H$	GEN_STATUS1	General status register 1	197
$8F10_H$	GEN_STATUS2	General status register 2	198
$8F11_H$	GEN_STATUS3	General status register 3	199
$8F12_H$	CONFIG_STS1	Configuration pins status register 1	199
$8F13_H$	CONFIG_STS2	Configuration pins status register 2	200
$8F14_H$	SNR_BAND1	SNR for first received band	201
$8F15_H$	SNR_BAND2	SNR for second received band	201
8D37	R_FR_LOS_CNT	Loss of frame error counter	202
$8D38_H$	FAIL_CNT	Channel failures counter	202
$8D3F_H$	L_FR_LOS_CNT	Loss of frame error counter	203

Table 59 Main Status Registers (page 2 of 2)

Offset Address	Short Name	Long Name	Pg
$7F11_H$	**SNR_BER**	SNR margin and BER overflow status	**204**
$7F18_H$	**SNR_MAX**	SNR maximum	**205**
$7F19_H$	**SNR_MIN**	SNR minimum	**205**

Table 60 STPs

Offset Address	Short Name	Long Name	Pg
$5E11_H$:$5E2F_H$	**CR_STP**	Current set of parameters, STP	**106**
$5E30_H$:$5E4E_H$	**WS_STP**	Warm start set of parameters, STP	**106**
$5ECB_H$:$5EE9_H$	**DF_STP1**	Default STP1 set of parameters	**108**
$5EEA_H$:$5F08_H$	**DF_STP2**	Default STP2 set of parameters	**108**

Table 61 Notch Filter Registers (page 1 of 2)

Offset Address	Short Name	Long Name	Pg
$5DBD_H$	**NTCHA1_L** (DS1)	Notch filter coefficient registers for DS1	**249**
$5DBE_H$	**NTCHA2_L** (DS1)		**250**
$5DBF_H$	**NTCHA_H** (DS1)		**251**
$5DC0_H$	**NTCHB_L** (DS1)		**252**
$5DC1_H$	**NTCHB_H** (DS1)		**253**
$5DC2_H$	**NTCHA1_L** (US1)	Notch filter coefficient registers for US1	**249**
$5DC3_H$	**NTCHA2_L** (US1)		**250**
$5DC4_H$	**NTCHA_H** (US1)		**251**
$5DC5_H$	**NTCHB_L** (US1)		**252**
$5DC6_H$	**NTCHB_H** (US1)		**253**
$5DC7_H$	**NTCHA1_L** (DS2)	Notch filter coefficient registers for DS2	**249**
$5DC8_H$	**NTCHA2_L** (DS2)		**250**
$5DC9_H$	**NTCHA_H** (DS2)		**251**
$5DCA_H$	**NTCHB_L** (DS2)		**252**
$5DCB_H$	**NTCHB_H** (DS2)		**253**

Table 61 Notch Filter Registers (page 2 of 2)

Offset Address	Short Name	Long Name	Pg
$5DCC_H$	NTCHA1_L (US2)	Notch filter coefficient registers for US2	249
$5DCD_H$	NTCHA2_L (US2)		250
$5DCE_H$	NTCHA_H (US2)		251
$5DCF_H$	NTCHB_L (US2)		252
$5DD0_H$	NTCHB_H (US2)		253

Table 62 MII Control Registers

Offset Address	Short Name	Long Name	Pg
$8D40_H$	MIICNTL	MII control	226
$8D41_H$	BPCNTL1	MII back pressure control register 1	227
$8D42_H$	BPCNTL2	MII back pressure control register 2	228
$8D43_H$	BPCNTL3	MII back pressure control register 3	229
$8D44_H$	FLOWCTL	Flow control	230
$8D45_H$	SRCADD	Pause packet source address	231
$8D46_H$	ADDTCTL	Address table control	232
$8D47_H$	AGTIMER	Aging timer	233
$8D4D_H$:$8D48_H$	PFSRC	Current source address. MSB to LSB.	233

Table 63 MII Vendor Specific Registers

Offset Address	Short Name	Long Name	Pg
$8D4E_H$	VP_INF_L	Vendor PHY SMI Status Register, L	234
$8D4F_H$	VP_INF_H	Vendor PHY SMI Status Register, H	235

Table 64 MDIO Master Interface Registers

Offset Address	Short Name	Long Name	Pg
$8CB0_H$	MII_PHY	Physical address of slave MII	214
$8CB1_H$	MII_REG	Register address in slave	215
$8CB3_H$:$8CB2_H$	MII_D	Data to or from slave MII, MSB to LSB	215
$8CB4_H$	MII_CMD	MII command	216

Table 65 MII Status Registers

Offset Address	Short Name	Long Name	Pg
$8CE0_H$	MII_SALE	LSB of SNMP alignment errors counter	217
$8CE1_H$	MII_SSCF	LSB of SNMP single collision frames counter	217
$8CE2_H$	MII_SMCF	LSB of SNMP multiple collision frames counter	218
$8CE3_H$	MII_SDT	LSB of SNMP deferred transmissions counter	218
$8CE4_H$	MII_SLC	LSB of SNMP late collisions counter	219
$8CE5_H$	MII_SEC	LSB of excessive collisions counter	219
$8CE6_H$	MII_SRE	LSB of reception errors counter	220
$8CE7_H$	MII_SCSE	LSB of carrier sense errors counter	220
$8CE8_H$	MII_SFTL	LSB of frames too long counter	221
$8CE9_H$	MII_SFCS	LSB of frame check sequence errors counter	221
$8CEA_H$	MII_SOTO	LSB of bytes transmitted OK counter	222
$8CEB_H$	MII_SORO	LSB of bytes received OK counter	222
$8CEC_H$	MII_BCAST	LSB of broadcast frames received counter	223
$8CED_H$	RXPAUS	LSB of reception pause packet counter	223
$8CEE_H$	TXPAUS	LSB of transmission pause packet counter	224
$8CEF_H$	TXBCNT	LSB of received frames counter	224
$8CF0_H$	RXBCNT	LSB of transmitted frames counter	225
$8CF3_H$:$8CF1_H$	MII_CNTR_MSB	Three MSBs of current MII status counter	225

Table 66 PBO and PSD Registers

Offset Address	Short Name	Long Name	Pg
$5B00_H$	PBO_K	PBO K constant	236
$5B01_H$	PBO_US1D	PBO US1 Distance	236
$5B02_H$	PBO_US2D	PBO US2 Distance	237
$5B03_H$	PBO_MAXPSD	PBO Maximum PSD	237
$5B04_H$	PBO_MINPSD	PBO Minimum PSD	238

Table 67 RA Process Registers (page 1 of 2)

Offset Address	Short Name	Long Name	Pg
$5B10_H$	RA_COMMAND	Rate Adaptive Command	239
$5B11_H$	RA_MN_MRG_D1	RA Minimum Noise Margin for D1	239
$5B12_H$	RA_MN_MRG_D2	RA Minimum Noise Margin for D2	240
$5B13_H$	RA_MN_MRG_U1	RA Minimum Noise Margin for U1	240
$5B14_H$	RA_MN_MRG_U2	RA Minimum Noise Margin for U2	240
$5B19_H$:$5B1A_H$	RA_MX_RATE_DS	RA Maximum Downstream Rate	240
$5B1B_H$:$5B1C_H$	RA_MX_RATE_US	RA Maximum Upstream Rate	241
$5B1D_H$:$5B1E_H$	RA_CF_D1	RA Center Frequency (CF) for D1	239
$5B1F_H$:$5B20_H$	RA_CF_D2	RA Center Frequency (CF) for D2	242
$5B21_H$:$5B22_H$	RA_CF_U1	RA Center Frequency (CF) for U1	242
$5B23_H$:$5B24_H$	RA_CF_U2	RA Center Frequency (CF) for U2	242
$5B25_H$	RA_SR_D1	RA Symbol Rate (SR) for D1	242
$5B26_H$	RA_SR_D2	RA Symbol Rate (SR) for D2	242
$5B27_H$	RA_SR_U1	RA Symbol Rate (SR) for U1	243
$5B28_H$	RA_SR_U2	RA Symbol Rate (SR) for U2	243
$5B29_H$	RA_PSD_D1	RA Power Spectral Density (PSD) for D1	243
$5B2A_H$	RA_PSD_D2	RA Power Spectral Density (PSD) for D2	243
$5B2B_H$	RA_PSD_U1	RA Power Spectral Density (PSD) for U1	243
$5B2C_H$	RA_PSD_U2	RA Power Spectral Density (PSD) for U2	243
$5B2D_H$	RA_PSD_MASK	RA Power Spectral Density (PSD) Mask	244
$5B2E_H$	RA_PSD_MAX	RA Power Spectral Density (PSD) Max	245
$5B2F_H$	RA_INTR_DS	RA Interleaver Delay, DS Register	245
$5B2F_H$	RA_INTR_US	RA Interleaver Delay, US Register	245
$5B31_H$	RA_MN_MRG_U0	RA Minimum Noise Margin for U0	246
$5B40_H$	RA_STATUS	RA Process Status	247
$5B41_H$	RA_RESTRT_CNT	RA Process Rerun Counter	247

Table 67 RA Process Registers (page 2 of 2)

Offset Address	Short Name	Long Name	Pg
$5B42_H$	RA_RSLT_D1	D1 Band Use as a Result of RA Process	248
$5B43_H$	RA_RSLT_D2	D2 Band Use as a Result of RA Process	249
$5B44_H$	RA_RSLT_U1	U1 Band Use as a Result of RA Process	249
$5B45_H$	RA_RSLT_U2	U2 Band Use as a Result of RA Process	249

10.3 Detailed Register Descriptions – Digital Block

This section contains detailed descriptions of the registers specific to the digital block on the PEF 22827, grouped as follows:

Note: Reserved bits are for internal use only.

10.4 Main Control Registers

Base Address: 0000_H

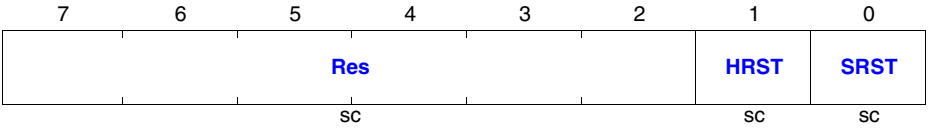
Main control registers include the following:

- **Main Control Register (MAIN_CTL)**
- **Main Operation Mode Register (MAIN_MODE)**
- **Link Operation Mode Register (LINK_MODE)**
- **VOC Control Register (VOC_CNTL)**
- **VOC Message Opcode to Send Register (VOC_OC)**
- **VOC Data to Send Register (VOC_DAT)**
- **PSD Output Adjustment Register (PSDADJ)**
- **Attenuation Input Adjustment Register (ATTADJ)**

10.4.1 Main Control Register (MAIN_CTL)

The **MAIN_CTL** register triggers control procedures. All bits are cleared as soon as the action finishes.

MAIN_CTL
Main Control Register **($8F00_H$)** **Reset Value: 00_H**

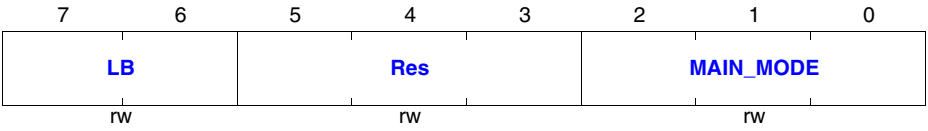


Field	Bits	Type	Description
Res	7:2	sc	Reserved
HRST	1	sc	**Hard Reset** After hard reset: • Parameters may be uploaded from EEPROM. • Modem samples general purpose I/O pins. 0_B No operation. 1_B Reset.
SRST	0	sc	**Soft Reset** After soft reset: • Parameters may not be uploaded from EEPROM. • Modem does not sample general purpose I/O pins. 0_B No operation. 1_B Reset.

10.4.2 Main Operation Mode Register (MAIN_MODE)

The **MAIN_MODE** register defines the conditions for the main operations of the device.

MAIN_MODE
Main Operation Mode Control Register($8F01_H$) **Reset Value: 03_H**



Field	Bits	Type	Description
LB	7:6	rw	**Loop Back Request** Unused values are reserved. 00_B No loop back. 01_B Local loop back. 10_B Remote loop back.
Res	5:3	rw	**Reserved**
MAIN_MODE	2:0	rw	**Main Operation Mode for LT Configuration** When the chip is configured as an NT, this bit is always 001 (unchanged by the user). Unused values are reserved. 000_B No operation. Link is deactivated. 001_B Establish a warm start link as defined by the WS_STP. 011_B Establish cold start, based on the default (DF_STP). 100_B Establish boot link.

10.4.3 Link Operation Mode Register (LINK_MODE)

The **LINK_MODE** register defines conditions for link operation. The reset value is 0100 1000 (48_H).

LINK_MODE
Link Operation Mode Register ($8F02_H$) Reset Value: 48_H

7	6	5	4	3	2	1	0
LR_EN	AH_EN	DF0_SKIP	Res	PBO_EN	EOC_EN	ADD_MRGN	INITIATOR
rw			rw	rw	rw	rw	rw

Field	Bits	Type	Description
LR_EN	7	rw	**Long Reach Capability** 0_B LR not supported. Any DF_STP with long-reach parameters is rejected. (Default) 1_B Long Reach (LR) capability supported (filters or AH, and 25 MHz clock on LT side). The RA process determines whether or not to implement LR.

Field	Bits	Type	Description
AH_EN	6	rw	**Adaptive Hybrid (AH) Enable** If the AH algorithm is enabled on the CO side, it is run under the following conditions (on the CPE side, this bit is don't care): • Cold start • Warm start, if the AH algorithm has not yet been run. 0_B AH algorithm is disabled. 1_B AH algorithm is enabled. (Default)
DF0_SKIP	5	rw	**Skip DF_STP0, Use DF_STP1 or DF_STP2** If the fixed standard default STP is not used (DF0_SKIP is 1), link establishment is attempted with the programmable STPs, DF_STP1 first, and then DF_STP2 until a link is successful. 0_B Load and activate using one of the default standard DF_STPs. 1_B Skip DF_STP0, and try to establish a link using programmable DF_STP1 or DF_STP2 alternately, until a link is successful. For parameter mapping in DF_STP1 and DF_STP2, see: • In EEPROM - **"DF_STP1 and DF_STP2 Parameter Mapping in EEPROM" on Page 92** • In RAM - **"Default STP Mapping" on Page 108**
Res	4	rw	**Reserved**
PBO_EN	3	rw	**Power Back Off (PBO) Control** 0_B Disable power back off. 1_B Enable power back off. (Reset)
EOC_EN	2	rw	**EOC Pins and Signals Control** 0_B Disable EOC pins and signals for use for LEDs. (Reset) 1_B Enable EOC pins and signals.
ADD_MRGN	1	rw	This bit adds 2.5dB of additional margin.
INITIATOR	0	rw	**Modem Link Initiator Control at the NT** 0_B Modem waits for other side to initiate link. (Default) 1_B Modem initiates link.

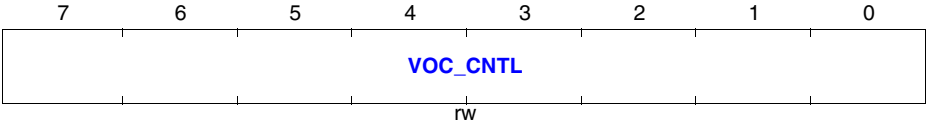
10.4.4 VOC Control Register (VOC_CNTL)

The **VOC_CNTL** register enables access to local and remote parameters by triggering a read or write operation by the VOC API. It is cleared as soon as the operation is complete.

For details and descriptions of opcodes and related data fields see:

- **“Link Control” on Page 192**.
- **“Link Performance Parameters” on Page 193**.
- **“Access to Remote Registers” on Page 194**.

VOC_CNTL
VOC Control Register **(8F04$_H$)** **Reset Value: NA**



Field	Bits	Type	Description
VOC_CNTL	7:0	rw	**VOC API Read or Write Operation Enable** 0000 0000$_B$ No operation. 0001 0000$_B$ Get local parameters listed in **Table 69 "Link Performance Parameters" on Page 193**. 0100 0000$_B$ Send VOC opcode and data to enable access to remote registers or read of link performance data. 1000 0000$_B$ Send a VOC of type CHANGE (opcode A0$_H$) to remote modem, to apply a new current STP.

10.4.5 VOC Message Opcode to Send Register (VOC_OC)

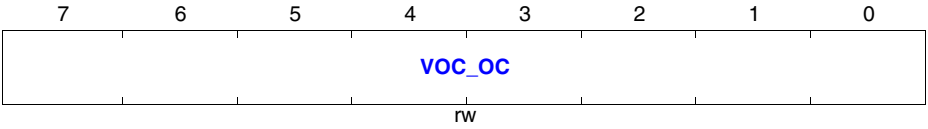
The **VOC_OC** register holds the opcode of the VDSL overhead channel (VOC) message, which specifies the type of data in the 16-bit **VOC_DAT** (8F07$_H$:8F06$_H$) register.

Read VOC_OC to verify the operation (refer to Section 7.6.4.1):

- If it contains the same opcode that was sent, read bits 11:0 of VOC_DAT for the requested parameters.
- If it contains 00$_H$, there is a communication error.
- If it contains F0$_H$ (Unable to Comply VOC), the remote modem cannot comply with the request.

For detailed descriptions of opcodes and related data fields see **Table 68**, **Table 69** and **Table 70**, on pages **192**, **193** and **194**, respectively.

VOC_OC
VOC Message Opcode to Send Register ($8F05_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
VOC_OC	7:0	rw	**Valid VOC Message Opcode** For a list of opcodes and their meanings, see: • **"Link Control" on Page 192**. • **"Link Performance Parameters" on Page 193**. • **"Access to Remote Registers" on Page 194**.

10.4.6 VOC Data to Send Register (VOC_DAT)

The 16-bit **VOC_DAT**specifies VDSL overhead channel (VOC) message parameters and the 12 bits of VOC data to send or receive. The most significant bits of the 12-bit VOC data are at $8F06_H$.

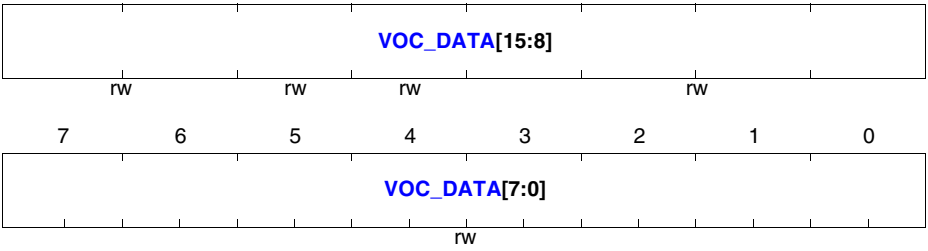
The bitmap for this register depends on the content:

- For Link Control, bits 15:12 are as shown in the detailed bit description below and **Table 68**.
- For Link Performance parameters, the values of bits 11:0 are as shown in **Table 69** and bits 15:12 must be set as follows:
  0000 = DS 1 or US1
  0100 = DS 2 or US2
- For Access to Remote Registers, the values of bits 15:0 are as shown in **Table 70**.

VOC_DAT
VOC Data to Send Register ($8F06_H$:$8F07_H$) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8

VOC_DAT
VOC Data to Send Register **($8F06_H$:$8F07_H$)** **Reset Value: 0000_H**



Field	Bits	Type	Description
STP_CODE	15:14	rw	**STP Select for Link Control Only** Unused values are reserved. 01_B WS_STP 10_B CR_STP
CARRIER_DIR	13	rw	**Carrier Direction, for Link Control Only** 0_B Downstream 1_B Upstream
CARRIER_NUM	12	rw	**First or Second Carrier, for Link Control Only** Must be cleared to 0 for INTERLV parameter in **Table 68**. 0_B The first carrier. 1_B The second carrier.
VOC_DATA	11:0	rw	**VOC Data for the VOC API to Send or Receive** Data is specified by the opcode (VOC_OC register at $8F05_H$) and described in detail in **Table 68**, **Table 69** and **Table 70**, on pages **192**, **193** and **194**, respectively.

Table 68 Link Control (page 1 of 2)

Parameter	Opcode	VOC_DAT Data Fields (Bits 11:0)
PROFILE (Not currently supported)	0010 0000$_B$ (20$_H$)	**Profile Name of target STP (not used for current STP).** Before using PROFILE, make sure a profile was saved in the EEPROM of the NT. Direction and carrier number are not needed. The profile name describes the complete link. Bits 11:4 and 2:0 specify profile name. Bit 3 is reserved.
INTERLV	0010 0001$_B$ (21$_H$)	**Interleaver Block Length and Depth for Specified Direction** Bit 12 must be cleared to 0. Valid values: 0-64 (0000 0000 through 0100 000) Bits 11:10 - Interleaver block length I, as follows: – 11 - $I = S / 8$ – 10 - $I = S / 4$ – 00 and 01 are reserved. Bits 9:8 are reserved. Bits 7:0 - Interleaver depth M (0 disables the Interleaver.)
FRAME	0010 0010$_B$ (22$_H$)	**Fast Frame Parameters for the Specified Direction** Bits 11:4 = F If I in INTERLV parameter = $S/4$, set to multiple of 4. If I in INTERLV parameter = $S/8$, set to multiple of 8. Bits 3:0 = RF / 2
PSDMASK	0010 0011$_B$ (23$_H$)	**Notch Control for a Direction and Carrier** One notch per band supported, with bits 7:4 reserved and: Bit 3: notch on US2 at the NT, 10.1 - 10.15 MHz. Bit 2: notch on DS2 at the LT, 7.0 - 7.1 MHz. Bit 1: notch on US1 at the NT, 3.5 - 3.8 MHz. Bit 0: notch on DS1 at the LT, 1.81 - 2.0 MHz.
PSDLEVEL	0010 0100$_B$ (24$_H$)	**PSD Level of Specified Direction and Carrier** For upstream operations this parameter defines the maximum PSD level. Bits 11:8 are reserved. Bits 7:0 specify PSD_LVL, where: PSD level (in dBm/Hz) = PSD_LVL/4 – 100
SMBLRATE	0010 0110$_B$ (26$_H$)	**Symbol Rate for Specified Direction and Carrier** Bits 11:8 are reserved. Bits 7:0 specify the symbol rate in units of 67.5 kbit/s.

Table 68 Link Control (page 2 of 2)

Parameter	Opcode	VOC_DAT Data Fields (Bits 11:0)
CONSTEL	0010 0111$_B$ (27$_H$)	**Constellation Size for Specified Direction and Carrier** Bits 11:5 are reserved. Bit 4 = Reduced constellation (not valid for target STP) Bits 3:0 = Log2 (constellation size)
CENFREQN	0010 1000$_B$ (28$_H$)	Center Frequency of Specified Direction and Carrier Bits 11:9 are reserved. Bits 8:0 specify frequency, in units of 33.75 kHz.

Table 69 Link Performance Parameters

Parameter	Opcode	VOC_DAT Data Fields (Bits 11:0)
SNR	0000 0001$_B$ (01$_H$)	**SNR for Specified Carrier** • Bit 14 specifies band. 0 is band 1; 1 is band 2. • Bits 11:8 are 0. • Bits 7:0 specify SNR, in units of 0.25 dB
ATT	0000 0011$_B$ (03$_H$)	**Attenuation Level for Specified Carrier** • Bit 14 specifies band. 0 is band 1; 1 is band 2. • Bits 11:8 are reserved. • Bits 7:0 = Attenuation, in units of 0.25 dB
FECS	0001 0000$_B$ (10$_H$)	**Number of Erroneous Bytes Corrected by the FEC in the Slow Channel Since the Last Read Operation**
FECF	0001 0010$_B$ (12$_H$)	**Number of Erroneous Bytes Corrected by the FEC in the Fast Channel Since the Last Read Operation**
ERRS	0001 0100$_B$ (14$_H$)	**Number of Uncorrectable Code Words (Reed Solomon Errors) in Slow Channel since Last Read Operation**
ERRF	0001 0110$_B$ (16$_H$)	**Number of Uncorrectable Code Words (Reed Solomon Errors) in Fast Channel Since the Last Read Operation**

Table 70 Access to Remote Registers

Parameter	VOC_OC Opcode	VOC_DAT Data Fields (Bits 15:0)
REMOTE_RD	$1001\ 0011_B$ (93_H)	**Address of Register From Which to Begin to Read (Transmission) and the Read Data (Two Bytes)** • During transmission, bits 15:8 are the high byte of the address and bits 7:0 are the low byte. • During reception, bits 15:8 contain the requested data and bits 7:0 are not relevant.
NEXT_WORD_R	$1110\ 0100_B$ ($E4_H$)	**Request for Next Two Consecutive Bytes after the Address in REMOTE_RD, and Echo of Read Data** • During transmission, the content of both bytes is not relevant. • During reception, bits 15:0 contain the next two requested bytes of data.
REMOTE_WR	$1001\ 0100_B$ (94_H)	**Address of Register to Which to Write the Contents of NEXT_WORD_W** • Bits 15:8 specify the high byte of the address. • Bits 7:0 specify the low byte of the address.
NEXT_WORD_W	$1110\ 0011_B$ ($E3_H$)	**Data (1 byte, Bits 15:8) in Register to be Written from Address Specified in Previous REMOTE_WR or Following the Previous NEXT_WORD_W** • Bits 15:8 contain the data. • Bits 7:0 are not relevant.
REMOTE_WR_BT	$0000\ 0110_B$ (06_H)	**Address of Register from Which to Begin to Write 25 Consecutive Bytes During a Boot Link** • Bits 15:8 specify the low start address. • Bits 7:0 specify the high start address. *Note: High and low bytes are reverse of standard.*

Table 70 Access to Remote Registers

Parameter	VOC_OC Opcode	VOC_DAT Data Fields (Bits 15:0)
REM_16_WR_BT	*xxxx* 0010_B ($x2_H$) *x = number of bytes to write.*	**Address of Register from Which to Begin to Write 1 through 16 Consecutive Bytes During Boot Link** 02_H indicates 16 bytes. • Bits 15:8 specify the low start address. • Bits 7:0 specify the high start address. *Note: High and low bytes are reverse of standard.*
REM_16_RD_BT	*xxxx* 0001_B ($x1_H$) *x = number of bytes to write.*	**Address of Register from Which to Begin to Read 1 through 16 Consecutive Bytes During Boot Link** 01_H indicates 16 bytes. • Bits 15:8 specify the low start address. • Bits 7:0 specify the high start address. *Note: High and low bytes are reverse of standard.*

10.4.7 PSD Output Adjustment Register (PSDADJ)

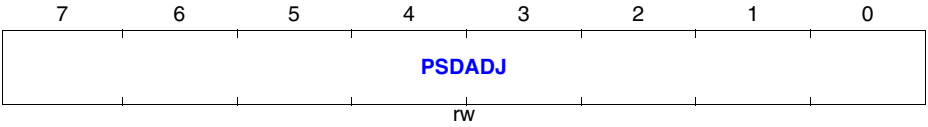
The **PSDADJ** register specifies a signed value to add to the PSD power level output from the board, in units of 0.25 dB. This value is added to the PSDLEVEL STP opcode VOC parameter for both carriers that are transmitting.

For example:

- To add 3 dB to the general PSD output, do the following:
  a) Multiply 3 dB x 4 = 12 (or $0C_H$)
  b) Perform the command <WR 8F0C 0C>
- To subtract 4 dB from the general PSD output, do the following:
  a) Multiply 4 dB x 4 = 16 (or 10_H)
  b) Perform the command <WR 8F0C F0>

When firmware determines that synthesized impedance is selected (using the **EOC_TCLK** configuration pin), it automatically decreases the value of this register by 8 db to calibrate the line driver.

PSDADJ
Output PSD Adjustment Register ($8F0C_H$) Reset Value: 00_H



Field	Bits	Type	Description
PSDADJ	7:0	rw	**Adjustment of PSD Output from the Board**

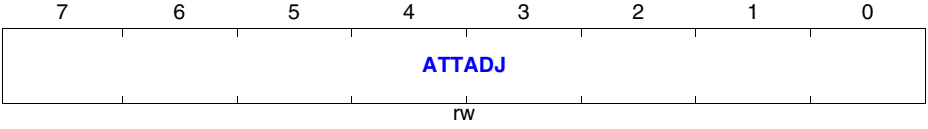
10.4.8 Attenuation Input Adjustment Register (ATTADJ)

The **ATTADJ** register specifies a value in units of 0.25 dBm to adjust attenuation. This value is added to the result of attenuation measurement for each board when the ATT VOC parameter is issued or during the PBO process. See **"Power Back Off (PBO)" on Page 115**.

To determine the adjustment required (the value of this register) at the LT, do the following:

1. Connect modems directly (0m distance).
2. Set the modem to default link (make sure that the default is not long reach default).
3. Set register ATTADJ (0x8F0D) to 0 on both sides (LT and NT).
4. Trigger the attenuation measurement by issuing the ATT link performance VOC command (opcode 03_H).
5. Record US1 PSD at 0x5E23 on NT side (USPSD).
6. Set ATTADJ register on NT side with the value 256-ATT(DS1) and on LT side with the value 256-(ATT(US1)-(0xA0-USPSD)).
7. Repeat Step 4 until the attenuation measurement on the NT side is 0. For the LT side, the attenuation should be 0xA0-USPSD.
8. Apply the changes by saving this register to EEPROM at location 0x7813.

ATTADJ
Input Attenuation Adjustment Register ($8F0D_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
ATTADJ	7:0	rw	**Adjustment of PSD Input to the Board**

10.5 Main Status Registers

This section describes the following status registers for standard firmware:

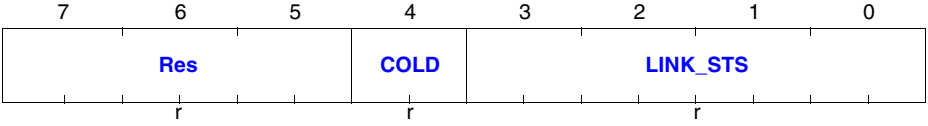
- **General Status Register 1 (GEN_STATUS1)**
- **General Status Register 2 (GEN_STATUS2)**
- **General Status Register 3 (GEN_STATUS3)**

- Configuration Pins Status Register 1 (CONFIG_STS1)
- Configuration Pins Status Register 2 (CONFIG_STS2)
- SNR for Band 1 (SNR_BAND1)
- SNR for Band 2 (SNR_BAND2)
- Remote Loss of Frame Counter (R_FR_LOS_CNT)
- Channel Failures Counter (FAIL_CNT)
- Loss of Signal on Bands 1 and 2
- Local Loss of Frame Counter (L_FR_LOS_CNT)
- SNR Margin and BER Overflow Status Register (SNR_BER)

10.5.1 General Status Register 1 (GEN_STATUS1)

The **GEN_STATUS1** register is one of three registers that provide general status information. The others are **GEN_STATUS2** at $8F10_H$ and **GEN_STATUS3** at $8F11_H$.

GEN_STATUS1
General Status Register 1 **($8F0F_H$)** **Reset Value: 00_H**

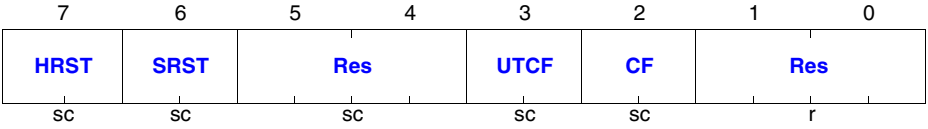


Field	Bits	Type	Description
Res	7:5	r	**Reserved**
COLD	4	r	**Next Link Indicator** 0_B Next link will be warm. 1_B Next link will be cold, with DF_STP.
LINK_STS	3:0	r	**Link Status Indicator** Unused values are reserved. 0000_B No active link. 0001_B Waiting for other side to establish link. 0010_B Trying to establish link. 0011_B Default link is established. 0100_B Reduced link is established. 0101_B Target link is established. 0110_B Idle link is established. (Not currently supported.) 0111_B Boot link is established.

10.5.2 General Status Register 2 (GEN_STATUS2)

The **GEN_STATUS2** register is one of three registers that provide general status information. The others are **GEN_STATUS1** at $8F0F_H$ and **GEN_STATUS3** at $8F11_H$.

GEN_STATUS2
General Status Register 2 **($8F10_H$)** **Reset Value: 00_H**

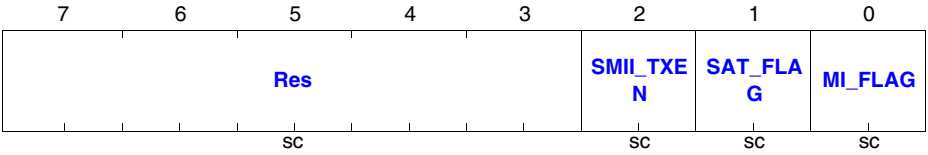


Field	Bits	Type	Description
HRST	7	sc	**Hard Reset Indicator** Cleared on read. 0_B No indication. 1_B Hard reset occurred.
SRST	6	sc	**Soft Reset Indicator** Cleared on read. 0_B No indication. 1_B Soft reset occurred.
Res	5:4	r	**Reserved**
UTCF	3	sc	**Unable to Comply Flag** Cleared on read. 0_B No indication. 1_B NT is unable to comply with the last VOC message.
CF	2	sc	**Comply Flag** Cleared on read. 0_B No indication. 1_B Valid message received from the NT.
Res	1:0	r	Reserved.

10.5.3 General Status Register 3 (GEN_STATUS3)

The **GEN_STATUS3** register is one of three registers that provide general status information. The others are **GEN_STATUS1** at $8F0F_H$ and **GEN_STATUS2** at $8F10_H$.

GEN_STATUS3
General Status Register 3 **(8F11$_H$)** **Reset Value: 00$_H$**

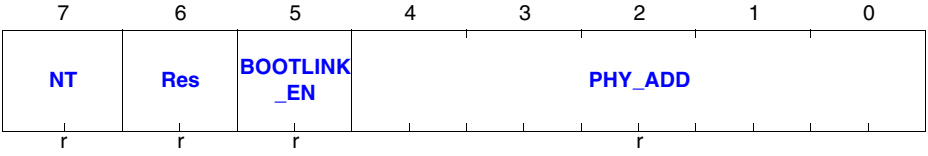


Field	Bits	Type	Description
Res	7:3	sc	**Reserved**
SMII_TXEN	2	sc	**SMII Typical Mode Transmission Indicator** Cleared on read. 0_B Transmission disabled. 1_B Transmission enabled.
SAT_FLAG	1	sc	**ADC Saturation Caused by Noise Indicator** Cleared on read. 0_B No indication. 1_B Strong noise caused ADC saturation condition.
MI_FLAG	0	sc	**Micro-interruption Indicator** Cleared on read. 0_B No indication. 1_B Micro-interruption occurred.

10.5.4 Configuration Pins Status Register 1 (CONFIG_STS1)

The fields of the **CONFIG_STS1** and **CONFIG_STS2** (8F13$_H$) registers describe the values of some configuration pins after hard reset. See **"Configuration Pins During Hard Reset" on Page 81**.

CONFIG_STS1
Configuration Pins Status Register 1 (8F12$_H$) **Reset Value: 00$_H$**

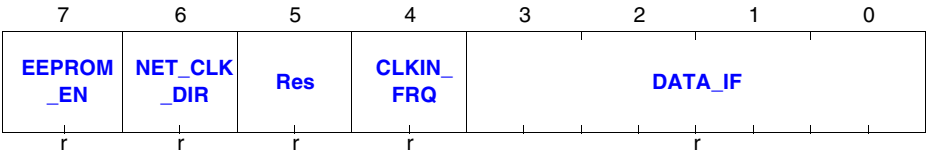


Field	Bits	Type	Description
NT	7	r	**Current Operation Mode** 0_B Modem works as line terminal (LT). 1_B Modem works as network terminal (NT).
Res	6	r	**Reserved**
BOOTLINK_EN	5	r	**Boot Link Status** 0_B No indication. 1_B Boot link is enabled.
PHY_ADD	4:0	r	**PHY Address for MDIO**

10.5.5 Configuration Pins Status Register 2 (CONFIG_STS2)

The fields of the **CONFIG_STS1** ($8F12_H$) and **CONFIG_STS2** registers describe the values of some configuration pins after reset. See **"Configuration Pins During Hard Reset" on Page 81**.

CONFIG_STS2
Configuration Pins Status Register 2 ($8F13_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
EEPROM_EN	7	r	**Status of EEPROM Enable Pin 38** 0_B EEPROM is disabled. 1_B EEPROM is enabled.
NET_CLK_DIR	6	r	**Direction of Network Clock Signals (Pin71)** 0_B Clocks externally derived (pins configured for input). 1_B Clocks internally derived (pins configured for output).
Res	5	r	**Reserved**
CLKIN_FRQ	4	r	**Frequency of CLKIN** 0_B 25.92 MHz 1_B 38.88 MHz

Field	Bits	Type	Description
DATA_IF	3:0	r	**Data Interface Pins 47 (MSB), 48, 49 and 90 (LSB), in That Order** Unused values are reserved. 0100_B MII MAC. 0101_B RMII MAC. 0110_B Typical SMII PHY. 1000_B TC layer parallel. 1100_B MII PHY. 1101_B RMII PHY. 1110_B Source Synchronous SMII PHY.

10.5.6 SNR for Band 1 (SNR_BAND1)

The **SNR_BAND1** register specifies the SNR of the first received band, in units of 0.25 dB.

SNR_BAND1
SNR for Band 1 **($8F14_H$)** **Reset Value: 00_H**

Field	Bits	Type	Description
SNR_BAND1	7:0	rw	**First Received Band SNR, in Units of 0.25 dB**

10.5.7 SNR for Band 2 (SNR_BAND2)

The **SNR_BAND2** register specifies the SNR of the first received band, in units of 0.25 dB.

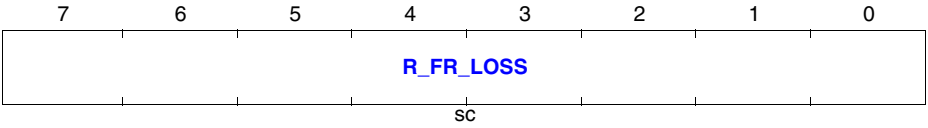
SNR_BAND2
SNR for Band 2 **($8F15_H$)** **Reset Value: 00_H**

Field	Bits	Type	Description
SNR_BAND2	7:0	rw	**Second Received Band SNR, in Units of 0.25 dB**

10.5.8 Remote Loss of Frame Counter (R_FR_LOS_CNT)

The **R_FR_LOS_CNT** counter counts the number of frames lost at the remote modem (LOF transitions from S5 to S6 in the Link State Machine). See **Figure 16, The Link State Machine, on page 103**. This register is cleared on read.

R_FR_LOS_CNT
Remote Loss of Frame Counter **($8D37_H$)** **Reset Value: 00_H**

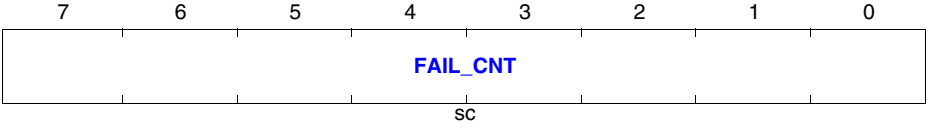


Field	Bits	Type	Description
R_FR_LOSS	7:0	sc	**Number of Frames Lost at the Remote Modem** Count of LOF transitions from S5 to S6.

10.5.9 Channel Failures Counter (FAIL_CNT)

The **FAIL_CNT** counter counts disconnections in the link state machine. This register is cleared on read.

FAIL_CNT
Channel Failures Counter **($8D38_H$)** **Reset Value: 00_H**



Field	Bits	Type	Description
FAIL_CNT	7:0	sc	**Disconnections in the Link State Machine**

10.5.10 Loss of Signal on Bands 1 and 2

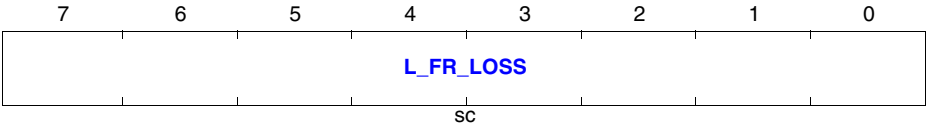
The N1_LOSS_CNT and N2_LOSS_CNT counters to count the number of times the signal is lost (LOS transitions from S5 to S6 in the Link State Machine) on Bands 1 and 2 are no longer supported.

Use the **FAIL_CNT**, **L_FR_LOS_CNT** (local modem) and **R_FR_LOS_CNT** (remote modem) counters to monitor signal failures instead.

10.5.11 Local Loss of Frame Counter (L_FR_LOS_CNT)

The **L_FR_LOS_CNT** counter counts the number of frames lost at the local modem (LOF transitions from S5 to S6 in the Link State Machine). See **Figure 16, The Link State Machine, on page 103**. This register is cleared on read.

L_FR_LOS_CNT
Local Loss of Frame Counter **($8D3F_H$)** **Reset Value: 00_H**



Field	Bits	Type	Description
L_FR_LOSS	7:0	sc	**Number of Frames Lost at the Local Modem** Count of LOF transitions from S5 to S6.

10.5.12 SNR Margin and BER Overflow Status Register (SNR_BER)

The **SNR_BER** register indicates when the SNR margin for bands 1 and 2 is too high or too low and when the BER is too high.

The bits in this register are sticky bits that are set by firmware.

During Rate Adaptive (RA) process monitoring:

- Firmware reads bits 0, 1 (SNR too high), bits 2, 3 (SNR too low) and bit 4 (BER too high), to determine whether or not to rerun the RA process. Bit 4 restarts the RA automatically. Bits 0 to 3 set bit RA_RERUN in register RA_STATUS.
- Firmware clears bits 0, 1, 2, 3 and 4 after they are set.
- The user must clear bits 0, 1, 2 and 3, to initialize them, before start of RA.

When the RA process monitoring is not active, all bits must be cleared to 0 by the user.

SNR_BER
SNR Margin and BER Overflow Status Register
(7F11$_H$) **Reset Value: 00$_H$**

7	6	5	4	3	2	1	0
Res			BER_HI	SNR_LO_2	SNR_LO_1	SNR_HI_2	SNR_HI_1
	rw		rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	7:5	rw	**Reserved**
BER_HI	4	rw	**BER Too High** Maximum BER varies, as follows: • During normal operation, three uncorrected RS errors within one second is the maximum. • During the RA process with TLAN, five uncorrected RS errors within one second is the maximum. 0 No indication. 1 Bit Error Rate (BER) is too high. When RA is not active, must be cleared by user.
SNR_LO_2	3	rw	**SNR Too Low on Band 2** Minimum SNR is set by the SNR_MIN register at 7F19$_H$. 0 No indication. 1 SNR on band 2 is lower than the minimum.
SNR_LO_1	2	rw	**SNR Too Low on Band 1** Minimum SNR is set by the SNR_MIN register at 7F19$_H$. 0 No indication. 1 SNR on band 1 is lower than the minimum.
SNR_HI_2	1	rw	**SNR Too High on Band 2** Maximum SNR is set by the SNR_MAX register at 7F18$_H$. 0 No indication. 1 SNR on band 2 is higher than maximum.
SNR_HI_1	0	rw	**SNR Too High on Band 1** Maximum SNR is set by the SNR_MAX register at 7F18$_H$. 0 No indication. 1 SNR on band 1 is higher than maximum.

10.6 SNR Registers

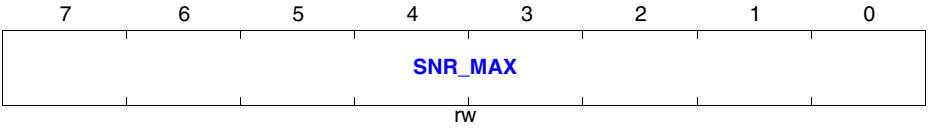
This section describes the following:

- SNR Maximum Register (SNR_MAX)
- SNR Minimum Register (SNR_MIN)

10.6.1 SNR Maximum Register (SNR_MAX)

The SNR_MAX register specifies the maximum SNR margin threshold that the RA process will accept before clearing the appropriate status bits in the SNR_BER register at $7F11_H$ and rerunning the RA process. This value is expressed in 0.25 dB units. The default is 18_H, or 6 dB.

SNR_MAX
SNR Maximum Register **($7F18_H$)** **Reset Value: 18_H**

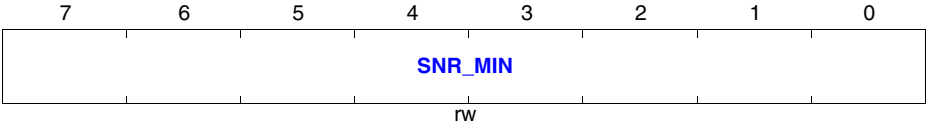


Field	Bits	Type	Description
SNR_MAX	7:0	rw	**Maximum SNR Threshold**

10.6.2 SNR Minimum Register (SNR_MIN)

The SNR_MIN register specifies the minimum SNR margin threshold that the RA process will accept before clearing the appropriate status bits in the SNR_BER register at $7F11_H$ and rerunning the RA process. This value is expressed in 0.25 dB units. The default is $0C_H$, or 3 dB.

SNR_MIN
SNR Minimum Register **($7F19_H$)** **Reset Value: $0C_H$**



Field	Bits	Type	Description
SNR_MIN	7:0	rw	**Minimum SNR Threshold**

10.7 Version Status Registers

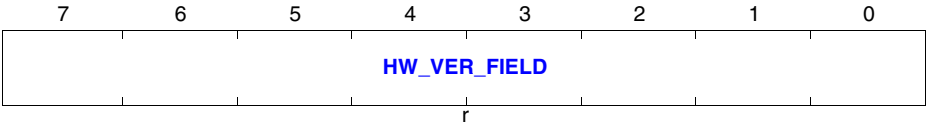
This section describes the following version status registers :

- Hardware Version Register (HW_VER_FIELD)
- ROM Version Register (ROM_VER_FIELD)
- Application Version Register (FW_VER_FIELD)
- Application Release Register (FW_REL_FIELD)
- Application Build Register (FW_BLD_FIELD)

10.7.1 Hardware Version Register (HW_VER_FIELD)

The **HW_VER_FIELD** register specifies the version of the hardware.

HW_VER_FIELD
Hardware Version Register **($5F62_H$)** **Reset Value: 91_H**

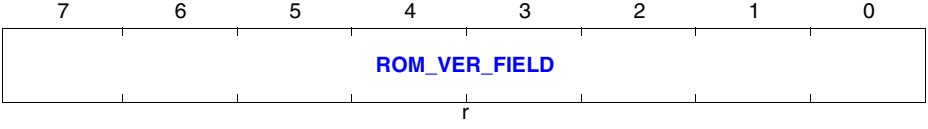


Field	Bits	Type	Description
HW_VER_FIELD	7:0	r	**Hardware Version Number**

10.7.2 ROM Version Register (ROM_VER_FIELD)

The **ROM_VER_FIELD** register specifies the version of the ROM.

ROM_VER_FIELD
Hardware Version Register **($5F63_H$)** **Reset Value: 48_H**

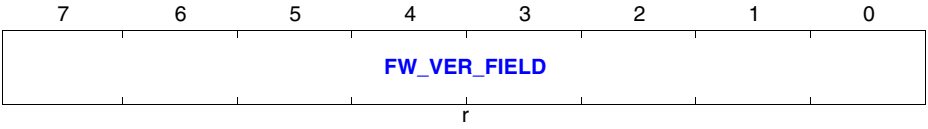


Field	Bits	Type	Description
ROM_VER_FIELD	7:0	r	**ROM Version Number**

10.7.3 Application Version Register (FW_VER_FIELD)

The **FW_VER_FIELD** register specifies the version of the current firmware application.

FW_VER_FIELD
Application Version Register **(5F64$_H$)** **Reset Value: N/A**

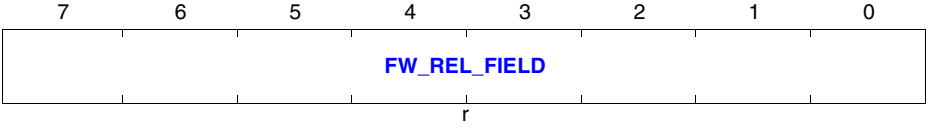


Field	Bits	Type	Description
FW_VER_FIELD	7:0	r	**Application Firmware Version Number**

10.7.4 Application Release Register (FW_REL_FIELD)

The **FW_REL_FIELD** register specifies the release number of the current firmware application.

FW_REL_FIELD
Application Release Register **(5F65$_H$)** **Reset Value: N/A**

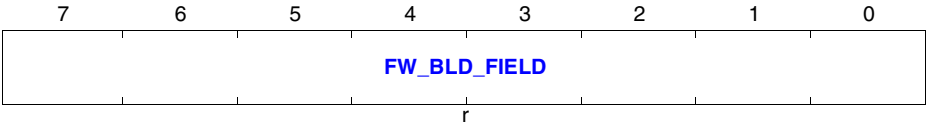


Field	Bits	Type	Description
FW_REL_FIELD	7:0	r	**Application Release Version Number**

10.7.5 Application Build Register (FW_BLD_FIELD)

The **FW_BLD_FIELD** register specifies the build number of the current firmware application specified in the register.

FW_BLD_FIELD
Application Build Number **($5F66_H$)** **Reset Value: N/A**



Field	Bits	Type	Description
FW_BLD_FIELD	7:0	r	**Build Number for Application Firmware**

10.8 RAM Check Registers

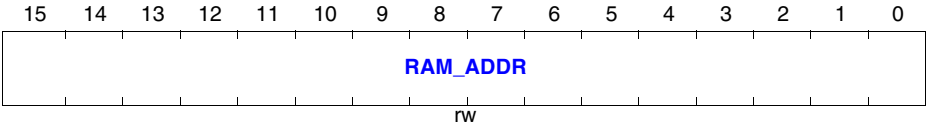
This section describes the following RAM check registers for all firmware:

- **RAM Check Start Address (RAM_ADDR)**
- **RAM Check Length (RAM_LENGTH)**
- **RAM Check Expected Checksum (RAM_CHKSUM)**
- **RAM Check Command or Status Register (RAM_CMD_STS)**

10.8.1 RAM Check Start Address (RAM_ADDR)

This 16-bit register specifies the start address of a RAM block to be checked, with the most significant byte at $5F67_H$.

RAM_ADDR
RAM Check Start Address **($5F67_H$:$5F68_H$)** **Reset Value: 0000_H**

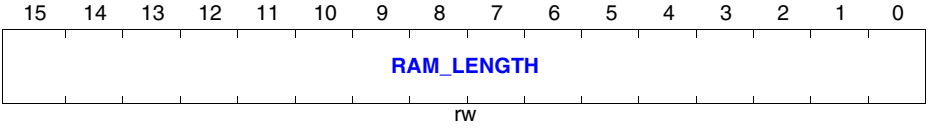


Field	Bits	Type	Description
RAM_ADDR	15:0	rw	**Start Address of RAM Block to be Checked**

10.8.2 RAM Check Length (RAM_LENGTH)

This 16-bit register specifies the length of the RAM check block, with the most significant byte of the length at $5F69_H$.

RAM_LENGTH
RAM Check Length ($5F69_H$:$5F6A_H$) Reset Value: 0000_H

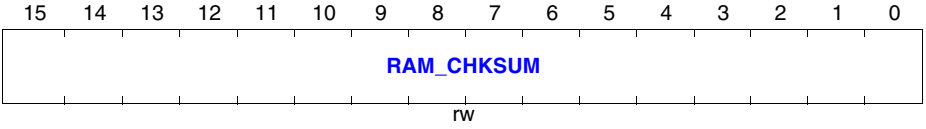


Field	Bits	Type	Description
RAM_LENGTH	15:0	rw	**Length of RAM Block to be Checked**

10.8.3 RAM Check Expected Checksum (RAM_CHKSUM)

This 16-bit register specifies the expected checksum produced by a RAM check, with the most significant byte at $5F6B_H$.

RAM_CHKSUM
RAM Check Expected Checksum ($5F6B_H$:$5F6C_H$) Reset Value: 0000_H

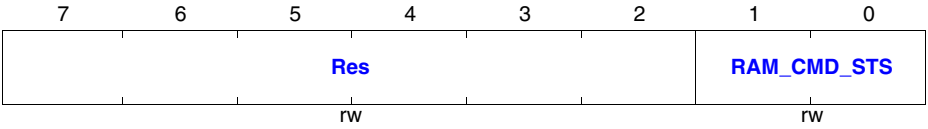


Field	Bits	Type	Description
RAM_CHKSUM	15:0	rw	**Expected CHKSUM of RAM Block to be Checked**

10.8.4 RAM Check Command or Status Register (RAM_CMD_STS)

Bits1:0 of the **RAM_CMD_STS** register specifies either the status of the checksum or issues a command to activate the checksum process.

RAM_CMD_STS
RAM Check Command or Status Register ($5F6D_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
Res	7:2	rw	**Reserved**
RAM_ CMD_ STS	1:0	rw	**RAM Check Status or Command** 00_B Status - Expected checksum was correct. 01_B Status - Expected checksum was not correct. 10_B Command - Activate checksum process. 11_B Command - Activate checksum process. If process succeeds, activate normal operation mode.

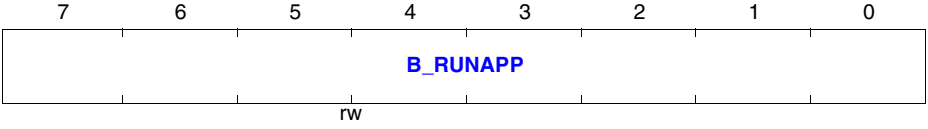
10.9 Firmware Control Register

This section describes the Firmware Control Register (FW_DLOAD).

10.9.1 Firmware Control Register (FW_DLOAD)

The **FW_DLOAD** register controls firmware activation during the boot loop.

FW_DLOAD
Firmware Control Register **($5F6F_H$)** **Reset Value: 00_H**



Field	Bits	Type	Description
B_RUNAPP	7:0	rw	**Firmware Activate During a Boot Loop** $0000\ 0000_B$ RAM application disabled. (00_H) $0000\ 0001_B$ RAM application enabled. (01_H)

10.10 EEPROM Control Registers

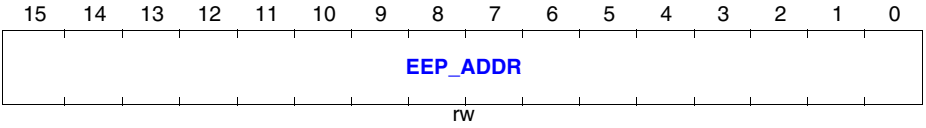
This section describes the following EEPROM control registers for all firmware:

- **Start Address of Page to Access in EEPROM (EEP_ADDR)**
- **Page Length to Read or Save in EEPROM (EEP_LENGTH)**
- **EEPROM Checksum Register (EEP_CHKSUM)**
- **EEPROM Data Register (EEP_DATA)**
- **EEPROM Command Register (EEP_COMMAND)**
- **EEPROM Status Register (EEP_STATUS)**

10.10.1 Start Address of Page to Access in EEPROM (EEP_ADDR)

The **EEP_ADDR** register holds the 16-bit start address of the relevant data block in the EEPROM, with the most significant byte at $5F70_H$.

EEP_ADDR
Start Address of Page to Access in EEPROM ($5F70_H$:$5F71_H$) **Reset Value: 0000_H**

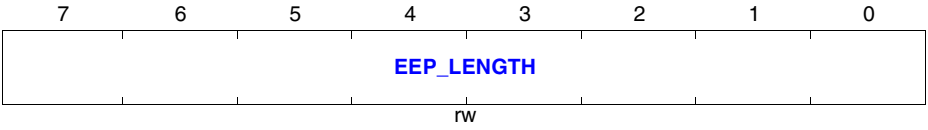


Field	Bits	Type	Description
EEP_ADDR	15:0	r	**Start Address to Read or Write in EEPROM**

10.10.2 Page Length to Read or Save in EEPROM (EEP_LENGTH)

The **EEP_LENGTH** register specifies the length of the page to read or save in EEPROM.

EEP_LENGTH
Page Length to Read or Save in EEPROM ($5F72_H$) **Reset Value: 00_H**

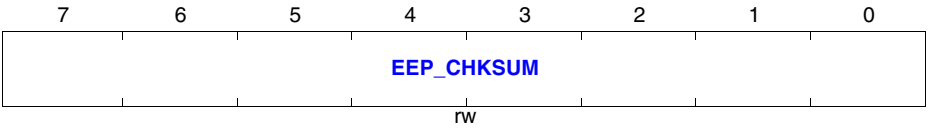


Field	Bits	Type	Description
EEP_LENGTH	7:0	rw	**Page Length to Read or Save in EEPROM**

10.10.3 EEPROM Checksum Register (EEP_CHKSUM)

For write operations, the **EEP_CHKSUM** register holds the EEPROM page checksum value calculated as:
EEP_CHKSUM = INV(ADDRESS_H + ADDRESS_L + LENGTH + SUM(DATA))+1.

EEP_CHKSUM
EEPROM Checksum Register **($5F73_H$)** **Reset Value: 00_H**

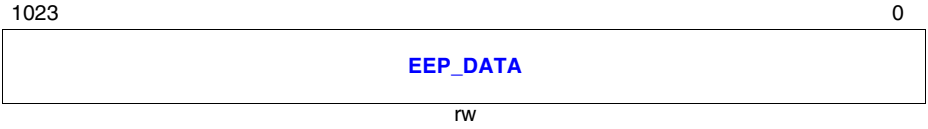


Field	Bits	Type	Description
EEP_CHKSUM	7:0	rw	**EEPROM Page Checksum Value**

10.10.4 EEPROM Data Register (EEP_DATA)

The **EEP_DATA** register holds up to 128 bytes of data to be read from or saved in EEPROM, with the most significant byte at $5F74_H$.

EEP_DATA
EEPROM Data Register **($5F74_H$:$5FF3_H$)** **Reset Value: 00_H**

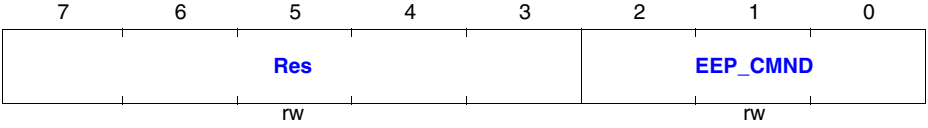


Field	Bits	Type	Description
EEP_DATA	1023:0	rw	**Data to Read from or Write to EEPROM**

10.10.5 EEPROM Command Register (EEP_COMMAND)

Bits 2:0 of the **EEP_COMMAND** register specify the command for the EEPROM handler.

EEP_COMMAND
EEPROM Command Register **(5FF6$_H$)** **Reset Value: 00$_H$**

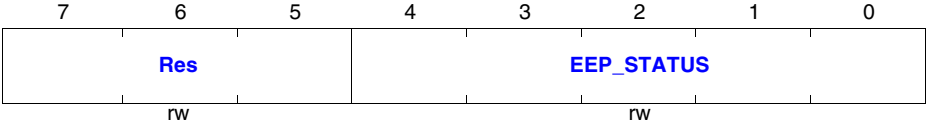


Field	Bits	Type	Description
Res	7:3		**Reserved**
EEP_CMND	2:0	rw	**Command for the EEPROM Handler** 000_B No operation. 001_B Write to header zone (0000_H through $007F_H$). 010_B Write to boot link zone ($7F00_H$ through $7FFF_H$). 011_B Write to common zone (other than header or boot link). See **"EEPROM Structure" on Page 83**. 100_B Read operation.

10.10.6 EEPROM Status Register (EEP_STATUS)

Bits 4:0 of the **EEP_STATUS** register hold the status of the last read or write from the EEPROM.

EEP_STATUS
EEPROM Status Register **(5FF7$_H$)** **Reset Value: 18$_H$**



Field	Bits	Type	Description
Res	7:5		**Reserved**
EEP_STATUS	4:0	rw	**Command for the EEPROM Handler** $0\ 1001_B$ Checksum operation failed. $0\ 1010_B$ Write operation succeeded. $0\ 1011_B$ Write operation failed. $0\ 1100_B$ Read operation succeeded. $0\ 1101_B$ Read operation failed. $1\ 0011_B$ Address header zone not valid. $1\ 0100_B$ Address boot link zone not valid. $1\ 0101_B$ Address common zone not valid.

10.11 MDIO Master Interface Registers

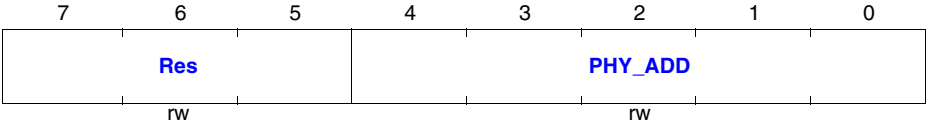
This section describes the following MDIO master interface registers for standard firmware:

- **Physical Address of the Slave MII (MII_PHY)**
- **Register Address of the Slave MII (MII_REG)**
- **Data to or from Slave Register (MII_D)**
- **MII Command Register (MII_CMD)**

10.11.1 Physical Address of the Slave MII (MII_PHY)

Bits 4:0 of the **MII_PHY** register specify the physical address of the slave MII. This field is reset with the values of the UTOD4:UTOD0 pins.

MII_PHY
Physical Address of the Slave MII (8CB0$_H$) Reset Value: COLO, ETHOD(3:0)

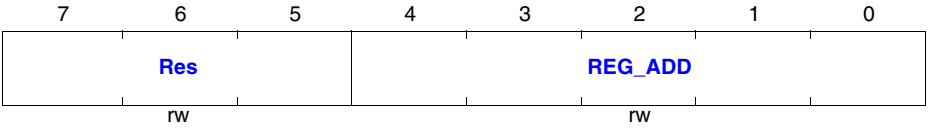


Field	Bits	Type	Description
Res	7:5	rw	**Reserved**
PHY_ADD	4:0	rw	**Physical Address of the Slave MII**

10.11.2 Register Address of the Slave MII (MII_REG)

Bits 4:0 of the **MII_REG** register specify the register address in the slave MII. During hard reset, the value of these bits is determined by sampling the PHY_ADD configuration pins.

MII_REG
Register Address of the Slave MII ($8CB1_H$) Reset Value: PHY_ADD pins

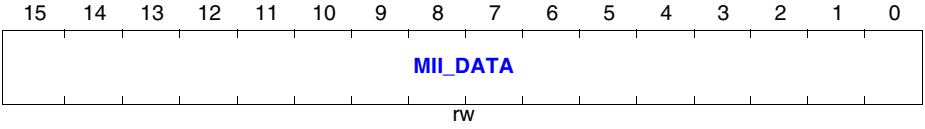


Field	Bits	Type	Description
Res	7:5	rw	**Reserved**
REG_ADD	4:0	rw	**Register Address in the Slave MII**

10.11.3 Data to or from Slave Register (MII_D)

The 16-bit **MII_D** register holds data to write to the MII slave or a result from the MII slave. The address of the low byte is $8CB2_H$ and of the high byte is $8CB3_H$.

MII_D
Data to or from Slave Register ($8CB3_H$:$8CB2_H$) Reset Value: 0000_H

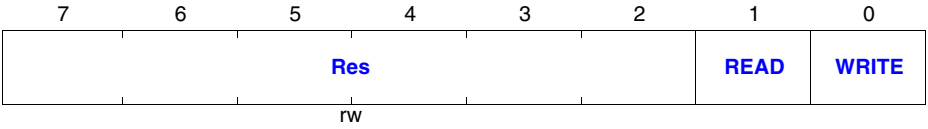


Field	Bits	Type	Description
MII_DATA	15:0	rw	**Data to Write to MII Slave or Result from MII Slave**

10.11.4 MII Command Register (MII_CMD)

Bits 1:0 of the **MII_CMD** register enable or disable MII read and write operations.

MII_CMD
MII Command Register **(8CB4$_H$)** **Reset Value: 00$_H$**



Field	Bits	Type	Description
Res	7:2	rw	**Reserved**
READ	1		**Read Operation Status** 0_B Read disabled. 1_B Read enabled.
WRITE	0	rw	**Write Operation Status** 0_B Write disabled. 1_B Write enabled.

10.12 MII Status Registers

This section describes the following MII status registers for standard firmware:

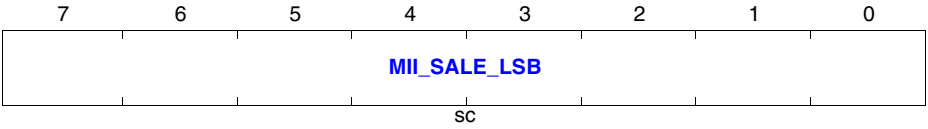
- **SNMP Alignment Errors Counter (MII_SALE)**
- **SNMP Single Collision Frames Counter (MII_SSCF)**
- **SNMP Multiple Collisions Frame Counter (MII_SMCF)**
- **SNMP Deferred Transmission Counter (MII_SDT)**
- **SNMP Late Collisions Counter (MII_SLC)**
- **Excessive Collisions Counter (MII_SEC)**
- **Reception Errors Counter (MII_SRE)**
- **Carrier Sense Errors Counter (MII_SCSE)**
- **Frame Too Long Counter (MII_SFTL)**
- **Frame Check Sequence Error Counter (MII_SFCS)**
- **Bytes Transmitted OK Counter (MII_SOTO)**
- **Bytes Received OK Counter (MII_SORO)**
- **Broadcast Frames Received Counter (MII_BCAST)**
- **Reception Pause Packets Counter (RXPAUS)**
- **Transmission Pause Packets Counter (TXPAUS)**
- **Transmitted Frames Counter (TXBCNT)**
- **Received Frames Counter (RXBCNT)**
- **Three MSBs for MII Counters (MII_CNTR_MSB)**

10.12.1 SNMP Alignment Errors Counter (MII_SALE)

The **MII_SALE** register holds the LSB of the 2-byte counter for alignment errors (odd number of nibbles) detected.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE0_H$ first. The other is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SALE
SNMP Alignment Errors Counter ($8CE0_H$) **Reset Value: 00_H**



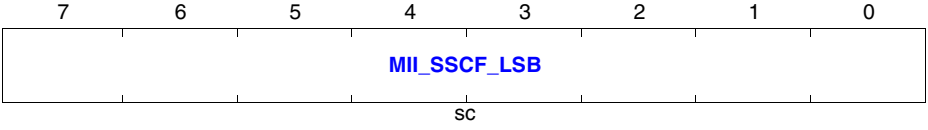
Field	Bits	Type	Description
MII_SALE_LSB	7:0	sc	**LSB of Counter for Alignment Errors**

10.12.2 SNMP Single Collision Frames Counter (MII_SSCF)

The **MII_SSCF** register holds the LSB of the 2-byte counter for frames successfully transmitted after a single collision.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE1_H$ first. The other is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SSCF
SNMP Single Collision Frames Counter ($8CE1_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
MII_SSCF_LSB	7:0	sc	**LSB of Counter of Frames Transmitted after a Single Collision**

10.12.3 SNMP Multiple Collisions Frame Counter (MII_SMCF)

The **MII_SMCF** register holds the LSB of the 2-byte counter for frames successfully transmitted after multiple collisions.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE2_H$ first. The other is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SMCF
SNMP Multiple Collision Frames Counter ($8CE2_H$) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
MII_SMCF_LSB							
sc							

Field	Bits	Type	Description
MII_SMCF_LSB	7:0	sc	**LSB of Counter of Frames Transmitted after Multiple Collisions**

10.12.4 SNMP Deferred Transmission Counter (MII_SDT)

The **MII_SDT** register holds the LSB of the 2-byte counter for frames for which the first transmission attempt was delayed because media were busy.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE3_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SDT
SNMP Deferred Transmission Counter ($8CE3_H$) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
MII_SDT_LSB							
sc							

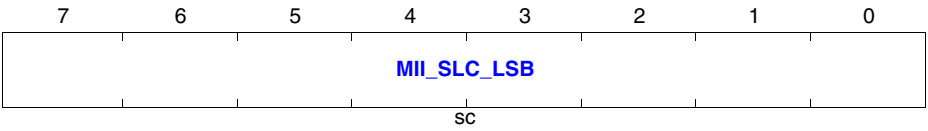
Field	Bits	Type	Description
MII_SDT_LSB	7:0	sc	**LSB of Counter for Frames with Transmission Delayed**

10.12.5 SNMP Late Collisions Counter (MII_SLC)

The **MII_SLC** register holds the LSB of the 2-byte counter for times a collision was detected after the time it takes for 512 bits to be transmitted.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE4_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SLC
SNMP Late Collisions Counter **($8CE4_H$)** **Reset Value: 00_H**



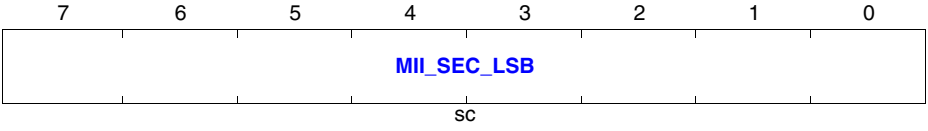
Field	Bits	Type	Description
MII_SLC_LSB	7:0	sc	**LSB of Counter of Collisions after 512 Bits Transmitted**

10.12.6 Excessive Collisions Counter (MII_SEC)

The **MII_SEC** register holds the LSB of the 2-byte counter for times the retransmission counter reached its maximum limit. If this happens, the packets are transmitted again.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE5_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SEC
Excessive Collisions Counter **($8CE5_H$)** **Reset Value: 00_H**



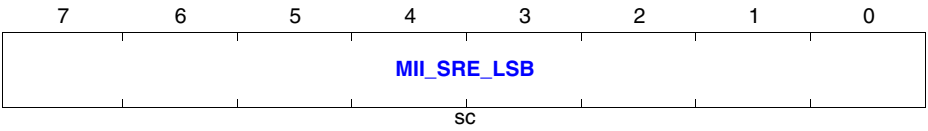
Field	Bits	Type	Description
MII_SEC_LSB	7:0	sc	**LSB of Counter of Times Retransmission Counter Reached Its Limit**

10.12.7 Reception Errors Counter (MII_SRE)

The **MII_SRE** register holds the LSB of the 2-byte counter for received frames that had an incorrect number of bytes.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE6_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SRE
Reception Errors Counter **($8CE6_H$)** **Reset Value: 00_H**



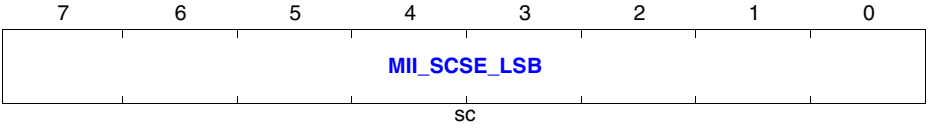
Field	Bits	Type	Description
MII_SRE_LSB	7:0	sc	**LSB of Counter of Received Frames with Wrong Number of Bytes**

10.12.8 Carrier Sense Errors Counter (MII_SCSE)

The **MII_SCSE** register holds the LSB of the 2-byte counter for times the carrier sense condition was lost or not activated during an attempt to transmit a frame.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE7_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SCSE
Carrier Sense Errors Counter **($8CE7_H$)** **Reset Value: 00_H**



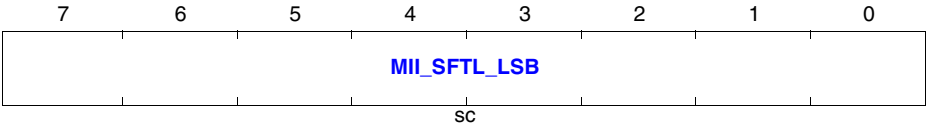
Field	Bits	Type	Description
MII_SCSE_LSB	7:0	sc	**LSB of Counter of Times Carrier Sense Was Lost During Transmission Attempt**

10.12.9 Frame Too Long Counter (MII_SFTL)

The **MII_SFTL** register holds the LSB of the 2-byte counter for frames received that exceed the maximum packet size. The maximum packet size is specified in the MPS field, bit 5 of the **MIICNTL** register ($8D40_H$).

Both bytes are read from a buffer that is latched by reading the LSB at $8CE8_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SFTL
Frame Too Long Counter ($8CE8_H$) Reset Value: 00_H



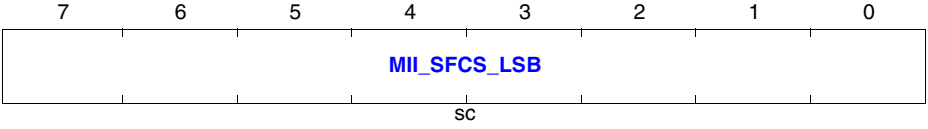
Field	Bits	Type	Description
MII_SFTL_LSB	7:0	sc	**LSB of Counter of Times Frames Were Larger than the Maximum Packet Size**

10.12.10 Frame Check Sequence Error Counter (MII_SFCS)

The **MII_SFCS** register holds the LSB of the 2-byte counter for frames that are an integer number of bytes in length and do not pass the frame check sequence (FCS) check.

Both bytes are read from a buffer that is latched by reading the LSB at $8CE9_H$ first. The other byte is read from the LSB of the **MII_CNTR_MSB** register at $8CF1_H$. After both bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SFCS
Frame Check Sequence Error Counter ($8CE9_H$) Reset Value: 00_H



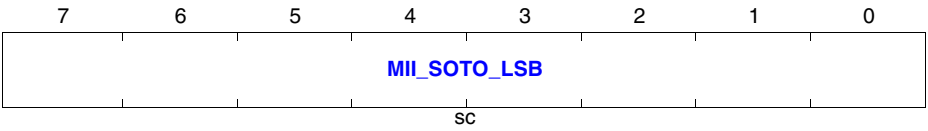
Field	Bits	Type	Description
MII_SFCS_LSB	7:0	sc	**LSB of Counter of Frames that Fail FCS Check and are an Integer Number of Bytes Long**

10.12.11 Bytes Transmitted OK Counter (MII_SOTO)

The **MII_SOTO** register holds the LSB of the 4-byte counter for data plus padding bytes that were successfully transmitted.

All four bytes are read from a buffer that is latched by reading the LSB at $8CEA_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SOTO
Bytes Transmitted OK Counter ($8CEA_H$) Reset Value: 00_H



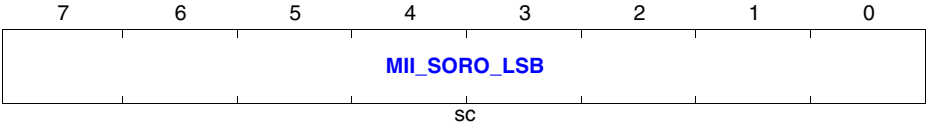
Field	Bits	Type	Description
MII_SOTO_LSB	7:0	sc	**LSB of Counter of Successfully Transmitted Bytes**

10.12.12 Bytes Received OK Counter (MII_SORO)

The **MII_SORO** register holds the LSB of the 4-byte counter for data plus padding bytes that were successfully received.

All four bytes are read from a buffer that is latched by reading the LSB at $8CEB_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

MII_SORO
Bytes Received OK Counter ($8CEB_H$) Reset Value: 00_H



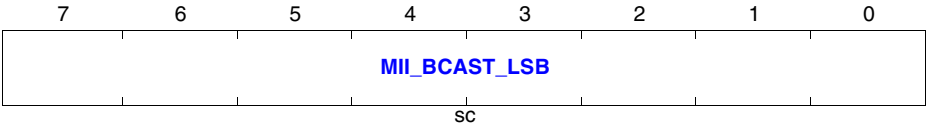
Field	Bits	Type	Description
MII_SORO_LSB	7:0	sc	**LSB of Counter of Successfully Received Bytes**

10.12.13 Broadcast Frames Received Counter (MII_BCAST)

The **MII_BCAST** register holds the LSB of the 4-byte counter for frames successfully received and directed to the broadcast group address.

All four bytes are read from a buffer that is latched by reading the LSB at $8CEC_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

MII_BCAST
Broadcast Frames Received Counter ($8CEC_H$) **Reset Value: 00_H**



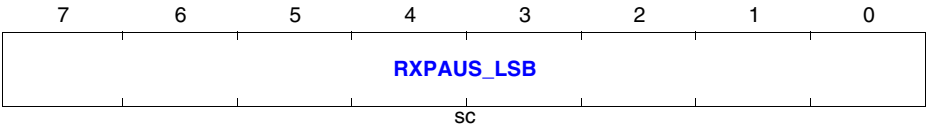
Field	Bits	Type	Description
MII_BCAST_LSB	7:0	sc	**LSB of Counter of Frames Received and Broadcast**

10.12.14 Reception Pause Packets Counter (RXPAUS)

The **RXPAUS** register holds the LSB of the 4-byte counter for pause packets received.

All four bytes are read from a buffer that is latched by reading the LSB at $8CED_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

RXPAUS
Reception Pause Packets Counter ($8CED_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
RXPAUS_LSB	7:0	sc	**LSB of Counter of Pause Packets Received**

10.12.15 Transmission Pause Packets Counter (TXPAUS)

The **TXPAUS** register holds the LSB of the 4-byte counter for pause packets transmitted.

All four bytes are read from a buffer that is latched by reading the LSB at $8CEE_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

TXPAUS
Transmission Pause Packets Counter ($8CEE_H$) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
TXPAUS_LSB							
sc							

Field	Bits	Type	Description
TXPAUS_LSB	7:0	sc	**LSB of Counter of Pause Packets Transmitted**

10.12.16 Transmitted Frames Counter (TXBCNT)

The **TXBCNT** register holds the LSB of the 4-byte counter for valid data frames transmitted.

All four bytes are read from a buffer that is latched by reading the LSB at $8CEF_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

TXBCNT
Transmitted Frames Counter ($8CEF_H$) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
TXBCNT_LSB							
sc							

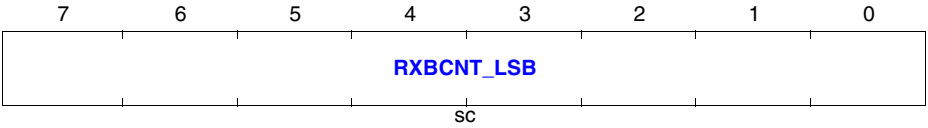
Field	Bits	Type	Description
TXBCNT_LSB	7:0	sc	**LSB of Counter of Valid Data Frames Transmitted**

10.12.17 Received Frames Counter (RXBCNT)

The **RXBCNT** register holds the LSB of the 4-byte counter for valid data frames received.

All four bytes are read from a buffer that is latched by reading the LSB at $8CF0_H$ first. The other three bytes are read from the **MII_CNTR_MSB** register at $8CF3_H$:$8CF1_H$. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

RXBCNT
Received Frames Counter **($8CF0_H$)** **Reset Value: 00_H**



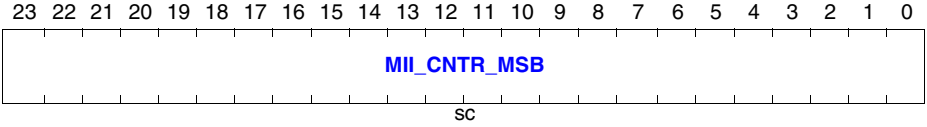
Field	Bits	Type	Description
RXBCNT_LSB	7:0	sc	**LSB of Counter of Valid Data Frames Received**

10.12.18 Three MSBs for MII Counters (MII_CNTR_MSB)

The 3-byte **MII_CNTR_MSB** register holds the three MSBs of one of the 4-byte counters for MII operations.

All four bytes of the required counter are read from a buffer that is latched by first reading the LSB of that counter. Then, the remaining three bytes are read from this register. After all four bytes are read, the counter is reset. The counter stops counting when it is full.

MII_CNTR_MSB
Three MSBs for MII Counters **($8CF3_H$:$8CF1_H$)** **Reset Value: 00 0000_H**



Field	Bits	Type	Description
MII_CNTR_MSB	23:0	rw	**Three MSBs of a 4-byte Counter for MII Operations**

10.13 MII Control Registers

This section describes the following MII control registers for standard firmware:

- **MII Control Register (MIICNTL)**

- MII Back Pressure Control Register 1 (BPCNTL1)
- MII Back Pressure Control Register 2 (BPCNTL2)
- MII Back Pressure Control Register 3 (BPCNTL3)
- Flow Control Register (FLOWCTL)
- Pause Packet Source Address Register (SRCADD)
- Address Table Control Register (ADDTCTL)
- Aging Timer Register (AGTIMER)
- Current Source Address Register (PFSRC)

10.13.1 MII Control Register (MIICNTL)

The **MIICNTL** register contains parameters that control MII operations.

MIICNTL
MII Control Register 1 **($8D40_H$)** **Reset Value: EE_H**

7	6	5	4	3	2	1	0
SPEED	DUPLEX	MPS	ADD_FILT	BSEN	ABP	AFC	Res
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SPEED	7	rw	***x*MII Speed** When the chip is configured as a MAC, or when it is configured as a PHY for non-transparent operation, this bit is read only (self-configured). When the chip is configured as a PHY for transparent operation, this bit can be set by the user. 0_B 10 Mbit/s 1_B 100 Mbit/s
DUPLEX	6	rw	**Ethernet Duplex Mode** When the chip is configured as a MAC, or when it is configured as a PHY for non-transparent operation, this bit is read only (self-configured). When the chip is configured as a PHY for transparent operation, this bit can be set by the user. 0_B Half duplex 1_B Full duplex
MPS	5	rw	**Maximum Packet Size** 0_B 1518 bytes- Standard Ethernet packet length. 1_B 1536 bytes - Extended length.

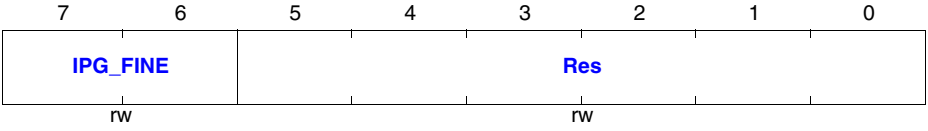
Field	Bits	Type	Description
ADD_FILT	4	rw	**Address Filtering Enable** 0_B Address filtering disabled. 1_B Address filtering enabled.
BSEN	3	rw	**Back Signaling Enable** 0_B Back signaling disabled. 1_B Back signaling enabled.
ABP	2	rw	**Automatic Back Pressure Enable** 0_B Turn back pressure off or on by changing **BPEN** (bit 7) in the **BPCNTL3** register at $8D43_H$. 1_B Back pressure turned off or on automatically in MAC mode, according to the speed and duplex mode.
AFC	1	rw	**Automatic Flow Control Enable** 0_B Turn flow control off or on by changing bit 7 (**FLOW_EN**) in the **FLOWCTL** register at $8D44_H$. 1_B Flow control turned off or on automatically.
Res	0	rw	**Reserved**

10.13.2 MII Back Pressure Control Register 1 (BPCNTL1)

The **BPCNTL1**, **BPCNTL2** and **BPCNTL3** registers at $8D41_H$:$8D43_H$, respectively, contain parameters that control back pressure and inter packet gap (IPG) handling.

IPG_FINE in this register defines the length of the IPG during transmission of normal packets as: 16 ∗ (IPG_LENGTH + 1) – IPG_FINE bit times

BPCNTL1
MII Back Pressure Control Register 1($8D41_H$) **Reset Value: 00_H**

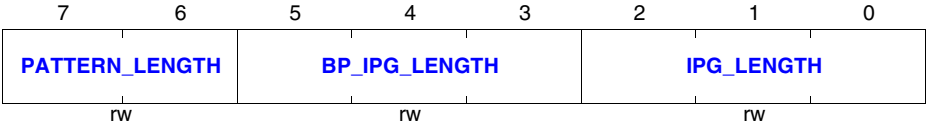


Field	Bits	Type	Description
IPG_FINE	7:6	rw	**IPG Length During Transmission of Normal Packets**
Res	6	rw	**Reserved**

10.13.3 MII Back Pressure Control Register 2 (BPCNTL2)

The **BPCNTL1**, **BPCNTL2**, and **BPCNTL3** registers at $8D41_H$:$8D43_H$, respectively, contain parameters that control back pressure and inter packet gap (IPG) handling.

BPCNTL2
MII Back Pressure Control Register 2($8D42_H$) **Reset Value: CD_H**

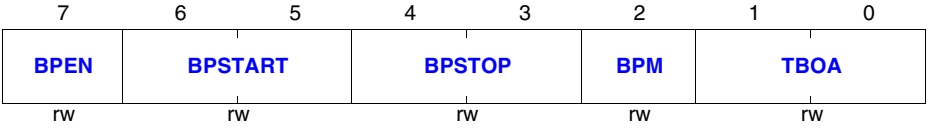


Field	Bits	Type	Description
PATTERN_LENGTH	7:6	rw	**Length of Continuous Back Pressure Preamble Before Insertion of an IPG** 00_B 12 kbit times 01_B 28 kbit times 00_B 36 kbit times 11_B 53 kbit times
BP_IPG_LENGTH	5:3	rw	**Length of the IPG Inserted into Continuous Back Pressure Preamble** Calculated as: 16 ∗ (BP_IPG_LENGTH + 1) bit times. 000_B 16 kbit times 001_B 32 kbit times 010_B 48 kbit times 011_B 64 kbit times 100_B 80 kbit times 101_B 96 kbit times 110_B 112 kbit times 111_B 128 kbit times
IPG_LENGTH	2:0	rw	**Normal Operation IPG Length** 000_B 20 kbit times 001_B 32 kbit times 010_B 48 kbit times 011_B 64 kbit times 100_B 80 kbit times 101_B 96 kbit times 110_B 112 kbit times 111_B 128 kbit times

10.13.4 MII Back Pressure Control Register 3 (BPCNTL3)

The **BPCNTL1**, **BPCNTL2**, and **BPCNTL3** registers at $8D41_H$:$8D43_H$, respectively, contain parameters that control back pressure and inter packet gap (IPG) handling.

BPCNTL3
MII Back Pressure Control Register 3($8D43_H$) **Reset Value: 54_H**



Field	Bits	Type	Description
BPEN	7	rw	**Back Pressure Enable** When the ABP bit (bit 2) in the MIICNTL register ($8D40_H$) is 1, this bit is read only. 0_B Back pressure is disabled. 1_B Back pressure is enabled.
BPSTART	6:5	rw	**Back Pressure Start Threshold** Back pressure starts when the space in the buffer drops below the space specified in this field. 01_B 2 Kbytes 10_B 4 Kbytes 11_B 6 Kbytes
BPSTOP	4:3	rw	**Back Pressure Stop Threshold** Back pressure stops when the space in the buffer rises above BPSTART (bits 6:5) plus the space specified here. 00_B 0 bytes 01_B 64 bytes 10_B 1024 bytes 11_B 1536 bytes
BPM	2		**Back Pressure Method of IPG Insertion** Valid only when there is back pressure. 0_B Append data packet to back pressure pattern of any length. 1_B Insert IPG before data packet.

Field	Bits	Type	Description
TBOA	1:0		**Truncated Back Off Algorithm for Resetting Collision Counter** 00_B After 16 consecutive retransmission attempts. 01_B After eight consecutive retransmission attempts. 10_B After four consecutive retransmission attempts. 11_B After two consecutive retransmission attempts.

10.13.5 Flow Control Register (FLOWCTL)

The **FLOWCTL** register specifies parameters for flow control.

FLOWCTL
Flow Control Register **(8D44$_H$)** **Reset Value: 17$_H$**

7	6	5	4	3	2	1	0
FLOW_EN	FPP	FC_START		FC_STOP		BACK_SIG	
rw	rw	rw		rw		rw	

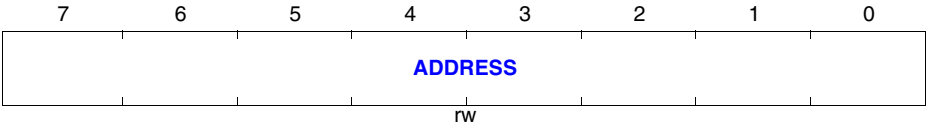
Field	Bits	Type	Description
FLOW_EN	7	rw	**Enable Flow Control** When the AFC bit (bit 1) in the MIICNTL (8D40$_H$) register is 1, this bit is read only. 0_B Disable flow control. 1_B Enable flow control.
FPP	6	rw	**Forward Pause Packet Control** 0_B Discard pause packets. 1_B Forward pause packets across link.
FC_START	5:4	rw	**Flow Control Start Level** Pause packets are generated while less than this amount of free space remains in the buffer. 01_B 2048 bytes. 10_B 4096 bytes. 11_B 6144 bytes.

Field	Bits	Type	Description
FC_STOP	3:2		**Flow Control Stop Level** Generation of pause packets stops when more than FC_START bytes of free space remain in the buffer. 00_B 64 bytes. 01_B 512 bytes. 10_B 1024 bytes. 11_B 2048 bytes.
BACK_SIG	1:0		**Back Signaling Threshold** 00_B 1 byte. 01_B 1536 bytes. 10_B 4096 bytes. 11_B 6144 bytes.

10.13.6 Pause Packet Source Address Register (SRCADD)

The **SRCADD** register holds the first byte of the address of the source of a pause packet. The next 40 bits are 0s.

SRCADD
Pause Packet Source Address Register ($8D45_H$) **Reset Value: 00_H**

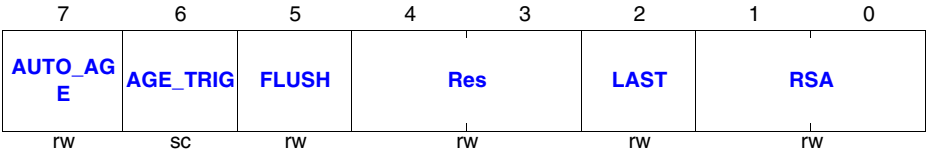


Field	Bits	Type	Description
ADDRESS	7:0	rw	**First byte of Address of Pause Packet Source**

10.13.7 Address Table Control Register (ADDTCTL)

The **ADDTCTL** register holds parameters that control the address table.

ADDTCTL
Address Table Control Register (8D46$_H$) Reset Value: 80$_H$

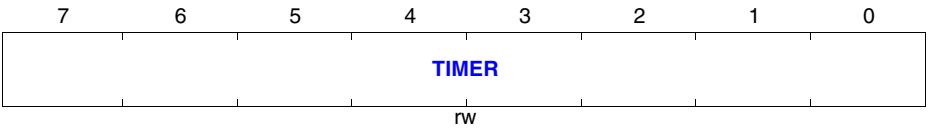


Field	Bits	Type	Description
AUTO_AGE	7	rw	Automatic Aging or Aging Triggered by Host 0_B Aging triggered by host. 1_B Automatic aging, triggered by timer.
AGE_TRIG	6	sc	**Trigger Aging Scan of Address Table** Applicable when aging is triggered by the host. Not applicable for automatic aging. Two scans clear the entire address table to 0. This bit is cleared automatically. 0_B Do not trigger aging scan. 1_B Scan aging table to clear old entries.
FLUSH	5	rw	**Flush (Clear) Aging Table** 0_B Do not flush (clear) aging table. 1_B Flush aging table.
Res	4:3	rw	**Reserved**
LAST	2	rw	**Read Address Counter Points to the Last Valid Address in the Address Table** 0_B Does not point to the last valid address in the table. 1_B Points to the last valid address in the address table.
RSA	1:0	rw	**Control Read Source Address** Unused values are invalid. 00_B Write: NOP Read: Valid address is in **PFSRC** register at 8D4D$_H$. 01_B Fetch next address from table. 11_B Fetch first address from table.

10.13.8 Aging Timer Register (AGTIMER)

The value held in the **AGTIMER** register is used to trigger an aging scan of the aging address table every TIMER ∗ 256 bits.

AGTIMER
Aging Timer Register **($8D47_H$)** **Reset Value: 40_H**

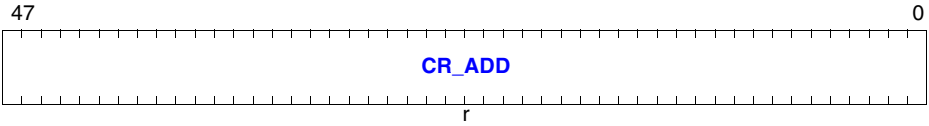


Field	Bits	Type	Description
TIMER	7:0	rw	**Value for Calculating Intervals Between Aging Scans**

10.13.9 Current Source Address Register (PFSRC)

The 6-byte **PFSRC** register specifies the current source address from the address table, with the most significant byte at $8D4D_H$.

PFSRC
Current Source Register **($8D4D_H$:$8D48_H$)** **Reset Value: 0000 0000 0000_H**



Field	Bits	Type	Description
CR_ADD	47:0	r	**Current Source Address**

10.14 MII Vendor Specific Registers

The **VP_INF_H** and **VP_INF_L** registers at $8D4F_H$ and $8D4E_H$, respectively, provide vendor specific information about the status register for the PHY SMI.

These registers are mapped in EEPROM as follows:

- **VP_INF_L** - $780E_H$
- **VP_INF_H** - $780F_H$

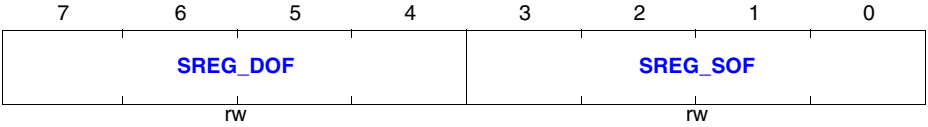
10.14.1 Vendor PHY SMI Status Register Information, L (VP_INF_L)

The **VP_INF_L** register, provides vendor specific information about the offset of duplex mode and speed fields in the status register for the PHY SMI, whose address is specified in bits 7:3 of the **VP_INF_H** register at $8D4F_H$.

Change the reset value of this register according to the PHY manufacturer, for example:

- For a Broadcom PHY (BCM5221), make the reset value 01_H.
- For a National Semiconductor PHY (DP83843), make the reset value 21_H.
- For an Intel PHY (LXT971A), make the reset value $9E_H$.
- For a Kendin PHY (KS8737), make the reset value 43_H.

VP_INF_L
Vendor PHY SMI Status Register Information, L
($8D4E_H$) **Reset Value: $9E_H$**



Field	Bits	Type	Description
SREG_DOF	7:4	rw	**Offset of Duplex Mode Bit in PHY SMI Status Register**
SREG_SOF	3:0	rw	**Offset of Speed Bit in PHY SMI Status Register**

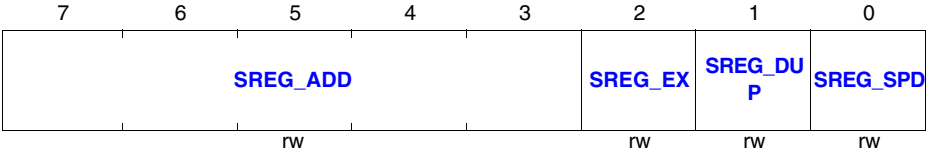
10.14.2 Vendor PHY SMI Status Register Information, H (VP_INF_H)

The **VP_INF_H** register, together with the **VP_INF_L** register at $8D4E_H$, provides vendor specific information about the status register for the PHY SMI.

Change the reset value of this register according to the PHY manufacturer, for example:

- For a Broadcom PHY (BCM5221), make the reset value $E4_H$.
- For a National Semiconductor PHY (DP83843), make the reset value 85_H.
- For an Intel PHY (LXT971A), make the reset value $8C_H$.
- For a Kendin PHY (KS8737), make the reset value FC_H.

VP_INF_H
Vendor PHY SMI Status Register Information, H
(8D4F$_H$) **Reset Value: 8C$_H$**



Field	Bits	Type	Description
SREG_ADD	7:3	rw	**Address of the Status Register**
SREG_EX	2	rw	**Status Register Existence Indicator** 0 There is no status register. 1 Status register is at the address specified in bits 7:3.
SREG_DUP	1	rw	**Interpretation of Duplex Mode Bit** 0 In duplex bit, 0 = half duplex and 1 = full duplex. 1 In duplex bit, 0 = full duplex and 1 = half duplex.
SREG_SPD	0		**Interpretation of the Speed Bit** 0 In speed bit, 0 = 10 Mbit/s and 1 = 100 Mbit/s. 1 In speed bit, 0 = 100 Mbit/s and 1 = 10 Mbit/s.

10.15 Power Back Off Registers (PBO)

The Power Back Off (PBO) registers support the PBO algorithm. See also:

- **“Power Back Off (PBO)” on Page 115**
- **“Attenuation Input Adjustment Register (ATTADJ)” on Page 196**

This section describes the following registers:

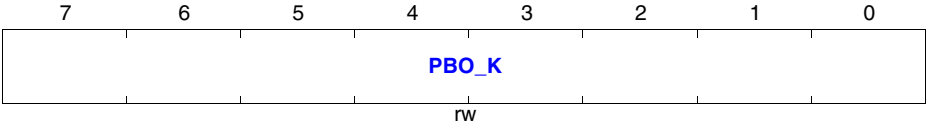
- **PBO K Constant Register (PBO_K)**
- **PBO US1 Distance Register (PBO_US1D)**
- **PBO US2 Distance Register (PBO_US2D)**
- **PBO Maximum PSD Register (PBO_MAXPSD)**
- **PBO Minimum PSD Register (PBO_MINPSD)**

10.15.1 PBO K Constant Register (PBO_K)

The **PBO_K** register value is used to calculate the line constant K for the PBO algorithm. The contents of this register are divided by 5,000 to obtain the appropriate constant. The default constant is 0.021[dB / km / (Hz)$^{0.5}$] for an ANSI standard AWG 24 line segment.

For details, see **“Power Back Off (PBO)” on Page 115**.

PBO_K
PBO K Constant Register **($5B00_H$)** **Reset Value: 69_H**

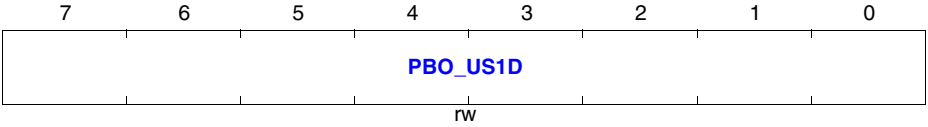


Field	Bits	Type	Description
PBO_K	7:0	rw	**Value Used to Calculate K for PBO Algorithm**

10.15.2 PBO US1 Distance Register (PBO_US1D)

The **PBO_US1D** register value is used to calculate the maximum distance for upstream channel 1. Divide the value of this register by 100 to determine the maximum distance for upstream channel 1 in kilometers. The default maximum distance is 640 meters.

PBO_US1D
PBO US1 Distance Register **($5B01_H$)** **Reset Value:40_H**

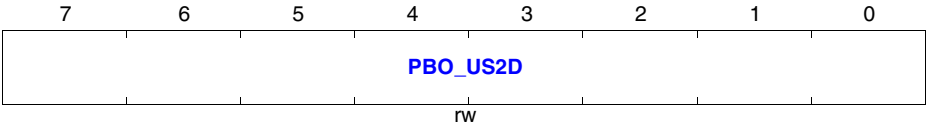


Field	Bits	Type	Description
PBO_US1D	7:0	rw	**Value for Calculating Maximum Distance for US1 in km**

10.15.3 PBO US2 Distance Register (PBO_US2D)

The **PBO_US2D** register value is used to calculate the maximum distance for upstream channel 2. Divide the value of this register by 100 to determine the maximum distance for upstream channel 2 in kilometers. The default maximum distance is 480 meters.

PBO_US2D
PBO US2 Distance Register **(5B02$_H$)** **Reset Value: 30$_H$**

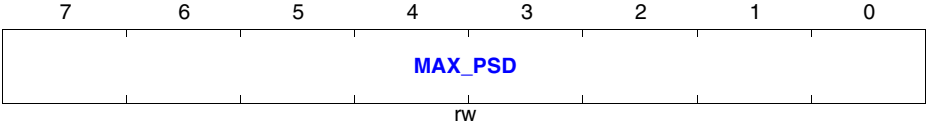


Field	Bits	Type	Description
PBO_US2D	7:0	rw	**Value for Calculating Maximum Distance for US2 in km**

10.15.4 PBO Maximum PSD Register (PBO_MAXPSD)

The **PBO_MAXPSD** register value is used to calculate the maximum Power Spectral Density (PSD) level for line attenuation. The maximum PSD level is the value of this register divided by 4, less 100 or [(**PBO_MAXPSD** / 4) – 100] dBm/Hz. The default maximum PSD level is – 60 dBm/Hz.

PBO_MAXPSD
PBO PSD Maximum Register **(5B03$_H$)** **Reset Value: A0$_H$**

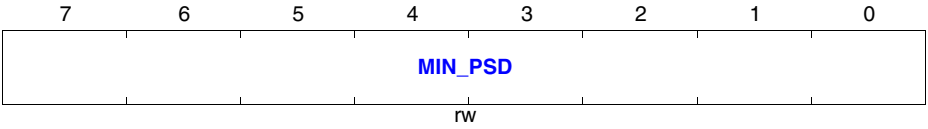


Field	Bits	Type	Description
MAX_PSD	7:0	rw	**Value for Calculating Maximum PSD in dBm/Hz**

10.15.5 PBO Minimum PSD Register (PBO_MINPSD)

The **PBO_MINPSD** register value is used to calculate the minimum Power Spectral Density (PSD) level for line attenuation in dBm/Hz. The minimum PSD level is the value of this register divided by 4, less 100 or [(**PBO_MINPSD** / 4) – 100] dBm/Hz. The default minimum PSD level is – 100 dBm/Hz.

PBO_MINPSD
PBO PSD Minimum Register (5B04$_H$) Reset Value: 00$_H$



Field	Bits	Type	Description
MIN_PSD	7:0	rw	**Value for Calculate Minimum PSD in dBm/Hz**

10.16 Rate Adaptive Module Registers

This section describes the following registers:

- **Rate Adaptive Command Register (RA_COMMAND)**
- **RA Minimum Noise Margin for D1 (RA_MN_MRG_D1)**
- **RA Maximum Downstream Rate Register (RA_MX_RATE_DS)**
- **RA Maximum Upstream Rate Register (RA_MX_RATE_US)**
- **RA Center Frequency for D1 Register (RA_CF_D1)**
- **RA Symbol Rate (SR) for D1 Register (RA_SR_D1)**
- **RA Power Spectral Density (PSD) for D1 Register (RA_PSD_D1)**
- **RA PSD Mask Register (RA_PSD_MASK)**
- **RA PSD Maximum Level, DS1 Register (RA_PSD_MAX)**
- **RA Interleaver Delay DS (RA_INTR_DS)**
- **RA Interleaver Delay US (RA_INTR_US)**
- **RA Process Minimum Noise Margin for US0 (RA_MN_MRG_U0)**
- **RA TLAN PSD Maximum Level, DS1 Register ((RA_TLAN _PSD_ MAX_DS1)**
- **RA Process Status Register (RA_STATUS)**
- **RA Process Rerun Counter (RA_RESTRT_CNT)**
- **D1 Band Use as a Result of RA Process (RA_RSLT_D1)**

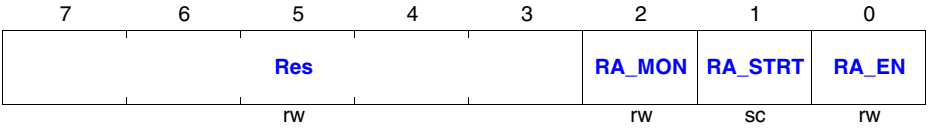
For Rate Adaptive module operation, see **“The Rate Adaptive Process” on Page 117**.

10.16.1 Rate Adaptive Command Register (RA_COMMAND)

To trigger specific RA operations, set **RA_COMMAND** as follows:

- To disable RA, set **RA_COMMAND** to 00$_H$ at both the LT and NT.
- To restart the RA loop without monitoring, set **RA_COMMAND** to 03$_H$ at the LT.
- To activate monitoring, set **RA_COMMAND** to 05$_H$ at both the LT and the NT.
- To restart the RA loop with monitoring, set **RA_COMMAND** to 07$_H$ at the LT.

RA_COMMAND
Rate Adaptive Command Register (5B10$_H$) **Reset Value: 00$_H$**



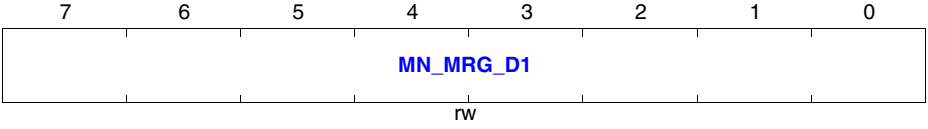
Field	Bits	Type	Description
Res	7:3	rw	**Reserved**
RA_MON	2	rw	**Rate Adaptive (RA) Process Monitor** 0_B Monitor disabled. 1_B Monitor enabled.
RA_STRT	1	sc	**Rate Adaptive (RA) Process Restart** 0_B No operation. 1_B Restart RA process.
RA_EN	0	rw	**Rate Adaptive (RA) Process Enable** 0_B RA process is disabled. 1_B RA process is enabled.

10.16.2 RA Minimum Noise Margin for D1 (RA_MN_MRG_D1)

The **RA_MN_MRG_D1** register specifies the minimum noise margin for the highest constellation during the Rate Adaptive (RA) process on the first downstream channel (D1).

The corresponding registers for the second downstream channel (D2), the first upstream channel (U1) and the second upstream channel (U2) have the same layout. See **Table 71** for the names and addresses of these registers.

RA_MN_MRG_D1
RA Process Minimum Noise Margin for D1(5B11$_H$) **Reset Value: 18$_H$**



Field	Bits	Type	Description
MN_MRG_D1	7:0	rw	**Minimum Noise Margin on D1** Expressed in 1/4 dB increments.

Table 71 Rate Adaptive Process Noise Margin Registers

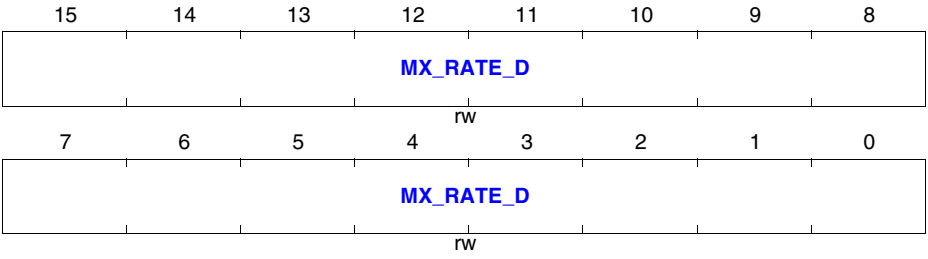
Short Name	Long Name	Offset Address	Reset Value
RA_MN_MRG_D1	**RA Minimum Noise Margin for D1**	$5B11_H$	18_H
RA_MN_MRG_D2	**RA Minimum Noise Margin for D2**	$5B12_H$	18_H
RA_MN_MRG_U1	**RA Minimum Noise Margin for U1**	$5B13_H$	18_H
RA_MN_MRG_U2	**RA Minimum Noise Margin for U2**	$5B14_H$	18_H
RA_MN_MRG_U0	**RA Minimum Noise Margin for U0**	$5B31_H$	20_H

10.16.3 RA Maximum Downstream Rate Register (RA_MX_RATE_DS)

The 16-bit value in the **RA_MX_RATE_DS** register is used to determine the maximum downstream bit rate for the RA module.

The minimum value for this register is 6_H (405 kHz). The minimum value for this register is 6_H (405 kHz). The value of this register is the desired rate. The acutal rate may equal to this value or less, depending on the QAM constellation specified. The deviation from the desired value is greater for higher QAM constellations.

RA_MX_RATE_DS
RA Maximum Downstream Rate Register($5B19_H$:$5B1A_H$) Reset Value: $FFFF_H$



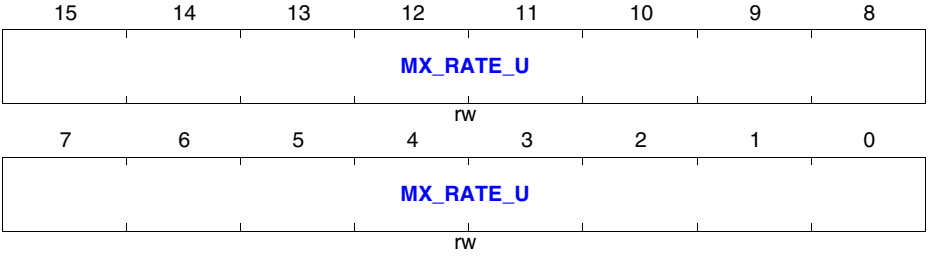
Field	Bits	Type	Description
MX_RATE_D	15:0	rw	**Value Used for Maximum DS Bit Rate for RA Process** Expressed as a multiple of 67.5 kbit/s

10.16.4 RA Maximum Upstream Rate Register (RA_MX_RATE_US)

The 16-bit value in the **RA_MX_RATE_US** register is used to determine the maximum upstream bit rate for the RA module.

The minimum value for this register is 6_H (405 kHz). The minimum value for this register is 6_H (405 kHz). The value of this register is the desired rate. The acutal rate may equal to this value or less, depending on the QAM constellation specified. The deviation from the desired value is greater for higher QAM constellations.

RA_MX_RATE_US
RA Maximum Upstream Rate Register($5B1B_H$:$5B1C_H$) **Reset Value: $FFFF_H$**



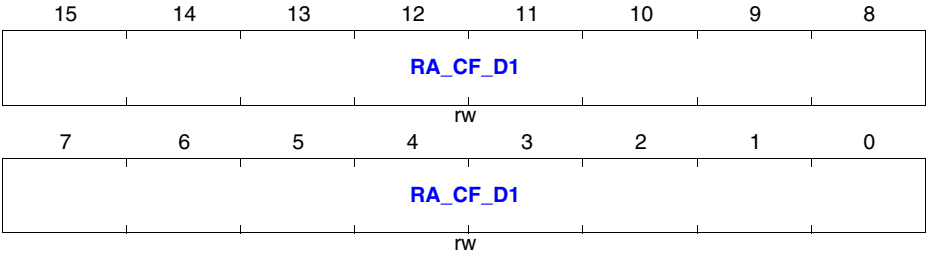
Field	Bits	Type	Description
MX_RATE_U	15:0	rw	**Value Used for Maximum US Bit Rate for RA Process** Expressed as a multiple of 67.5 kHz

10.16.5 RA Center Frequency for D1 Register (RA_CF_D1)

The 16-bit **RA_CF_D1** register specifies the center frequency (CF) of the first downstream channel (D1) for the Rate Adaptive (RA) band plan.

The corresponding registers for the second downstream channel (D2), the first upstream channel (U1) and the second upstream channel (U2) have the same layout. See **Table 72** for the names, addresses and reset values of these registers.

RA_CF_D1
RA Center Frequency for D1 Register($5B1D_H$:$5B1E_H$) **Reset Value: 0039_H**



Field	Bits	Type	Description
RA_CF_D1	15:0	rw	**RA Center Frequency for D1** Expressed in 33.75 kHz units.

Table 72 Rate Adaptive Process CF Registers

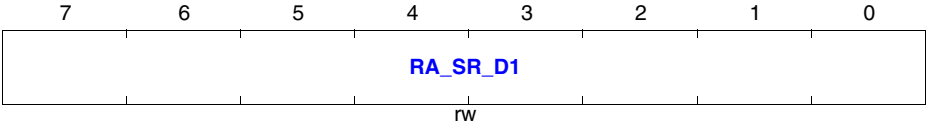
Short Name	Long Name	Offset Address	Reset Value
RA_CF_D1	**RA Center Frequency for D1, $5B1D_H$ is MSB**	$5B1D_H$:$5B1E_H$	0038_H
RA_CF_D2	**RA Center Frequency for D2, $5B1F_H$ is MSB**	$5B1F_H$:$5B20_H$	$00CC_H$
RA_CF_U1	**RA Center Frequency for U1, $5B21_H$ is MSB**	$5B21_H$:$5B22_H$	0086_H
RA_CF_U2	**RA Center Frequency for U2, $5B23_H$ is MSB**	$5B23_H$:$5B24_H$	0134_H

10.16.6 RA Symbol Rate (SR) for D1 Register (RA_SR_D1)

The **RA_SR_D1** register specifies the symbol rate (SR) of the first downstream channel (D1) for the Rate Adaptive (RA) band plan.

The corresponding registers for the second downstream channel (D2), the first upstream channel (U1) and the second upstream channel (U2) have the same layout. See **Table 73** for the names, addresses and reset values of these registers.

RA_SR_D1
RA Symbol Rate (SR) for D1 Register($5B25_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
RA_SR_D1	7:0	rw	**RA Symbol Rate (SR) for D1** Expressed in 67.5 kHz units.

Table 73 Rate Adaptive Process Symbol Rate (SR) Registers (page 1 of 2)

Short Name	Long Name	Offset Address	Reset Value
RA_SR_D1	**RA Symbol Rate for D1**	$5B25_H$	$2C_H$
RA_SR_D2	**RA Symbol Rate for D2**	$5B26_H$	$2C_H$

Table 73 Rate Adaptive Process Symbol Rate (SR) Registers (page 2 of 2)

Short Name	Long Name	Offset Address	Reset Value
RA_SR_U1	**RA Symbol Rate for U1**	$5B27_H$	$0E_H$
RA_SR_U2	**RA Symbol Rate for U2**	$5B28_H$	20_H

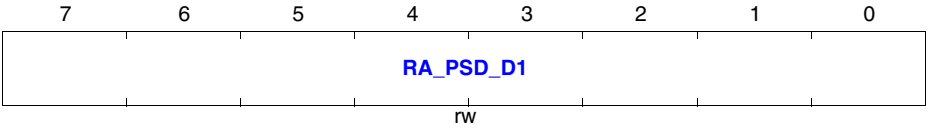
10.16.7 RA Power Spectral Density (PSD) for D1 Register (RA_PSD_D1)

The **RA_PSD_D1** register specifies the power spectral density (PSD) of the first downstream channel (D1) for the Rate Adaptive (RA) band plan.

The corresponding registers for the second downstream channel (D2), the first upstream channel (U1) and the second upstream channel (U2) have the same layout. See **Table 74** for the names, addresses and reset values of these registers.

Note: The reduced PSD values should be read from the NT side only. The LT values are not valid.

RA_PSD_D1
RA Power Spectral Density (PSD) for D1 Register($5B29_H$) **Reset Value: $9A_H$**



Field	Bits	Type	Description
RA_PSD_D1	7:0	rw	**RA Power Spectral Density (PSD) for D1** Expressed in dBm/kHz, where: PSD level = (RA_PSD_D1 / 4) – 100.

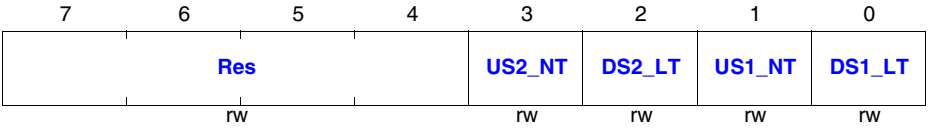
Table 74 Rate Adaptive Process Power Spectral Density (PSD) Registers

Short Name	Long Name	Offset Address	Reset Value
RA_PSD_D1	**RA PSD Value for D1**	$5B29_H$	$9A_H$
RA_PSD_D2	**RA PSD Value for D2**	$5B2A_H$	$A0_H$
RA_PSD_U1	**RA PSD Value for U1**	$5B2B_H$	$A0_H$
RA_PSD_U2	**RA PSD Value for U2**	$5B2C_H$	$A0_H$

10.16.8 RA PSD Mask Register (RA_PSD_MASK)

The **RA_PSD_MASK** register defines notch filtering for direction and carrier, where one notch per band is supported. The contents of this register define an initial power spectral density mask (PSD_MASK in STPs) for the Rate Adaptive (RA) process.

RA_PSD_MASK
RA PSD Mask Register **(5B2D$_H$)** **Reset Value: 00$_H$**

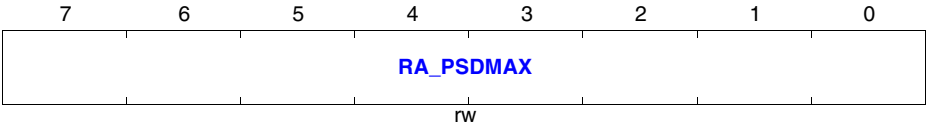


Field	Bits	Type	Description
Res	7:4	rw	**Reserved**
US2_NT	3	rw	**US2 Notch at NT** Notch on US2 at NT, in range 10.1 through 10.15 MHz. 0_B Disabled 1_B Enabled
DS2_LT	2	rw	**DS2 Notch at LT** Notch on DS2 at LT, in range 7.0 through 7.1 MHz. 0_B Disabled 1_B Enabled
US1_NT	1	rw	**US1 Notch at NT** Notch on US1 at NT, in range 3.5 through 3.8 MHz. 0_B Disabled 1_B Enabled
DS1_LT	0	rw	**DS1 Notch at LT** Notch on DS1 at LT, in range 1.81 through 2.0 MHz. 0_B Disabled 1_B Enabled

10.16.9 RA PSD Maximum Level, DS1 Register (RA_PSD_MAX)

The **RA_PSD_MAX** register defines the maximum PSD level on the DS1 channel while DS2 is disabled.

RA_PSD_MAX
RA PSD Maximum Level, DS1 Register($5B2E_H$) **Reset Value: $A0_H$**

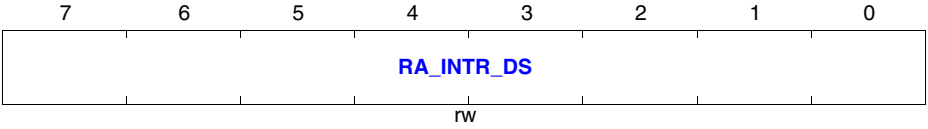


Field	Bits	Type	Description
RA_PSDMAX	7:0	rw	**PSD Maximum on DS1**

10.16.10 RA Interleaver Delay DS (RA_INTR_DS)

The **RA_INTR_DS** register defines the interleaver delay on the DS channel.

RA_INTR_DS
RA Interleaver Delay, DS Register ($5B2F_H$) **Reset Value: 00_H**

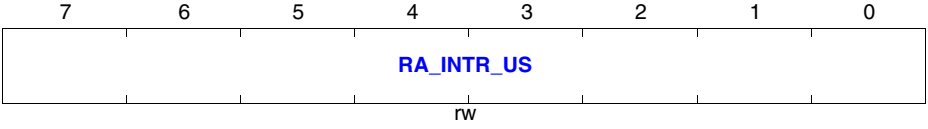


Field	Bits	Type	Description
RA_INTR_DS	7:0	rw	**Interleaver delay of DS** Expressed in 100 µs units

10.16.11 RA Interleaver Delay US (RA_INTR_US)

The **RA_INTR_US** register defines the interleaver delay on the US channel.

RA_INTR_US
RA Interleaver Delay, US Register ($5B30_H$) **Reset Value: 00_H**

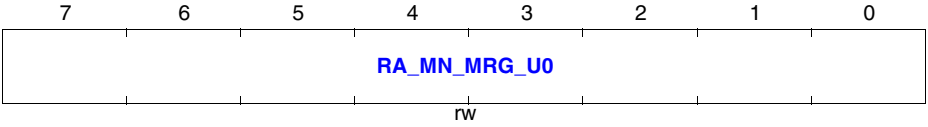


Field	Bits	Type	Description
RA_INTR_US	7:0	rw	**Interleaver delay of US** Expressed in 100 µs units

10.16.12 RA Process Minimum Noise Margin for US0 (RA_MN_MRG_U0)

The register **RA_MN_MRG_U0** defines the minimum noise margin for upstream channel 0, expressed in .25 dB units. This register is relevant on the CO (LT) side only, and its default value is 0010 0000_B or 8 dB.

RA_MN_MRG_U0
RA Process Minimum Noise Margin for US0 ($5B31_H$) **Reset Value: 20_H**

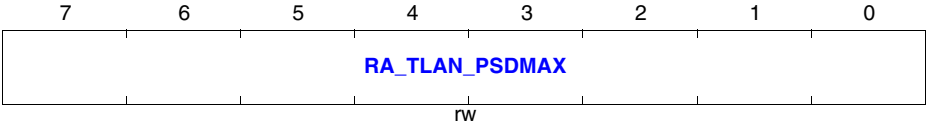


Field	Bits	Type	Description
RA_MN_MRG_U0	7:0	rw	**Noise margin of US0 expressed in 1/4 dB increments.** Default value is 0010 0100_B or 9 dB.

10.16.13 RA TLAN PSD Maximum Level, DS1 Register ((RA_TLAN _PSD_MAX_DS1)

The **RA_TLAN_PSDMAX** register defines the maximum TLAN PSD level on the DS1 channel while DS2 is disabled.

RA_TLAN_PSD_DS1_MAX
RA TLAN PSD Maximum Level, DS1 Register($5B32_H$) **Reset Value: $B8_H$**

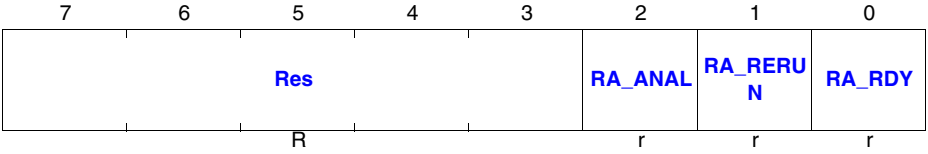


Field	Bits	Type	Description
RA_TLAN_PSDMAX	7:0	rw	**TLAN PSD Maximum on DS1**

10.16.14 RA Process Status Register (RA_STATUS)

Bits 4:0 of the **RA_STATUS** register shows the status of different aspects of the Rate Adaptive (RA) process.

RA_STATUS
RA Process Status Register **(5B40$_H$)** **Reset Value: 00$_H$**



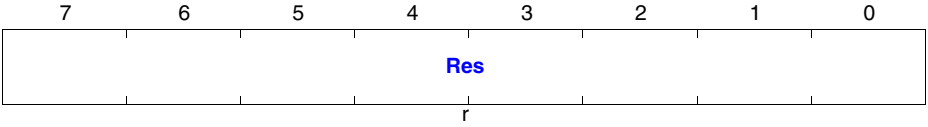
Field	Bits	Type	Description
Res	7:3	r	**Reserved**
RA_ANAL	2	r	**RA Analysis in Progress** 0_B No indication. 1_B RA analysis in progress.
RA_RERUN	1	r	**Recommendation for Rerun of RA Process** Valid only while monitoring is enabled. 0_B No indication. 1_B RA rerun recommended.
RA_RDY	0	r	**RA Process Status Indicator** 0_B No indication. 1_B RA process finished successfully.

10.16.15 RA Process Rerun Counter (RA_RESTRT_CNT)

The **RA_RESTRT_CNT** register counts the number of auto-reruns of the RA process.

Note: During the first three auto-reruns, 1 dB is added to the user requested margin. This ensures that the RA mechanism does not lock up in an infinite loop.

RA_RESTRT_CNT
RA Process Link Restart Counter **(5B41$_H$)** **Reset Value: 00$_H$**



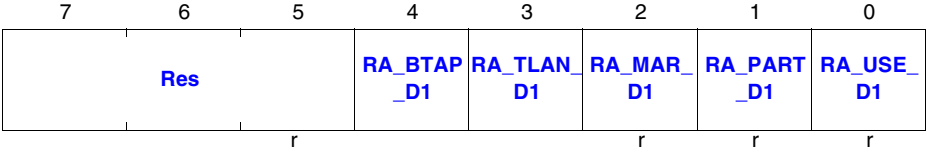
Field	Bits	Type	Description
RESTRT_CNT	7:0	r	**Count of Link Restarts Triggered by RA Process**

10.16.16 D1 Band Use as a Result of RA Process (RA_RSLT_D1)

Bits 4:0 of the **RA_RSLT_D1** register indicate the band use resulting from the RA process for the first downstream channel (D1).

The corresponding registers for the second downstream channel (D2), the first upstream channel (U1) and the second upstream channel (U2) have the same layout. See **Table 75** for the names, addresses and reset values of these registers.

RA_RSLT_D1
D1 Band Use as a Result of RA Process($5B42_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
Res	7:5	r	**Reserved**
RA_BTAP_D1	4	r	**Bridge tap detected on Band D1** 0_B No bridge tap detected 1_B Bridge tap detected
RA_TLAN_D1	3	r	**TLAN detected on Band D1** 0_B No TLAN detected 1_B TLAN detected
RA_MAR_D1	2	r	**Normal or High Margin Use with Band D1** 0_B Use with normal margin. 1_B Use band with high margin.
RA_PART_D1	1	r	**Partial or Full Use with Band D1** 0_B Use part of band. 1_B Use full band.
RA_USE_D1	0	r	**D1 Band Use as a Result of RA Process** 0_B Band not used. 1_B Band used.

Table 75 Rate Adaptive Process Result Registers

Short Name	Long Name	Offset Address	Reset Value
RA_RSLT_D1	**D1 Band Use as a Result of RA Process**	$5B42_H$	00_H
RA_RSLT_D2	**D2 Band Use as a Result of RA Process**	$5B43_H$	00_H
RA_RSLT_U1	**U1 Band Use as a Result of RA Process**	$5B44_H$	00_H
RA_RSLT_U2	**U2 Band Use as a Result of RA Process**	$5B45_H$	00_H

10.17 Notch Filter Registers Registers

This section describes the following link registers:

- **Notch Filter Coefficient NTCHA1 (DS1), Low Byte (NTCHA1_L)**
- **Notch Filter Coefficient NTCHA2 (DS1), Low Byte (NTCHA2_L)**
- **Notch Filter Coefficients NTCHA2 and NTCHA1 (DS1), High Bits (NTCHA_H)**
- **Notch Filter Coefficient NTCHB (DS1), Low Bits (NTCHB_L)**
- **Notch Filter Coefficient NTCHB (DS1), High Bits (NTCHB_H)**

10.17.1 Notch Filter Coefficient NTCHA1 (DS1), Low Byte (NTCHA1_L)

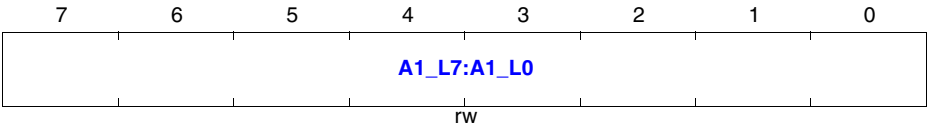
The notch filter for each band is defined by three, 12-bit coefficients: NTCHA1, NTCHA2 and NTCHB. The **NTCHA1_L** register contains the eight least significant bits of the 12-bit field that specifies the first coefficient (NTCHA1) for DS1. Bits 3:0 of the NTCHA_H register ($5DBF_H$) contain the four most significant bits 11:8 of this coefficient.

The corresponding registers for the second downstream channel (DS2), the first upstream channel (US1) and the second upstream channel (US2) have the same names and layout, but unique addresses. See **Table 76** for the addresses and reset values of these registers.

For details on notch filters, refer to standards documents (see **“References” on Page 291**). For possible values for this register, see also:

- **“ETSI Standard Values for Notch Registers, 38.88 MHz Clock” on Page 61**
- **“ANSI Standard Values for Notch Registers, 38.88 MHz Clock” on Page 61**

NTCHA1_L
Notch Filter Coefficient NTCHA1 (DS1), Low Byte ($5DBD_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
A1_L7:A1_L0	7:0	rw	**LSB of First 12-bit Notch Filter Coefficient (A1)**

Table 76 First Notch Filter Coefficient Registers, Low Byte

Short Name	Long Name	Offset Address	Reset Value
NTCHA1_L	**First US1 Notch Filter Coefficient, Low Byte**	$5DC2_H$	00_H
NTCHA1_L	**First DS2 Notch Filter Coefficient, Low Byte**	$5DC7_H$	00_H
NTCHA1_L	**First US2 Notch Filter Coefficient, Low Byte**	$5DCC_H$	00_H

10.17.2 Notch Filter Coefficient NTCHA2 (DS1), Low Byte (NTCHA2_L)

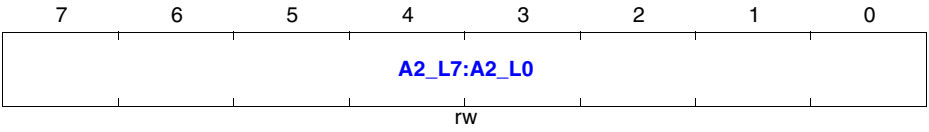
The notch filter for each band is defined by three, 12-bit coefficients: NTCHA1, NTCHA2 and NTCHB. The **NTCHA2_L** register contains the eight least significant bits of the 12-bit field that specifies the second coefficient (NTCHA2) for DS1. Bits 7:4 of the NTCHA_H register ($5DBF_H$) contain the four most significant bits 11:8 of this coefficient.

The corresponding registers for the second downstream channel (DS2), the first upstream channel (US1) and the second upstream channel (US2) have the same names and layout, but unique addresses. See **Table 77** for the addresses and reset values of these registers.

For details on notch filters, refer to standards documents (see **"References" on Page 291**). For possible values for this register, see also:

- **"ETSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**
- **"ANSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**

NTCHA2_L
Notch Filter Coefficient NTCHA2 (DS1), Low Byte ($5DBE_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
A2_L7:A2_L0	7:0	rw	**LSB of Second 12-bit Notch Filter Coefficient (A2)**

Table 77 Second Notch Filter Coefficient Registers, Low Byte

Short Name	Long Name	Offset Address	Reset Value
NTCHA2_L	Second US1 Notch Filter Coefficient, Low Byte	$5DC3_H$	00_H
NTCHA2_L	Second DS2 Notch Filter Coefficient, Low Byte	$5DC8_H$	00_H
NTCHA2_L	Second US2 Notch Filter Coefficient, Low Byte	$5DCD_H$	00_H

10.17.3 Notch Filter Coefficients NTCHA2 and NTCHA1 (DS1), High Bits (NTCHA_H)

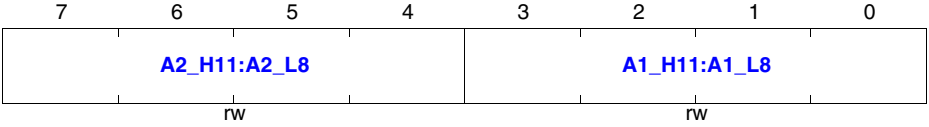
The notch filter for each band is defined by three, 12-bit coefficients: NTCHA1, NTCHA2 and NTCHB. The **NTCHA_H** register holds the four most significant bits of the NTCHA1 and NTCHA2 coefficients for DS1. **NTCHA1_L** ($5DBD_H$) and **NTCHA2_L** ($5DBE_H$) contain the eight least significant bits 7:0 of these coefficients, respectively.

The corresponding registers for the second downstream channel (DS2), the first upstream channel (US1) and the second upstream channel (US2) have the same names and layout, but unique addresses. See **Table 78** for the addresses and reset values of these registers.

For details on notch filters, refer to standards documents (see **"References" on Page 291**). For possible values for this register, see also:

- **"ETSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**
- **"ANSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**

NTCHA_H
Notch Filter Coefficients NTCHA2 and NTCHA1 (DS1), High Bits ($5DBF_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
A2_H11:A2_L8	7:4	rw	**Most Significant Bits of Second Notch Filter Coefficient (A2)**
A1_H11:A1_L8	3:0	rw	**Most Significant Bits of First Notch Filter Coefficient (A1)**

Table 78 First and Second Notch Filter Coefficient Registers, High Bits

Short Name	Long Name	Offset Address	Reset Value
NTCHA_H	US1 Notch Filter Coefficients, High Bits	$5DC4_H$	00_H
NTCHA_H	DS2 Notch Filter Coefficients, High Bits	$5DC9_H$	00_H
NTCHA_H	US2 Notch Filter Coefficients, High Bits	$5DCE_H$	00_H

10.17.4 Notch Filter Coefficient NTCHB (DS1), Low Bits (NTCHB_L)

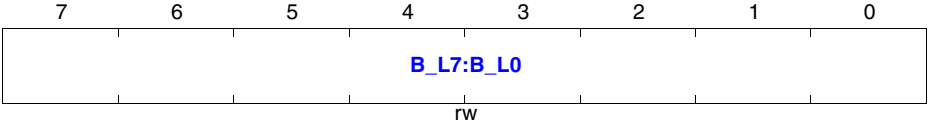
The notch filter for each band is defined by three, 12-bit coefficients: NTCHA1, NTCHA2 and NTCHB. The **NTCHB_L** register contains the eight least significant bits of the third coefficient, NTCHB for DS1. Bits 3:0 of the **NTCHB_H** register ($8C4D_H$) contain the four most significant bits of NTCHB.

The corresponding registers for the second downstream channel (DS2), the first upstream channel (US1) and the second upstream channel (US2) have the same names and layout, but unique addresses. See **Table 79** for the addresses and reset values of these registers.

For details on notch filters, refer to standards documents (see **"References" on Page 291**). For possible values for this register, see also:

- **"ETSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**
- **"ANSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**

NTCHB_L
Notch Filter Coefficient NTCHB (DS1), Low Byte ($5DC0_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
B_L7:B_L0	7:0	rw	**LSB of Third 12-bit Notch Filter Coefficient (NTCHB)**

Table 79 Third Notch Filter Coefficient Registers, Low Bits

Short Name	Long Name	Offset Address	Reset Value
NTCHB_L	**Third US1 Notch Filter Coefficient, Low Bits**	$5DC5_H$	00_H
NTCHB_L	**Third DS2 Notch Filter Coefficient, Low Bits**	$5DCA_H$	00_H
NTCHB_L	**Third US2 Notch Filter Coefficient, Low Bits**	$5DCF_H$	00_H

10.17.5 Notch Filter Coefficient NTCHB (DS1), High Bits (NTCHB_H)

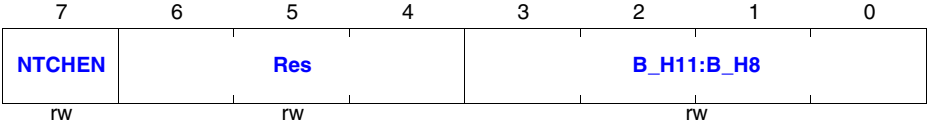
The notch filter for each band is defined by three, 12-bit coefficients: NTCHA1, NTCHA2 and NTCHB. The **NTCHB_H** register holds the four most significant bits of the third coefficient, NTCHB for DS1, and the notch filter enable bit. **NTCHB_L** ($5DC0_H$) contains the eight most significant bits of NTCHB. Bits 6:4 are reserved.

The corresponding registers for the second downstream channel (DS2), the first upstream channel (US1) and the second upstream channel (US2) have the same names and layout, but unique addresses. See **Table 79** for the addresses and reset values of these registers.

For details on notch filters, refer to standards documents (see **"References" on Page 291**). For possible values for this register, see also:

- **"ETSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**
- **"ANSI Standard Values for Notch Registers, 38.88 MHz Clock" on Page 61**

NTCHB_H
Notch Filter Coefficient NTCHB (DS1), High Bits ($5DC1_H$) **Reset Value: 00_H**



Field	Bits	Type	Description
NTCHEN	7	rw	**Notch Filter Enable Bit** 0_B The notch filter is disabled. 1_B The notch filter is enabled.
Res	6:4	rw	**Reserved**
B_H11:B_H8	3:0	rw	**Most Significant Bits of Third Notch Filter Coefficient (NTCHB)**

Table 80 Third Notch Filter Coefficient Registers, High Bits and Enable

Short Name	Long Name	Offset Address	Reset Value
NTCHB_H	**Third US1 Notch Filter Coefficient, High Bits**	$5DC6_H$	00_H
NTCHB_H	**Third DS2 Notch Filter Coefficient, High Bits**	$5DCA_H$	00_H
NTCHB_H	**Third US2 Notch Filter Coefficient, High Bits**	$5DD0_H$	00_H

11 Memory and Register Descriptions – Analog Block

This section describes the registers that are dedicated to analog operations. It includes a list of the registers with their offset addresses and detailed descriptions of each.

11.1 Register Overview – Analog Block

Table 81 lists the registers of the analog block. Offset addresses not used are reserved for internal use only. Do not change the default values at these addresses.

Table 81 Analog Registers Overview

Register Short Name	Register Long Name	Offset Address
ADC	ADC Operation Parameters	00_H
DAC	DAC Control	02_H
PREFI_POFI	PREFI and POFI Power Down	03_H
ACE_MBUF_AGC	ACE, Measurement Buffer and AGC Mode	04_H
POCO	Power Control	05_H
AGC	Value for AGC Gain Calculation	06_H
ALOOP_BIAS	Analog Loop and Bias Control	07_H
DCXO	Digital Crystal Frequency	08_H
FC_TUNE	Corner Frequency and Tuning	$0C_H$
WAK_PLL_TUN_RF	Wake-up, PLL, Tuning and RFS Status	$0D_H$
XTAL_TUN_PAR	Clock, Test, Crystal and Tuning Parameters	$0F_H$
PLL_PAR	PLL Parameters	12_H
GPO_PADS	General Purpose Output Pad Parameters	19_H

11.2 Detailed Register Descriptions – Analog Block

This section describes the registers of the Analog Block in detail.

Note: Do not change the value of reserved bits and fields named Res0 or Res.

11.2.1 ADC Operation Parameters

The **ADC** register sets ADC operation parameters.

ADC
ADC Operation Parameters **(00_H)** **Reset Value: 28_H**

7	6	5	4	3	2	1	0
Res						ADC_CLK_INV	PD_ADC
rw						rw	rw

Field	Bits	Type	Description
Res	7:2	rw	**Reserved** Always 001010_B.
ADC_CLK_INV	1	rw	**Control ADC Clock Signal** 0_B Normal operation. 1_B Invert clock signal for ADC.
PD_ADC	0	rw	**Control ADC Power Down** 0_B Normal operation. 1_B Power down ADC.

11.2.2 DAC Control

The **DAC** register sets DAC operation parameters.

DAC
DAC Control **(02_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Res						DAC_CLK_INV	PD_DAC
rw						rw	rw

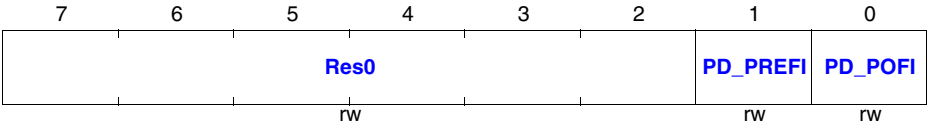
Field	Bits	Type	Description
Res	7:2	rw	**Reserved** Always 0.
DAC_CLK_INV	1	rw	**Control DAC Clock Signal** 0_B Normal operation (Default). 1_B Invert DAC clock.

Field	Bits	Type	Description
PD_DAC	0	rw	**Control DAC Power Down** 0_B Normal operation. 1_B Power down DAC.

11.2.3 PREFI and POFI Power Down

The **PREFI_POFI** register controls power down for the pre-filter (PREFI) and the post-filter (POFI).

PREFI_POFI
PREFI and POFI Power Down **(03_H)** **Reset Value: 00_H**



Field	Bits	Type	Description
Res0	7:2	rw	**Reserved** Always 0.
PD_PREFI	1	rw	**Control Pre-Filter (PREFI) Power Down** 0_B Normal operation. 1_B Power down PREFI.
PD_POFI	0	rw	**Control Post-Filter (POFI) Power Down** 0_B Normal operation. 1_B Power down POFI.

11.2.4 ACE, Measurement Buffer and AGC Mode

The **ACE_MBUF_AGC** register controls the following:

- Automatic Gain Control (AGC) operation mode
- Source and power down of measurement buffer
- Analog Channel Equalizer (ACE) mode and power down

ACE_MBUF_AGC
ACE, Power Measurement and AGC Mode(04_H) **Reset Value: 06_H**

7	6	5	4	3	2	1	0
Res0	AGC_MODE	Res				ACE_MODE	PD_ACE
rw	rw	rw			rw	rw	rw

Field	Bits	Type	Description
Res0	7	rw	**Reserved** Always 0.
AGC_MODE	6	rw	**AGC Operation Mode** 0_B Mode 0, AGC_{10} in the range 0 through 89. 1_B Mode 1, AGC_{10} in the range 12 through 89. See also, **"Value for AGC Gain Calculation" on Page 259**.
Res	5:2	rw	**Reserved** Always 0001_B
ACE_MODE	1	rw	**Enable Analog Channel Equalizer (ACE)** 0_B Enable. 1_B Disable. Constant gain of 0 dB for all frequencies up to 20 MHz.
PD_ACE	0	rw	**Power Down Analog Channel Equalizer (ACE)** 0_B Normal operation. 1_B Power down ACE.

11.2.5 Power Control

The **POCO** register controls gain and power down of the power controller. Gain ($POCO_{GAIN}$) is programmed to a value from -24 through 0 dB, in 6 dB steps plus 3 dB as shown by the following expression:

$POCO_{GAIN} = (3 * POCO3) – (6 * POCO[2:0])$ dB

The default settings are for maximum power (0).

POCO
Power Control **(05_H)** **Reset Value: 10_H**

7	6	5	4	3	2	1	0
Res			POCO3	POCO[2:0]			PD_POCO
rw			rw	rw			rw

Field	Bits	Type	Description
Res	7:5	rw	**Reserved**
POCO3	4	rw	**POCO3 Factor for Power Control Gain Calculation** 0_B Add 0 dB to value in bits 3:1 (POCO[2:0]) for gain. 1_B Add 3 dB to value in bits 3:1 (POCO[2:0]) for gain.
POCO[2:0]	3:1	rw	**POCO[2:0] Factor for Power Control Gain Calculation** 000_B Use 0_D for POCO[2:0] in gain calculation. 001_B Use 1_D for POCO[2:0] in gain calculation. 010_B Use 2_D for POCO[2:0] in gain calculation. 011_B Use 3_D for POCO[2:0] in gain calculation. 100_B Use 4_D for POCO[2:0] in gain calculation.
PD_POCO	0	rw	**Power Down Control** 0_B Normal operation. 1_B Power down.

11.2.6 Value for AGC Gain Calculation

The **AGC** register controls power down of AGC and specifies a decimal AGC value (**AGC[6:0]**) used to calculate AGC gain, depending on the AGC mode (**ACE_MODE**, bit 6 in the **ACE_MBUF_AGC** register at offset address 04_H) and external resistors, as follows:

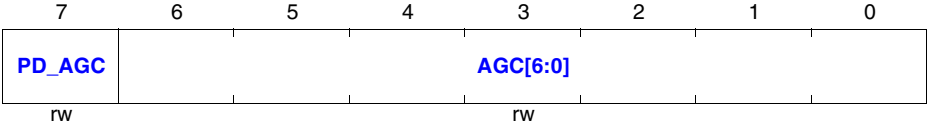
- If there is no external resistor:
  - and AGC_MODE = 0_B, then $AGC_{GAIN} = 0.5 \times$ **AGC[6:0]** – 6 dB
  - and AGC_MODE = 1_B, then $AGC_{GAIN} = 0.5 \times$ (**AGC[6:0]** – 12) – 6 dB
- If there is an external 800 Ω resistor:
  - and AGC_MODE = 0_B, then $AGC_{GAIN} = 0.5 \times$ **AGC[6:0]** – 12 dB
  - and AGC_MODE = 1_B, then $AGC_{GAIN} = 0.5 \times$ (**AGC[6:0]** – 12) – 12 dB

Table 82 summarizes the results of these calculations.

Table 82 AGC Gain Parameters

External Resistor	AGC_MODE	Calculated AGC Values
None	0_B	– 6 dB through 38.5 dB
	1_B	– 6 dB through 32.5 dB
External 800 Ω Resistor	0_B	– 12 dB through 32.5 dB
	1_B	– 12 dB through 26.5 dB

AGC
Value for AGC Gain Calculation (06_H) Reset Value: 00_H

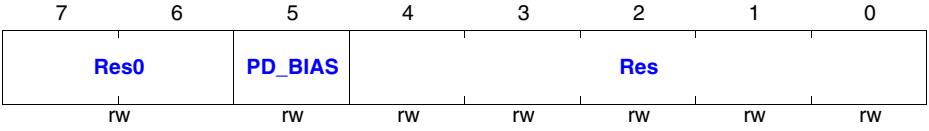


Field	Bits	Type	Description
PD_AGC	7	rw	**Power Down Control** 0_B Normal operation. 1_B Power down AGC.
AGC[6:0]	6:0	rw	**Decimal Value for AGC Gain Calculation** If **AGC_MODE** = 0_B, range of AGC is 0_D through 89_D. If **AGC_MODE** = 1_B, range of AGC is 12_D through 89_D. See also, **"AGC_MODE" on Page 258**.

11.2.7 Analog Loop and Bias Control

The **ALOOP_BIAS** register controls power reduction, power down bias and loops for analog operations.

ALOOP_BIAS
Analog Loop and Bias Control (07_H) Reset Value: 80_H

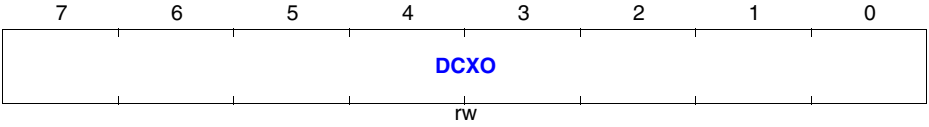


Field	Bits	Type	Description
Res0	7:6	rw	**Reserved** Always 10_B
PD_BIAS	5	rw	**Control Power Down Bias** 0_B Normal operation. 1_B Power down biasing active.
Res	4:0	rw	**Reserved** Always 0

11.2.8 Digital Crystal Frequency

The **DCXO** register tunes the crystal frequency specified in bits 2:0 (**XTAL**) of the **XTAL_TUN_PAR** register at $0F_H$.

DCXO
Digital Crystal Frequency **(08_H)** **Reset Value: 00_H**

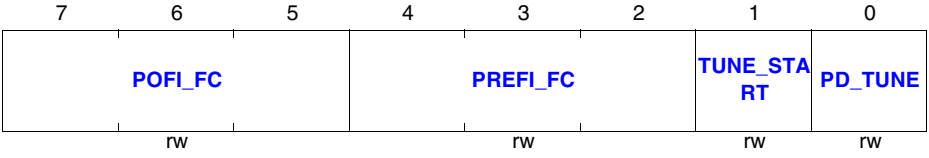


Field	Bits	Type	Description
DCXO	7:0	rw	**Tune Crystal Frequency** Not listed values are valid. 0000 0000_B Highest frequency, **XTAL** + 120 ppm. 0100 0111_B Nominal frequency, **XTAL** as specified. 1111 1111_B Lowest frequency, **XTAL** – 120 ppm.

11.2.9 Corner Frequency and Tuning

The **FC_TUNE** register sets corner frequencies for the pre-filter and post-filter, and starts and powers down tuning.

FC_TUNE
Corner Frequency and Tuning **($0C_H$)** **Reset Value: 00_H**



Field	Bits	Type	Description
POFI_FC	7:5	rw	**Set Corner Frequency (FC) for Post-Filter** 000_B 12.44 MHz 001_B 11.40 MHz 010_B 10.37 MHz 011_B 9.50 MHz 100_B 8.73 MHz 101_B 8.00 MHz 110_B 8.00 MHz 111_B 8.00 MHz
PREFI_FC	4:2	rw	**Set Corner Frequency (FC) for Pre-Filter** 000_B 12.44 MHz 001_B 11.40 MHz 010_B 10.37 MHz 011_B 9.50 MHz 100_B 8.73 MHz 101_B 8.00 MHz 110_B 8.00 MHz 111_B 8.00 MHz
TUNE_START	1	rw	**Start Tuning** Transition from 0 to 1 starts tuning. When tuning finishes, **TUNE_READY** (bit 5 of **WAK_PLL_TUN_RF** at $0D_H$) is set to 1. *Note: Set crystal (XTAL, bits 2:0 of **WAK_PLL_TUN_RF** at $0D_H$) and corner frequency for post-filter and pre-filter tuning (bits 7:2 of this register) before starting tuning.* 0_B No operation. 1_B Start tuning.
PD_TUNE	0	rw	**Power Down Tuning Unit** 0_B Normal operation. 1_B Power down tuning unit.

11.2.10 Wake-up, PLL, Tuning and RFS Status

The **WAK_PLL_TUN_RF** register reports detection of a wake-up sequence, and holds the status of the phase-locked loop (PLL) lock, the status of tuning and the reference filter value.

WAK_PLL_TUN_RF
Wake-up, PLL, Tuning and Status (0D$_H$) **Reset Value: 00$_H$**

7	6	5	4	3	2	1	0
WAKE_UP	PLL_LOCK	TUNE_READY	Res				
r	r	r	r				

Field	Bits	Type	Description
WAKE_UP	7	r	**Wake-up Sequence Detection Indicator** This bit is set whenever a valid wake-up sequence is detected. The value of this bit always reflects the value of the **WAKEUP_A** pin. 0_B No wake-up sequence detected. 1_B wake-up sequence detected.
PLL_LOCK	6	r	**Phase Locked Loop (PLL) Lock Status** 0_B PLL is not locked. 1_B PLL is locked.
TUNE_READY	5	r	**Tuning Measurement Status** 0_B No valid tuning or tuning procedure is in process. 1_B Valid tuning process finished.
Res	4:0	r	**Reserved** Internal use only.

11.2.11 Clock, Test, Crystal and Tuning Parameters

The **XTAL_TUN_PAR** register sets a crystal frequency.

XTAL_TUN_PAR
Clock, Test, Crystal and Tuning Parameters(0F$_H$) **Reset Value: 18$_H$**

7	6	5	4	3	2	1	0
Res					XTAL		
rw					rw		

Field	Bits	Type	Description
Res	7	rw	**Reserved**

Field	Bits	Type	Description
XTAL	2:0	rw	**Select Crystal Frequency (f_{xtal})** 000_B 38.88 MHz (Reset) 001_B 35.64 MHz 010_B 32.4 MHz 011_B 29.7 MHz 100_B 27.27 MHz 101_B:111_B 25 MHz

11.2.12 PLL Parameters

The **PLL_PAR** register controls scaling of input, format of input and output, and PLL power down.

PLL_PAR
PLL Parameters **(12_H)** **Reset Value: 04_H**

7	6	5	4	3	2	1	0
INT_SCAL_EN	Res		SEL_IOF	Res			PD_PLL
rw	rw		rw	rw			rw

Field	Bits	Type	Description
INT_SCAL_EN	7	rw	**Enable Shift or Scaling of Input to Interpolation Path** 0_B Bypass scaling block. 1_B Scale input to interpolation path by –3 dB.
Res	6:5	rw	**Reserved**
SEL_IOF	4	rw	**Select Data Input and Output Format** This bit selects the output for input and output data on the reception and transmission interfaces. 0_B Binary offset format. 1_B Twos complement format.
Res	3:1	rw	**Reserved**
PD_PLL	0	rw	**Control Power Down of PLL** 0_B PLL active. 1_B Power down PLL.

11.2.13 General Purpose Output Pad Parameters

The **GPO_PADS** register specifies parameters for General Purpose Output pads.

GPO_PADS
General Purpose Output Pad Parameters(19_H) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Res0		GPO5	GPO4	GPO3	GPO2	GPO1	GPO0
rw		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res0	7:6	rw	**Reserved** Always 0_B.
GPO5	5	rw	**General Purpose Output Pad**
GPO4	4	rw	**General Purpose Output Pad**
GPO3	3	rw	**General Purpose Output Pad**
GPO2	2	rw	**General Purpose Output Pad**
GPO1	1	rw	**General Purpose Output Pad**
GPO0	0	rw	**General Purpose Output Pad**

12 Electrical Characteristics - Overview

This section specifies the electrical characteristics of the integrated PEF 22827 and its primary functional blocks, as follows:

- Electrical characteristics for the integrated IC in the following sections:
  - **Absolute Maximum Ratings**
  - **Recommended Operating Conditions**
  - **Heat Dissipation Parameters**
  - **JTAG Interface**
- **Electrical Characteristics – Digital Block**, starting on **Page 269**
- **Electrical Characteristics – Analog Block**, starting on **Page 280**
- **Electrical Characteristics – Line Driver Block**, starting on **Page 286**

12.1 Absolute Maximum Ratings

Table 83 lists the absolute maximum ratings.

Table 83 Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Maximum junction temperature	T_J			125	°C	
Ambient temperature under bias	T_A	-40		+85	°C	
Storage temperature		-65		150	°C	
Power dissipation	PDmax		1.1		W	25°C (without heat sink)

Attention: Stresses beyond those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

12.2 Recommended Operating Conditions

The IC meets all standards for operation in indoor and outdoor environments in communication systems. See **“References” on Page 291**.

Extended operation outside recommended limits may degrade performance and affect reliability.

12.3 Heat Dissipation Parameters

In accordance with JEDEC JESD51-1 specifications, natural convection thermal resistance Θ_{JA} is calculated from the formula:

$$\Theta_{JA} = (T_{junction} - T_{ambient})/P_{dissipation} \quad (3)$$

where T = temperature and P = power.

The Θ junction to ambient represents the package dissipation through the ball, PCB and mold compound.

Θ_{JC} is the rate of heat flow to an external heat sink connected to the package. To find the thermal resistance at the junction-to-case, set the area attached to the heat sink to a constant temperature, and solve for the junction temperature.

For a P-TQFP package, the top package surface dissipates the heat generated by the die. Calculate Θ_{JC} from the formula:

$$\Theta_{JC} = (T_{junction} - T_{case})/P_{dissipation} \quad (4)$$

where Θ is constant.

For a BGA package, you can cool the package via a heat sink mounted on the top of the package (Θ_{JC}) or via the balls (Θ_{JB}).

Table 84 Thermal Resistance and Natural Convection

PCB size (mm²)	PCB area (mm²)	Θ_{JA} (K/W)	Θ_{JB} (K/W)[1]	Θ_{JC}(K/W)[1]
100x100	10000	24.5	17.6[2]	18.0[2]
70x70	4900	25.7		
50x50	2500	28.4		
34x34	1156	35.5		
24x24	576	49.5		
16x16	256	81.9		
13x13	169	109.5		

1) Package characteristic only, independent of PCB size.

2) Based on a total power of 1.4 W

12.4 JTAG Interface

This section describes the electrical characteristics of the JTAG interface.

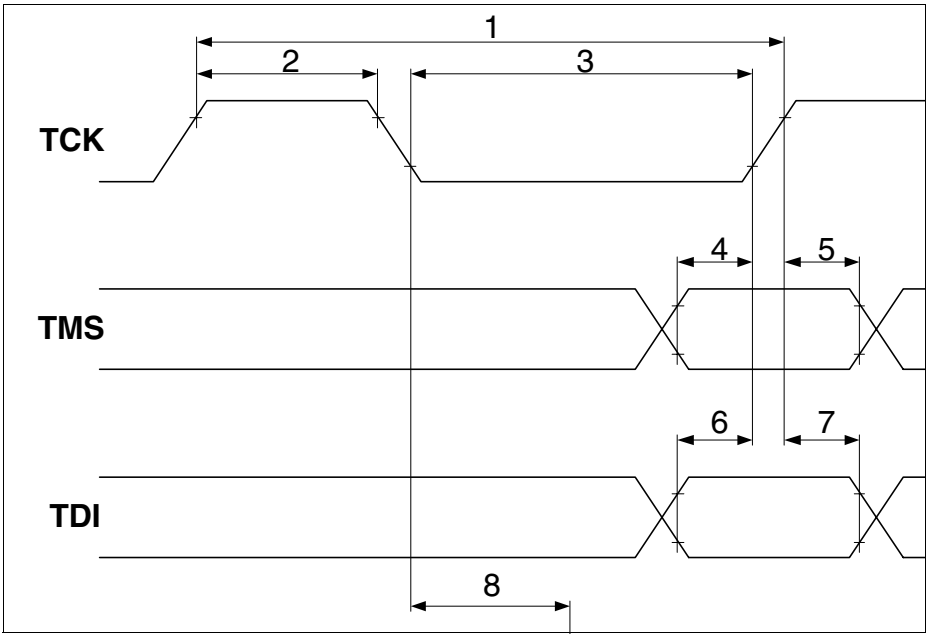


Figure 41 JTAG Boundary Scan Timing

Table 85 JTAG Boundary Scan Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
TCK period	1	250			ns	
TCK high time	2	80			ns	
TCK low time	3	80			ns	
TMS_D or TMS_A setup time	4	40			ns	
TMS_D or TMS_A hold time	5	40			ns	
TDI_D or TDI_A setup time	6	40			ns	
TDI_D or TDI_A hold time	7	40			ns	
TDO_D or TDO_A valid delay	8			100	ns	

12.5 Electrical Characteristics – Digital Block

This section includes the following sections:

- **Absolute Maximum Ratings – Digital Block**
- **DC Electrical Characteristics – Digital Block**
- **AC Characteristics – Digital Block**
- **Management Interfaces**
- **Network Interfaces**
- **EOC Interface**
- **EEPROM Interface**

12.5.1 Absolute Maximum Ratings – Digital Block

Table 86 shows the absolute maximum ratings for the digital block.

Table 86 Absolute Maximum Ratings – Digital Block

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Voltage on any pin with respect to ground	V_S	-0.4		V_{DDP} + 0.4	V	
Power dissipation				0.6	W	

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

12.5.2 DC Electrical Characteristics – Digital Block

Listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Table 87 DC Characteristics – Digital Block (page 1 of 2)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Input low voltage	V_{IL}	– 0.4		0.8	V	
Input high voltage	V_{IH}	2.4		3.6	V	

Table 87 DC Characteristics – Digital Block (page 2 of 2)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Input capacitance	IC			6.04	fF	
Output low voltage (3.3 V pads)	V_{OL}			0.4	V	I_{OL} = 28 mA[1], I_{OL} = 7 mA[2] Sink current
Output high voltage	V_{OH}	2.4			V	I_{OH} = -28 mA[1], I_{OH} = -8 mA[2] Source current
Power supply current (operational)	I_{CC}				mA	V_{DD} = 1.2 V, T_A = 25 °C: Clock = 38.88 MHz
Input leakage current	I_{IL}				µA	V_{DD} = 1.2 V, GND = 0 V; All other pins are floating; V_{IN} = 0 V, V_{DDP} + 0.4
Output leakage current	I_{OZ}				µA	V_{DDD} = 1.2 V, GND = 0 V; V_{OUT} = 0 V, V_{DDP} + 0.4

1) Interface output pins.

2) All output pins except those used for the SMII interface.

12.5.3 AC Characteristics – Digital Block

T_A = - 40 to 85 °C, V_{DD} = 1.2 V ± 5%, V_{DDP} = 3.3 V ± 5%

Input signals are driven to 2.4 V for a logical 1 and to 0.45 V for a logical 0. Timing is measured at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input and output waveforms are shown in **Figure 42**.

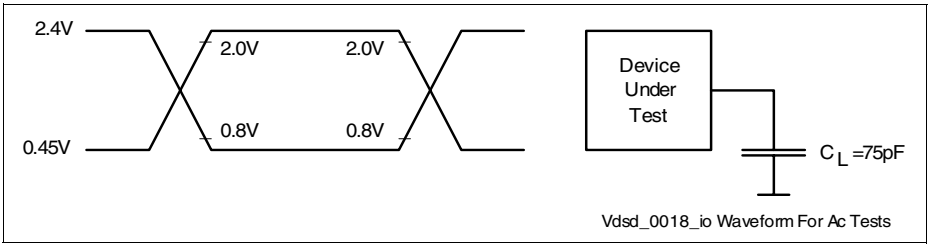


Figure 42 Input Output Waveforms for AC Tests

12.5.4 Management Interfaces

The following sections describe the electrical characteristics of the management interfaces of the digital block.

12.5.4.1 Parallel Host Interface

Parallel port access time is dependent on the external clock. A slower clock is required for slower access from the external device.

Figure 43 illustrates the timing during read operations from a parallel port register, and **Figure 44** illustrates the timing during write operations. **Table 88** describes the AC requirement for both read and write operations to or from a parallel port register.

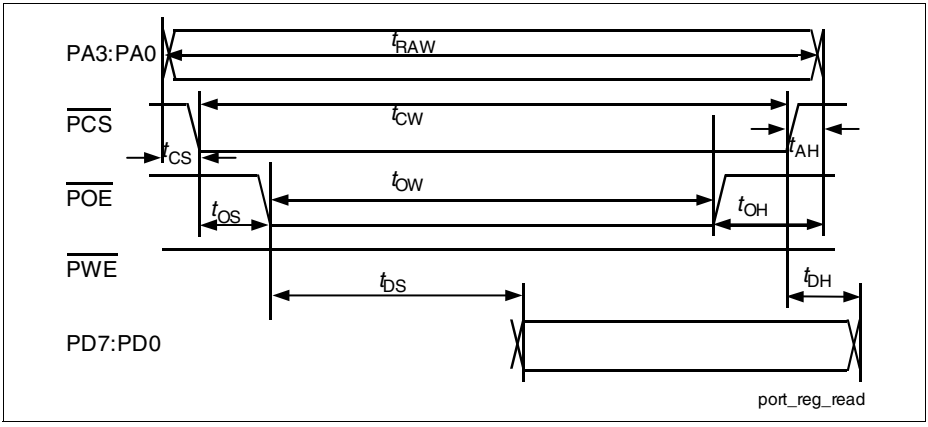


Figure 43 Parallel Port Register Read Timing

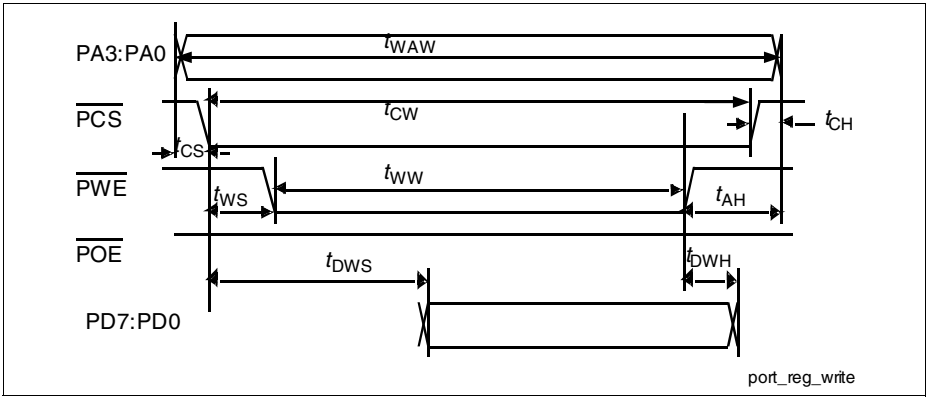


Figure 44 Parallel Port Register Write Timing

Table 88 AC Parallel Port Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Address width	t_{RAW}	6			CLKOUT	
Setup time, $\overline{PCS}$ falling edge after PA change	t_{CS}	0			CLKOUT	
$\overline{PCS}$ width	t_{CW}	6			CLKOUT	
Address hold after $\overline{PCS}$ negation	t_{AH}	0			CLKOUT	
$\overline{POE}$ falling edge after $\overline{PCS}$ falling edge	t_{OS}	0		2	CLKOUT	
$\overline{POE}$ width	t_{OW}	4			CLKOUT	
$\overline{POE}$ negation to data go to Z	t_{OH}	10			ns	
POE assertion to DATA valid	t_{DS}			3	CLKOUT	
$\overline{PWE}$ assertion after $\overline{PCS}$ assertion	t_{WS}			2	CLKOUT	
$\overline{PWE}$ pulse width	t_{WW}	4			CLKOUT	
Data valid after $\overline{PCS}$ assertion during write transaction	t_{DWS}			2	CLKOUT	
Data hold after $\overline{PWE}$ negation during write transaction	t_{DWH}	0			CLKOUT	

12.5.4.2 MII Serial Management Interface (SMI) in a Slave Configuration

Figure 45 shows the timing characteristics of SMI in MII PHY mode.

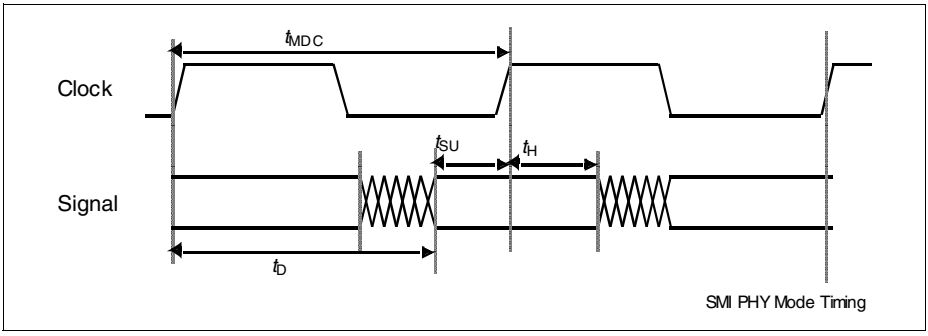


Figure 45 SMI PHY Mode Timing Diagram

Table 89 SMI PHY Mode Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
MDC period	t_{MDC}	400			ns	
MDIO (input) setup to MDC (input)	t_{SU}	10			ns	
MDIO (input) hold after MDC (input)	t_H	10			ns	
MDIO (output) delay from MDC (input)	t_D	0		300	ns	

12.5.4.3 MII Serial Management Interface (SMI) in a Master Configuration

Figure 46 shows the timing characteristics of SMI in MII MAC mode.

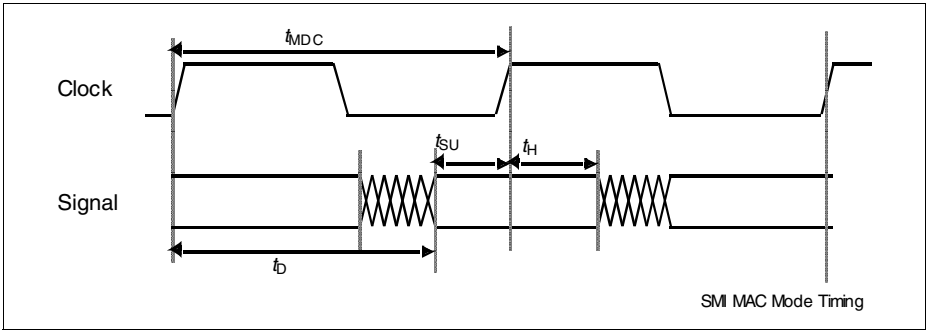


Figure 46 SMI MAC Mode Timing Diagram

Table 90 SMI MAC Mode Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
MDC period	t_{MDC}	400			ns	
MDIO (input) setup to MDC (output)	t_{SU}	0			ns	
MDIO (input) hold after MDC (output)	t_H	5			ns	
MDIO (output) delay from MDC (output)	t_D	0		300	ns	

12.5.5 Network Interfaces

Network interfaces serve as the main data path between the IC and the outside world. Data received on these interfaces is output and transmitted over the VDSL line.

12.5.5.1 MII Interface

Figure 47 and **Table 91** specify the timing characteristics of both the MII PHY and the MII MAC interfaces.

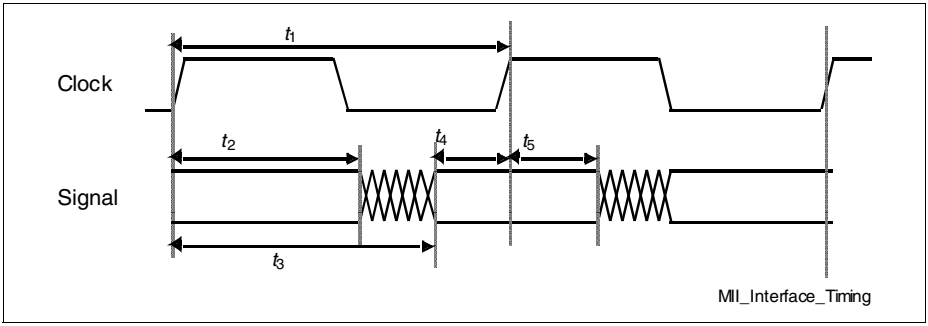


Figure 47 MII Interface Timing Diagram

Table 91 MII Mode Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
TXCLK or RXCLK frequency	t_1	40		400	ns	ECLK1, ECLK3
Input setup to TXCLK	t_4	1.47			ns	ETHID3:ETHID0, ETHCTLI
Input hold from TXCLK	t_5	0.31			ns	
Output delay from RXCLK	t_3			11.93	ns	ETHOD3:ETHOD0, ETHCTLO
Output hold from RXCLK	t_2	3.21			ns	

12.5.5.2 RMII Interface

Figure 48 and **Table 92** specify the timing characteristics of both the RMII PHY and the RMII MAC interfaces.

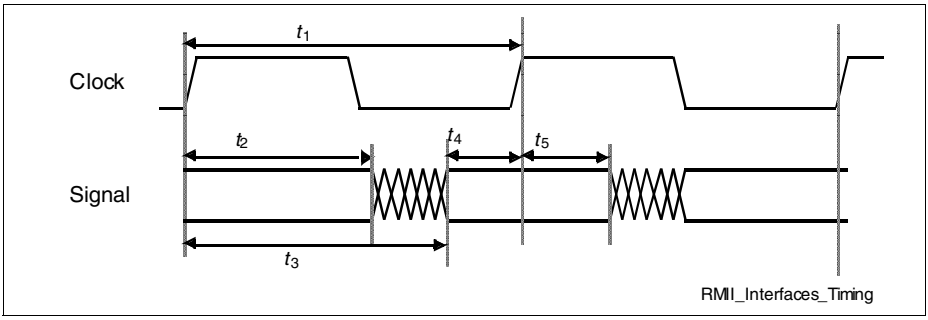


Figure 48 RMII Interfaces Timing Diagram

Table 92 RMII Interfaces Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
TXCLK or RXCLK frequency	t_1	20		20	ns	ECLK1
Input setup to TXCLK	t_4	2.1			ns	ETHID1:ETHID0, ETHCTLI
Input hold from TXCLK	t_5	0.26			ns	
Output delay from RXCLK	t_3			9	ns	ETHOD1:ETHOD0, ETHCTLO
Output hold from RXCLK	t_2	2.8			ns	

12.5.5.3 Serial MII Interface, Typical Mode

Figure 49 and Table 93 specify the timing characteristics of the typical Serial MII interface. External load in typical mode is 5 pF.

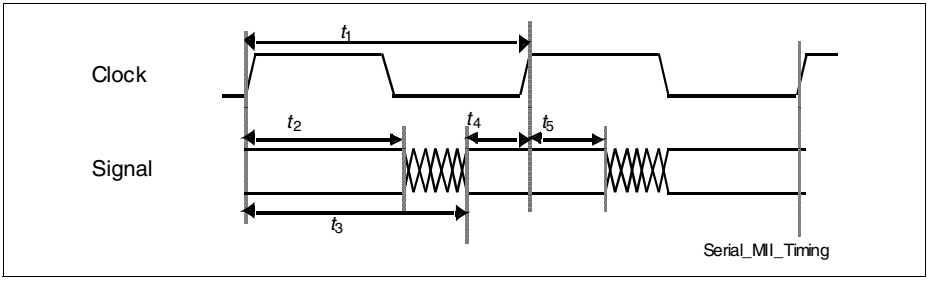


Figure 49 Typical Serial MII Interface Timing Diagram

Table 93 Typical Serial MII Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Clock cycle time	t_1	8		8	ns	ECLK1
SYNC setup time	t_4	0.77			ns	ETHCTLI
SYNC hold time	t_5	0.45			ns	
Reception delay after rising edge of clock (TXCLK)	t_3			4.7	ns	ETHOD0
Reception hold after rising edge of clock (TXCLK)	t_2	2			ns	
Transmission setup time before rising edge of clock (TXCLK)	t_4	0.7			ns	ETHID0
Transmission hold time after rising edge of clock (TXCLK)	t_5	0.71			ns	

12.5.5.4 Serial MII Interface, Source Synchronous Mode

Figure 50 and Table 94 specify the timing characteristics of source synchronous Serial MII interface. External load in SMII source mode is 40 pF.

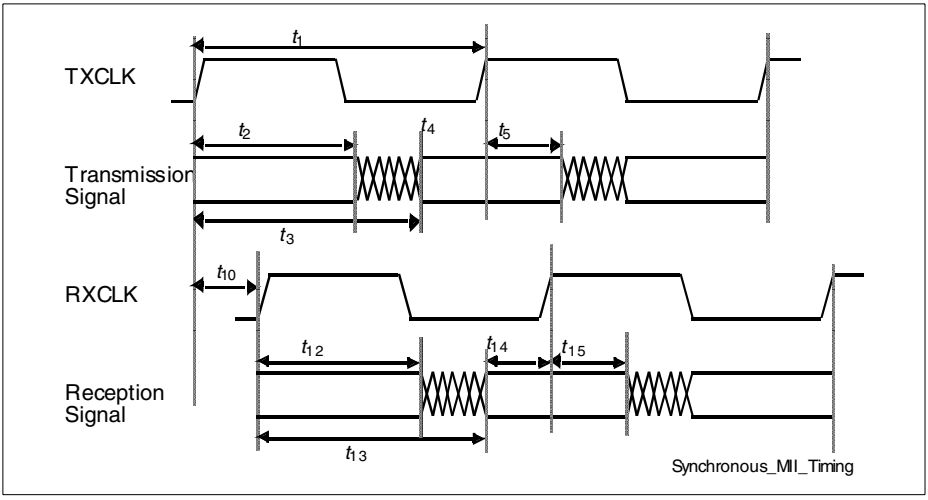


Figure 50 Source Synchronous MII Interface Timing Diagram

Table 94 Source Synchronous SMII Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Clock cycle time	t_1	8		8	ns	ECLK3
TX_SYNC setup time	t_4	1.16			ns	ETHCTLI
TX_SYNC hold time	t_5	0.46			ns	
Reception rising edge after transmission rising edge	t_{10}	3.15		9.95	ns	MDCO, ECLK3
Reception delay after RXCLK rising edge	t_{13}			7.7	ns	ETHOD0
Reception hold after RXCLK rising edge	t_{12}	5.45			ns	
Transmission setup time before TXCLK rising edge	t_4	1.16			ns	ETHID0, TXSYNC
Transmission hold time after TXCLK rising edge	t_5	0.46			ns	
RX_SYNC delay after RXCLK rising edge	t_{14}	0.05			ns	ETHCTLI
RX_SYNC hold after RXCLK rising edge	t_{15}	0.5			ns	

12.5.6 EOC Interface

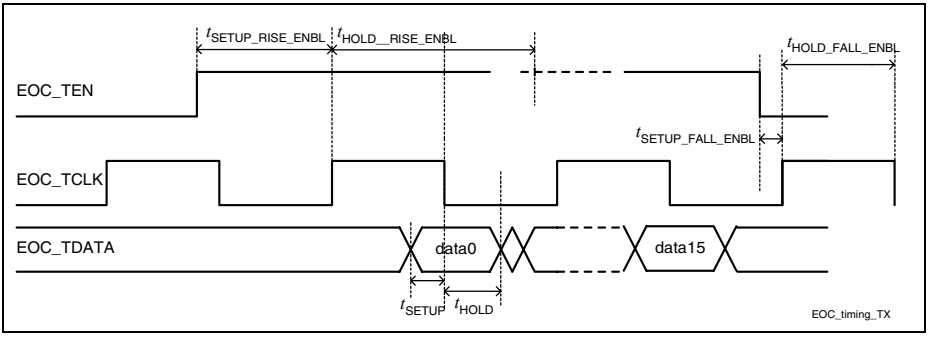


Figure 51 EOC Transmission Timing

Table 95 EOC Timing Parameters for Transmission

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
EOC_TCLK period	t_{EOC_TCLK}	8			CLKOUT	
Setup time between falling edge of EOC_TEN and rising edge of EOC_TCLK	$t_{SETUP\_FALL\_ENBL}$			1	CLKOUT	
Guaranteed delay after rising edge of EOC_TCLK	$t_{HOLD\_FALL\_ENBL}$	4			CLKOUT	
Setup time between rising edge of EOC_TEN and rising edge of EOC_TCLK	$t_{SETUP\_RISE\_ENBL}$			5	CLKOUT	
Guaranteed delay after rising edge of EOC_TCLK	$t_{HOLD\_RISE\_ENBL}$	9			CLKOUT	
Setup time required for EOC_TDATA to be valid	t_{SETUP}			0	CLKOUT	
Hold time required for EOC_TDATA to be valid	t_{HOLD}	2			CLKOUT	

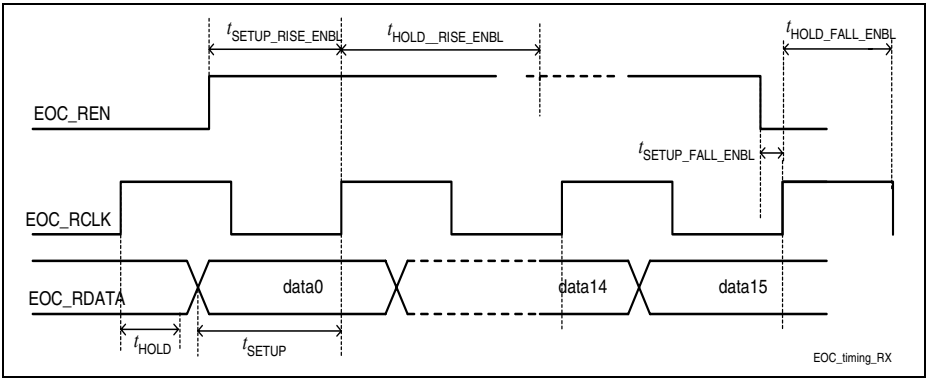


Figure 52 EOC Reception Timing

Table 96 EOC Timing Parameters for Reception

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
EOC_RCLK period	t_{EOC_RCLK}	8			CLKOUT	
Setup time between falling edge of EOC_REN and rising edge of EOC_RCLK	$t_{SETUP\_FALL\_ENBL}$			1	CLKOUT	
Guaranteed delay after rising edge of EOC_RCLK	$t_{HOLD\_FALL\_ENBL}$	4			CLKOUT	
Setup time between rising edge of EOC_REN and rising edge of EOC_RCLK	$t_{SETUP\_RISE\_ENBL}$			5	CLKOUT	
Guaranteed delay after rising edge of EOC_RCLK	$t_{HOLD\_RISE\_ENBL}$	9			CLKOUT	
Setup time for EOC_RDATA to be valid	t_{SETUP}			0	CLKOUT	
Hold time for EOC_RDATA to be valid	t_{HOLD}	2			CLKOUT	

12.5.7 EEPROM Interface

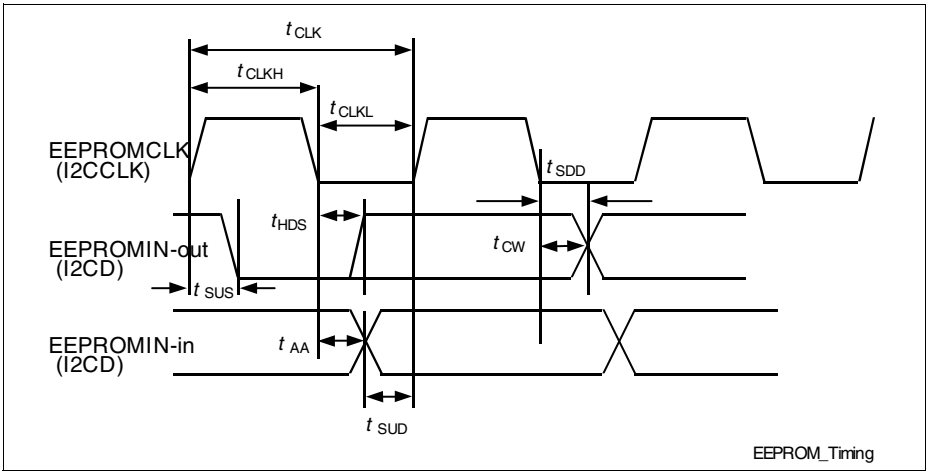


Figure 53 EEPROM Timing

Table 97 EEPROM Timing Parameters

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Serial clock pulse	t_{CLK}	18			µs	I2CCLK
Serial clock high	t_{CLKH}	9			µs	
Serial clock low	t_{CLKL}	9			µs	
Start or stop bit setup time from clock rise	t_{SUS}	7			µs	I2CD
Start or stop bit hold time from clock fall	t_{HDS}	7			µs	
EEPROMIN-in hold from clock fall	t_{AA}	3.3			µs	
EEPROMIN-in setup before clock rise	t_{SUD}	7			µs	
EEPROMIN-out valid from clock fall	t_{SDD}					
EEPROMIN-out hold from clock fall	t_{CW}	3.3			µs	

12.6 Electrical Characteristics – Analog Block

This section specifies the following electrical characteristics for the Analog Block:

- **Absolute Maximum Ratings – Analog Block**
- **Operating Range – Analog Block**
- **DC Characteristics – Analog Block**
- **AC Characteristics – Analog Block**

12.6.1 Absolute Maximum Ratings – Analog Block

Table 98 lists the absolute maximum ratings of the AFE.

Table 98 Absolute Maximum Ratings – Analog Block

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Analog supply voltage	V_{DDA}	-0.1		1.98	V	
Digital supply voltage	V_{DDD}	-0.1		1.98	V	
Digital I/O supply voltage	V_{DDIO}	-0.3		3.6	V	
Analog input voltages	V_{in}	-0.1		1.98	V	
Digital input voltages	V_{Din}	-0.1		1.98	V	
Power dissipation in power down (stand by)	PDs	20		50	mW	
Power dissipation during operation	PDo	470		520	mW	

12.6.2 Operating Range – Analog Block

Unless stated otherwise, all values are for the full temperature range: from -40 through +85° C.

Table 99 Operating Range – Analog Block

Parameter	Symbol	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Analog supply voltage	V_{DDA}	1.71	1.8	1.89	V	
Digital supply	V_{DDD}	1.71	1.8	1.89	V	
Digital supply I/O	V_{DDIO}	3.14	3.3	3.46	V	

Table 100 Clocking Characteristics for Internal and External[1] Clocks

Parameter	Values			Unit	Test Condition
	Min.	Typ.	Max.		
Sampling frequency				MHz	CLK, DAC_CLK
Mode 1		25		MHz	
Mode 2		27.27		MHz	
Mode 3		29.7		MHz	
Mode 4		32.4		MHz	
Mode 5		35.64		MHz	
Mode 6		38.88		MHz	
Clock duty cycle	45	50	55	%	CLK, DAC_CLK
Clock accuracy	-50		+50	ppm	For crystal or external clock
Jitter (RMS)		25		ps	For 11.5 $bits_{eff}$ and f_{max} = 12 MHz

[1] For external clocks, an accuracy of ±50 ppm is recommended. An external clock must fulfill the limits of V_{in} in **Table 98**.

12.6.3 DC Characteristics – Analog Block

Table 101 lists the DC characteristics of the Analog Block.

Table 101 DC Characteristics – Analog Block

Parameter	Symbol	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Input low voltage[1)]	V_{IL}	-0.3	0.8		V	
Input high voltage[1)]	V_{IH}	2.0	3.6		V	Test conditions defined in Figure 54
Output low voltage[1)]	V_{OL}		0.5		V	I_{OL} =10 mA sink current
Output high voltage[1)]	V_{OH}	2.4			V	I_{OH} =-10 mA source current
Power supply current (operational)	I_{CC}	10	25		mA	VDD_IO = 3.3 V
	I_{CC}	170	265		mA	VDDD/VDDA/VDDT/VDDR = 1.8 V
Input leakage current	I_{IL}		1.0		µA	VDDIO =3.3V, GND=0 V; all other pins are floating; V_{IN} =0 V, VDDP + 0.4

[1)] Valid for all digital I/O pins. All digital I/O pins are 3.3 V pads.

Test Conditions

TA=-40 °C to 85 °C, VDD = 3.3 V 5%

Input signals are driven to 2.4 V for a logical 1 and to 0.4 V for a logical 0. Testing input and output waveforms are shown in Figure 54.

Figure 54 Input and Output Waveform for AC Tests

12.6.4 AC Characteristics – Analog Block

This section describes the AC characteristics of the Analog Block.

12.6.4.1 AFE Transmission Path

Table 102 describes the electrical characteristics of the AFE transmission path.

Table 102 AFETransmission Path

Parameter	Values			Unit	Test Condition
	Min.	Typ.	Max.		
Power controller range		0...24	± 0.25	dB	
Power controller resolution		6	±0.2	dB	
External load resistor (= line driver)	> 2k			Ω	Minimum value must be > 2 kΩ differential
Linear voltage range		1		Vp	Differential
Absolute gain error			± 1	dB	
Harmonic distortion		≤ -56		dBc	At –6 dB full scale full scale = 1 Vp, f = 3.5 MHz
SNR			60	dB	At –6 dB full scale sine wave At f = 3.5 MHz

12.6.4.2 AFE Reception Path

Table 103 describes the electrical characteristics of the AFE reception path.

Table 103 AFE Reception Path (page 1 of 2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
AGC Range			-12...32.5	± 1.5	dB	Including external resistance
AGC Resolution			0.5	± 0.3	dB	
AGC Step Accuracy within course gain adjustment			strictly monotone for all codes			
Input Resistance			1600	±15%	Ω	Differential
External Resistance			2 x 800	± 2%	Ω	1)
Input Signal Range (for each pin)			0-1.8 V	-0.1-1.98 V	V	Max 1.8 vp Differential at Pin
Absolute Gain Error			-1.5	+1.5		dB

Table 103 AFE Reception Path (page 2 of 2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Offset Error				< 100 at 20 dB < 200 at 30 dB	mV	Depends highly on AGC setting, <50 LSB at 20 dB <100 LSB at 30 dB
Harmonic Distortion			≤56		dBc	At -6db full scale, = 1 vp f = 3.5 Mhz
SNR			63		dB	At -6 dB full scale sine wave at f = 3.5 MHz

1) Two external resisters are required in series on receptioninput to limit the pad voltage V_{PAD} between the pads of pin RX_N and RX_P (see **Figure 55**).

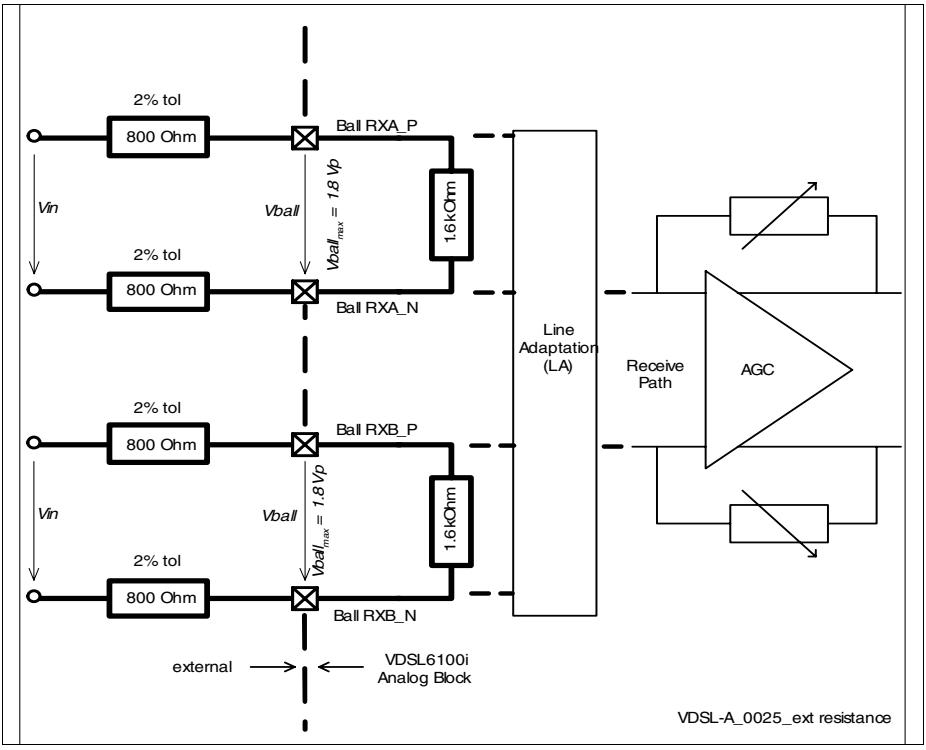


Figure 55 Input Resistance for Reception Input

12.6.4.3 Filter Specification (Transmission and Reception Paths)

A third order Chebychev filter is implemented as transmission and reception filters with a ripple of 0.5 dB. Depending on Modes 1-6, the nominal pass band corner frequencies are specified in **Table 104**.

Table 104 Filter Specification for PREFI and POFI Filters

Parameter	Mode					
	1	2	3	4	5	6
Nominal Pass-band Corner Frequency $f_{c,nom}$ MHz for Modes 1 through 6	8	8.73	9.50	10.37	11.40	12.44

12.6.4.4 DCXO Characteristics

Table 105 describes the electrical characteristics of the DCXO.

Table 105 DCXO Characteristics

Parameter	Values			Unit	Notes
	Min.	Typ.	Max.		
Tolerance External Crystal	-50		50	ppm	
Center Frequency	25		38.88	MHz	± 50 ppm, Nominal values - 25/27.27/29.7/ 32.4/ 35.64/ 38.88MHz. See **"Operating Range – Analog Block" on Page 281**
Tuning Range		±120		ppm	
Step Size		<0.3	5	ppm	
Frequency coding DCXO_FO	0 (≥ +120)		255 (≤- 120)	code (ppm)	Crystal spec (38.88 MHz): f_{nom} = 38.88 MHz C1 >= 35 fF R1 <= 30 Ohm C0 = 8 pF CL_{nom} = 31.3 pF CL = 22 pF to 50 pF

The DCXO frequency is controlled directly via the DCXO register. The DCXO register can be accessed via the serial control interface.

12.7 Electrical Characteristics – Line Driver Block

This chapter describes the following electrical characteristics for the Line Driver Block:

- **Absolute Maximum Ratings – Line Driver Block**
- **Operating Range – Line Driver Block**
- **DC Characteristics – Line Driver Block**
- **AC Characteristics – Line Driver Block**

12.7.1 Absolute Maximum Ratings – Line Driver Block

Table 106 lists the absolute maximum ratings for the Line Driver block.

Table 106 Absolute Maximum Ratings – Line Driver Block

Parameter	Symbol	Values		Unit	Test Condition
		Min.	Max.		
Positive supply voltage	$+V_S$	-0.3	+9	V	
Negative supply voltage	$-V_S$	+0.3	-9	V	
Driver V_{+IN} Voltage	V_{+IN}	$-V_S$ - 0.3	$+V_S$+ 0.3	V	
Current into negatitve inputs	I_{-IN}		±10	mA	
Maximum junction temperature	T_J		150	°C	
Ambient Temperature under Bias	T_A	-40 -5	+85 +85	°C °C	Functionality Full Performance
Max. Power Dissipation	PDmax		0.8	W	25°C (without heat sink)

12.7.2 Operating Range – Line Driver Block

Unless stated otherwise, all values are for the full temperature range from -5 to +85°C.

Table 107 Operating Range – Line Driver Block

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
Positive Supply Voltage referenced to GND	$+V_S$	+4.5	+7	+8	V	
Negative Supply Voltage referenced to GND	$-V_S$	-4.5	-7	-7	V	
Ambient Temperature under Bias	TA	-40		85	°C	
Static Thermal Resistance	$R_{TH,,jA}$		155		°K/W	
	$R_{TH,,jC}$		TBD		°K/W	

12.7.3 DC Characteristics – Line Driver Block

Table 108 specfies the DC characteristics of the Line Driver block.

Table 108 DC Characteristics – Line Driver Block

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Equivalent Differential Input Offset Voltage		-20		+20	mV	
Negative Input Bias Current		-70		+70	µA	T_a= 25°C
Positive Input Bias Current		-70	3	+70	µA	T_a= 25°C
Output voltage swing			11		$\pm V_p$	Differential, R_{LOAD} = 112 Ω, ±7V supply T_a= 25°C
Output Current		175			mA	R_L = 10 Ω single ended, ±7V supply
Output Impedance			0.2 2		Ω Ω	at 1 MHz at 10 MHz
Differential Input Resistance			85		kΩ	+Input
			20		Ω	-Input
Open Loop Transresistance			450		kΩ	
Input Common Mode Voltage Range		-5.5		+5.5	V	±7V supply
Short Circuit Current		250			mA	
Quiescent Current	I_Q	17	21	25	mA	±7V supply T_a= 25°C
Quiescent Current in Power Down	I_{QPDN}	0.5	0.7	0.9	mA	±7V supply
Power Down threshold	V_{PD}	0.7	–	1.6	V	±7 V supply, related to $-V_S$
Power Down input impedance	R_{PD}	32	–	–	kΩ	related to $-V_S$

12.7.4 AC Characteristics – Line Driver Block

Table 109 specfies the AC characteristics of the Line Driver block.

Table 109 AC Characteristics – Line Driver Block

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Small Signal Bandwidth (-3 dB)			90		MHz	Vs = ±7 V
Differential Slew Rate			1100		V/µs	Vout = 20 V_{p-p}
Harmonic Distortion					dBc	Vout = 10 V_{p-p} (differential)
2nd Harmonic			-78 -65			100 kHz R_L = 112 Ω (differential) 6MHz R_L = 112 Ω (differential)
3rd Harmonic			-80 -65			100 kHz R_L = 112 Ω (differential) 6MHz R_L = 112 Ω (differential)
Equivalent Input Voltage Noise			6	12	nV/ $Hz^{0.5}$	f = 10 kHz (single ended)
Common Mode Rejection	CMR		44		dB	(single ended)
Power Supply Rejection	PSR+		49		dB	(single ended)
	PSR-		54		dB	(single ended)

13 Package Outline

Figure 56 presents the PEF 22827 package outline.

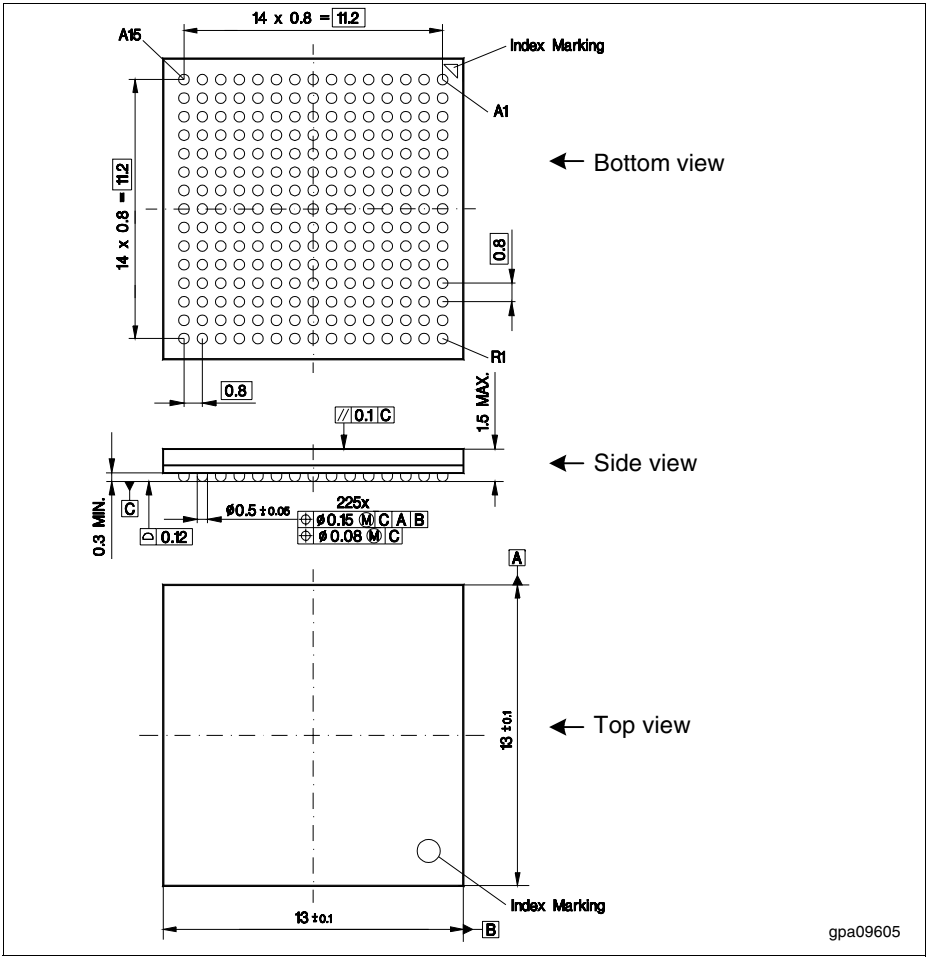


Figure 56 PG-LFBGA-225-1 Outline

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

References

This data sheet may refer to material in the following documents:

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[3] —, "Very-high-speed Digital Subscriber Line Foundation", ITU-T G.993.1 Recommendation.

[4] —, "B-ISDN operation and maintenance principles and functions", ITU-T recommendation I.610.

[5] —, "Physical Layer Management for Digital Subscriber Line (DSL) Transceivers", ITU-T G.997.1 Recommendation, Telecommunication Standardization Sector of ITU, Feb. 1999.

[6] —, "Integrated Service Digital Network (ISDN). B-ISDN User Network Interface - Physical Layer Specification Draft VDSL Standard", ITU-T I.432 Recommendation.

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[8] —, IEEE Standard 802.3.

[9] —, IEEE Standard 1149.1.

[10] —, "Serial MII Specification", Rev 2.1, Cisco Systems Inc, Broadcom Corp, National Semiconductor Corp and Texas Instruments Inc., Feb. 9, 2000.

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Terminology

ACE	Analog Channel Equalizer
ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AFE	Analog Front End
AGC	Automatic Gain Control
AI	Analog Input levels
AO	Analog Output levels
ANSI	American National Standards Institute
BER	Bit Error Rate
BGA	Ball Grid Array
BPSK	Binary Phase Shift Keying (QAM 2)
CPE	Customer Premises Equipment
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCXO	Digitally Controlled Crystal Oscillator
Downstream	In the direction from a central box (office) to a local (home) connection
DSLAM	DSL Access Multiplexer
EOC	Embedded Overhead or Operations Channel
EoVDSL	Ethernet over VDSL
ETSI	European Telecommunications Standards Institute
FCS	Frame Check Sequence
FDD	Frequency Division Duplexing
FEC	Forward Error Correction
FEXT	Far End Crosstalk
FTTC	Fiber to the Curb
HDLC	High level Data Link Control
HDSL	High Bit-rate Digital Subscriber Line
HEC	Header Error Correction
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit (IIC)

IEEE	Institute of Electrical and Electronics Engineers
ISDN	Integrated Services Digital Network
ISDN-BRA	ISDN Basic Rate Access
ISDN-PRA	ISDN Primary Rate Access
JTAG	Joint Test Action Group
LAN	Local Area Network
LOS	Loss of Signal
LR	Long Reach
LT	Line Termination (VTU-O, in ETSI standard)
LUT	Look-Up Table
MAC	Media Access Control Layer 2
MIB	Management Information Base
MII	Media Independent Interface
NT	Network Termination (VTU-R, in ETSI standard)
NTR	Network Timing Reference
NC	Not Connected
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
PCM	Pulse Code Modulation
PD	Pull Down. Connect to external pull-down.
PHY	Physical Layer
PDV	Pulse Density Violation
PLL	Phase Locked Loop
PMD	Physical Medium Dependent
PMS-TC	Physical Medium Specific Transmission Convergence
POTS	Plain Old Telephone Service
PSD	Power Spectral Density
PVC	Permanent Virtual Connection
QAM	Quadrature Amplitude Modulation
RA	Rate Adaptive module
RFI	Radio Frequency Interference

RLOS	Reception Loss of Signal
RS	Reed Solomon
RX	Reception related Signal or Operation
SAR	Segmentation and Reassembly
SDSL	Symmetric Digital Subscriber Line
SMI	Serial Management Interface
SMII	Serial Media Independent Interface (MII) Interface
SNMP	Simple Network Management Protocol
SNR	Signal to Noise Ratio
STP	Set of Transmission Parameters
TAP	Test Access Point
TC	Transmission Convergence (layer)
TQFP	Thin Quad Flat Package
TX	Transmission related Signal or Operation
TPS	Transport Protocol Specific
UART	Universal Asynchronous Receiver-Transmitter
upstream	In the direction from the local box (home) to the central box (office)
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier
VCXO	Voltage Controlled Crystal Oscillator
VDSL	Very high bit rate Digital Subscriber Line
VOC	VDSL Overhead Control
WDF	Wave Digital Filter

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