

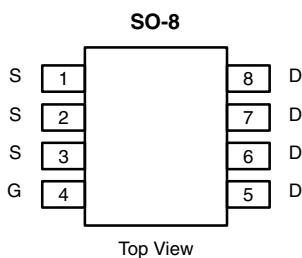
N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A) ^a	Q_g (Typ.)
100	0.0100 at $V_{GS} = 10$ V	19.7	27.9 nC
	0.0105 at $V_{GS} = 7.5$ V	19.2	
	0.0120 at $V_{GS} = 6.0$ V	18	

FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912

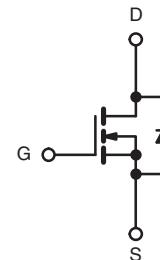


Top View

Ordering Information:
Si4090DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server
- Motor Drive Control
- Synchronous Rectification



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	19.7	A
		15.8	
		13.2 ^{b, c}	
		10.4 ^{b, c}	
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	70	A
Continuous Source-Drain Diode Current	I_S	7	
		3.1 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	30	mJ
Avalanche Energy	E_{AS}	45	
Maximum Power Dissipation	P_D	7.8	W
		5	
		3.5 ^{b, c}	
		2.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	29	35	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under steady state conditions is 80 °C/W.

Si4090DY

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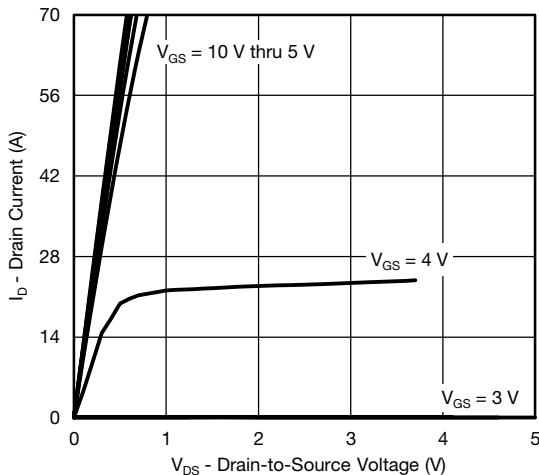
**SPECIFICATIONS** ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		67		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 6.4		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2		3.3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		0.0080	0.0100	Ω
		$V_{GS} = 7.5 \text{ V}$, $I_D = 12 \text{ A}$		0.0085	0.0105	
		$V_{GS} = 6.0 \text{ V}$, $I_D = 10 \text{ A}$		0.0090	0.0120	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 15 \text{ A}$		54		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		2410		pF
Output Capacitance	C_{oss}			790		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge	Q_g	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$		45.6	69	nC
Gate-Source Charge	Q_{gs}			27.9	42	
Gate-Drain Charge	Q_{gd}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 6 \text{ V}$, $I_D = 10 \text{ A}$		8.5		
Output Charge	Q_{oss}			9.2		
Gate Resistance	R_g	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$	0.4	1.3	2.6	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 5 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 7.5 \text{ V}$, $R_g = 1 \Omega$		16	32	ns
Rise Time	t_r			11	22	
Turn-Off Delay Time	$t_{d(\text{off})}$			35	70	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(\text{on})}$			14	28	
Rise Time	t_r	$V_{DD} = 50 \text{ V}$, $R_L = 5 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		10	20	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			36	70	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			7	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 5 \text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		49	95	ns
Body Diode Reverse Recovery Charge	Q_{rr}			58	115	
Reverse Recovery Fall Time	t_a			21		ns
Reverse Recovery Rise Time	t_b			28		

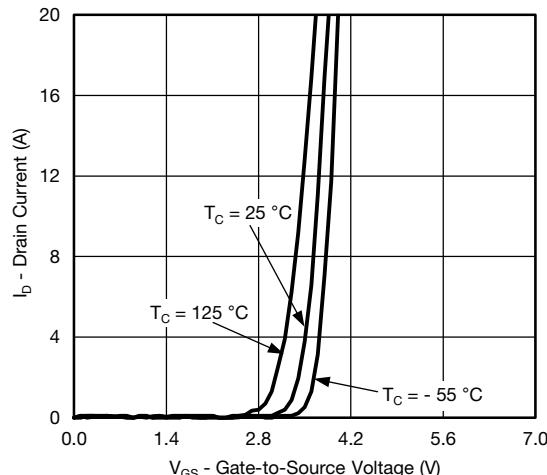
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

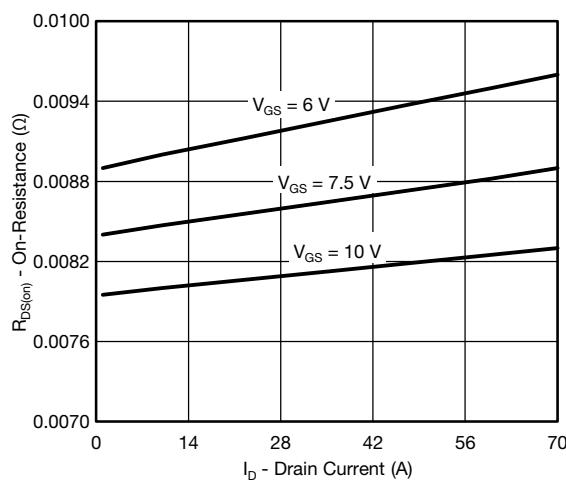
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


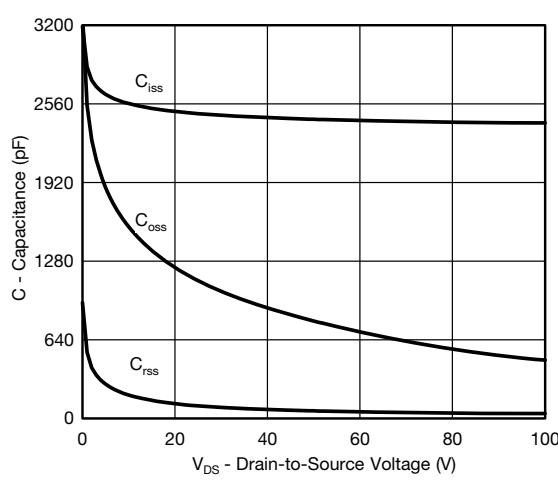
Output Characteristics



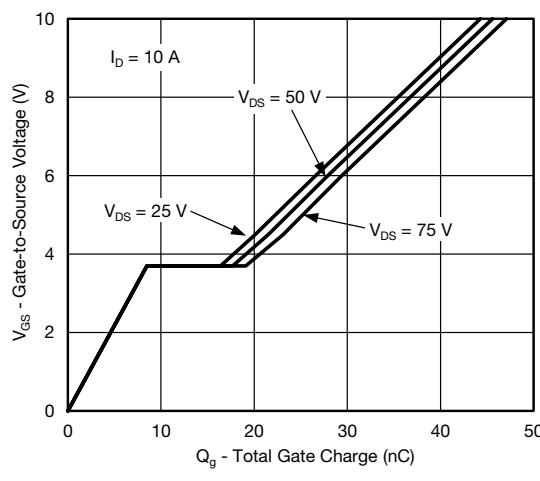
Transfer Characteristics



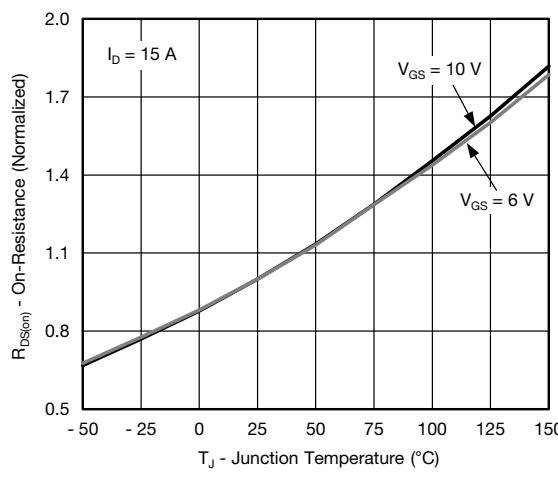
On-Resistance vs. Drain Current



Capacitance



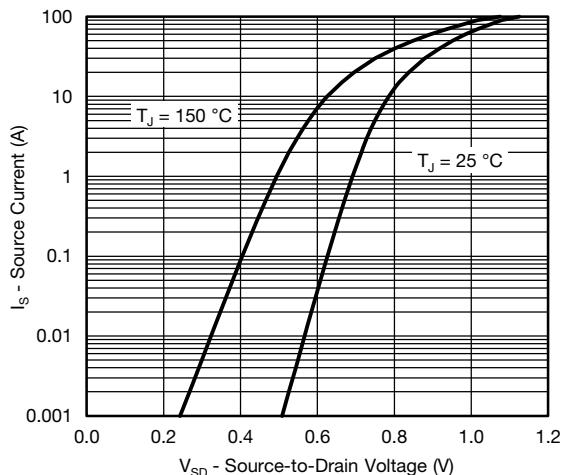
Gate Charge



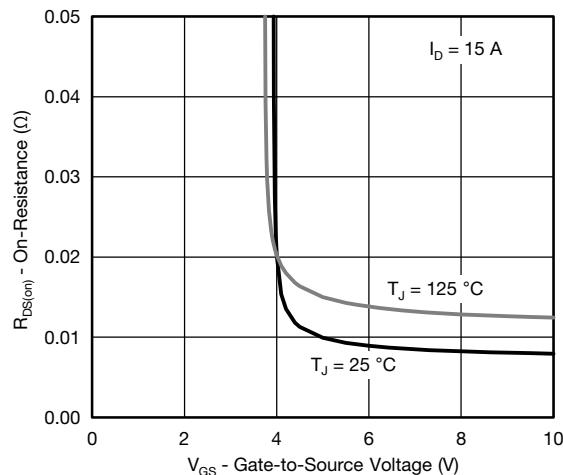
On-Resistance vs. Junction Temperature

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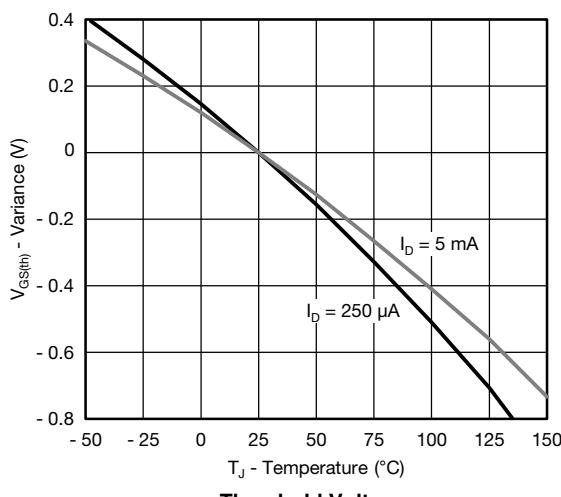
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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

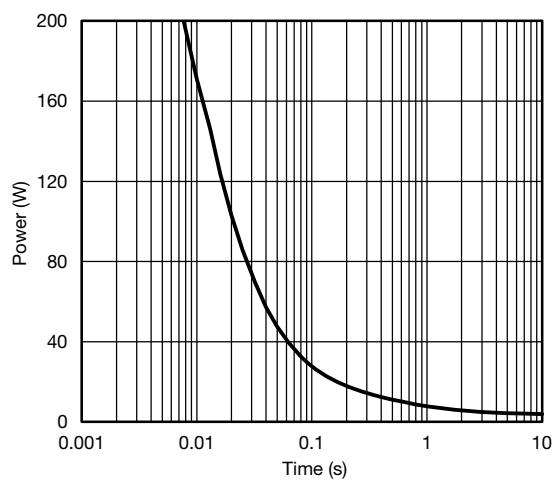
Source-Drain Diode Forward Voltage



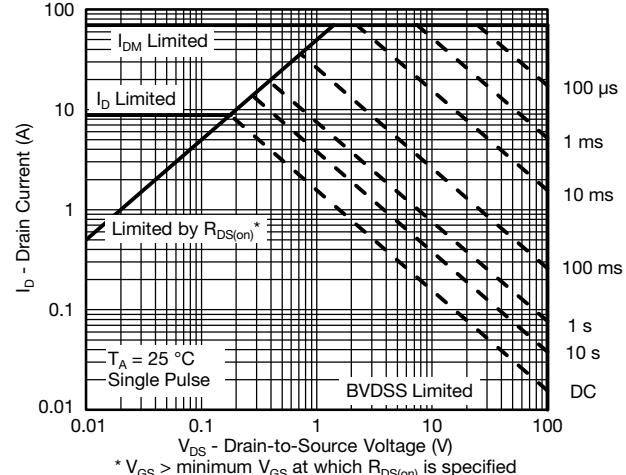
On-Resistance vs. Gate-to-Source Voltage



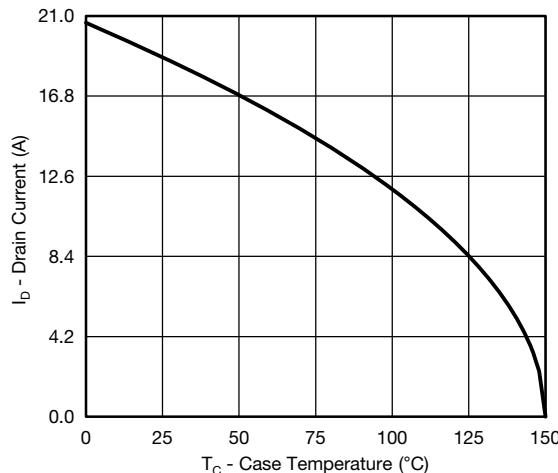
Threshold Voltage



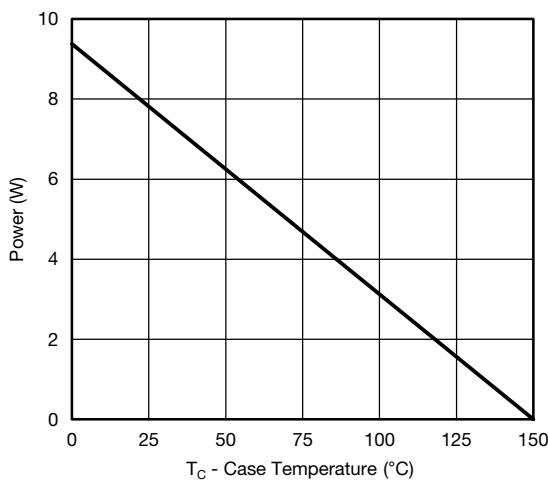
Single Pulse Power, Junction-to-Ambient



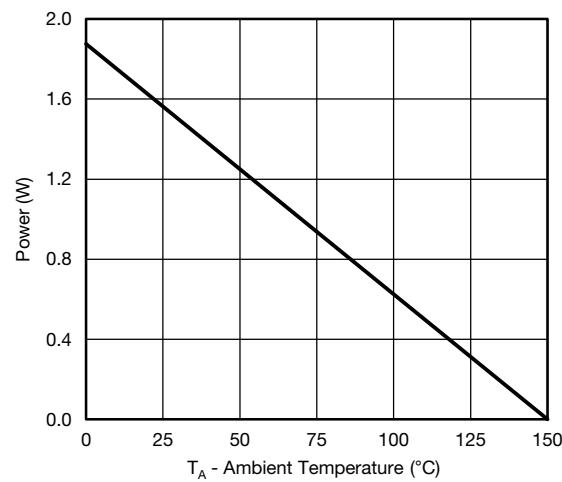
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Current Derating*



Power, Junction-to-Foot



Power, Junction-to-Ambient

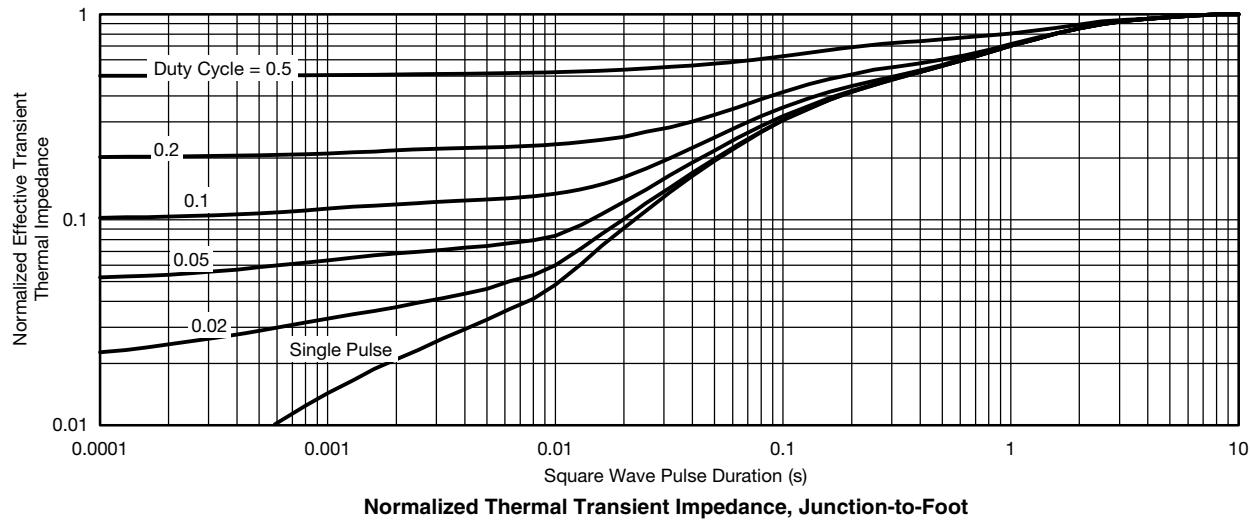
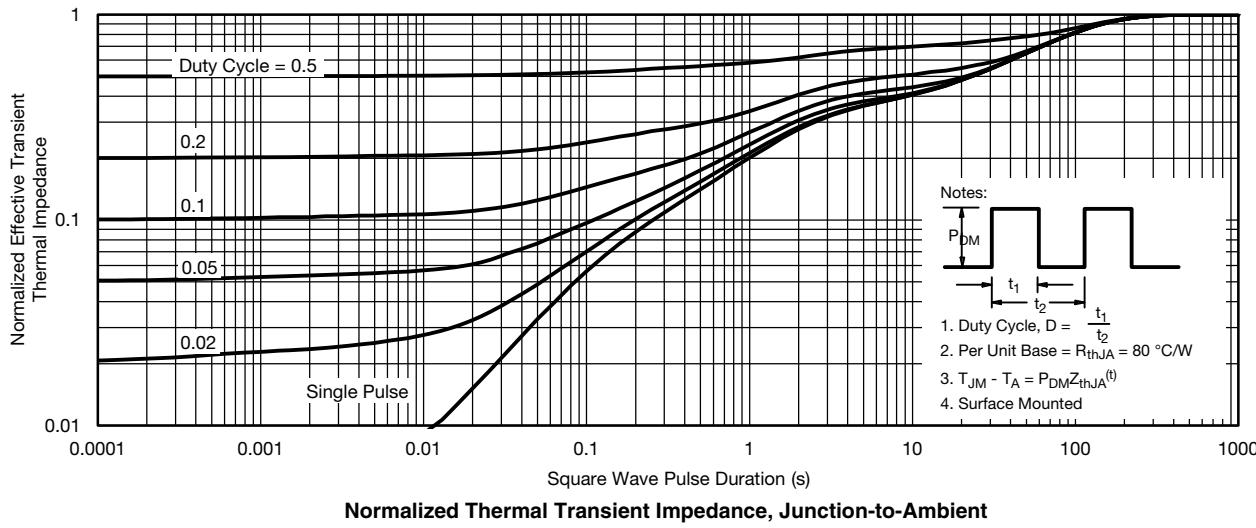
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63917.

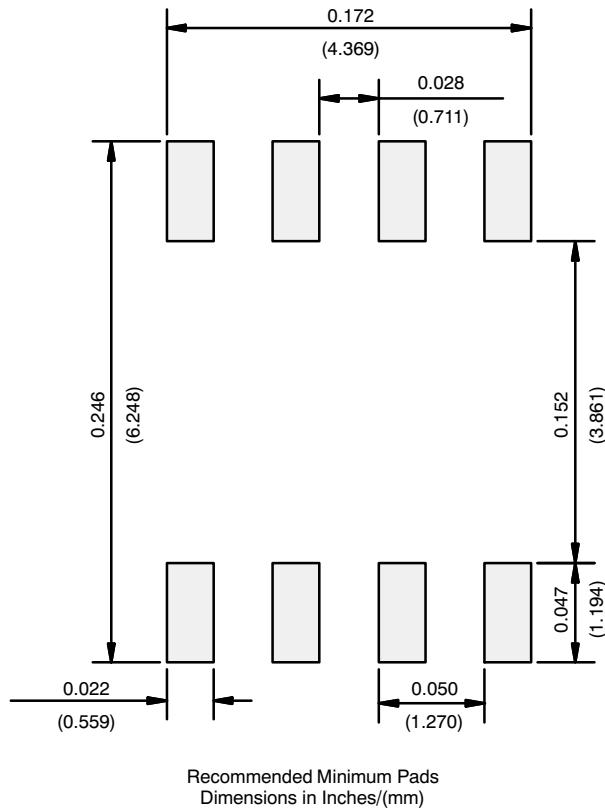
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



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