



# HMC824\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- HMC824LP6CE Evaluation Board

## DOCUMENTATION

### Application Notes

- Frequency Hopping with Hittite PLLVCOs Application Note
- PLL & PLLVCO Serial Programming Interface Mode Selection Application Note
- Power-Up & Brown-Out Design Considerations for RF PLL +VCO Products Application Note
- Wideband RF PLL+VCO and Clock Generation Products FAQs

### Data Sheet

- HMC824 Data Sheet

### User Guides

- PLLs with Integrated VCO - RF Applications Product & Operating Guide

## REFERENCE MATERIALS

### Quality Documentation

- HMC Legacy PCN: LP6CE and LP6GE QFN - Alternate assembly source
- Package/Assembly Qualification Test Report: LP6, LP6C, LP6G (QTR: 2014-00368)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

### Technical Articles

- RF/Microwave PLLs Integrate Low Noise VCOs

## DESIGN RESOURCES

- HMC824 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all HMC824 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

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## FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO, 780 - 870 MHz

### General Description

The HMC824LP6CE is a fully functioned Fractional-N Phase-Locked-Loop (PLL) with an Integrated Voltage Controlled Oscillator (VCO). The PLL consists of an integrated low noise VCO with divide-by-2 output, an autocalibration subsystem for low voltage VCO tuning, a very low noise digital Phase Detector (PD), a precision controlled charge pump, a low noise reference path divider and a fractional divider.

The fractional PLL features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and low spurious products. The phase detector (PD) features cycle slip prevention (CSP) technology to allow faster frequency hopping times. Ultra low in-close phase noise and low spurious also allows wider loop bandwidths for faster frequency hopping and low micro-phonics.

For theory of operation and register map refer to the “PLLs with Integrated VCOs - RF VCOs Operating Guide”. To view the Operating Guide, please visit [www.hittite.com](http://www.hittite.com) and choose HMC824LP6CE from the “Search by Part Number” pull down menu.

### Electrical Specifications, $T_A = +25^\circ \text{C}$

**VPPCP, VDDCP, VCC1, VCC2 = 5V  $\pm$ 4%; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3V  $\pm$ 6% GNDCP = GNDLS = Ground Paddle = 0V**

Parameter	Condition	Min.	Typ.	Max.	Units
<b>RF Output Characteristics</b>					
VCO Frequency at PLL Input		1560		1740	MHz
RF Output Frequency at $f_{VCO}/2$		780		870	MHz
RF Output Power at $f_{VCO}/2$		11	14	16.5	dBm
VCO Tuning Sensitivity	Measured at 2 GHz, 2V		15		MHz/V
VCO Supply Pushing	Measured at 2 GHz, 2V	-2		1.5	MHz/V
RF Output 2nd Harmonic			-25		dBc
RF Output 3rd Harmonic			-23		dBc
RF Output 4th Harmonic			-31		dBc
<b>RF Divider Characteristics</b>					
19-Bit N-Divider Range (Integer)	Max = $2^{19} - 1$	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
<b>REF Input Characteristics</b>					
Max Ref Input Frequency	Synthesizer phase noise can degrade by about 5dB when operating with a reference frequency near the low end of this range.	10	50	200	MHz
Ref Input Range	AC Coupled	1.5	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
<b>Phase Detector (PD)</b>					
PD Frequency Fractional Feedback Mode	[1]	0.1		100	MHz
PD Frequency Fractional Feedforward Mode (and Register 6 [17:16]= 10)		0.1		80	MHz
PD Frequency Integer Mode	[1]	0.1		125	MHz

Note 1: This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate =  $f_{vco}/20$  or 100MHz, whichever is less.


**FRACTIONAL-N SYNTHESIZER WITH  
INTEGRATED VCO, 780 - 870 MHz**
**Electrical Specifications** (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
<b>Charge Pump</b>					
Max Output Current		0.2		2.54	mA
Charge Pump Gain Step Size (5-Bits)			20		μA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-141		dBc/Hz
10 kHz	Add 1 dB for Fractional		-149		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
<b>Logic Inputs</b>					
VIH Input High Voltage		DVDD3V-0.4		DVDD3V	V
VIL Input Low Voltage		0		0.4	V
<b>Logic Outputs</b>					
VOH Output High Voltage		DVDD3V-0.4		DVDD3V	V
VOL Output Low Voltage		0		0.4	V
<b>Power Supply Voltages</b>					
Analog 3.3V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD	3.0	3.3	3.5	V
Digital Supply	DVDD3V	3.0	3.3	3.5	V
Analog 5V Supplies	VPPCP, VDDCP, VCC1, VCC2	4.8	5	5.2	V
<b>Power Supply Currents</b>					
+5V Analog Charge Pump	VPPCP, VDDCP		5.3		mA
+5V VCO Core and PLL Buffer	VCC2		56		mA
+5V VCO Divider and RF Buffer	VCC1		36		mA
+3.3V Analog	AVDD, VCCHF, VCCPS, VCCPD, RVDD		45		mA
+3.3V Digital	DVDD3V		6.5		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		μA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		10	200	μA
<b>Power on Reset</b>					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		μs
<b>VCO Open Loop Phase Noise at f<sub>vco</sub>/2</b>					
825 MHz Divide-by-2 Output	10 kHz Offset		-93		dBc/Hz
825 MHz Divide-by-2 Output	100 kHz Offset		-123		dBc/Hz
825 MHz Divide-by-2 Output	1 MHz Offset		-148		dBc/Hz
825 MHz Divide-by-2 Output	10 MHz Offset		-162		dBc/Hz
825 MHz Divide-by-2 Output	100 MHz Offset		-166		dBc/Hz
<b>Closed Loop Phase Noise PLL + VCO at f<sub>vco</sub>/2</b>					
Integer, 25 MHz PFD	1 kHz Offset		-112		dBc/Hz
Integer, 25 MHz PFD	10 kHz Offset		-116		dBc/Hz
Integer, 25 MHz PFD	100 kHz Offset		-118		dBc/Hz
Integer, 25 MHz PFD	1 MHz Offset		-146		dBc/Hz

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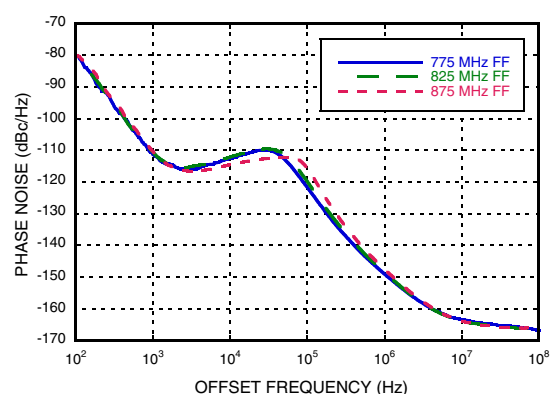


## FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO, 780 - 870 MHz

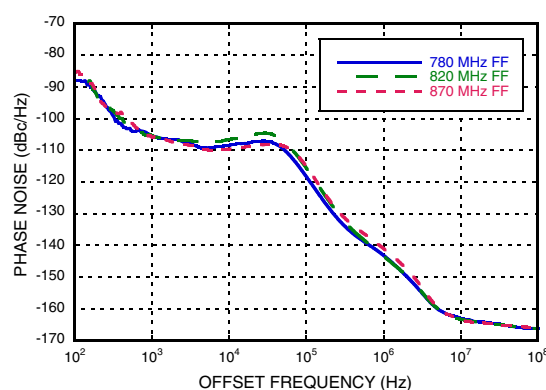
### Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
Fractional, 25 MHz PFD	1 kHz Offset		-107		dBc/Hz
Fractional, 25 MHz PFD	10 kHz Offset		-113		dBc/Hz
Fractional, 25 MHz PFD	100 kHz Offset		-115		dBc/Hz
<b>Figure of Merit</b>					
Integer Mode	Measured w/ 50 MHz PD at 30 kHz Offset		-229		dBc/Hz
Fractional Mode	Measured w/ 50 MHz PD at 30 kHz Offset		-227		dBc/Hz

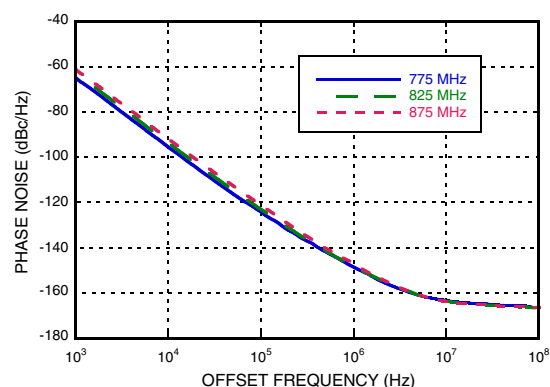
### Closed Loop Integer Phase Noise



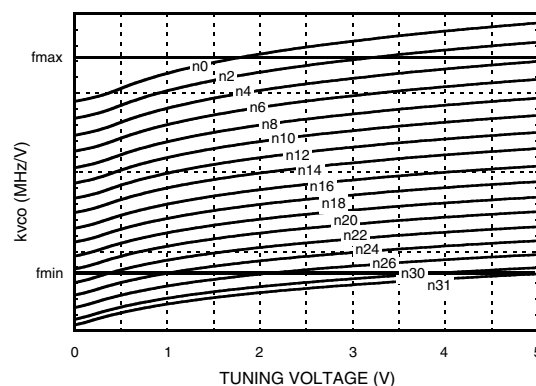
### Typical Closed Loop Fractional Phase Noise [1]



### VCO/2 Free Running Phase Noise



### Typical VCO/2 Tuning Curves vs. Switch Position



[1] Fractional Mode, 50 MHz Crystal, R=1, ~80 kHz Loop BW, (Loop filter values: Contact factory for component values) 2mA Charge Pump, -385μA Offset.

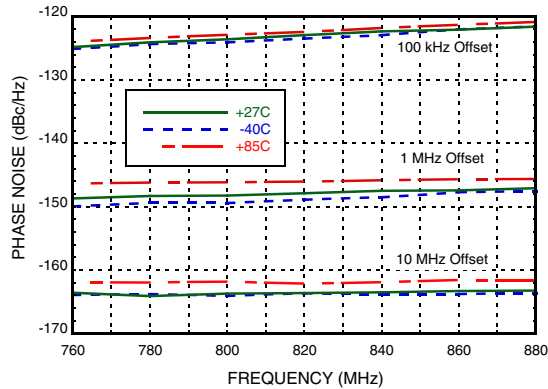
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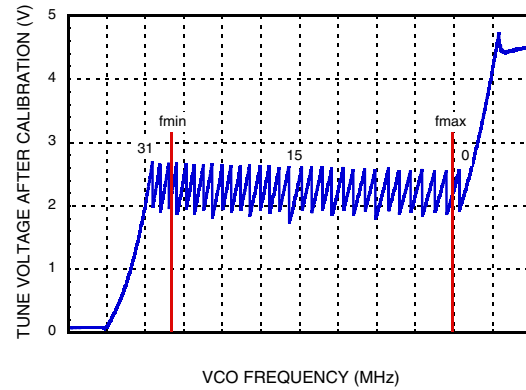


## FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO, 780 - 870 MHz

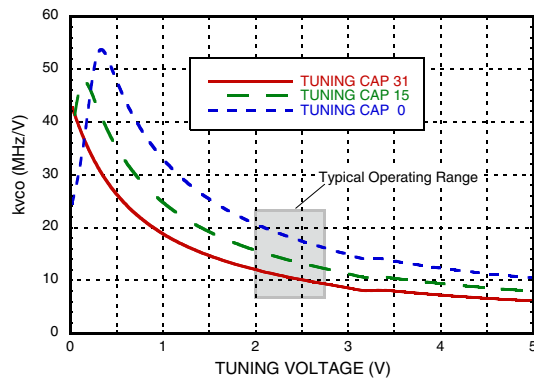
**Free Running VCO Phase Noise**  
( $V_{TUNE}$  Set by AutoCal)



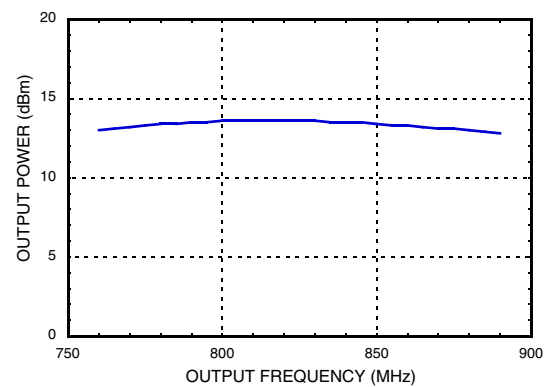
**Typical VCO Tuning Voltage After Calibration**



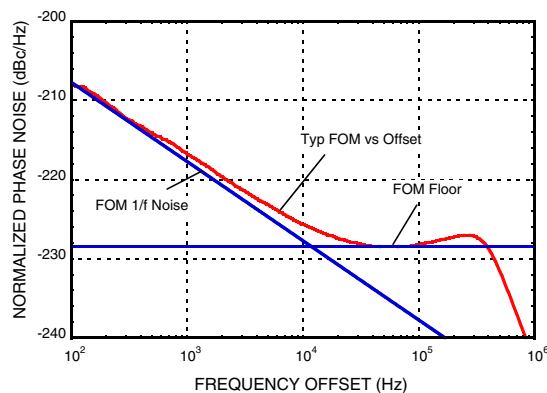
**Typical VCO Sensitivity vs. Cap @  
Fo Voltage**



**Typical Output Power - Narrow Band  
Match**



**Figure of Merit**




**FRACTIONAL-N SYNTHESIZER WITH  
INTEGRATED VCO, 780 - 870 MHz**
**Pin Descriptions**

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDCP	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	VCO Divide by 2 RF Positive Output
29	RF_P	VCO Divide by 2 RF Negative Output
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V $\pm$ 20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10G $\Omega$ meter such as Agilent 34410A, normal 10M $\Omega$ DVM will read erroneously.

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PLLS w/ INTEGRATED VCO - SMT



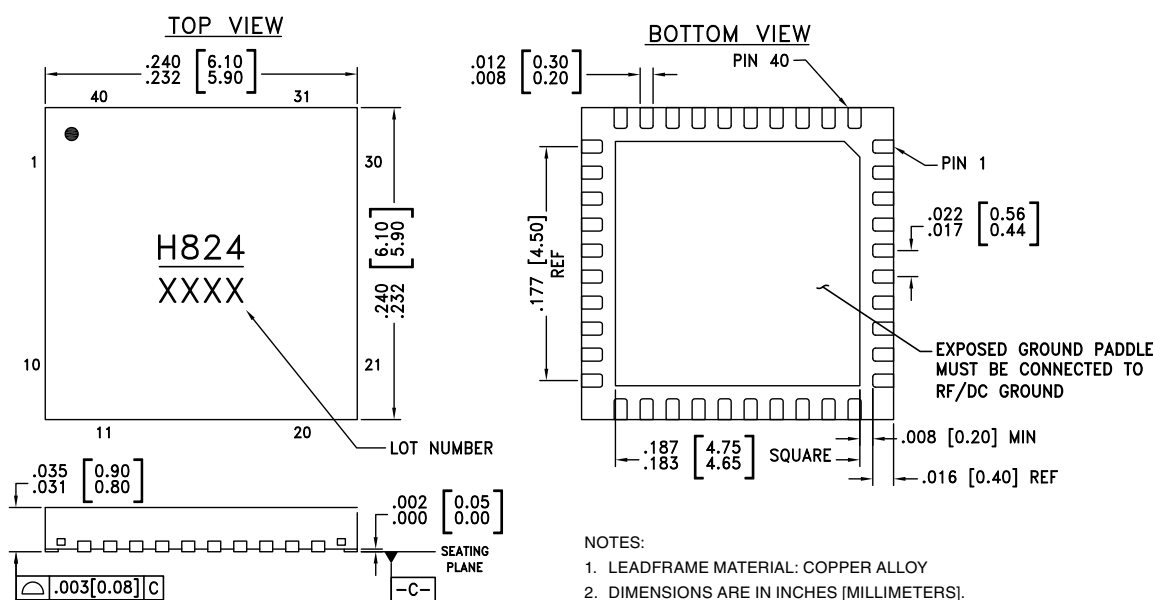
## FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO, 780 - 870 MHz

### Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDCP, VCC1	-0.3V to +5.8V
VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 125°C
Maximum Junction Temperature	125 °C
Thermal Resistance ( $R_{TH}$ ) (junction to ground paddle)	20 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Outline Drawing

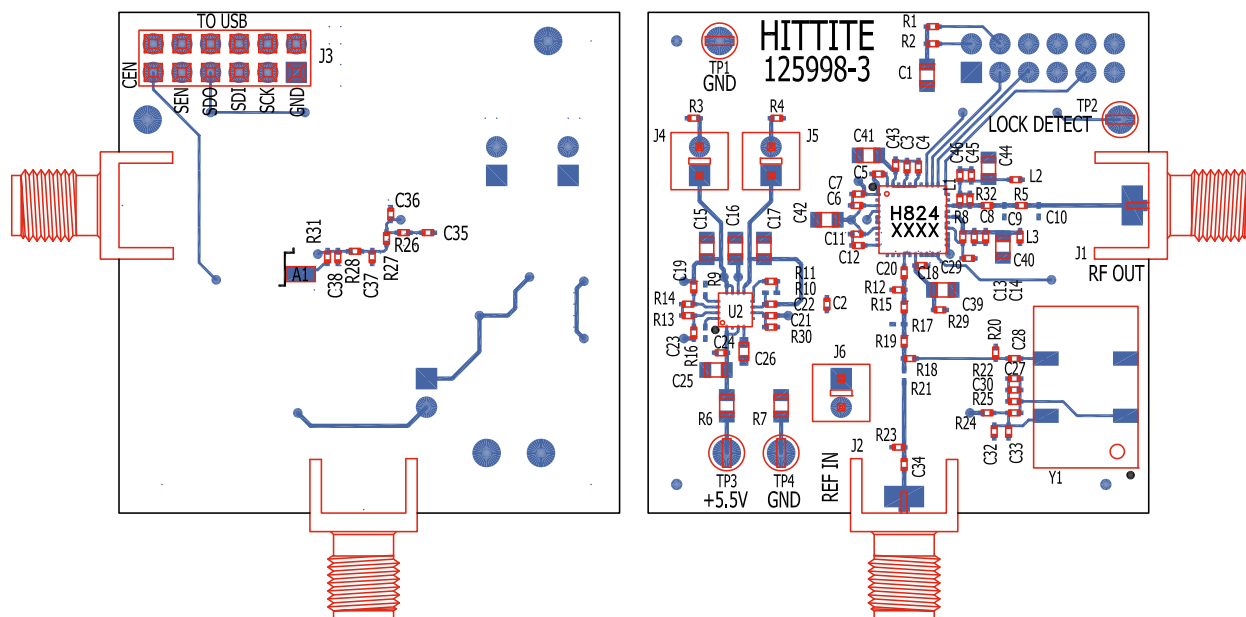






## FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO, 780 - 870 MHz

### Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

### Evaluation PCB Schematic

To view this [Evaluation PCB Schematic](http://www.hittite.com) please visit [www.hittite.com](http://www.hittite.com) and choose HMC824LP6CE from the "Search by Part Number" pull down menu to view the product splash page.


**FRACTIONAL-N SYNTHESIZER WITH  
INTEGRATED VCO, 780 - 870 MHz**
**List of Materials for Evaluation PCB 127828 <sup>[1]</sup>**

Item	Description
J1, J2	PCB Mount SMA RF Connector
J3	Dual Row Terminal Strip
J4 - J6	Connector Header
C1, C15 - C17, C25	10 $\mu$ F Capacitor, 0805 Pkg.
C2, C3, C6, C7, C11, C12, C14, C18, C27, C43, C45	0.47 $\mu$ F Capacitor, 0402 Pkg.
C4, C13	22 pF Capacitor, 0402 Pkg.
C5, C33	1000 pF Capacitor, 0402 Pkg.
C8	2.2 pF Capacitor, 0402 Pkg.
C19 - C24, C28, C30, C32, C34	0.1 $\mu$ F Capacitor, 0402 Pkg.
C26	1.0 $\mu$ F Capacitor, 0603 Pkg.
C29	47 pF Capacitor, 0402 Pkg.
C35	3300 pF Capacitor, 0402 Pkg.
C36	270 pF Capacitor, 0402 Pkg.
C37, C38	68 pF Capacitor, 0402 Pkg.
C39 - C42, C44	4.7 $\mu$ F Tantalum Capacitor, 0805 Pkg
C46	27 pF Capacitor, 0402 Pkg.
R1, R2, R5, R11, R15, R18, R19, R21, R24	Zero Ohm Resistor, 0402 Pkg.
R3, R4	1 Ohm Resistor, 0402 Pkg.
R6, R7	0 Ohm Resistor, 0805 Pkg.
R8	22 Ohm Resistor, 0402 Pkg.
R12, R20, R29	51 Ohm Resistor, 0402 Pkg.
R22, R25	20 kOhm Resistor, 0402 Pkg.
R26 - R28	1k Ohm Resistor, 0402 Pkg.
L1	12 nH Inductor, 0402 Pkg.
L2, L3	47 nH Inductor, 0402 Pkg/
TP3, TP4	Test Point PC Compact SMT
U1	HMC824LP6CE PLL with Integrated VCO
U2	HMC860LP3E Low Noise Quad Linear Regulator
Y1	3.3V, 50 MHz VCXO Crystal Oscillator
PCB <sup>[2]</sup>	125998 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR and FR4

**FRACTIONAL-N SYNTHESIZER WITH  
INTEGRATED VCO, 780 - 870 MHz****Notes:****7****PLLS w/ INTEGRATED VCO - SMT**