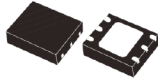
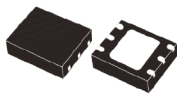


1 A very low drop voltage regulator



DFN6 (2x2)



DFN6 (3x3)

Features

- Input voltage from 2.6 to 16 V
- Very low-dropout voltage (500 mV max. at 1 A load)
- Low quiescent current (200 μ A typ. @ 1 A load)
- Available in 1% precision in DFN6 package
- 1 A guaranteed output current
- Wide range of output voltages available on request: adjustable from 0.8 V
- Logic-controlled electronic shutdown
- Power Good DFN package
- Fast dynamic response to line and load changes
- Internal current and thermal protections
- Temperature range: -40 °C to 125 °C

Applications

- Computer and laptop
- Battery-powered equipments
- Industrial and medical equipment
- Consumer and set-top box

Description

The LDF is a fast, very low drop linear regulator which operates from an input supply voltage in the range of 2.6 V to 16 V.

It is available in adjustable output voltage versions, from 0.8 V to 12 V.

The LDF features are: high output precision, very low-dropout voltage, low noise, and low quiescent current, therefore suitable for low voltage microprocessors and memory applications.

Enable logic control pin and Power Good output are featured on DFN package.

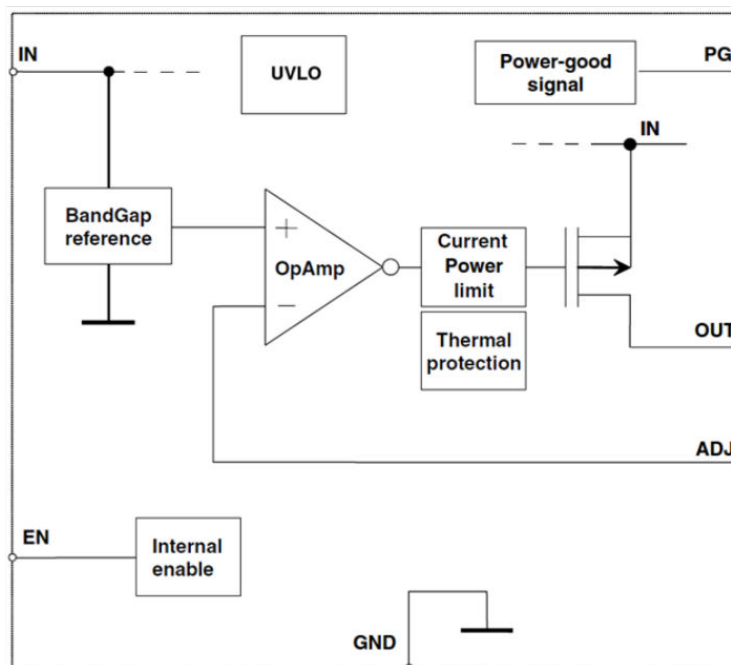
Current and thermal protection are provided.

Maturity status link

[LDF](#)

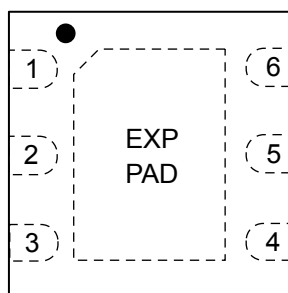
1 Block diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection (top view)



DFN6

Table 1. DFN6-2x2 and 3x3 pin description

Pin n°	Symbol	Function
2	ADJ	For adjustable versions: error amplifier input pin
6	V_{IN}	Input voltage
1	V_{OUT}	Output voltage
5	EN	Enable pin logic input: low = shutdown, high = active
3	PG	Power-good output
4	GND	Ground
Exposed pad	GND	Ground

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 20	V
V_{OUT}	DC output voltage	- 0.3 to $V_{IN} + 0.3$	V
V_{EN}	Enable input voltage	- 0.3 to $V_{IN} + 0.3$	V
V_{ADJ}	ADJ pin voltage	-0.3 to 2	V
V_{PG}	PG pin voltage	- 0.3 to $V_{IN} + 0.3$	V
I_{LOAD}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DFN6-2x2	DFN6-3x3	
R_{thJA}	Thermal resistance junction-ambient	65	55	°C/W
R_{thJC}	Thermal resistance junction-case	6.5	10	°C/W

4 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $I_{LOAD} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, unless otherwise specified.

Table 4. LDF (adjustable version) electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.6		16	V
V_{ADJ}	Reference voltage	$V_{IN} = V_{OUT} + 1\text{ V}$ ⁽¹⁾		0.8		V
	Reference voltage tolerance	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$ $I_{LOAD} = 10\text{ mA}$ ⁽¹⁾ $10\text{ mA} \leq I_{LOAD} \leq 1\text{ A}$ $T_J = -40\text{ to }125\text{ }^{\circ}\text{C}$	-1 -1.5		1 1.5	%
ΔV_{OUT}	Static line regulation	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$ Section 4: Electrical characteristics		0.01		%V
		$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$, $T_J = -40\text{ to }125\text{ }^{\circ}\text{C}$ Section 4: Electrical characteristics			0.04	
ΔV_{OUT}	Static load regulation	$10\text{ mA} \leq I_{LOAD} \leq 1\text{ A}$		0.2		%A
		$10\text{ mA} \leq I_{LOAD} \leq 1\text{ A}$, $T_J = -40\text{ to }125\text{ }^{\circ}\text{C}$		0.2	0.6	
V_{DROP}	Dropout voltage ⁽²⁾	V_{OUT} fixed to 2.5 V, $I_{LOAD} = 1\text{ A}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		200	500	mV
I_q	Quiescent current	ON mode: $V_{EN} = 2\text{ V}$ $I_{LOAD} = 10\text{ mA to }1\text{ A}$, $T_J = -40\text{ to }125\text{ }^{\circ}\text{C}$		200	800	μA
		OFF mode: $V_{EN} = \text{GND}$, PPAK and DFN versions		30		
		OFF mode: $V_{EN} = \text{GND}$, PPAK and DFN versions, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			120	
I_{SC}	Short-circuit current	$V_{IN} > 3\text{ V}$		1.5		A
V_{EN}	Enable input logic low	$V_{IN} = 2.6\text{ V to }16\text{ V}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.8	V
	Enable input logic high		2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$		5	10	μA
PG	Power-good output threshold	Rising edge		$0.92 \cdot V_{ADJ}$		V
		Falling edge		$0.8 \cdot V_{ADJ}$		
	Power-good output voltage low	$I_{SINK} = 6\text{ mA}$, open drain output		0.4		
SVR	Supply voltage rejection	$V_{IN} = 3\text{ V} \pm 0.5\text{ V}$ $V_{RIPPLE} f = 120\text{ Hz}$, $V_{OUT} = 0.8\text{ V}$		62		dB
		$V_{IN} = 3\text{ V} \pm 0.5\text{ V}$ $V_{RIPPLE} f = 120\text{ Hz to }100\text{ kHz}$ $V_{OUT} = 0.8\text{ V}$		55		
e_N	Output noise voltage	$B_w = 10\text{ Hz to }100\text{ kHz}$, $I_{LOAD} = 100\text{ mA}$ $C_{OUT} = 2.2\text{ }\mu\text{F}$		50		$\mu\text{V}_{RMS} / V_{OUT}$
T_{SHDN}	Thermal shutdown			170		$^{\circ}\text{C}$
	Hysteresis			10		

1. For $V_{OUT} < 1.6\text{ V}$; $V_{IN} = 2.6\text{ V}$.

2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.6 V.

5 Application information

5.1 External capacitors

The LDF voltage regulator requires external ceramic capacitors to assure the control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see [Section 6: Typical characteristics](#) and [Section 6: Typical characteristics](#)). Input/output capacitors should be located as closer as possible to the relative pins.

5.1.1 Input capacitor

An input capacitor, whose minimum value is 1 μF , must not be located farther than 0.5" from the input pin of the device and returned to a clean analog ground.

5.1.2 Output capacitor

Ceramic capacitors could be used on the output, provided that they must meet the minimum amount of capacitance and E.S.R. (equivalent series resistance) value required. 2.2 μF is suggested as minimum capacitance to guarantee the stability of the regulator. Anyway, other COUT values can be used according to the [Section 6: Typical characteristics](#) and [Section 6: Typical characteristics](#) showing the allowable ESR range as a function of the output capacitance. The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Besides, capacitor tolerance and temperature variation must be taken into account to assure the minimum amount of capacitance.

5.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.8 V up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider could be selected by the following equation:

$$V_{OUT} = V_{ADJ} \left(1 + \frac{R1}{R2} \right), \text{ with } V_{ADJ} = 0.8 \text{ V (Typ.)} \quad (1)$$

It is recommended to use resistors with values in the range of 10 k Ω to 100 k Ω . Lower values can also be suitable, but current consumption increases.

5.3 Enable pin operation

This pin can be used to turn OFF the regulator when it is pulled down, so to drastically reduce the current consumption. When the enable feature is not used, this pin must be tied to V_{IN} to keep the regulator output in ON state every time. To assure the proper operation, the signal source, used to drive the EN pin, must be able to swing above and below the specified thresholds listed in the electrical characteristics (V_{EN}). The EN pin must not be left floating because it is not internally pulled down/up.

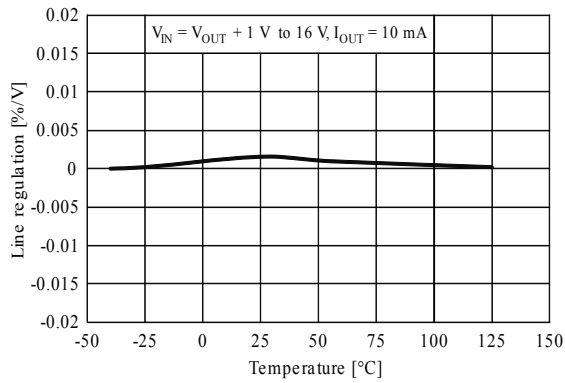
5.4 Power Good

The LDF features an open drain PG pin to sequence either external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull Power Good high when the output is within the power-good tolerance window. Typical values for this resistor range from 10 k Ω to 100 k Ω .

6 Typical characteristics

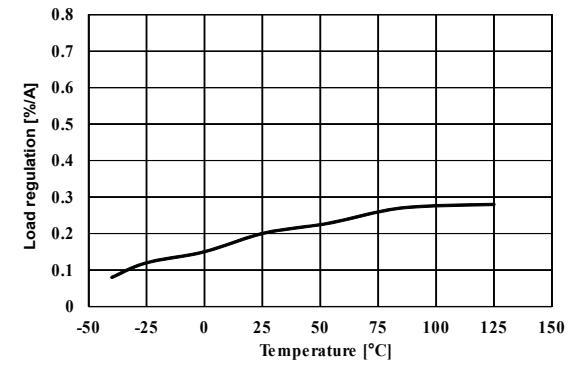
$C_{IN} = C_{OUT} = 1 \mu F$, $V_{IN} = V_{OUT} + 1 V$, V_{EN} to V_{IN} , $I_{OUT} = 10 \text{ mA}$, unless otherwise specified.

Figure 3. Line regulation vs. temperature



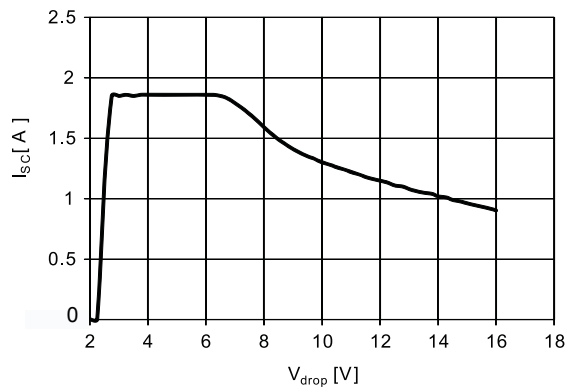
GIPD151020150845MT

Figure 4. Load regulation vs. temperature



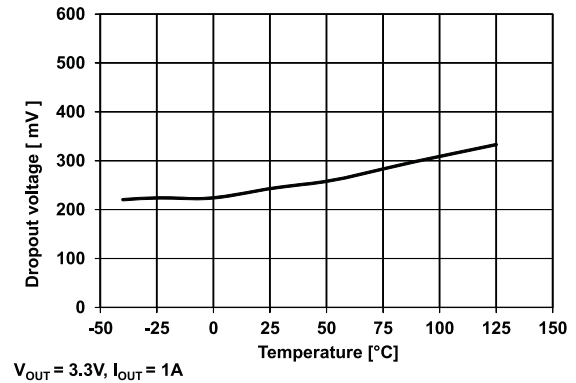
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Figure 5. Short-circuit current vs. dropout



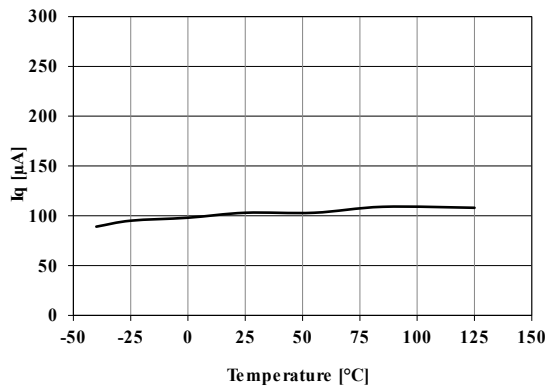
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Figure 6. Dropout voltage vs. temperature



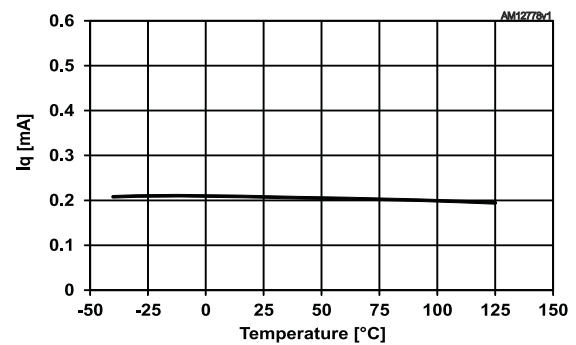
GIPD151020150940MT

Figure 7. Quiescent current vs. temperature, $I_{OUT} = 10 \text{ mA}$



GIPD151020150944MT

Figure 8. Quiescent current vs. temperature, $I_{OUT} = 1 \text{ A}$



GIPD151020150945MT

Figure 9. Shutdown current vs. temperature

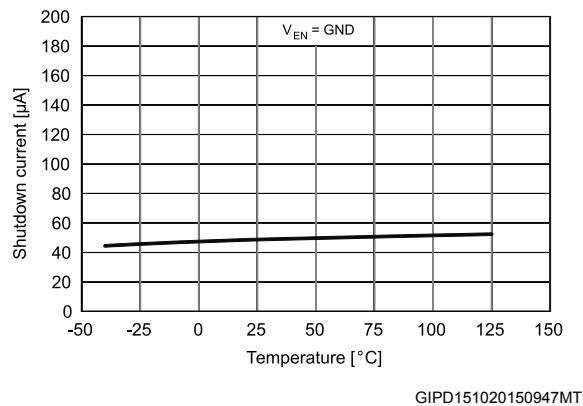


Figure 10. Enable pin current vs. temperature

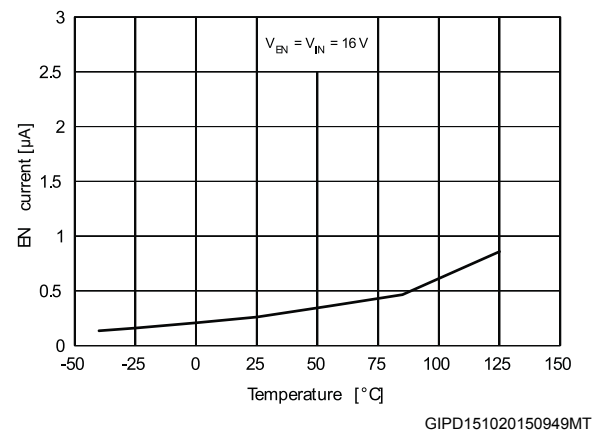


Figure 11. Enable high threshold vs. temperature

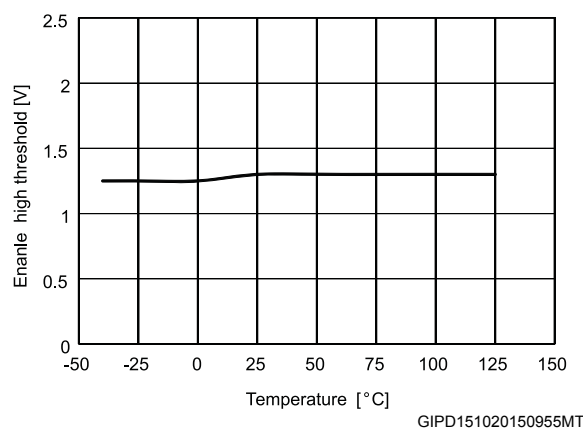


Figure 12. Enable low threshold vs. temperature

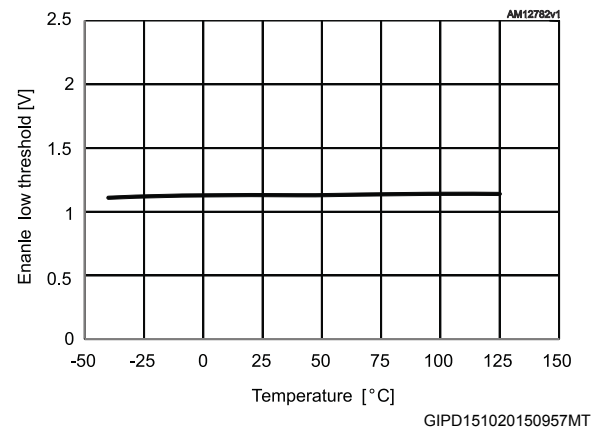


Figure 13. Output voltage vs. temperature, adjustable version

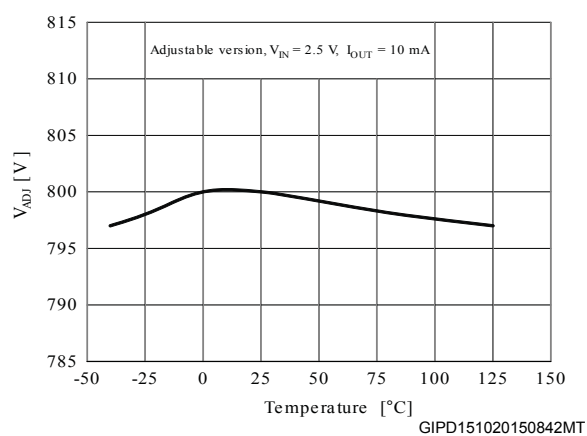
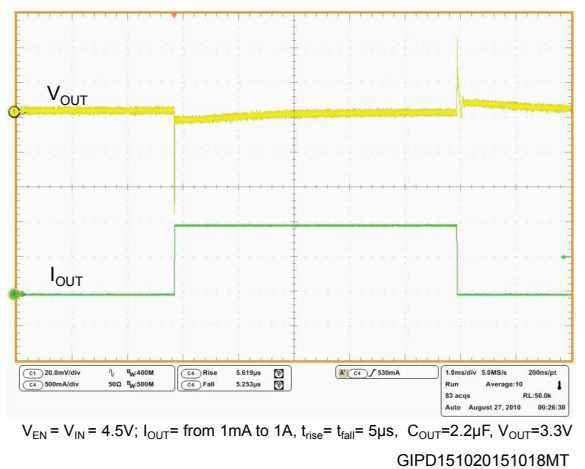
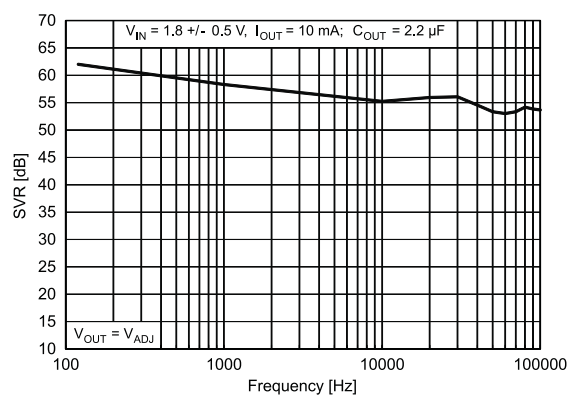
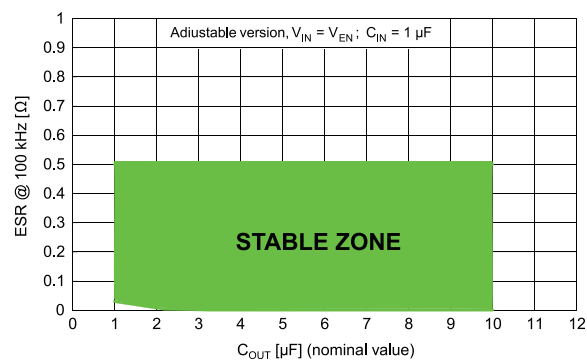

Figure 14. Load transient ($V_{OUT} = V_{ADJ}$)


Figure 15. SVR vs. frequency ($V_{OUT} = V_{ADJ}$)



GIPD151020151031MT

Figure 16. Stability plane ADJ (C_{OUT} , ESR)



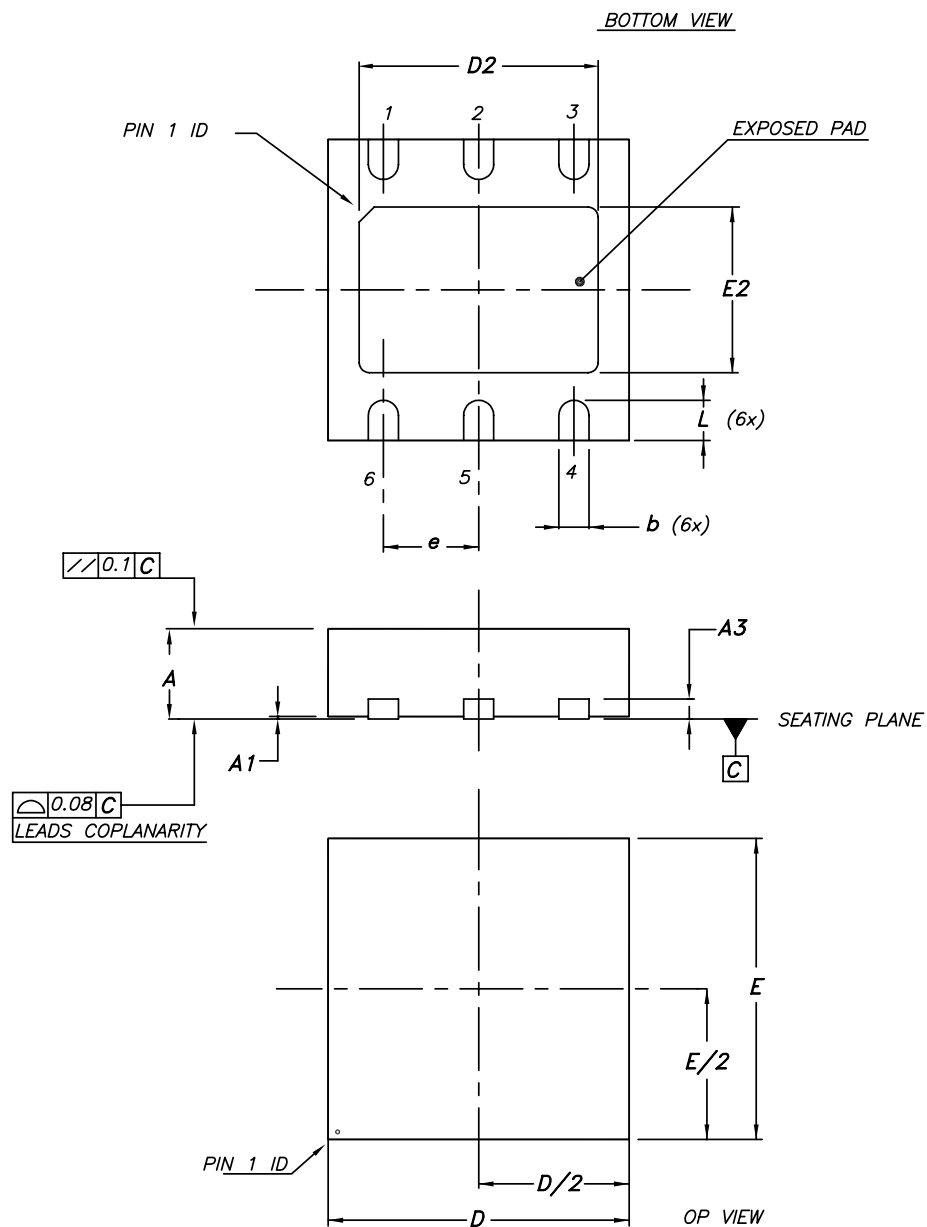
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7 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN6 (3x3) package information

Figure 17. DFN6 (3x3) package outline



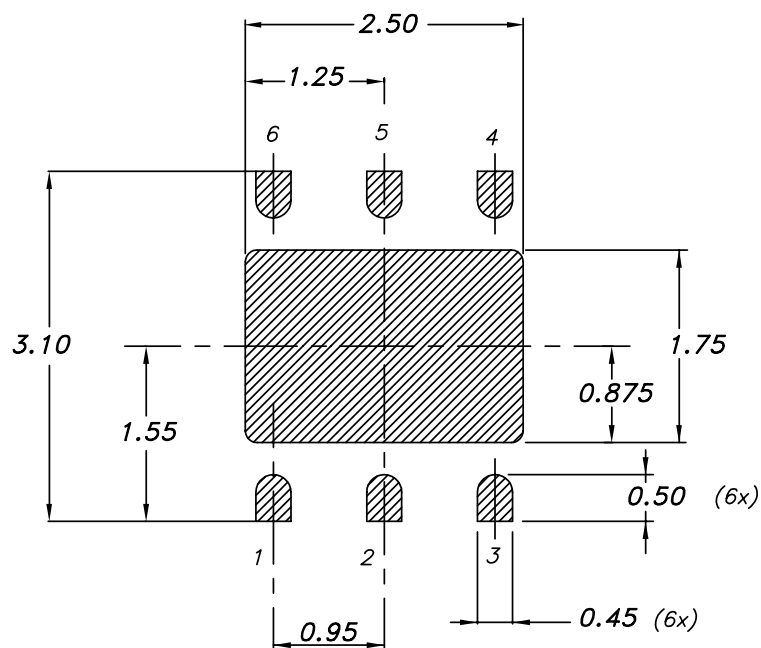
7946637_C

Table 5. DFN6 (3x3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 18. DFN6 (3x3) recommended footprint

FOOTPRINT RECOMMENDED



7946637_C

7.3 DFN6 (2x2x0,90) package information

Figure 19. DFN6 (2x2) package outline

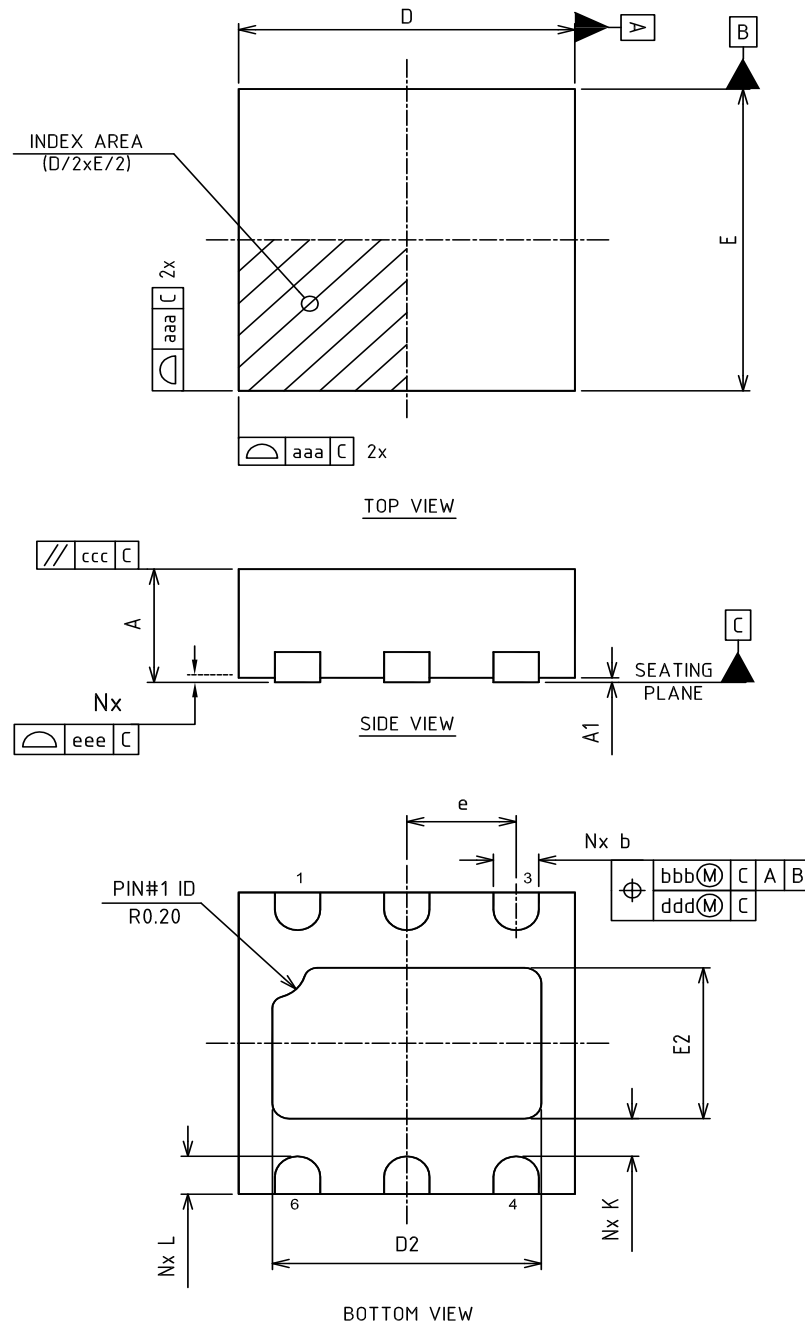
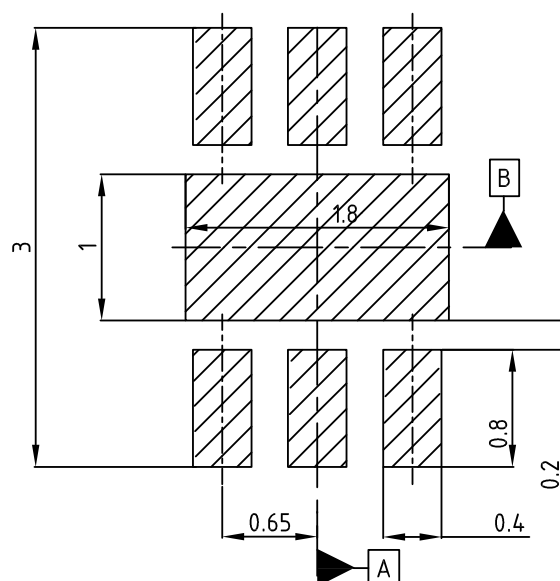


Table 6. DFN6 (2x2) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D	2.00 BSC		
E	2.00 BSC		
e	0.65 BSC		
D2	1.45		1.70
E2	0.85		1.10
L	0.20		0.30
K	0.15		
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	6		

Figure 20. DFN6 (2x2) recommended footprint



Notes:

- 1) This footprint is able to ensure insulation up to 60 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within

$\oplus$	0.02	A	B
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8518828_B

8 Ordering information

Table 7. Order code

Package		Output voltage (V)
DFN6-3x3	DFN6-2x2	
LDFPUR	LDFPVR	ADJ

Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Dec-2013	1	Initial release.
12-Apr-2017	2	Updated Figure 14: "Enable pin current vs. temperature" and Section 8: "Package information". Added Section 6.2: "Output voltage setting for ADJ version". Minor text changes.
08-Oct-2024	3	Updated Table 7 . Order code .

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