

**S1D13715**  
**Mobile Graphics Engine with Megapixel Support**

# **Hardware Functional Specification**

**Document Number: X52A-A-001-07.4**

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# 1 Introduction

## 1.1 Scope

This is the Hardware Functional Specification for the S1D13715 Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at [vdc.epson.com](http://vdc.epson.com).

We appreciate your comments on our documentation. Please contact us via email at [vdc-documentation@ea.epson.com](mailto:vdc-documentation@ea.epson.com).

## 1.2 General Description

The S1D13715 is an Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13715 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types and many extended TFT types, eliminating the need for an external timing control IC. The S1D13715, with it's 320K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory, transparent to the software application. The S1D13715 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13715 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

### 1.3 Internal Memory

The S1D13715 contains 320K bytes of internal SRAM memory. This internal memory is divided into three physical SRAM banks that contain independent arbitration logic. The boundaries between the memory banks are transparent to the user. Memory Bank1 is 64K bytes, Bank2 is 128K bytes, and Bank3 is 128K bytes.

The internal memory can be used in 5 main ways:

1. **Main Window Display Only:** 320K bytes available. If the JPEG functions and the PIP<sup>+</sup> window are not required (therefore disabled), the entire 320K bytes of memory is available for main window image storage. In this case, the image written to the main display window can either come from the Host (RGB data) over the host interface, and/or input by the camera (YUV or RGB data) through the camera interface. The Main Window Display Start Address registers (REG[0212h]-[0214h]) determines where the main window image is stored in memory. Additionally, if the main window image is being updated by a camera, the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) determines where the camera data is written and typically equals the address of the Main Window Display Start Address.
2. **Main Window and PIP<sup>+</sup> Window Display Only:** 320K bytes available. If the JPEG functions are not required (therefore disabled), the entire 320K bytes of memory is available for image storage and must be shared between the Main Window Display Image and the PIP<sup>+</sup> Window Display Image. It is recommended that the Main Window and the PIP<sup>+</sup> Window be located in different memory banks for improved performance. Since the PIP<sup>+</sup> Window is typically smaller than the Main Window, it is recommended that the PIP<sup>+</sup> Window Display Image be set to Bank1 using the PIP<sup>+</sup> Display Start Address registers (REG[0218h]-[021Ah]), and the Main Window Display Image be set to Bank2 and/or Bank3 using the Main Window Display Start Address registers (REG[0212h]-[0214h]). As in option 1, the image data for either of these windows can come from the Host or from the camera. Typically, in this setup the camera will input image data to the PIP<sup>+</sup> Window and the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) will equal the PIP<sup>+</sup> Display Start Address.
3. **JPEG Functions Enabled:** 288K bytes - JPEG FIFO size available. If either the JPEG Encoder or Decoder is used, segments of Bank1 and Bank3 are automatically reserved for JPEG use only. The JPEG FIFO uses Bank1 and its size is configurable from 4K bytes to 64K bytes using the JPEG FIFO Size bits (REG[09A4h] bits 3-0). The JPEG FIFO starts at address 0 of Bank1 and is accessed using the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO is used as an interface between the JPEG module and the HOST. When the S1D13715 is encoding a JPEG image, the JPEG FIFO stores JPEG data for the HOST to read. When the S1D13715 is decoding a JPEG file, the JPEG FIFO stores incoming JPEG data from the HOST. The size of the JPEG FIFO should be set to optimize performance based on the HOST operating speed, S1D13715 operating speed, and the size of the JPEG image. The JPEG Line Buffer uses the upper 32K bytes of Bank3, from 48000h - 4FFFFh. During an encode operation, the JPEG Line Buffer is used to organize incoming YUV data from the

camera and send it to the JPEG Encoder. During a decode operation, the JPEG Line Buffer organizes the YUV data output of the JPEG decoder to be sent to the View Resizer and YUV/RGB Converter for display on the LCD panel.

4. **YUV Data Output:** 288K bytes - JPEG FIFO size available. If YUV data from the camera is directly sent to the HOST, the JPEG Codec is bypassed, however the JPEG FIFO and JPEG Line Buffer are still utilized. The JPEG FIFO and JPEG Line Buffer are used as described for the decode operation in option 3 (JPEG Functions Enabled).
5. **YUV Data Input:** 288K bytes available. If YUV data from the Host is sent directly to the S1D13715, the JPEG Codec and JPEG FIFO are bypassed. YUV data is written directly to the JPEG Line Buffer. In this mode, the JPEG Line Buffer is accessed using the JPEG Line Buffer Write Port register (REG[09E0h]). The JPEG Line Buffer then sends the YUV data to the View Resizer and the YUV/RGB Converter for display on the LCD panel.

All data stored in the internal memory that is intended for display on the LCD panel, must be stored in RGB format. YUV data from the camera interface or from the HOST must be converted to RGB by the YUV/RGB Converter. Color depth data formats of 8/16/32 bit-per-pixel are supported.

## 1.4 Host CPU Interface

The S1D13715 supports four CPU Host interfaces with 16-bit wide data buses. Each interface can support little or big endian data formats, direct or indirect addressing, and the option to use a wait signal or not. See Section 5.4, “Summary of Configuration Options” on page 43 for a description on how to configure the S1D13715 for these various options. In addition to these four CPU Host interfaces, the S1D13715 also has a serial CPU port which allows the CPU Host to directly control a serial LCD panel connected to the S1D13715.

The Host CPU that is used to connect to the S1D13715 must meet all specified timing parameters for the Host interface being used, as shown in Section 7.3, “Host Interface Timing” on page 60.

It is recommended that the WAIT# signal be used for all host interfaces as this will ensure that the highest performance is achieved when accessing the S1D13715. When this mode is selected, the WAIT# signal is only asserted when needed (i.e. the S1D13715 cannot accept or present data immediately). If the WAIT# signal is not used, the CPU must guarantee that all cycles meet the maximum cycle length as shown in Table 7-46: “Wait Length,” on page 91.

### 1.4.1 Direct Addressing Host Interfaces

The direct addressing host interfaces (Direct 80 Type 1, Direct 80 Type 2, Direct 80 Type 3, and Direct 68) are generic asynchronous CPU interfaces that provide addressing along with the data in one transfer. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used to connect to the external memory bus of the host CPU and offer the highest performance when accessing the S1D13715.

The direct addressing host interfaces also have the ability to combine the S1D13715 registers and internal memory into one contiguous memory segment or into separate memory segments. In the contiguous mode (1 CS# mode), only one chip select is used to select the S1D13715 on the host bus. Memory and register accesses are differentiated by the M/R# pin which is typically connected to address pin A19 of the host CPU bus. In the separate memory mode (2 CS# mode), two chip selects select the S1D13715. One chip select is used for memory accesses and the other is used for register accesses. In this mode, the host CPU can be programmed to assign different memory spaces for the memory and registers of the S1D13715.

### 1.4.2 Indirect Addressing Host Interfaces

The indirect addressing host interfaces (Indirect 80 Type 1, Indirect 80 Type 2, Indirect 80 Type 3, and Indirect 68) are generic asynchronous CPU interfaces that provide addressing and data in two separate transfers. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used when the address and data lines of the host CPU are multiplexed together and two transfers are needed to complete a data transfer.

### 1.4.3 Serial Port Interface for Serial LCD Control

The S1D13715 also supports a Serial Host Interface that is used to directly control a serial LCD panel connected to the S1D13715. This bypass mode is controlled by the Serial Port Bypass Enable bit (REG[0032h] bit 8). Typically, this interface is used when the S1D13715 is in power save mode and a serial LCD panel is required to show an image such as a status display.

## 1.5 LCD Controller

The S1D13715 Mobile Graphics Engine contains a versatile LCD controller which supports many LCD panel types and offers a rich feature set. The S1D13715 has three LCD interface modes where either one or two LCD panels (referred to as LCD1 and LCD2) can be connected to the S1D13715. These modes are selected using the Panel Interface bits (REG[0032h] bits 1-0). LCD1 and LCD2 each have their own vertical and horizontal LCD panel size setting and other specific features, in order to easily switch from the LCD1 panel display to the LCD2 panel display or vice versa.

In Mode 1, LCD1 is defined as a TFT RGB type LCD panel. The various TFT LCD panel types supported are listed in Table 10-12: “RGB Panel Type Selection,” on page 151 and are selected using the RGB Panel Type bits (REG[0032h] bits 15-10). LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 2, LCD1 is defined as a parallel interface LCD panel with integrated RAM to store the image data. LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 3, LCD1 and LCD2 are both defined as parallel interface LCD panels with integrated RAM to store the image data.

In Mode 4, LCD1 is defined as a TFT RGB type LCD panel. The various LCD panel types supported are listed in Table 10-12: “RGB Panel Type Selection,” on page 151 and are selected using the RGB Panel Type bits (REG[0032h] bits 15-10). LCD2 is defined as a parallel interface LCD panel with integrated RAM to store the image data.

In each mode, only one display (LCD1 or LCD2) at a time can be the active display. A typical application for using two separate LCD panels would be a clamshell type cellular phone where there is a main display and a smaller status display on the outside of the phone. LCD1 would be the main display and LCD2 would be the small status display, typically a serial interface LCD panel. Two images would be stored in the internal memory of the S1D13715 for each LCD display. When each display is selected as active, (LCD1 when the cellular phone is open and LCD2 when the cellular phone is closed) the correct image to be displayed is selected using the Main Window Display Start Address registers (REG[0210h]-[0212h]).

For LCD Interface Pin Mapping refer to Table 5-12: “LCD Interface Pin Mapping for Mode 1,” on page 46 and Table 5-13: “LCD Interface Pin Mapping for Modes 2/3,” on page 47.

### 1.5.1 RGB LCD Interface

The RGB LCD interface supports a wide range of TFT panels. TFT panels that can be programmed via various serial type interface are also supported and are selected with the LCD1 Serial Data Type bits (REG[0054h] bits 7-5). If this type of panel is connected to LCD1, the RGB Panel Type must be set to the General TFT, ND-TFT setting.

The RGB LCD panel data bus width is selectable to support 9/12/16/24-bit panels using the RGB Interface Panel Data Bus Width bits (REG[0032h] bits 6-4). Other configurable options include non-display period times and polarity, width, and position of control signals.

### 1.5.2 Parallel LCD Interface

The Parallel LCD Interface supports multiple output data formats, providing the flexibility to support various RAM integrated Parallel Interface LCD panels. If a parallel panel is connected to LCD1, the LCD1 Parallel Data Format bits (REG[0056h] bits 2-0) are used to program the output data format, otherwise the LCD2 Parallel Data Format bits (REG[005Eh] bits 2-0) are used.

The LCD panel image can be updated in three different ways. Manual Transfer is accomplished by setting REG[003Ah] bit 1 = 1 which sends one frame of panel data to the Parallel LCD panel. LCD Module VSYNC Manual Transfer mode synchronizes a manual frame transfer to an external VSYNC signal sent by the parallel LCD panel. The VSYNC Input Enable bit for either LCD1 or LCD2 (REG[0056h] bit 7 or REG[005Eh] bit 7) must be set to enable this mode. The last transfer method is Automatic Transfer which sends frames to the LCD panel whenever a camera vertical sync signal is detected. If the VYSNC Input mode is also enabled, an external LCD panel VSYNC must also be detected. Automatic Transfer mode is enabled by setting REG[003Ch] bit 1 = 1. Automatic Transfer mode is intended for displaying a camera image on a serial or parallel interface LCD panel without the need to manually update the panel display.

### 1.5.3 Serial LCD Interface

The Serial LCD Interface supports serial type LCD panels only on LCD2. Serial Data Type, Data Direction, Data Format, and Serial Clock Phase and Polarity are all selectable and are controlled in the LCD2 Serial Interface Setting register (REG[005Ch]). Serial Interface Panels are updated with image data as described in Section 1.5.2, “Parallel LCD Interface” on page 16.

## 1.6 Display Features

The S1D13715 contains display features that enhance the functionality of the Mobile Graphics Engine. These features are Picture-in-Picture Plus (PIP<sup>+</sup>), Overlay, SwivelView, Mirror, and Pixel Doubling.

PIP<sup>+</sup> is a sub-window within the Main Window and typically is used to display the camera image or a decoded JPEG image. PIP<sup>+</sup> can be used with the overlay functions so that only the part of the PIP<sup>+</sup> window that overlaps the overlay color in the Main Window is displayed (according to the overlay function selected). Various overlay functions can be employed such as transparency, averaging, ANDing, ORing, and Inverting. Multiple overlay functions can be enabled, but only the overlay function with the highest priority is processed.

SwivelView is a hardware rotation of the display image by either 90, 180, or 270 degrees. By processing the rotation of the image in hardware, SwivelView offers a performance advantage over software rotation. SwivelView can be used to support portrait sized panels mounted in a landscape orientation or vice versa.

Mirror can be used to mirror the image in either the PIP<sup>+</sup> window display, Main Window display, or both. A typical application for mirroring is to support swivelling on a clamshell phone. When the large display is on the outside of the phone and the camera is pointing at the user, mirroring allows the camera image to be displayed properly.

Pixel Doubling is a feature that can be used to double the size of an image in either the PIP<sup>+</sup> window display, Main Window display or both. Typical applications for pixel doubling include increasing the displayed size of a decoded JPEG image or using a larger panel size than is supported natively by an operating system. For example, if a 320x320 resolution panel is used with an OS that supports only a main display of 160x160 (such as in many PDAs), pixel doubling can be enabled to utilize the whole display.

## 1.7 Camera Interface

The S1D13715 supports two 8-bit parallel Camera Interfaces. Only one camera interface can be active at a given time. The input data format supported is YUV 4:2:2. Embedded sync signals, as defined by the ITU-R BT656 standard, are also supported. A clock is supplied to the camera from the camera interface (CM1CLKOUT or CM2CLKOUT) and the camera in turn outputs YUV data, horizontal and vertical sync signals, and a pixel clock that the S1D13715 camera interface uses to sample the incoming YUV data. The CMxCLKOUT frequencies are controlled by the Camera1 Clock Divide Select bits (REG[0100h] bits 3-0) and Camera2 Clock Divide Select bits (REG[0104h] bits 3-0). The output control of these two clocks is controlled by REG[0110h] bit 0. The camera interface supports various types of YUV cameras by allowing the selection of different formats of YUV 4:2:2 signals. Features such as YUV Data Format, YUV Data Range, HSYNC and VSYNC polarity, and Camera Pixel Clock Input Polarity are all selectable.

Since the Camera Pixel Clock can be, at most, 1/3 the S1D13715 System Clock, the frames per second of the camera image displayed on the LCD display is dependant on the internal speed of the S1D13715. For example, a setting of 54MHz for the System Clock results in the camera returning a Pixel Clock of 6.5MHz when the S1D13715 Camera Clock Out Divide is set to a divide of 4 (typical cameras use a divide by 2 of the input clock to generate the pixel clock). For CIF resolutions (352x288), this translates into 29 fps. For a Camera Clock Out Divide of 2 and VGA resolutions (640x480), 21 fps is achieved.

In addition to the main function of the two camera interfaces, other video functions are supported. For the Camera Interface Pin Mappings refer to Section 5.7.1, “Camera1 Interface Pin Mapping” on page 52 and Section 5.7.2, “Camera2 Interface Pin Mapping” on page 52.

## 1.8 Resizers and YUV/RGB Converter

There are two resizers in the S1D13715: the view resizer and the capture resizer. Both resizers can be used to resize (crop) and/or scale incoming YUV data from the camera interface, from the JPEG Decoder, or from the Host CPU in YUV bypass mode. Once the YUV data has been resized and scaled, it gets converted to RGB data by the YUV/RGB Converter (YRC), so that it can be displayed on the LCD panel. The location in memory where the YRC writes the RGB data is defined by the YUV/RGB Converter Write Start Address registers (REG[0242h]–[0244h]). The output bpp of the YRC must match either the Main Window color depth (bpp) or the PIP<sup>+</sup> Window color depth (bpp) setting, depending on which window the image is being displayed in. The YRC color depth (bpp) output is controlled by the YRC Output Bpp Select bits (REG[0240h] bits 11–10). The resizers can support a maximum image size up to 2048 x 2048 pixels.

Although each resizer can be configured to be the source for the YRC using the Output Source Select bit (REG[0940h] bit 3), typically the view resizer is set as the source since only the capture resizer can be the source for the JPEG Encoder or for YUV bypass mode to the Host CPU. A typical application has the view resizer resizing the camera data and has the YRC converting it for display on the LCD panel, while the capture resizer is used to send camera YUV data for JPEG encoding or for raw storage by the Host CPU. When the desired viewed camera image is the same dimensions as the desired captured JPEG or YUV image, only the capture resizer needs to be used.

### Note

Only the view resizer can be used to resize YUV data from the JPEG Decoder or from the Host CPU.

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## 1.9 JPEG Encoder / Decoder

The S1D13715 contains a full JPEG Codec capable of encoding an incoming camera data stream or decoding a JPEG image sent from the Host CPU.

### 1.9.1 Encoder

Either the YUV data stream from the camera interface or the display buffer memory via the RGB to YUV Converter can be encoded into a JPEG image. The YUV data from the capture resizer is organized into 8 x 8 blocks in the JPEG Line Buffer, as required for JPEG processing, and then sent to the JPEG Encoder. As the JPEG Encoder is encoding the YUV data, it starts filling up the JPEG FIFO with JPEG data. This data must be read by the Host CPU before the JPEG FIFO overflows. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO can be set as large as 128K bytes and typically this will be large enough to contain the whole JPEG image. A smaller JPEG file size can be achieved using the capture resizer's trimming and scaling functions or a higher JPEG compression ratio can be achieved by using different Quantization and Huffman Tables.

As mentioned in Section 1.3, "Internal Memory" on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Encoder can encode YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats and will convert the incoming YUV data to the desired format. This encoding option is set by the YUV Format Select bits (REG[1000h] bits 1-0). The JPEG file size can be reduced if a smaller UV:Y ratio format is used.

The intended use of the JPEG Encoder is to "take a snapshot" of the currently viewed camera image or display image, or to encode YUV data sent by the Host CPU. This JPEG image is then downloaded to the Host CPU through the JPEG FIFO and stored as a JPEG file.

### 1.9.2 Decoder

The S1D13715 contains a JPEG Decoder which allows the Host CPU to send a JPEG image file for conversion and display on the LCD panel, or to send the resulting YUV decoded data back to the Host CPU. The incoming JPEG data is written to the JPEG FIFO and then goes to the JPEG Decoder for decoding into YUV format. The YUV format output is based on the original format the JPEG file was encoded from and is reported in the YUV Format Select bits (REG[1000h] bits 1-0). The output of the JPEG Decoder goes to the JPEG Line Buffer which then organizes the 8 x 8 blocks of YUV data into the correct YUV format and sends this data to the view resizer. The view resizer can trim and scale the image and then it is converted by the YRC to be displayed on the LCD panel or sent to the Host CPU.

While writing the JPEG data to the JPEG FIFO, the Host CPU may be interrupted. When this happens, the JPEG Decoder completes decoding the data stored in the JPEG FIFO and then waits for more data from the Host CPU. The decode operation will continue until the

JPEG Decoder detects the End-of-File Marker. The JPEG FIFO must not be overflowed by the Host CPU. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]).

As mentioned in Section 1.3, “Internal Memory” on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Decoder can decode YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats.

### 1.10 2D BitBLT Engine

The purpose of the 2D BitBLT Engine is to improve the overall system performance by off-loading the work of the Host CPU in moving display data between the CPU and display memory. There are five BitBLTs (Bit Block Load Transfer) that can move display data from one location to another. Additionally, data functions can be performed that manipulate the source and/or destination data. For more information on the 2D BitBLT Engine, see Section 16, “2D BitBLT Engine” on page 344.

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## 2 Features

### 2.1 Internal Memory

- Embedded 320K byte SRAM memory used for:
  - Display Buffer
  - JPEG FIFO
  - JPEG Line Buffer

### 2.2 Host CPU Interface

- Four generic asynchronous CPU interfaces
- 16-bit data bus
  - 16-bit register and FIFO access
  - 8/16-bit display buffer access
- Direct / Indirect addressing
- Little / Big endian support
- Registers are memory-mapped
  - M/R# input selects between memory and register address space
  - M/R# and CS# inputs select between memory and register address space in 2 CS# mode
- CPU serial port for direct control of a serial LCD
- CPU parallel port for direct control of a parallel LCD

### 2.3 Display Support

- Active Matrix TFT displays: 9/12/18/24-bit interface
  - Extended TFT interface (Type 2 and Type 5)
  - TFT with u-Wire interface
  - a-Si TFT interface
  - Epson ND-TFD interface
- ‘Direct’ support for the Casio TFT LCD (or compatible interfaces)
- ‘Direct’ support for a-TFT Samsung TFT LCD (or compatible interfaces)
- ‘Direct’ support for the Sharp HR-TFT LCD (or compatible interfaces)

- ‘Direct’ support for Toshiba low power LCDs. Contact your Epson sales representative for details.
- 8/9-bit serial interface LCDs with integrated RAM
- 8/16/18/24-bit MPU parallel interface LCDs with integrated RAM
- Supports a maximum of 2 panels (LCD1 and LCD2 can’t be refreshed simultaneously)

## 2.4 Display Modes

- Supports three panel interface modes which each allow two LCDs (LCD1 and LCD2) to be connected to the S1D13715. Only one LCD can be active at a time.
  - Mode 1:
    - LCD1: RGB type panel
    - LCD2: Serial interface panel
  - Mode 2:
    - LCD1: Parallel interface panel
    - LCD2: Serial interface panel
  - Mode 3:
    - LCD1: Parallel interface panel
    - LCD2: Parallel interface panel
  - Mode 4:
    - LCD1: RGB type panel
    - LCD2: Parallel interface panel
- Host CPU can directly control serial interface panels on LCD2
- Host CPU can directly control parallel interface panels on LCD1 or LCD2
- 8/16/32 bit-per-pixel (bpp) color depths
- Separate Look-up Tables (LUTs) for the Main Window and the PIP<sup>+</sup> Window
- LUTs can be bypassed

## 2.5 Display Features

- Overlay functions
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Mirror Display: provides a “mirror” image of the display
- Virtual display support: displays images larger than the panel size through the use of panning and scrolling
- Picture-in-Picture Plus (PIP<sup>+</sup>): displays a variable size window overlaid over background image
- Pixel Doubling
- Video Invert: Data output to the LCD is inverted

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## 2.6 Camera Interface

- 2-port Camera Interface (only one camera interface can be used at a time)
- Supports YUV 4:2:2 format
- Supports ITU-R BT.656 format
- 8-bit data bus (YUV Multi Out)
- MPU type interface camera support on Camera1 interface
- MPEG Codec input interface support on Camera2 interface
- Strobe control function

## 2.7 Digital Video Features

- Hardware JPEG codec based on the JPEG baseline standard
  - JPEG Encode supports YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - JPEG Decode supports YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - Arithmetic accuracy satisfies the compatibility test of JPEG Part-2
  - Software control of image size
  - Maximum horizontal image size for JPEG encoding (YUV 4:2:2 format: up to 2880 pixels)
- Two resizers: View resizer receives YUV data from the camera interface, or from the JPEG decoder, or from the Host CPU. Capture resizer receives YUV data only from the camera interface.
  - YUV Data can be resized (trimmed and scaled) then:
    - Converted to RGB data for display on the LCD
    - Converted to JPEG data and read by the CPU Host via the JPEG FIFO
    - Read by the Host CPU directly (YUV format)
- YUV to RGB Converter (YRC): YUV data from the View Resizer or Capture Resizer is converted to RGB format to be displayed on the LCD.

## 2.8 Picture Input / Output Functions

- The YUV data (YUV 4:2:2 format) from Camera Interface can be:
  - Stored in the display buffer after resizing and conversion to RGB format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and conversion to YUV (format 4:2:2 or 4:2:0).

- The JPEG file downloaded from the Host CPU can be:
  - Decoded by the internal JPEG decoder, resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Decoded by the internal JPEG decoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- YUV data (format 4:2:2 or 4:2:0) downloaded from the Host CPU can be:
  - Resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Encoded by the internal JPEG encoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- RGB data in the display buffer can be:
  - Converted to YUV, then transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.

## 2.9 2D BitBLT Acceleration

- 2D BitBLT engine including: (this function does not support 32bpp modes)
  - Move BitBLT
  - Transparent Move BitBLT
  - Solid Fill BitBLT
  - Read BitBLT
  - Pattern Fill BitBLT

## 2.10 Clock

- Internal PLL driven by a single external reference clock, 32.768KHz
- 40 - 55MHz PLL output
- PLL bypass mode for external clock input

## 2.11 Power Save

- Software initiated power save mode
- Software initiated display blank

## 2.12 Miscellaneous

- General Purpose Input/Output pins are available

### 3 System Diagrams

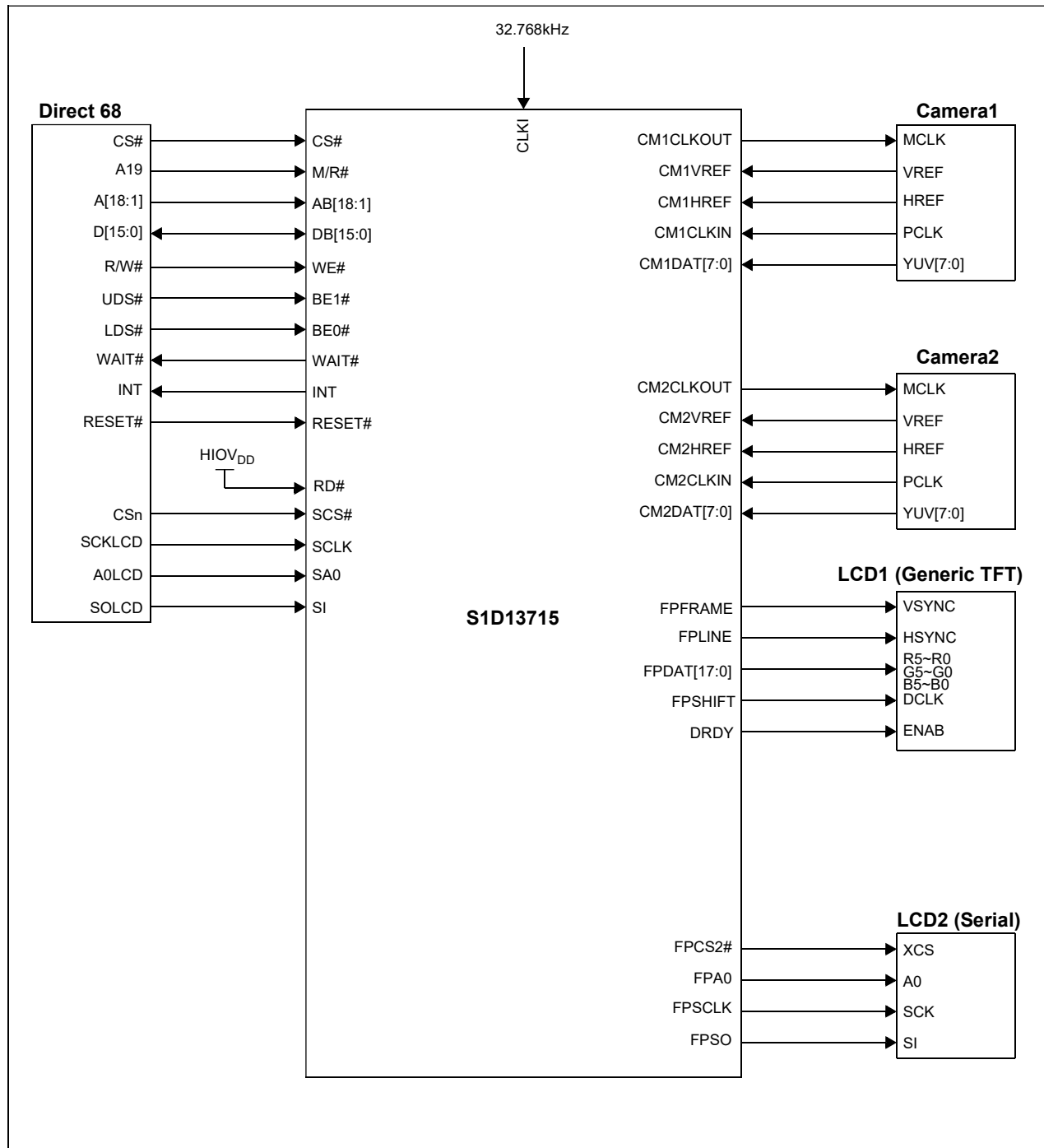


Figure 3-1: S1D13715 System Diagram 1

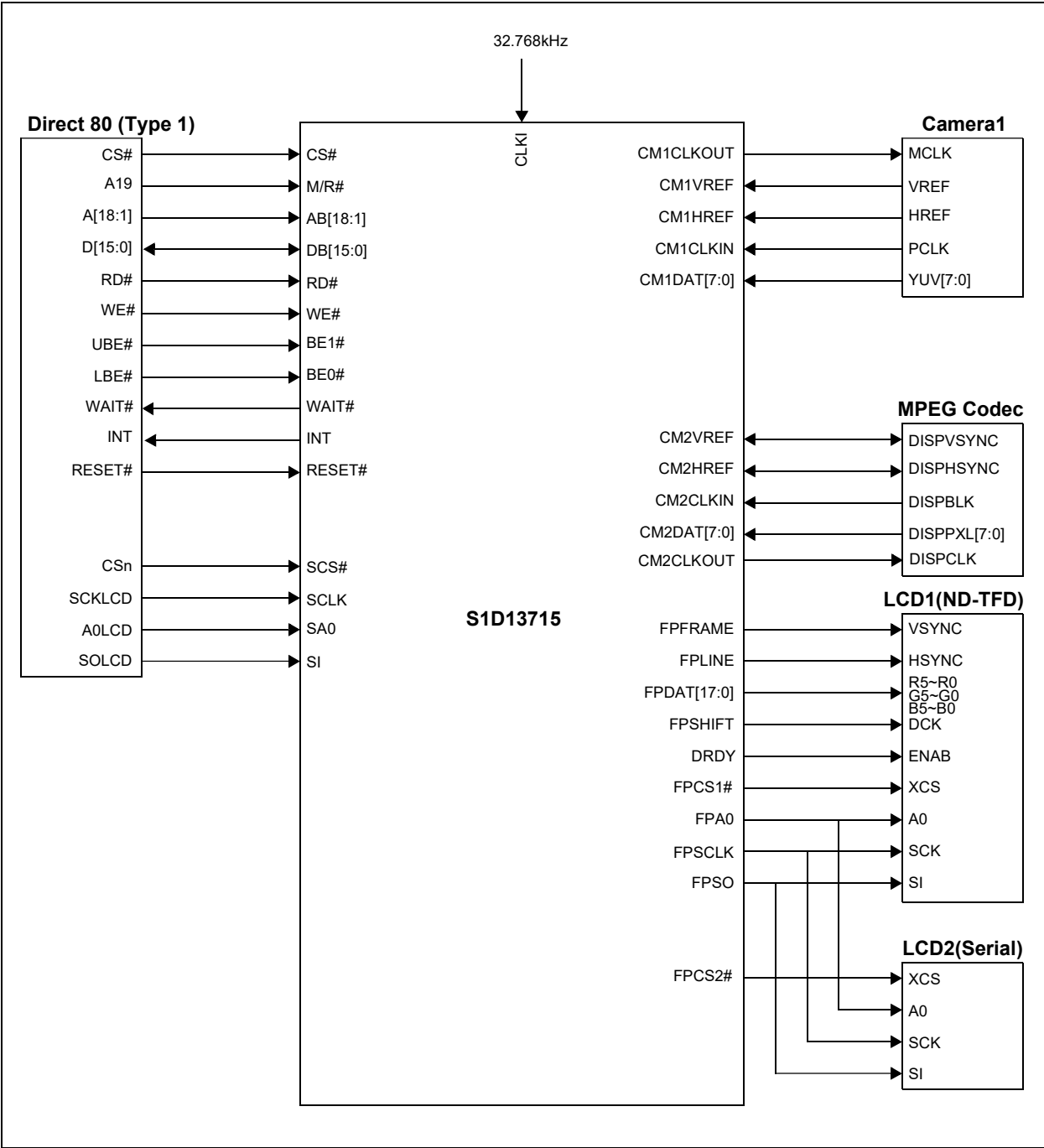


Figure 3-2: S1D13715 System Diagram 2

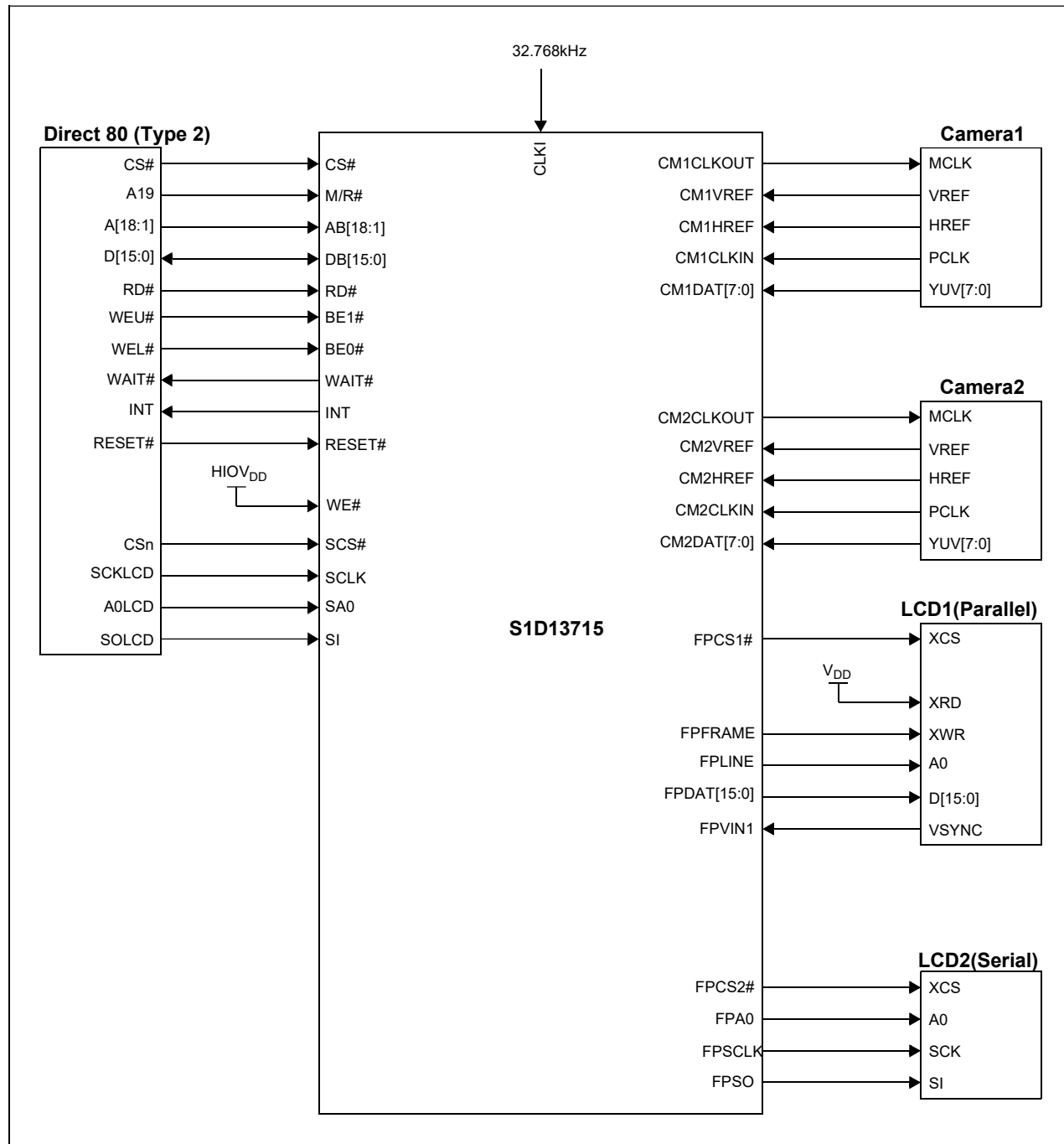


Figure 3-3: S1D13715 System Diagram 3

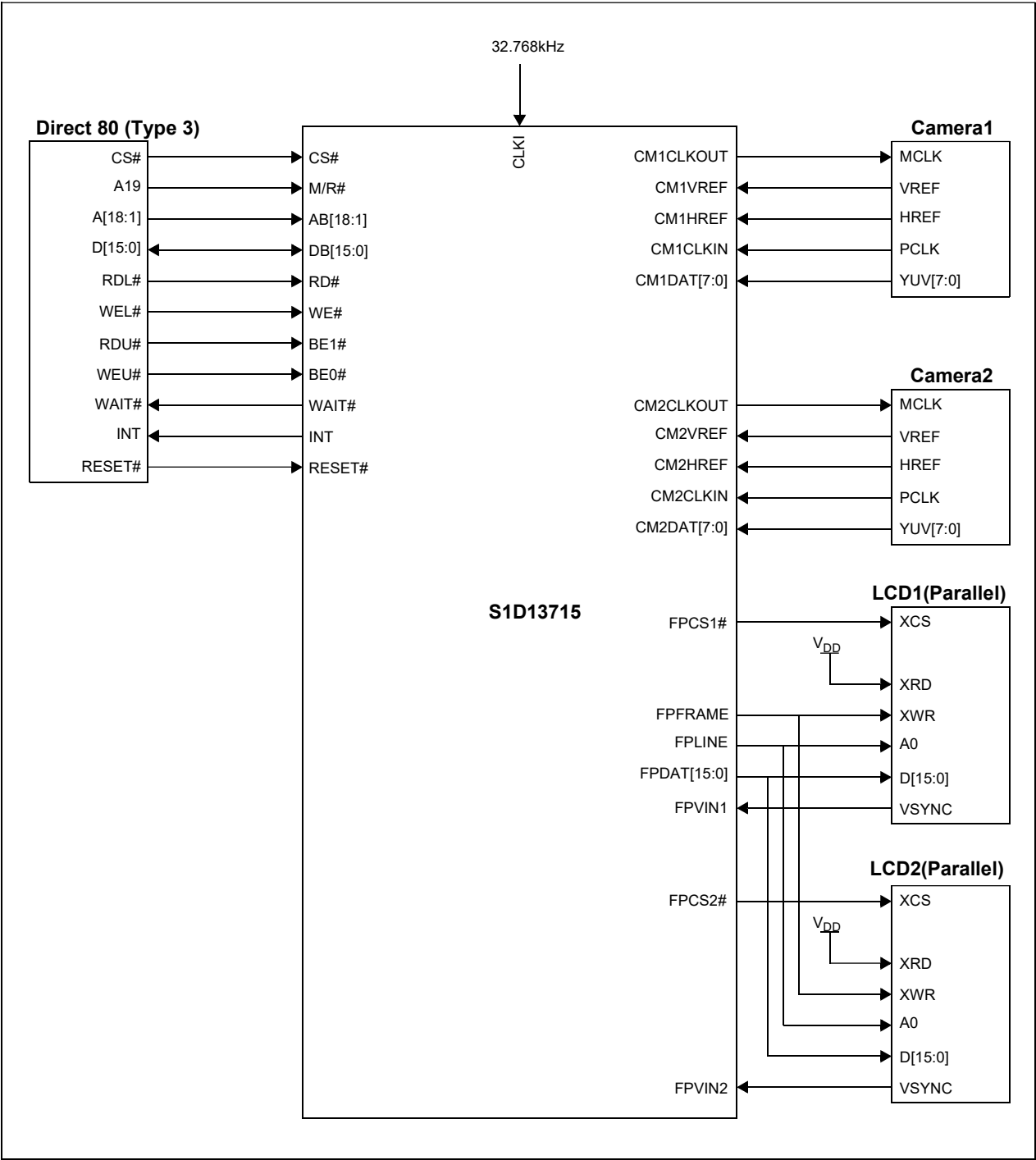


Figure 3-4: S1D13715 System Diagram 4

## 4 Block Diagram

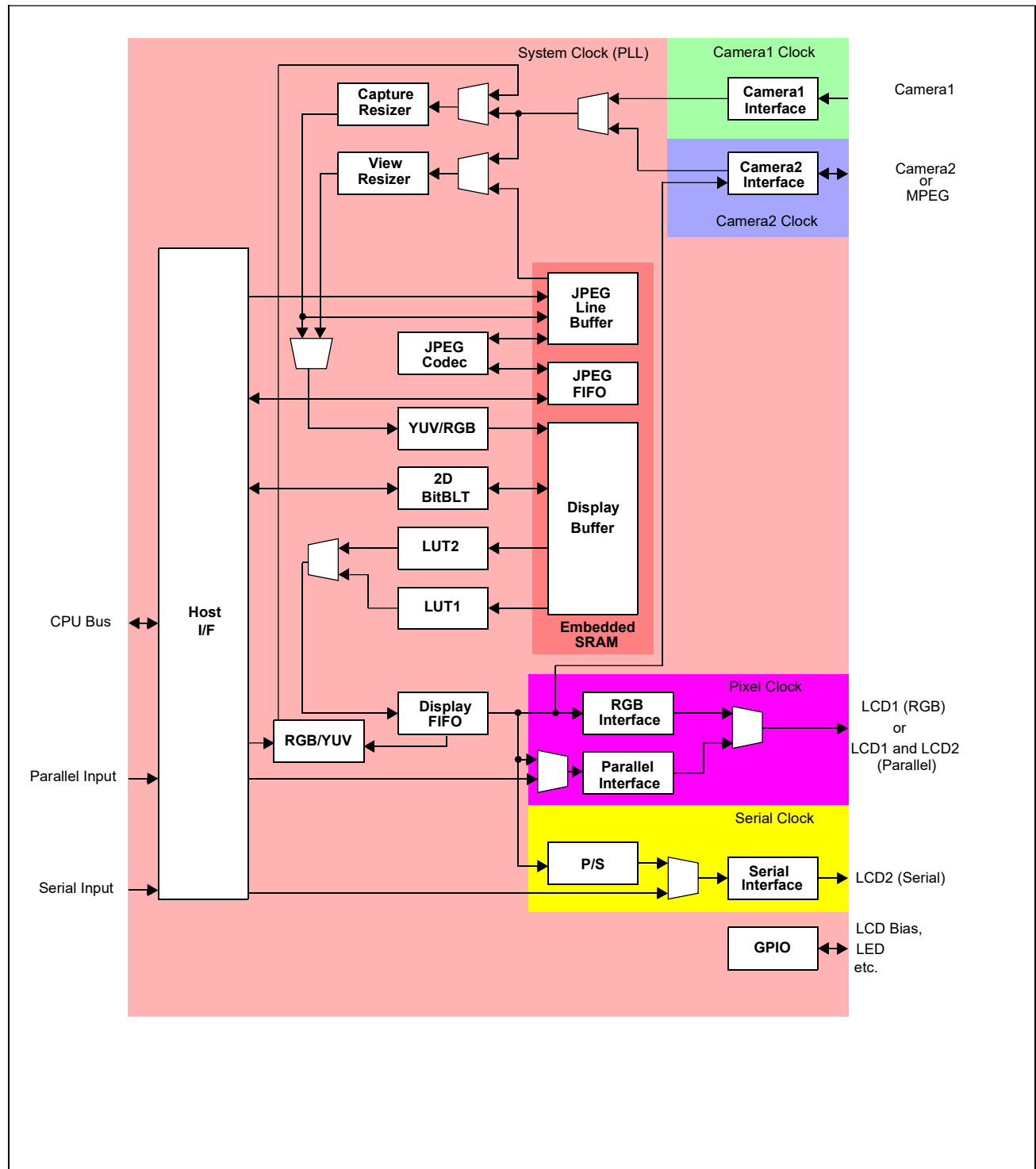


Figure 4-1: S1D13715 Block Diagram

# 5 Pins

## 5.1 S1D13715 Pinout Diagram (PFBGA-160)

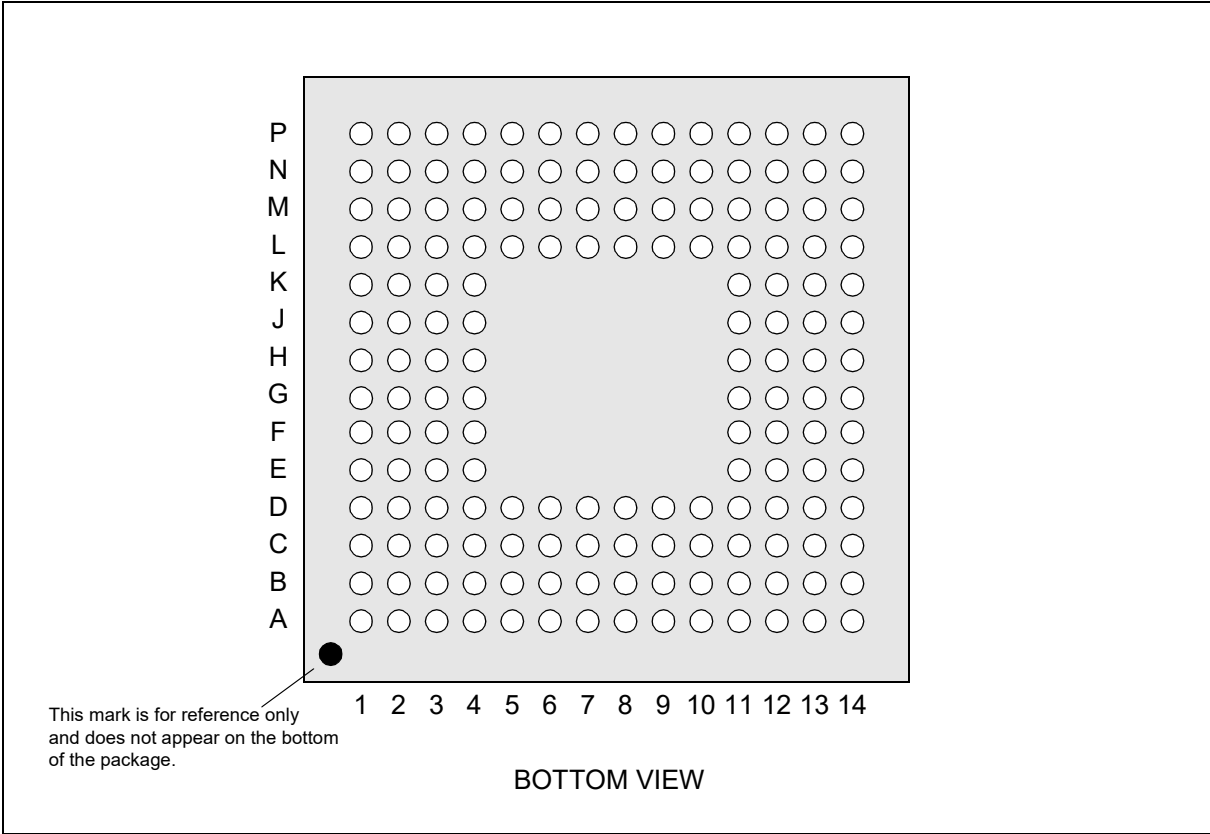


Figure 5-1: S1D13715 PFBGA-160 Pin Mapping

Table 5-1: S1D13715 PFBGA-160 Pin Mapping

|   |          |          |        |         |         |         |           |           |          |         |         |         |         |         |
|---|----------|----------|--------|---------|---------|---------|-----------|-----------|----------|---------|---------|---------|---------|---------|
| P | NC       | DB2      | M/R#   | BE1#    | INT     | RESET#  | TESTEN    | GPIO19    | GPIO6    | GPIO21  | GPIO17  | FPDAT0  | FPLINE  | NC      |
| N | AB15     | VSS      | DB1    | WE#     | WAIT#   | RD#     | VSS       | GPIO0     | GPIO8    | DRDY    | GPIO20  | FPDAT1  | FPDAT15 | FPFRAME |
| M | AB17     | AB16     | DB0    | CS#     | BE0#    | AB2     | HIOVDD    | FPVIN1    | GPIO15   | FPDAT8  | GPIO18  | GPIO16  | SCANEN  | COREVDD |
| L | DB9      | DB7      | AB18   | HIOVDD  | SCLK    | SA0     | SI        | FPVIN2    | CNF3     | FPCS2#  | PIOVDD  | FPDAT6  | FPDAT5  | FPDAT4  |
| K | DB10     | DB12     | DB11   | DB8     |         |         |           |           |          |         | CNF5    | FPDAT3  | FPDAT2  | GPIO14  |
| J | DB15     | DB14     | HIOVDD | DB13    |         |         |           |           |          |         | CNF4    | GPIO13  | PIOVDD  | FPSHIFT |
| H | Reserved | Reserved | VSS    | SCS#    |         |         |           |           |          |         | CNF0    | VSS     | FPCS1#  | FPDAT7  |
| G | AB1      | AB3      | AB4    | AB6     |         |         |           |           |          |         | FPSCCLK | FPDAT9  | FPDAT17 | COREVDD |
| F | AB5      | AB7      | AB8    | AB12    |         |         |           |           |          |         | FPA0    | FPDAT16 | FPDAT12 | FPDAT14 |
| E | AB9      | AB10     | AB11   | COREVDD |         |         |           |           |          |         | FPSO    | FPDAT11 | FPDAT13 | FPDAT10 |
| D | AB13     | AB14     | DB4    | VSS     | CM2DAT3 | CM2DAT7 | CM1DAT2   | CM1DAT6   | CNF6     | CNF2    | CNF1    | GPIO12  | PIOVDD  | GPIO11  |
| C | DB3      | DB5      | VCP    | CM2DAT1 | CM2DAT5 | CM2VREF | CM1HREF   | CM1DAT1   | CM1DAT3  | CM1DAT7 | CIOVDD  | GPIO7   | GPIO10  | GPIO9   |
| B | DB6      | CLKI     | PLLVD  | CM2DAT2 | CM2DAT6 | VSS     | CM2CLKIN  | CM1CLKOUT | CM1DAT0  | CM1DAT5 | PIOVDD  | GPIO3   | GPIO2   | GPIO5   |
| A | NC       | PLLSS    | HIOVDD | CM2DAT0 | CM2DAT4 | CM2HREF | CM2CLKOUT | CM1VREF   | CM1CLKIN | CM1DAT4 | VSS     | GPIO1   | GPIO4   | NC      |
|   | 1        | 2        | 3      | 4       | 5       | 6       | 7         | 8         | 9        | 10      | 11      | 12      | 13      | 14      |

# 5.2 S1D13715 Pinout Diagram (QFP21-176)

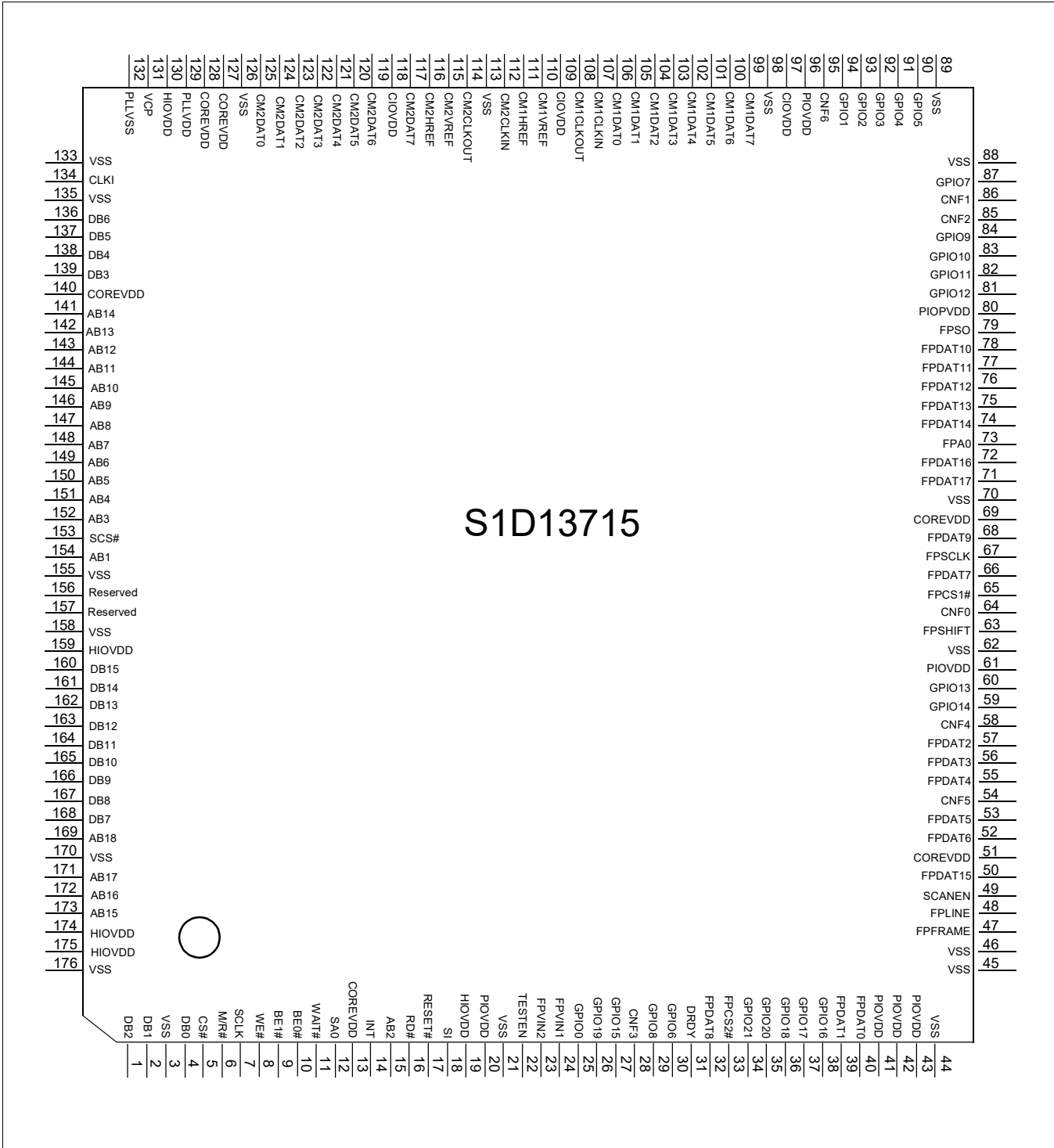


Figure 5-2: S1D13715 QFP21-176 Pin Mapping (Top View)

## 5.3 Pin Descriptions

Key:

|      |   |                               |
|------|---|-------------------------------|
| I    | = | Input                         |
| O    | = | Output                        |
| IO   | = | Bi-Directional (Input/Output) |
| P    | = | Power pin                     |
| Hi-Z | = | High Impedance                |

Table 5-2: Cell Descriptions

| Item     | Description                                                                                          |
|----------|------------------------------------------------------------------------------------------------------|
| IC       | LVC MOS <sup>1</sup> input                                                                           |
| ICU      | LVC MOS input with pull-up resistor (60K $\Omega$ @3.0V)                                             |
| ICD      | LVC MOS input with pull-down resistor (60K $\Omega$ @3.0V)                                           |
| IHCS     | H System LVC MOS level Schmitt input                                                                 |
| ILCS     | L System LVC MOS level Schmitt input                                                                 |
| OLN35    | Low noise output buffer (3.5mA/-3.5mA@3.0V)                                                          |
| OLN35T   | Low noise Tri-state output buffer (3.5mA/-3.5mA@3.0V)                                                |
| BLNC35   | Low noise LVC MOS IO buffer (3.5mA/-3.5mA@3.0V)                                                      |
| BLNC35D  | Low noise LVC MOS IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60K $\Omega$ @3.0V)         |
| BLNC35DS | Low noise LVC MOS Schmitt IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60K $\Omega$ @3.0V) |
| ITD      | Test mode control input with pull-down resistor (60K $\Omega$ @3.0V)                                 |
| ILTR     | Low Voltage Transparent Input                                                                        |
| IHTR     | High Voltage Transparent Input                                                                       |
| OHTR     | High Voltage Transparent Output                                                                      |

1. LVC MOS is Low Voltage CMOS (see Section 6, "D.C. Characteristics" on page 53).

### 5.3.1 Host Interface

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-9: “Summary of Power-On/Reset Options,” on page 43). For a summary of host interface pins, see Table 5-10: “Host Interface Pin Mapping (1 CS# mode),” on page 44 and Table 5-11: “Host Interface Pin Mapping (2 CS# mode),” on page 45.

Table 5-3: Host Interface Pin Descriptions

| Pin Name | Type | PFBGA Pin#                                                                | QFP Pin#                                                                                                        | Cell   | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|------|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|--------|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AB[18:1] | I    | L3,M1,M2,<br>N1,D2,D1,<br>F4,E3,E2,<br>E1,F3,F2,<br>G4,F1,G3,<br>G2,M6,G1 | 169, 171,<br>172, 173,<br>141, 142,<br>143, 144,<br>145, 146,<br>147, 148,<br>149, 150,<br>151, 152,<br>15, 154 | IC     | HIOVDD | —            | System address bits 18:1.<br><ul style="list-style-type: none"><li>For Indirect Host Bus Interfaces, these pins must be connected to V<sub>SS</sub>.</li></ul>                                                                                                                                                                                                                                                                                                 |
| DB[15:0] | IO   | J1,J2,J4,<br>K2,K3,K1,<br>L1,K4,L2,<br>B1,C2,D3,<br>C1,P2,N3,<br>M3       | 160, 161,<br>162, 163,<br>164, 165,<br>166, 167,<br>168, 136,<br>137, 138,<br>139, 1, 2, 4                      | BLNC35 | HIOVDD | Hi-Z         | System data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| CS#      | I    | M4                                                                        | 5                                                                                                               | IC     | HIOVDD | —            | This input pin has multiple functions.<br><ul style="list-style-type: none"><li>For 1 CS# mode, this pin inputs the chip select signal (CS#).</li><li>For 2 CS# mode, this pin inputs the memory chip select signal (CSM#).</li></ul>                                                                                                                                                                                                                          |
| M/R#     | I    | P3                                                                        | 6                                                                                                               | IC     | HIOVDD | —            | This input pin has multiple functions.<br><ul style="list-style-type: none"><li>For 1 CS# mode, this pin selects between the display buffer and register address spaces. When M/R# is set high, the display buffer is accessed and when M/R# is set low the registers are accessed.</li><li>For 2 CS# mode, this pin inputs the register chip select (CSR#).</li><li>For Indirect Host Bus Interfaces, this pin must be connected to V<sub>SS</sub>.</li></ul> |
| RD#      | I    | N6                                                                        | 16                                                                                                              | IC     | HIOVDD | —            | This input pin has multiple functions.<br><ul style="list-style-type: none"><li>For Indirect and Direct 68, this pin must be connected to HIOV<sub>DD</sub>.</li><li>For Indirect and Direct 80 Type 1 and Type 2, this pin is the read enable signal (RD#).</li><li>For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte read enable signal (RDL#).</li></ul>                                                                                |

Table 5-3: Host Interface Pin Descriptions (Continued)

| Pin Name | Type | PFBGA Pin# | QFP Pin# | Cell   | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|------|------------|----------|--------|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WE#      | I    | N4         | 8        | IC     | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Indirect and Direct 68, this pin is the read/write signal (R/W#).</li> <li>For Indirect and Direct 80 Type 1, this pin is the write enable signal (WE#).</li> <li>For Indirect and Direct 80 Type 2, this pin must be connected to HIOV<sub>DD</sub>.</li> <li>For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte write enable signal (WEL#).</li> </ul>                                      |
| BE1#     | I    | P4         | 9        | IC     | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Indirect and Direct 68, this pin is the D[15:8] upper data strobe (UDS#).</li> <li>For Indirect and Direct 80 Type 1, this pin is the D[15:8] upper byte enable signal (UBE#).</li> <li>For Indirect and Direct 80 Type 2, this pin is the DB[15:8] upper byte write enable signal (WEU#).</li> <li>For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte read enable signal (RDU#).</li> </ul> |
| BE0#     | I    | M5         | 10       | IC     | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Indirect and Direct 68, this pin is the D[7:0] lower data strobe (LDS#).</li> <li>For Indirect and Direct 80 Type 1, this pin is the D[7:0] lower byte enable signal (LBE#).</li> <li>For Indirect and Direct 80 Type 2, this pin is the DB[7:0] lower byte write enable signal (WEL#).</li> <li>For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte write enable signal (WEU#).</li> </ul>   |
| WAIT#    | O    | N5         | 11       | OLN35T | HIOVDD | Hi-Z         | During a data transfer, WAIT# is driven active (low) to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. This pin can be masked using the CNF0 pin.                                                                                                                                                                                                          |
| INT      | O    | P5         | 14       | OLN35  | HIOVDD | 0            | Interrupt output. When an internal interrupt occurs, this output pin is driven high. If the Host CPU clears the internal interrupt, this pin is driven low.                                                                                                                                                                                                                                                                                                                                               |
| RESET#   | I    | P6         | 17       | IHCS   | HIOVDD | —            | This active low input sets all internal registers to their default state and forces all signals to their inactive states.                                                                                                                                                                                                                                                                                                                                                                                 |

Table 5-3: Host Interface Pin Descriptions (Continued)

| Pin Name | Type | PFBGA Pin# | QFP Pin# | Cell | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|------|------------|----------|------|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SCS#     | I    | H4         | 153      | ICU  | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Serial Bypass Mode, this pin is the serial chip select input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD.</li> <li>For Parallel Bypass Mode, this pin is the LCD2 parallel chip select input for the Host CPU parallel interface. When Parallel Bypass Mode is enabled, the Host CPU can directly control the LCD1 or LCD2 parallel interface LCD.</li> </ul> |
| SCLK     | I    | L5         | 7        | ICD  | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Serial Bypass Mode, this pin is the serial clock input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD.</li> <li>For Parallel Bypass Mode, this pin is the write command input. When Parallel Bypass Mode is enabled, the Host CPU can directly control the LCD1 or LCD2 parallel interface LCD.</li> </ul>                                                       |
| SA0      | I    | L6         | 12       | ICD  | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Serial Bypass Mode, this pin is the serial A0 command input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD.</li> <li>For Parallel Bypass Mode, this pin is the parallel A0 command input. When Parallel Bypass Mode is enabled, the Host CPU can directly control the LCD1 or LCD2 parallel interface LCD.</li> </ul>                                            |
| SI       | I    | L7         | 18       | ICD  | HIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Serial Bypass Mode, this pin is the serial data input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD.</li> <li>For Parallel Bypass Mode, this pin is the LCD1 parallel chip select input for the Host CPU parallel interface. When Parallel Bypass Mode is enabled, the Host CPU can directly control the LCD1 or LCD2 parallel interface LCD.</li> </ul>        |

### 5.3.2 LCD Interface

Many of the LCD Interface pins have different functions depending on the configured panel interface mode. See Table 5-12: “LCD Interface Pin Mapping for Mode 1,” on page 46 and Table 5-13: “LCD Interface Pin Mapping for Modes 2/3,” on page 47 for more details on the pin functions.

- Mode 1 is LCD1: RGB, LCD2: Serial
- Mode 2 is LCD1: Parallel, LCD2: Serial
- Mode 3 is LCD1: Parallel, LCD2: Parallel
- Mode 4 is LCD1: RGB, LCD2: Parallel

For further information on the three panel interface modes, see the bit description for REG[0032h] bits 1-0.

*Table 5-4: LCD Interface Pin Descriptions*

| Pin Name    | Type | PFBGA Pin#                                                                      | QFP Pin#                                                               | Cell   | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------|------|---------------------------------------------------------------------------------|------------------------------------------------------------------------|--------|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FPDAT[17:0] | O    | G13,F12, N13,F14, E13,F13, E12,E14, G12,M10, H14,L12, L13,L14, K12,K13, N12,P12 | 71, 72, 50, 74, 75, 76, 77, 78, 68, 32, 66, 52, 53, 55, 56, 57, 39, 40 | OLN35T | PIOVDD | 0            | These output pins have multiple functions. <ul style="list-style-type: none"> <li>• For Mode 1 and Mode 4 RGB interfaces, these pins are the LCD1 RGB data outputs.</li> <li>• For Mode 2, Mode 3 and Mode 4 parallel interfaces, FPDAT[17:0] are the parallel interface data outputs.</li> <li>• When REG[0056h] bit 13 = 1 or REG[005Eh] bit 13 = 1, these pins are controlled with tri-state.</li> <li>• For Parallel Bypass Mode, these pins output the Host CPU data. See Table 5-15: “Serial/Parallel Bypass Pin Mapping,” on page 49.</li> </ul> |
| FPFRAME     | O    | N14                                                                             | 47                                                                     | OLN35  | PIOVDD | 0            | This output pin has multiple functions. <ul style="list-style-type: none"> <li>• For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 frame pulse output.</li> <li>• For Mode 2, Mode 3 and Mode 4 parallel interfaces, this pin is the write command output.</li> <li>• For Parallel Bypass Mode, this pin outputs the Host CPU XWR signal.</li> </ul>                                                                                                                                                                                           |
| FPLINE      | O    | P13                                                                             | 48                                                                     | OLN35  | PIOVDD | 0            | This output pin has multiple functions. <ul style="list-style-type: none"> <li>• For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 line pulse output.</li> <li>• For Mode 2, Mode 3 and Mode 4 parallel interfaces, this pin is the A0 output.</li> <li>• For Parallel Bypass Mode, this pin outputs the Host CPU A0 signal.</li> </ul>                                                                                                                                                                                                        |
| FPSHIFT     | O    | J14                                                                             | 63                                                                     | OLN35  | PIOVDD | 0            | This output pin has multiple functions. <ul style="list-style-type: none"> <li>• For Mode 1 and Mode 4, this pin is the LCD1 pixel clock output.</li> <li>• For all other cases, this pin is not used.</li> </ul>                                                                                                                                                                                                                                                                                                                                       |
| DRDY        | O    | N10                                                                             | 31                                                                     | OLN35  | PIOVDD | 0            | This output pin has multiple functions. <ul style="list-style-type: none"> <li>• For Mode 1 and Mode 4, this pin is the LCD1 DRDY output.</li> <li>• For all other cases, this pin is not used.</li> </ul>                                                                                                                                                                                                                                                                                                                                              |

Table 5-4: LCD Interface Pin Descriptions (Continued)

| Pin Name | Type | PFBGA Pin# | QFP Pin# | Cell  | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|------|------------|----------|-------|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FPCS1#   | O    | H13        | 65       | OLN35 | PIOVDD | 1            | <p>This output pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 1 and Mode 4, this pin is the LCD1 serial interface chip select output.</li> <li>For Mode 2 and Mode 3, this pin is the LCD1 parallel interface chip select output.</li> <li>For Parallel Bypass Mode, this pin outputs the Host CPU NCS1 signal.</li> </ul>                                                                                                                                                                                                                                                                                                                    |
| FPCS2#   | O    | L10        | 33       | OLN35 | PIOVDD | 1            | <p>This output pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 1, this pin is the LCD2 serial interface chip select output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCS# pin.</li> <li>For Mode 2, this pin is the LCD2 serial interface chip select output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCS# pin.</li> <li>For Mode 3 and 4, this pin is the LCD2 parallel interface chip select output.</li> <li>For Serial or Parallel Bypass Mode, this pin outputs the Host CPU NCS2 signal.</li> </ul>               |
| FPSCCLK  | O    | G11        | 67       | OLN35 | PIOVDD | 0            | <p>This output pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 1, this pin is the LCD1 and LCD2 serial interface clock output. For Mode 4, this pin is the LCD1 serial interface clock output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCLK pin.</li> <li>For Mode 2, this pin is the LCD2 serial interface clock output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCLK pin.</li> <li>For Mode 3, this pin is not used.</li> <li>For Serial Bypass Mode, this pin outputs the Host CPU SCK signal.</li> </ul> |
| FPA0     | O    | F11        | 73       | OLN35 | PIOVDD | 0            | <p>This output pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 1, this pin is the LCD1 and LCD2 serial interface A0 output. For Mode 4, this pin is the LCD1 serial interface A0 output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SA0 pin.</li> <li>For Mode 2, this pin is the LCD2 serial interface A0 output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SA0 pin.</li> <li>For Mode 3, this pin is not used.</li> <li>For Serial Bypass Mode, this pin outputs the Host CPU A0 signal.</li> </ul>             |

Table 5-4: LCD Interface Pin Descriptions (Continued)

| Pin Name | Type | PFBGA Pin# | QFP Pin# | Cell  | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|------|------------|----------|-------|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FPSO     | O    | E11        | 79       | OLN35 | PIOVDD | 0            | <p>This output pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 1, this pin is the LCD1 and LCD2 serial interface data output. For Mode 4, this pin is the LCD1 serial interface data output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SI pin.</li> <li>For Mode 2, this pin is the LCD2 serial interface data output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SI pin.</li> <li>For Mode 3, this pin is not used.</li> <li>For Serial Bypass Mode, this pin outputs the Host CPU SI signal.</li> </ul> |
| FPVIN1   | I    | M8         | 24       | IC    | PIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 2, Mode 3 and Mode 4, this pin is the parallel interface LCD1 vertical sync input from the LCD panel.</li> </ul> <p>If this pin is not used, it must be connected to ground (VSS).</p>                                                                                                                                                                                                                                                                                                                                                                                   |
| FPVIN2   | I    | L8         | 23       | IC    | PIOVDD | —            | <p>This input pin has multiple functions.</p> <ul style="list-style-type: none"> <li>For Mode 2, this pin is the LCD2 serial interface vertical sync input from the LCD panel.</li> <li>For Mode 3 and Mode 4, this pin is the LCD2 parallel interface vertical sync input from the LCD panel.</li> </ul> <p>If this pin is not used, it must be connected to ground (VSS).</p>                                                                                                                                                                                                                                                                                        |

### 5.3.3 Camera Interface

Many of the pins for the 2 Camera Interfaces have different functions depending on the settings for these interfaces. See Table 5-18: “Camera1 Interface Pin Mapping,” on page 52 for details on the connections for the Camera1 Interface. See Table 5-19: “Camera2 Interface Pin Mapping,” on page 52 for details on the connections for the Camera2 Interface.

The Camera1 Interface supports a Type 1, 8/16-bit bus Camera interface.

The Camera2 Interface supports a Type 1, 8-bit bus Camera interface. It also supports input from an external MPEG codec.

Table 5-5: Camera Interface Pin Descriptions

| Pin Name    | Type | PFBGA Pin#                    | QFP Pin#                               | Cell     | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------|------|-------------------------------|----------------------------------------|----------|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CM1DAT[7:0] | IO   | C10,D8, B10,A10, C9,D7, C8,B9 | 99, 100, 101, 102, 103, 104, 105, 106  | BLNC35D  | CIOVDD | 0            | These input/output pins have multiple functions. <ul style="list-style-type: none"> <li>For the Camera1 8-bit interface (REG[0102h] bit 6 = 0), these pins are the 8-bit data input (CAMDAT[7:0]).</li> <li>For the Camera1 16-bit interface (REG[0102h] bit 6 = 1), these pins are the 8-bit luminance (Y) or chrominance (Cb/Cr) data input (CAMDAT[7:0]). The data type must be set using REG[0102h] bits 4-3.</li> </ul>                                                                    |
| CM1VREF     | IO   | A8                            | 110                                    | BLNC35D  | CIOVDD | 0            | For the Camera1 interface, this pin is the vertical sync input (VREF).                                                                                                                                                                                                                                                                                                                                                                                                                          |
| CM1HREF     | IO   | C7                            | 111                                    | BLNC35D  | CIOVDD | 0            | For the Camera1 interface, this pin is the horizontal sync input (HREF).                                                                                                                                                                                                                                                                                                                                                                                                                        |
| CM1CLKOUT   | O    | B8                            | 108                                    | OLN35    | CIOVDD | 0            | For the Camera1 interface, this pin is the Master clock output (CAMMCLK).                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CM1CLKIN    | IO   | A9                            | 107                                    | BLNC35DS | CIOVDD | 0            | For the Camera1 interface, this pin is the camera pixel clock input (CAMPCLK).                                                                                                                                                                                                                                                                                                                                                                                                                  |
| CM2DAT[7:0] | IO   | D6,B5, C5,A5, D5,B4, C4,A4    | 117, 119, 120, 121, 122, 123, 124, 125 | BLNC35D  | CIOVDD | 0            | These input/output pins have multiple functions. <ul style="list-style-type: none"> <li>For the Camera1 16-bit interface (REG[0102h] bit 6 = 1), these pins are the 8-bit chrominance (Cb/Cr) or luminance (Y) data input (CAMDAT[15:8]). The data type must be set using REG[0102h] bits 4-3.</li> <li>For the Camera2 interface, these pins are the 8-bit data input (CAMDAT[7:0]).</li> <li>For the Camera2 MPEG codec interface, these pins are the 8-bit data input (PXL[7:0]).</li> </ul> |

Table 5-5: Camera Interface Pin Descriptions (Continued)

| Pin Name  | Type | PFBGA Pin# | QFP Pin# | Cell     | Power  | RESET# State | Description                                                                                                                                                                                                                                                                 |
|-----------|------|------------|----------|----------|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CM2VREF   | IO   | C6         | 115      | BLNC35D  | CIOVDD | 0            | This input/output pin has multiple functions. <ul style="list-style-type: none"> <li>For the Camera2 interface, this pin is the vertical sync input (VREF).</li> <li>For the Camera2 MPEG codec interface, this pin is the vertical sync input (nDISPSYNC).</li> </ul>      |
| CM2HREF   | IO   | A6         | 116      | BLNC35D  | CIOVDD | 0            | This input/output pin has multiple functions. <ul style="list-style-type: none"> <li>For the Camera2 interface, this pin is the horizontal sync input (HREF).</li> <li>For the Camera2 MPEG codec interface, this pin is the horizontal sync input (nDISPHSYNC).</li> </ul> |
| CM2CLKOUT | O    | A7         | 114      | OLN35    | CIOVDD | 0            | This output pin has multiple functions. <ul style="list-style-type: none"> <li>For the Camera2 interface, this pin is the master clock output (CAMMCLK).</li> <li>For the Camera2 MPEG codec interface, this pin is the clock output (DISPCLK).</li> </ul>                  |
| CM2CLKIN  | IO   | B7         | 112      | BLNC35DS | CIOVDD | 0            | This input/output pin has multiple functions. <ul style="list-style-type: none"> <li>For the Camera2 interface, this pin is the camera pixel clock input (CAMPCLK).</li> <li>For the Camera2 MPEG codec interface, this pin is the blanking input (DISPCLK).</li> </ul>     |

## 5.3.4 Clock Input

Table 5-6: Clock Input Pin Descriptions

| Pin Name | Type | PFBGA Pin# | QFP Pin# | Cell | Power  | RESET# State | Description                                                                                                                                                                                                                                                                                           |
|----------|------|------------|----------|------|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLKI     | I    | B2         | 134      | ILCS | HIOVDD | —            | This input pin has multiple functions. <ul style="list-style-type: none"> <li>When the internal PLL is used, this pin is the input reference clock for the internal PLL (32.768KHz).</li> <li>When the PLL is bypassed, this pin is the digital clock input for the system clock (SYSCLK).</li> </ul> |
| Reserved | —    | H1         | 156      | —    | —      | —            | Reserved. This pin must be connected to GND.                                                                                                                                                                                                                                                          |
| Reserved | —    | H2         | 157      | —    | —      | —            | Reserved. This pin must be left unconnected.                                                                                                                                                                                                                                                          |

### 5.3.5 Miscellaneous

Table 5-7: Miscellaneous Pin Descriptions

| Pin Name   | Type | PFBGA Pin#                                                                                   | QFP Pin#                                                                               | Cell    | Power   | RESET# State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------|------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|---------|---------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CNF[6:0]   | I    | D9,K11, J11,L9, D10,D11, H11                                                                 | 95, 54, 58, 28, 85, 86, 64                                                             | IC      | PIOVDD  | —            | These inputs are used for configuring the S1D13715 and must be connected to either PIOVDD or VSS. The states of these pins are latched at RESET#. For more information, see Table 5-9: "Summary of Power-On/Reset Options," on page 43.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| GPIO[21:0] | IO   | P10,N11, P8,M11, P11,M12, M9,K14, J12,D12, D14,C13, C14,N9, C12,P9, B14,A13, B12,B13, A12,N8 | 34, 35, 26, 36, 37, 38, 27, 59, 60, 81, 82, 83, 84, 29, 87, 30, 90, 91, 92, 93, 94, 25 | BLNC35D | PIOVDD  | see note     | <p>These pins are general purpose input/output pins. Their default configuration (input or output) is controlled using CNF1.</p> <ul style="list-style-type: none"> <li>For various LCD panel settings, GPIO[13:0] are used to output LCD interface signals. See Table 5-12: "LCD Interface Pin Mapping for Mode 1," on page 46 and Table 5-13: "LCD Interface Pin Mapping for Modes 2/3," on page 47 for which GPIO pins are available for use as GPIOs for a given LCD panel setting.</li> <li>In serial bypass mode or in power-save mode, GPIO19 inputs the Host CPU serial interface chip select signal (CMCSi#).</li> <li>GPIO20 outputs the strobe control signal when the strobe function is enabled (REG[0124h] bit 3 = 1).</li> </ul> |
| TESTEN     | I    | P7                                                                                           | 22                                                                                     | ITD     | PIOVDD  | 0            | Test Enable input used for production test only. This pin should be left unconnected for normal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SCANEN     | I    | M13                                                                                          | 49                                                                                     | ICD     | PIOVDD  | 0            | Scan Enable input used for production test only. This pin should be left unconnected for normal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| VCP        | IO   | C3                                                                                           | 131                                                                                    | ILTR    | COREVDD |              | PLL output monitor pin used for production test only. This pin should be left unconnected for normal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

#### Note

When CNF1 = 0 (GPIO pins are outputs), the reset state of GPIO[21:3, 0] is 0.

When CNF1 = 1 (GPIO pins default to inputs), the reset state of GPIO[21:3, 0] is 0.

When REG[0056h] bit 13 = 1, or REG[005Eh] bit 13 = 1, the reset state of GPIO[2:1] is always Hi-Z.

When REG[0056h] bit 13 = 0 and REG[005Eh] bit 13 = 0, the reset state of GPIO[2:1] depends on CNF1 as above.

### 5.3.6 Power And Ground

Table 5-8: Power And Ground Pin Descriptions

| Pin Name | Type | PFBGA Pin#                   | QFP Pin#                                                                   | Cell | RESET# State | Description                                |
|----------|------|------------------------------|----------------------------------------------------------------------------|------|--------------|--------------------------------------------|
| HIOVDD   | P    | A3, J3, L4, M7               | 19, 130, 159, 174, 175                                                     | P    | —            | IO power supply for the host interface     |
| PIOVDD   | P    | B11, D13, J13, L11           | 20, 41, 42, 43, 61, 80, 96                                                 | P    | —            | IO power supply for the panel interface    |
| CIOVDD   | P    | C11                          | 97, 109, 118                                                               | P    | —            | IO power supply for the camera interface   |
| COREVDD  | P    | E4, G14, M14                 | 13, 51, 69, 127, 128, 140,                                                 | P    | —            | Core power supply                          |
| VSS      | P    | A11, B6, D4, H3, H12, N2, N7 | 21, 44, 45, 46, 62, 70, 88, 89, 98, 113, 126, 133, 135, 155, 158, 170, 176 | P    | —            | GND for HIOVDD, PIOVDD, CIOVDD and COREVDD |
| PLLVD    | P    | B3                           | 129                                                                        | P    | —            | PLL power supply                           |
| PLLVSS   | P    | A2                           | 132                                                                        | P    | —            | GND for PLLVD                              |

## 5.4 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to PIOVDD or VSS. The state of CNF[6:0] are latched on the rising edge of RESET#. Changing state at any other time has no effect.

Table 5-9: Summary of Power-On/Reset Options

| Configuration Input | Power-On/Reset State                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------|------|----------|---|---|---|------------------|---|---|---|------------------|---|---|---|--------------------|---|---|---|--------------------|---|---|---|------------------|---|---|---|-----------|---|---|---|--------------------|---|---|---|-------------|
|                     | 1 (connected to PIOVDD)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0 (connected to VSS)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| CNF6                | 2 CS# mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1 CS# mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| CNF5                | Big Endian                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Little Endian                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| CNF[4:2]            | Select host bus interface as follows:<br><table><tr><th>CNF4</th><th>CNF3</th><th>CNF2</th><th>Host Bus</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Direct 80 Type 2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Direct 80 Type 3</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Indirect 80 Type 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Indirect 80 Type 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Direct 80 Type 1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Direct 68</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Indirect 80 Type 1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Indirect 68</td></tr></table> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | CNF4               | CNF3 | CNF2 | Host Bus | 0 | 0 | 0 | Direct 80 Type 2 | 0 | 0 | 1 | Direct 80 Type 3 | 0 | 1 | 0 | Indirect 80 Type 2 | 0 | 1 | 1 | Indirect 80 Type 3 | 1 | 0 | 0 | Direct 80 Type 1 | 1 | 0 | 1 | Direct 68 | 1 | 1 | 0 | Indirect 80 Type 1 | 1 | 1 | 1 | Indirect 68 |
| CNF4                | CNF3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | CNF2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Host Bus           |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 0                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Direct 80 Type 2   |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 0                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Direct 80 Type 3   |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 0                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Indirect 80 Type 2 |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 0                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Indirect 80 Type 3 |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 1                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Direct 80 Type 1   |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 1                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Direct 68          |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 1                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Indirect 80 Type 1 |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| 1                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Indirect 68        |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| CNF1                | All GPIO pins (GPIO[21:0]) are configured as inputs.<br><br>Note: When CNF1=1 at RESET#, REG[0300h]-REG[0302h] can be used to change individual GPIO pins between inputs/outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | All GPIO pins (GPIO[21:0]) are configured as outputs.<br><br>Note: When CNF1=0 at RESET#, REG[0300h]-REG[0302h] are ignored and the GPIO pins are always outputs.                                                                                                                                                                                                                                                                                                                                           |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
| CNF0                | For Direct Host Bus Interface Types (see CNF[4:2])                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
|                     | WAIT# is used.<br>The setup/hold time of A[19:1], UBE#, LBE# from the RD# edge is not 0 and the setup time of CS# edge from RD# is not 0 (Direct 80 Types, see Section 7.3, “Host Interface Timing” on page 60 for the signal names for other Direct host bus interfaces).<br><br>Note: When WAIT# is used (CNF0 = 1), WAIT# may not be asserted for all cycles. WAIT# is only asserted when needed.                                                                                                                                                                                                                                                | WAIT# is not used.<br>The setup/hold time of A[19:1], UBE#, LBE# from the RD# edge is 0 and the setup time of CS# edge from RD# is 0 (Direct 80 Types, see Section 7.3, “Host Interface Timing” on page 60 for the signal names for other Direct host bus interfaces).<br><br>Note: When WAIT# is not used (CNF0 = 0), WAIT# is never asserted for any cycles and the Host CPU must insert software wait states as needed to guarantee cycle length as outlined in Section 7.3.9, “WAIT Length” on page 91. |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
|                     | For Indirect Host Bus Interface Types (see CNF[4:2])                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |
|                     | WAIT# is not used.<br><br>The setup/hold time of A[2:1], UBE#, LBE# from the RD# edge is not 0 and the setup time of CS# edge from RD# is not 0 (Indirect 80 Types, see Section 7.3, “Host Interface Timing” on page 60 for the signal names for other Indirect host bus interfaces).                                                                                                                                                                                                                                                                                                                                                               | WAIT# is not used.<br><br>The setup/hold time of A[2:1], UBE#, LBE# from the RD# edge is 0 and the setup time of CS# edge from RD# is 0 (Indirect 80 Types, see Section 7.3, “Host Interface Timing” on page 60 for the signal names for other Indirect host bus interfaces).                                                                                                                                                                                                                               |                    |      |      |          |   |   |   |                  |   |   |   |                  |   |   |   |                    |   |   |   |                    |   |   |   |                  |   |   |   |           |   |   |   |                    |   |   |   |             |

**Note**

When WAIT# is used (CNF0 = 1), WAIT# may not be asserted for all cycles. WAIT# is only asserted when needed. When WAIT# is not used (CNF0 = 0), WAIT# is never asserted for any cycles and the Host CPU must insert software wait states as needed to guarantee cycle length as outlined in Section 7.3.9, “WAIT Length” on page 91.

## 5.5 Host Interface Pin Mapping

Table 5-10: Host Interface Pin Mapping (1 CS# mode)

| Pin Name                          | Direct 68       | Direct 80 Type 1 | Direct 80 Type 2 | Direct 80 Type 3 | Indirect 68 | Indirect 80 Type 1 | Indirect 80 Type 2 | Indirect 80 Type 3 | Serial       | Parallel      |
|-----------------------------------|-----------------|------------------|------------------|------------------|-------------|--------------------|--------------------|--------------------|--------------|---------------|
| AB[18:2]                          | A[18:2]         | A[18:2]          | A[18:2]          | A[18:2]          | Low         |                    |                    |                    | —            | —             |
| AB1                               | A1              | A1               | A1               | A1               | A1          | A1                 | A1                 | A1                 | —            | —             |
| DB[15:0]                          | D[15:0]         | D[15:0]          | D[15:0]          | D[15:0]          | D[15:0]     | D[15:0]            | D[15:0]            | D[15:0]            | —            | —             |
| CS#                               | CS#             | CS#              | CS#              | CS#              | CS#         | CS#                | CS#                | CS#                | —            | —             |
| M/R#                              | External Decode |                  |                  |                  | Low         |                    |                    |                    | —            | —             |
| RD#                               | High            | RD#              | RD#              | RDL#             | High        | RD#                | RD#                | RDL#               | —            | —             |
| WE#                               | R/W#            | WE#              | High             | WEL#             | R/W#        | WE#                | High               | WEL#               | —            | —             |
| BE#[1]                            | UDS#            | UBE#             | WEU#             | RDU#             | UDS#        | UBE#               | WEU#               | RDU#               | —            | —             |
| BE#[0]                            | LDS#            | LBE#             | WEL#             | WEU#             | LDS#        | LBE#               | WEL#               | WEU#               | —            | —             |
| WAIT#                             | WAIT#           | WAIT#            | WAIT#            | WAIT#            | WAIT#       | WAIT#              | WAIT#              | WAIT#              | —            | —             |
| INT                               | —               | —                | —                | —                | —           | —                  | —                  | —                  | —            | —             |
| RESET#                            | RESET#          | RESET#           | RESET#           | RESET#           | RESET#      | RESET#             | RESET#             | RESET#             | —            | —             |
| SCS#                              | —               | —                | —                | —                | —           | —                  | —                  | —                  | CS#          | PCS2# or PCS# |
| SCLK                              | —               | —                | —                | —                | —           | —                  | —                  | —                  | Serial Clock | PWR#          |
| SA0                               | —               | —                | —                | —                | —           | —                  | —                  | —                  | A0           | PA0           |
| SI                                | —               | —                | —                | —                | —           | —                  | —                  | —                  | Serial Data  | PCS# or PCS1# |
| GPIO19<br>(REG[0102h]<br>bit 6=1) | CMCSI#          | CMCSI#           | CMCSI#           | CMCSI#           | CMCSI#      | CMCSI#             | CMCSI#             | CMCSI#             | —            | —             |

Table 5-11: Host Interface Pin Mapping (2 CS# mode)

| Pin Name                            | Direct 68 | Direct 80 Type 1 | Direct 80 Type 2 | Direct 80 Type 3 | Indirect 68 | Indirect 80 Type 1 | Indirect 80 Type 2 | Indirect 80 Type 3 | Serial       | Parallel      |
|-------------------------------------|-----------|------------------|------------------|------------------|-------------|--------------------|--------------------|--------------------|--------------|---------------|
| AB[18:2]                            | A[18:2]   | A[18:2]          | A[18:2]          | A[18:2]          | Low         |                    |                    |                    | —            | —             |
| AB1                                 | A1        | A1               | A1               | A1               | A1          | A1                 | A1                 | A1                 | —            | —             |
| DB[15:0]                            | D[15:0]   | D[15:0]          | D[15:0]          | D[15:0]          | D[15:0]     | D[15:0]            | D[15:0]            | D[15:0]            | —            | —             |
| CS#                                 | CSM#      | CSM#             | CSM#             | CSM#             | CS#         | CS#                | CS#                | CS#                | —            | —             |
| M/R#                                | CSR#      | CSR#             | CSR#             | CSR#             | High        |                    |                    |                    | —            | —             |
| RD#                                 | High      | RD#              | RD#              | RDL#             | High        | RD#                | RD#                | RDL#               | —            | —             |
| WE#                                 | R/W#      | WE#              | High             | WEL#             | R/W#        | WE#                | High               | WEL#               | —            | —             |
| BE#[1]                              | UDS#      | UBE#             | WEU#             | RDU#             | UDS#        | UBE#               | WEU#               | RDU#               | —            | —             |
| BE#[0]                              | LDS#      | LBE#             | WEL#             | WEU#             | LDS#        | LBE#               | WEL#               | WEU#               | —            | —             |
| WAIT#                               | WAIT#     | WAIT#            | WAIT#            | WAIT#            | WAIT#       | WAIT#              | WAIT#              | WAIT#              | —            | —             |
| INT                                 | —         | —                | —                | —                | —           | —                  | —                  | —                  | —            | —             |
| RESET#                              | RESET#    | RESET#           | RESET#           | RESET#           | RESET#      | RESET#             | RESET#             | RESET#             | —            | —             |
| SCS#                                | —         | —                | —                | —                | —           | —                  | —                  | —                  | CS#          | PCS2# or PCS# |
| SCLK                                | —         | —                | —                | —                | —           | —                  | —                  | —                  | Serial Clock | PWR#          |
| SA0                                 | —         | —                | —                | —                | —           | —                  | —                  | —                  | A0           | PA0           |
| SI                                  | —         | —                | —                | —                | —           | —                  | —                  | —                  | Serial Data  | PCS# or PCS1# |
| GPIO19<br>(REG[0102h]<br>] bit 6=1) | CMCSI#    | CMCSI#           | CMCSI#           | CMCSI#           | CMCSI#      | CMCSI#             | CMCSI#             | CMCSI#             | —            | —             |

**Note**

2 CS# mode (CNF6=1) has no effect for Indirect Host Bus Interfaces. Indirect Host Bus Interfaces always function in 1 CS# mode.

## 5.6 LCD Interface Pin Mapping

Table 5-12: LCD Interface Pin Mapping for Mode 1

| Pin Name  | Mode 1      |           |           |                    |              |            |                       |            |            |
|-----------|-------------|-----------|-----------|--------------------|--------------|------------|-----------------------|------------|------------|
|           | LCD1        |           |           |                    |              |            |                       |            | LCD2       |
|           | General TFT | ND-TFD    | a-Si TFT  | TFT with uWIRE I/F | Sharp HR-TFT | Casio TFT  | Samsung $\alpha$ -TFT | Type 2 TFT | Serial I/F |
| FPFRAME   | VSYNC       | VSYNC     | VSYNC     | VSYNC              | SPS          | GSRT       | STV                   | STV        |            |
| FPLINE    | HSYNC       | HSYNC     | HSYNC     | HSYNC              | LP           | GPCK       | STH                   | STB        |            |
| FPSHIFT   | DCK         | DCK       | DCLK      | CLK                | DCLK         | CLK        | HCLK                  | CLK        |            |
| DRDY      | ENAB        | ENAB      | ENAB      | ENAB               | no connect   | no connect | no connect            | INV        |            |
| FPDAT0    | R7          | R7        | R7        | R7                 | R7           | R7         | R5                    | R7         |            |
| FPDAT1    | R6          | R6        | R6        | R6                 | R6           | R6         | R4                    | R6         |            |
| FPDAT2    | R5          | R5        | R5        | R5                 | R5           | R5         | R3                    | R5         |            |
| FPDAT3    | G7          | G7        | G7        | G7                 | G7           | G7         | G5                    | G7         |            |
| FPDAT4    | G6          | G6        | G6        | G6                 | G6           | G6         | G4                    | G6         |            |
| FPDAT5    | G5          | G5        | G5        | G5                 | G5           | G5         | G3                    | G5         |            |
| FPDAT6    | B7          | B7        | B7        | B7                 | B7           | B7         | B5                    | B7         |            |
| FPDAT7    | B6          | B6        | B6        | B6                 | B6           | B6         | B4                    | B6         |            |
| FPDAT8    | B5          | B5        | B5        | B5                 | B5           | B5         | B3                    | B5         |            |
| FPDAT9    | R4          | R4        | R4        | R4                 | R4           | R4         | R2                    | R4         |            |
| FPDAT10   | R3          | R3        | R3        | R3                 | R3           | R3         | R1                    | R3         |            |
| FPDAT11   | R2          | R2        | R2        | R2                 | R2           | R2         | R0                    | R2         |            |
| FPDAT12   | G4          | G4        | G4        | G4                 | G4           | G4         | G2                    | G4         |            |
| FPDAT13   | G3          | G3        | G3        | G3                 | G3           | G3         | G1                    | G3         |            |
| FPDAT14   | G2          | G2        | G2        | G2                 | G2           | G2         | G0                    | G2         |            |
| FPDAT15   | B4          | B4        | B4        | B4                 | B4           | B4         | B2                    | B4         |            |
| FPDAT16   | B3          | B3        | B3        | B3                 | B3           | B3         | B1                    | B3         |            |
| FPDAT17   | B2          | B2        | B2        | B2                 | B2           | B2         | B0                    | B2         |            |
| FPCS1#    |             | XCS       | SSTB      | LCDCS              | SPR          |            |                       |            |            |
| FPCS2#    |             |           |           |                    |              |            |                       |            | NCS2       |
| FPSCCLK   |             | SCK       | SCLK      | SCLK               |              |            |                       |            | SCK        |
| FPA0      |             | A0        |           |                    |              |            |                       |            | A0         |
| FPSO      |             | SI        | SDATA     | SDO                |              |            |                       |            | SI         |
| FPVIN1    |             |           |           |                    |              |            |                       |            |            |
| FPVIN2    |             |           |           |                    |              |            |                       |            | VIN2       |
| GPIO0     | GPIO0       | GPIO0     | GPIO0     | GPIO0              | PS           | POL        | CKV                   | VCLK       | GPIO0      |
| GPIO1     | GPIO1       | GPIO1     | GPIO1     | GPIO1              | CLS          | GRES       | LD                    | AP         | GPIO1      |
| GPIO2     | GPIO2       | GPIO2     | GPIO2     | GPIO2              | REV          | FRP        | INV                   | POL        | GPIO2      |
| GPIO3     | GPIO3       | GPIO3     | GPIO3     | GPIO3              | SPL          | STH        | VCOM                  | STH        | GPIO3      |
| GPIO4     | R1          | R1        | R1        | R1                 | R1           | R1         | GPIO4                 | R1         | GPIO4      |
| GPIO5     | R0          | R0        | R0        | R0                 | R0           | R0         | GPIO5                 | R0         | GPIO5      |
| GPIO6     | G1          | G1        | G1        | G1                 | G1           | G1         | GPIO6                 | G1         | GPIO6      |
| GPIO7     | G0          | G0        | G0        | G0                 | G0           | G0         | GPIO7                 | G0         | GPIO7      |
| GPIO8     | B1          | B1        | B1        | B1                 | B1           | B1         | GPIO8                 | B1         | GPIO8      |
| GPIO9     | B0          | B0        | B0        | B0                 | B0           | B0         | GPIO9                 | B0         | GPIO9      |
| GPIO10    | GPIO10      | GPIO10    | GPIO10    | GPIO10             | GPIO10       | GPIO10     | GPIO10                | GPIO10     | GPIO10     |
| GPIO11    | GPIO11      | GPIO11    | GPIO11    | GPIO11             | GPIO11       | GPIO11     | GPIO11                | GPIO11     | GPIO11     |
| GPIO12    | GPIO12      | GPIO12    | GPIO12    | GPIO12             | GPIO12       | GPIO12     | GPIO12                | GPIO12     | GPIO12     |
| GPIO13    | GPIO13      | GPIO13    | GPIO13    | GPIO13             | GPIO13       | GPIO13     | GPIO13                | GPIO13     | GPIO13     |
| GPIO14-21 | GPIO14-21   | GPIO14-21 | GPIO14-21 | GPIO14-21          | GPIO14-21    | GPIO14-21  | GPIO14-21             | GPIO14-21  | GPIO14-21  |

Table 5-13: LCD Interface Pin Mapping for Modes 2/3

| Pin Name  | Mode 2       |            | Mode 3       |              |
|-----------|--------------|------------|--------------|--------------|
|           | LCD1         | LCD2       | LCD1         | LCD2         |
|           | Parallel I/F | Serial I/F | Parallel I/F | Parallel I/F |
| FPFRAME   | XWR          |            | XWR          | XWR          |
| FPLINE    | A0           |            | A0           | A0           |
| FPSHIFT   |              |            |              |              |
| DRDY      |              |            |              |              |
| FPDAT0    | D0           |            | D0           | D0           |
| FPDAT1    | D1           |            | D1           | D1           |
| FPDAT2    | D2           |            | D2           | D2           |
| FPDAT3    | D3           |            | D3           | D3           |
| FPDAT4    | D4           |            | D4           | D4           |
| FPDAT5    | D5           |            | D5           | D5           |
| FPDAT6    | D6           |            | D6           | D6           |
| FPDAT7    | D7           |            | D7           | D7           |
| FPDAT8    | D8           |            | D8           | D8           |
| FPDAT9    | D9           |            | D9           | D9           |
| FPDAT10   | D10          |            | D10          | D10          |
| FPDAT11   | D11          |            | D11          | D11          |
| FPDAT12   | D12          |            | D12          | D12          |
| FPDAT13   | D13          |            | D13          | D13          |
| FPDAT14   | D14          |            | D14          | D14          |
| FPDAT15   | D15          |            | D15          | D15          |
| FPDAT16   | D16          |            | D16          | D16          |
| FPDAT17   | D17          |            | D17          | D17          |
| FPCS1#    | NCS1         |            | NCS1         |              |
| FPCS2#    |              | NCS2       |              | NCS2         |
| FPCLK     |              | SCK        |              |              |
| FPA0      |              | A0         |              |              |
| FPSO      |              | SI         |              |              |
| FPVIN1    | VIN1         |            | VIN1         |              |
| FPVIN2    |              | VIN2       |              | VIN2         |
| GPIO0     | GPIO0        | GPIO0      | GPIO0        | GPIO0        |
| GPIO1     | GPIO1        | GPIO1      | GPIO1        | GPIO1        |
| GPIO2     | GPIO2        | GPIO2      | GPIO2        | GPIO2        |
| GPIO3     | GPIO3        | GPIO3      | GPIO3        | GPIO3        |
| GPIO4     | GPIO4        | GPIO4      | GPIO4        | GPIO4        |
| GPIO5     | GPIO5        | GPIO5      | GPIO5        | GPIO5        |
| GPIO6     | D18          | GPIO6      | D18          | D18          |
| GPIO7     | D19          | GPIO7      | D19          | D19          |
| GPIO8     | D20          | GPIO8      | D20          | D20          |
| GPIO9     | D21          | GPIO9      | D21          | D21          |
| GPIO10    | D22          | GPIO10     | D22          | D22          |
| GPIO11    | D23          | GPIO11     | D23          | D23          |
| GPIO12    | GPIO12       | GPIO12     | GPIO12       | GPIO12       |
| GPIO13    | GPIO13       | GPIO13     | GPIO13       | GPIO13       |
| GPIO14-21 | GPIO14-21    | GPIO14-21  | GPIO14-21    | GPIO14-21    |

Table 5-14: LCD Interface Pin Mapping for Mode 4

| Pin Name  | Mode 4      |           |           |                    |             |            |               |            |                            |
|-----------|-------------|-----------|-----------|--------------------|-------------|------------|---------------|------------|----------------------------|
|           | LCD1        |           |           |                    |             |            |               |            | LCD2                       |
|           | General TFT | ND-TFD    | a-Si TFT  | TFT with uWIRE I/F | Sharp HRTFT | Casio TFT  | Samsung α-TFT | Type 2 TFT | Parallel I/F               |
| FPFRAME   | VSYNC       | VSYNC     | VSYNC     | VSYNC              | SPS         | GSRT       | STV           | STV        | XWR                        |
| FPLINE    | HSYNC       | HSYNC     | HSYNC     | HSYNC              | LP          | GPCK       | STH           | STB        | A0                         |
| FPSHIFT   | DCK         | DCK       | DCLK      | CLK                | DCLK        | CLK        | HCLK          | CLK        |                            |
| DRDY      | ENAB        | ENAB      | ENAB      | ENAB               | no connect  | no connect | no connect    | INV        |                            |
| FPDAT0    | R7          | R7        | R7        | R7                 | R7          | R7         | R5            | R7         | D0                         |
| FPDAT1    | R6          | R6        | R6        | R6                 | R6          | R6         | R4            | R6         | D1                         |
| FPDAT2    | R5          | R5        | R5        | R5                 | R5          | R5         | R3            | R5         | D2                         |
| FPDAT3    | G7          | G7        | G7        | G7                 | G7          | G7         | G5            | G7         | D3                         |
| FPDAT4    | G6          | G6        | G6        | G6                 | G6          | G6         | G4            | G6         | D4                         |
| FPDAT5    | G5          | G5        | G5        | G5                 | G5          | G5         | G3            | G5         | D5                         |
| FPDAT6    | B7          | B7        | B7        | B7                 | B7          | B7         | B5            | B7         | D6                         |
| FPDAT7    | B6          | B6        | B6        | B6                 | B6          | B6         | B4            | B6         | D7                         |
| FPDAT8    | B5          | B5        | B5        | B5                 | B5          | B5         | B3            | B5         | D8 <sup>1</sup>            |
| FPDAT9    | R4          | R4        | R4        | R4                 | R4          | R4         | R2            | R4         | D9 <sup>1</sup>            |
| FPDAT10   | R3          | R3        | R3        | R3                 | R3          | R3         | R1            | R3         | D10 <sup>1</sup>           |
| FPDAT11   | R2          | R2        | R2        | R2                 | R2          | R2         | R0            | R2         | D11 <sup>1</sup>           |
| FPDAT12   | G4          | G4        | G4        | G4                 | G4          | G4         | G2            | G4         | D12 <sup>1</sup>           |
| FPDAT13   | G3          | G3        | G3        | G3                 | G3          | G3         | G1            | G3         | D13 <sup>1</sup>           |
| FPDAT14   | G2          | G2        | G2        | G2                 | G2          | G2         | G0            | G2         | D14 <sup>1</sup>           |
| FPDAT15   | B4          | B4        | B4        | B4                 | B4          | B4         | B2            | B4         | D15 <sup>1</sup>           |
| FPDAT16   | B3          | B3        | B3        | B3                 | B3          | B3         | B1            | B3         | D16 <sup>1</sup>           |
| FPDAT17   | B2          | B2        | B2        | B2                 | B2          | B2         | B0            | B2         | D17 <sup>1</sup>           |
| FPCS1#    |             | XCS       | SSTB      | LCDCS              | SPR         |            |               |            |                            |
| FPCS2#    |             |           |           |                    |             |            |               |            | NCS2                       |
| FPCLK     |             | SCK       | SCLK      | SCLK               |             |            |               |            |                            |
| FPA0      |             | A0        |           |                    |             |            |               |            |                            |
| FPSO      |             | SI        | SDATA     | SDO                |             |            |               |            |                            |
| FPVIN1    |             |           |           |                    |             |            |               |            |                            |
| FPVIN2    |             |           |           |                    |             |            |               |            | VIN2                       |
| GPIO0     | GPIO0       | GPIO0     | GPIO0     | GPIO0              | PS          | POL        | CKV           | VCLK       | GPIO0                      |
| GPIO1     | GPIO1       | GPIO1     | GPIO1     | GPIO1              | CLS         | GRES       | LD            | AP         | GPIO1                      |
| GPIO2     | GPIO2       | GPIO2     | GPIO2     | GPIO2              | REV         | FRP        | INV           | POL        | GPIO2                      |
| GPIO3     | GPIO3       | GPIO3     | GPIO3     | GPIO3              | SPL         | STH        | VCOM          | STH        | GPIO3                      |
| GPIO4     | R1          | R1        | R1        | R1                 | R1          | R1         | GPIO4         | R1         | GPIO4                      |
| GPIO5     | R0          | R0        | R0        | R0                 | R0          | R0         | GPIO5         | R0         | GPIO5                      |
| GPIO6     | G1          | G1        | G1        | G1                 | G1          | G1         | GPIO6         | G1         | D18 <sup>1</sup> or GPIO6  |
| GPIO7     | G0          | G0        | G0        | G0                 | G0          | G0         | GPIO7         | G0         | D19 <sup>1</sup> or GPIO7  |
| GPIO8     | B1          | B1        | B1        | B1                 | B1          | B1         | GPIO8         | B1         | D20 <sup>1</sup> or GPIO8  |
| GPIO9     | B0          | B0        | B0        | B0                 | B0          | B0         | GPIO9         | B0         | D21 <sup>1</sup> or GPIO9  |
| GPIO10    | GPIO10      | GPIO10    | GPIO10    | GPIO10             | GPIO10      | GPIO10     | GPIO10        | GPIO10     | D22 <sup>1</sup> or GPIO10 |
| GPIO11    | GPIO11      | GPIO11    | GPIO11    | GPIO11             | GPIO11      | GPIO11     | GPIO11        | GPIO11     | D23 <sup>1</sup> or GPIO11 |
| GPIO12    | GPIO12      | GPIO12    | GPIO12    | GPIO12             | GPIO12      | GPIO12     | GPIO12        | GPIO12     | GPIO12                     |
| GPIO13    | GPIO13      | GPIO13    | GPIO13    | GPIO13             | GPIO13      | GPIO13     | GPIO13        | GPIO13     | GPIO13                     |
| GPIO14-21 | GPIO14-21   | GPIO14-21 | GPIO14-21 | GPIO14-21          | GPIO14-21   | GPIO14-21  | GPIO14-21     | GPIO14-21  | GPIO14-21                  |

**Note**

<sup>1</sup> Mode 4 supports 24-bit parallel panels if LCD Bypass Mode is not required. If LCD Bypass Mode is required, the bypass data is only 8-bit.

Table 5-15: Serial/Parallel Bypass Pin Mapping

|                        |      | LCD I/F Mode 1            |                 | LCD I/F Mode 2                             |               |                 | LCD I/F Mode 3                                           |                 | LCD I/F Mode 4                      |                 |
|------------------------|------|---------------------------|-----------------|--------------------------------------------|---------------|-----------------|----------------------------------------------------------|-----------------|-------------------------------------|-----------------|
| REG[0032h] bits 1-0    |      | 00                        |                 | 10                                         |               |                 | 11                                                       |                 | 01                                  |                 |
| REG[0014h] bits 10-8   |      | 010                       | 000             | 001                                        | 010           | 000             | 011                                                      | 000             | 100                                 | 000             |
| LCD1, LCD2 Panel Types |      | LCD1: RGB<br>LCD2: Serial |                 | LCD1: Parallel (16/18-bit)<br>LCD2: Serial |               |                 | LCD1: Parallel (16/18-bit)<br>LCD2: Parallel (16/18-bit) |                 | LCD1: RGB<br>LCD2: Parallel (8-bit) |                 |
| Pin Name               | Type | Serial Bypass             | Bypass Disabled | Parallel Bypass                            | Serial Bypass | Bypass Disabled | Parallel Bypass                                          | Bypass Disabled | Parallel Bypass                     | Bypass Disabled |
| SCS#                   | I    | SCS#                      |                 |                                            | SCS#          |                 | PCS2#                                                    |                 | PCS#                                |                 |
| SCLK                   | I    | SCLK                      |                 | PWR#                                       | SCLK          |                 | PWR#                                                     |                 | PWR#                                |                 |
| SA0                    | I    | SA0                       |                 | PA0                                        | SA0           |                 | PA0                                                      |                 | PA0                                 |                 |
| SI                     | I    | SI                        |                 | PCS#                                       | SI            |                 | PCS1#                                                    |                 |                                     |                 |
| GPIO0                  | IO   | RGB or GPIO0              | RGB or GPIO0    | GPIO0                                      | GPIO0         | GPIO0           | GPIO0                                                    | GPIO0           | RGB or GPIO0                        | RGB or GPIO0    |
| GPIO1                  | IO   | RGB or GPIO1              | RGB or GPIO1    | GPIO1                                      | GPIO1         | GPIO1           | GPIO1                                                    | GPIO1           | RGB or GPIO1                        | RGB or GPIO1    |
| GPIO2                  | IO   | RGB or GPIO2              | RGB or GPIO2    | GPIO2                                      | GPIO2         | GPIO2           | GPIO2                                                    | GPIO2           | RGB or GPIO2                        | RGB or GPIO2    |
| GPIO3                  | IO   | RGB or GPIO3              | RGB or GPIO3    | GPIO3                                      | GPIO3         | GPIO3           | GPIO3                                                    | GPIO3           | RGB or GPIO3                        | RGB or GPIO3    |
| GPIO4                  | IO   | RGB                       | RGB             | PI0                                        | GPIO4         | GPIO4           | PI0                                                      | GPIO4           | RGB                                 | RGB             |
| GPIO5                  | IO   | RGB                       | RGB             | PI1                                        | GPIO5         | GPIO5           | PI1                                                      | GPIO5           | RGB                                 | RGB             |
| GPIO6                  | IO   | RGB                       | RGB             | PI2                                        | D18           | D18             | PI2                                                      | D18             | RGB                                 | RGB             |
| GPIO7                  | IO   | RGB                       | RGB             | PI3                                        | D19           | D19             | PI3                                                      | D19             | RGB                                 | RGB             |
| GPIO8                  | IO   | RGB                       | RGB             | PI4                                        | D20           | D20             | PI4                                                      | D20             | RGB                                 | RGB             |
| GPIO9                  | IO   | RGB or GPIO9              | RGB or GPIO9    | PI5                                        | D21           | D21             | PI5                                                      | D21             | RGB or GPIO9                        | RGB or GPIO9    |
| GPIO10                 | IO   | GPIO10                    | GPIO10          | PI6                                        | D22           | D22             | PI6                                                      | D22             | GPIO10                              | GPIO10          |
| GPIO11                 | IO   | GPIO11                    | GPIO11          | PI7                                        | D23           | D23             | PI7                                                      | D23             | GPIO11                              | GPIO11          |
| GPIO12                 | IO   | GPIO12                    | GPIO12          | PI8                                        | GPIO12        | GPIO12          | PI8                                                      | GPIO12          | GPIO12                              | GPIO12          |
| GPIO13                 | IO   | GPIO13                    | GPIO13          | PI9                                        | GPIO13        | GPIO13          | PI9                                                      | GPIO13          | GPIO13                              | GPIO13          |
| GPIO14                 | IO   | GPIO14                    | GPIO14          | PI10                                       | GPIO14        | GPIO14          | PI10                                                     | GPIO14          | PI0                                 | GPIO14          |
| GPIO15                 | IO   | GPIO15                    | GPIO15          | PI11                                       | GPIO15        | GPIO15          | PI11                                                     | GPIO15          | PI1                                 | GPIO15          |
| GPIO16                 | IO   | GPIO16                    | GPIO16          | PI12                                       | GPIO16        | GPIO16          | PI12                                                     | GPIO16          | PI2                                 | GPIO16          |
| GPIO17                 | IO   | GPIO17                    | GPIO17          | PI13                                       | GPIO17        | GPIO17          | PI13                                                     | GPIO17          | PI3                                 | GPIO17          |
| GPIO18                 | IO   | GPIO18                    | GPIO18          | PI14                                       | GPIO18        | GPIO18          | PI14                                                     | GPIO18          | PI4                                 | GPIO18          |
| GPIO19                 | IO   | GPIO19                    | GPIO19          | PI15                                       | GPIO19        | GPIO19          | PI15                                                     | GPIO19          | PI5                                 | GPIO19          |
| GPIO20                 | IO   | GPIO20                    | GPIO20          | PI16 or GPIO20                             | GPIO20        | GPIO20          | PI16 or GPIO20                                           | GPIO20          | PI6                                 | GPIO20          |
| GPIO21                 | IO   | GPIO21                    | GPIO21          | PI17 or GPIO21                             | GPIO21        | GPIO21          | PI17 or GPIO21                                           | GPIO21          | PI7                                 | GPIO21          |
| FPFRAME                | O    | RGB                       | RGB             | XWR                                        | XWR           | XWR             | XWR                                                      | XWR             | RGB or XWR                          | RGB or XWR      |
| FPLINE                 | O    | RGB                       | RGB             | A0                                         | A0            | A0              | A0                                                       | A0              | RGB or A0                           | RGB or A0       |
| FPSHIFT                | O    | RGB                       | RGB             | —                                          | —             | —               | —                                                        | —               | RGB                                 | RGB             |
| DRDY                   | O    | RGB                       | RGB             | —                                          | —             | —               | —                                                        | —               | RGB                                 | RGB             |
| FPDAT0                 | O    | RGB                       | RGB             | D0                                         | D0            | D0              | D0                                                       | D0              | RGB or D0                           | RGB or D0       |
| FPDAT1                 | O    | RGB                       | RGB             | D1                                         | D1            | D1              | D1                                                       | D1              | RGB or D1                           | RGB or D1       |
| FPDAT2                 | O    | RGB                       | RGB             | D2                                         | D2            | D2              | D2                                                       | D2              | RGB or D2                           | RGB or D2       |
| FPDAT3                 | O    | RGB                       | RGB             | D3                                         | D3            | D3              | D3                                                       | D3              | RGB or D3                           | RGB or D3       |
| FPDAT4                 | O    | RGB                       | RGB             | D4                                         | D4            | D4              | D4                                                       | D4              | RGB or D4                           | RGB or D4       |
| FPDAT5                 | O    | RGB                       | RGB             | D5                                         | D5            | D5              | D5                                                       | D5              | RGB or D5                           | RGB or D5       |
| FPDAT6                 | O    | RGB                       | RGB             | D6                                         | D6            | D6              | D6                                                       | D6              | RGB or D6                           | RGB or D6       |
| FPDAT7                 | O    | RGB                       | RGB             | D7                                         | D7            | D7              | D7                                                       | D7              | RGB or D7                           | RGB or D7       |
| FPDAT8                 | O    | RGB                       | RGB             | D8                                         | D8            | D8              | D8                                                       | D8              | RGB                                 | RGB             |
| FPDAT9                 | O    | RGB                       | RGB             | D9                                         | D9            | D9              | D9                                                       | D9              | RGB                                 | RGB             |
| FPDAT10                | O    | RGB                       | RGB             | D10                                        | D10           | D10             | D10                                                      | D10             | RGB                                 | RGB             |
| FPDAT11                | O    | RGB                       | RGB             | D11                                        | D11           | D11             | D11                                                      | D11             | RGB                                 | RGB             |
| FPDAT12                | O    | RGB                       | RGB             | D12                                        | D12           | D12             | D12                                                      | D12             | RGB                                 | RGB             |
| FPDAT13                | O    | RGB                       | RGB             | D13                                        | D13           | D13             | D13                                                      | D13             | RGB                                 | RGB             |
| FPDAT14                | O    | RGB                       | RGB             | D14                                        | D14           | D14             | D14                                                      | D14             | RGB                                 | RGB             |
| FPDAT15                | O    | RGB                       | RGB             | D15                                        | D15           | D15             | D15                                                      | D15             | RGB                                 | RGB             |
| FPDAT16                | O    | RGB                       | RGB             | D16                                        | D16           | D16             | D16                                                      | D16             | RGB                                 | RGB             |
| FPDAT17                | O    | RGB                       | RGB             | D17                                        | D17           | D17             | D17                                                      | D17             | RGB                                 | RGB             |
| FPCS1#                 | O    | RGB                       | RGB             | NCS1                                       | NCS1          | NCS1            | NCS1                                                     | —               | RGB                                 | RGB             |
| FPCS2#                 | O    | NCS2                      | NCS2            | NCS2                                       | NCS2          | NCS2            | NCS2                                                     | NCS2            | NCS2                                | NCS2            |
| FPSCLK                 | O    | RGB or SCK                | RGB             | SCK                                        | SCK           | SCK             | —                                                        | —               | RGB                                 | RGB             |
| FPA0                   | O    | RGB or A0                 | RGB             | A0                                         | A0            | A0              | —                                                        | —               | RGB                                 | RGB             |
| FPSO                   | O    | RGB or SI                 | RGB             | SI                                         | SI            | SI              | —                                                        | —               | RGB                                 | RGB             |
| FPVIN1                 | I    | RGB                       | RGB             | VIN1                                       | VIN1          | VIN1            | VIN1                                                     | VIN1            | RGB                                 | RGB             |
| FPVIN2                 | I    | VIN2                      | VIN2            | VIN2                                       | VIN2          | VIN2            | VIN2                                                     | VIN2            | VIN2                                | VIN2            |

Input port when bypass is used

Output port when bypass is used

When bypass is not used, pull-up/pull-down resistors can be set using REG[0014h] bit 4

1. RGB refers to the signals used for RGB panels.

Table 5-16: LCD Interface Mode 1/2 Bypass Endian/Data Width Pin Mapping

| Panel Mode            | LCD I/F Mode1 |         | LCD I/F Mode2   |         |        |         |        |         |        |         |               |         |
|-----------------------|---------------|---------|-----------------|---------|--------|---------|--------|---------|--------|---------|---------------|---------|
| Bypass Mode           | Serial Bypass |         | Parallel Bypass |         |        |         |        |         |        |         | Serial Bypass |         |
| REG[0014h] bits 12-11 | -             |         | 00              |         | 01     |         | 10     |         | 11     |         | -             |         |
| Input/Output          | Input         | Output  | Input           | Output  | Input  | Output  | Input  | Output  | Input  | Output  | Input         | Output  |
| Pin Mapping           | SCS#          | FPCS2#  |                 |         |        |         |        |         |        |         | SCS#          | FPCS2#  |
|                       | SCLK          | FPSCCLK | SCLK            | FPFRAME | SCLK   | FPFRAME | SCLK   | FPFRAME | SCLK   | FPFRAME | SCLK          | FPSCCLK |
|                       | SA0           | FPA0    | SA0             | FPLINE  | SA0    | FPLINE  | SA0    | FPLINE  | SA0    | FPLINE  | SA0           | FPA0    |
|                       | SI            | FPSO    | SI              | FPCS1#  | SI     | FPCS1#  | SI     | FPCS1#  | SI     | FPCS1#  | SI            | FPSO    |
|                       |               |         | GPIO4           | FPDAT0  | GPIO4  | FPDAT17 | GPIO4  | FPDAT0  | GPIO4  | FPDAT17 |               |         |
|                       |               |         | GPIO5           | FPDAT1  | GPIO5  | FPDAT16 | GPIO5  | FPDAT1  | GPIO5  | FPDAT16 |               |         |
|                       |               |         | GPIO6           | FPDAT2  | GPIO6  | FPDAT15 | GPIO6  | FPDAT2  | GPIO6  | FPDAT15 |               |         |
|                       |               |         | GPIO7           | FPDAT3  | GPIO7  | FPDAT14 | GPIO7  | FPDAT3  | GPIO7  | FPDAT14 |               |         |
|                       |               |         | GPIO8           | FPDAT4  | GPIO8  | FPDAT13 | GPIO8  | FPDAT4  | GPIO8  | FPDAT13 |               |         |
|                       |               |         | GPIO9           | FPDAT5  | GPIO9  | FPDAT12 | GPIO9  | FPDAT5  | GPIO9  | FPDAT12 |               |         |
|                       |               |         | GPIO10          | FPDAT6  | GPIO10 | FPDAT11 | GPIO10 | FPDAT6  | GPIO10 | FPDAT11 |               |         |
|                       |               |         | GPIO11          | FPDAT7  | GPIO11 | FPDAT10 | GPIO11 | FPDAT7  | GPIO11 | FPDAT10 |               |         |
|                       |               |         | GPIO12          | FPDAT8  | GPIO12 | FPDAT9  | GPIO12 | FPDAT8  | GPIO12 | FPDAT9  |               |         |
|                       |               |         | GPIO13          | FPDAT9  | GPIO13 | FPDAT8  | GPIO13 | FPDAT9  | GPIO13 | FPDAT8  |               |         |
|                       |               |         | GPIO14          | FPDAT10 | GPIO14 | FPDAT7  | GPIO14 | FPDAT10 | GPIO14 | FPDAT7  |               |         |
|                       |               |         | GPIO15          | FPDAT11 | GPIO15 | FPDAT6  | GPIO15 | FPDAT11 | GPIO15 | FPDAT6  |               |         |
|                       |               |         | GPIO16          | FPDAT12 | GPIO16 | FPDAT5  | GPIO16 | FPDAT12 | GPIO16 | FPDAT5  |               |         |
|                       |               |         | GPIO17          | FPDAT13 | GPIO17 | FPDAT4  | GPIO17 | FPDAT13 | GPIO17 | FPDAT4  |               |         |
|                       |               |         | GPIO18          | FPDAT14 | GPIO18 | FPDAT3  | GPIO18 | FPDAT14 | GPIO18 | FPDAT3  |               |         |
|                       |               |         | GPIO19          | FPDAT15 | GPIO19 | FPDAT2  | GPIO19 | FPDAT15 | GPIO19 | FPDAT2  |               |         |
|                       |               |         |                 |         |        |         | GPIO20 | FPDAT16 | GPIO20 | FPDAT1  |               |         |
|                       |               |         |                 |         |        |         | GPIO21 | FPDAT17 | GPIO21 | FPDAT0  |               |         |

Table 5-17: LCD Interface Mode 3/4 Bypass Endian/Data Width Pin Mapping

| Panel Mode            | LCD I/F Mode3   |         |        |         |        |         |        |         | LCD I/F Mode4   |         |
|-----------------------|-----------------|---------|--------|---------|--------|---------|--------|---------|-----------------|---------|
| Bypass Mode           | Parallel Bypass |         |        |         |        |         |        |         | Parallel Bypass |         |
| REG[0014h] bits 12-11 | 00              |         | 01     |         | 10     |         | 11     |         | -               |         |
| Input/Output          | Input           | Output  | Input  | Output  | Input  | Output  | Input  | Output  | Input           | Output  |
| Pin Mapping           | SCS#            | FPCS2#  | SCS#   | FPCS2#  | SCS#   | FPCS2#  | SCS#   | FPCS2#  | SCS#            | FPCS2#  |
|                       | SCLK            | FPFRAME | SCLK   | FPFRAME | SCLK   | FPFRAME | SCLK   | FPFRAME | SCLK            | FPFRAME |
|                       | SA0             | FPLINE  | SA0    | FPLINE  | SA0    | FPLINE  | SA0    | FPLINE  | SA0             | FPLINE  |
|                       | SI              | FPCS1#  | SI     | FPCS1#  | SI     | FPCS1#  | SI     | FPCS1#  |                 |         |
|                       | GPIO4           | FPDAT0  | GPIO4  | FPDAT17 | GPIO4  | FPDAT0  | GPIO4  | FPDAT17 |                 |         |
|                       | GPIO5           | FPDAT1  | GPIO5  | FPDAT16 | GPIO5  | FPDAT1  | GPIO5  | FPDAT16 |                 |         |
|                       | GPIO6           | FPDAT2  | GPIO6  | FPDAT15 | GPIO6  | FPDAT2  | GPIO6  | FPDAT15 |                 |         |
|                       | GPIO7           | FPDAT3  | GPIO7  | FPDAT14 | GPIO7  | FPDAT3  | GPIO7  | FPDAT14 |                 |         |
|                       | GPIO8           | FPDAT4  | GPIO8  | FPDAT13 | GPIO8  | FPDAT4  | GPIO8  | FPDAT13 |                 |         |
|                       | GPIO9           | FPDAT5  | GPIO9  | FPDAT12 | GPIO9  | FPDAT5  | GPIO9  | FPDAT12 |                 |         |
|                       | GPIO10          | FPDAT6  | GPIO10 | FPDAT11 | GPIO10 | FPDAT6  | GPIO10 | FPDAT11 |                 |         |
|                       | GPIO11          | FPDAT7  | GPIO11 | FPDAT10 | GPIO11 | FPDAT7  | GPIO11 | FPDAT10 |                 |         |
|                       | GPIO12          | FPDAT8  | GPIO12 | FPDAT9  | GPIO12 | FPDAT8  | GPIO12 | FPDAT9  |                 |         |
|                       | GPIO13          | FPDAT9  | GPIO13 | FPDAT8  | GPIO13 | FPDAT9  | GPIO13 | FPDAT8  |                 |         |
|                       | GPIO14          | FPDAT10 | GPIO14 | FPDAT7  | GPIO14 | FPDAT10 | GPIO14 | FPDAT7  | GPIO14          | FPDAT0  |
|                       | GPIO15          | FPDAT11 | GPIO15 | FPDAT6  | GPIO15 | FPDAT11 | GPIO15 | FPDAT6  | GPIO15          | FPDAT1  |
|                       | GPIO16          | FPDAT12 | GPIO16 | FPDAT5  | GPIO16 | FPDAT12 | GPIO16 | FPDAT5  | GPIO16          | FPDAT2  |
|                       | GPIO17          | FPDAT13 | GPIO17 | FPDAT4  | GPIO17 | FPDAT13 | GPIO17 | FPDAT4  | GPIO17          | FPDAT3  |
|                       | GPIO18          | FPDAT14 | GPIO18 | FPDAT3  | GPIO18 | FPDAT14 | GPIO18 | FPDAT3  | GPIO18          | FPDAT4  |
|                       | GPIO19          | FPDAT15 | GPIO19 | FPDAT2  | GPIO19 | FPDAT15 | GPIO19 | FPDAT2  | GPIO19          | FPDAT5  |
|                       |                 |         |        |         | GPIO20 | FPDAT16 | GPIO20 | FPDAT1  | GPIO20          | FPDAT6  |
|                       |                 |         |        |         | GPIO21 | FPDAT17 | GPIO21 | FPDAT0  | GPIO21          | FPDAT7  |

## 5.7 Camera Interface Pin Mapping

### 5.7.1 Camera1 Interface Pin Mapping

*Table 5-18: Camera1 Interface Pin Mapping*

| Pin Name    | Type 1 Camera |
|-------------|---------------|
| CM1DAT[7:0] | CAMDAT[7:0]   |
| CM1VREF     | VREF          |
| CM1HREF     | HREF          |
| CM1CLKOUT   | CAMMCLK       |
| CM1CLKIN    | CAMPCLK       |
| GPIO21      | GPIO21        |
| GPIO20      | GPIO20        |

### 5.7.2 Camera2 Interface Pin Mapping

*Table 5-19: Camera2 Interface Pin Mapping*

| Pin Name    | Camera      | MPEG Codec Interface |
|-------------|-------------|----------------------|
| CM2DAT[7:0] | CAMDAT[7:0] | DISPPXL[7:0]         |
| CM2VREF     | VREF        | DISPVSYN             |
| CM2HREF     | HREF        | DISPHSYN             |
| CM2CLKOUT   | CAMMCLK     | DISPCLK              |
| CM2CLKIN    | CMCLKIN     | DISPBLK              |

## 6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

| Symbol        | Parameter      | Rating                               | Units |
|---------------|----------------|--------------------------------------|-------|
| Core $V_{DD}$ | Supply Voltage | $V_{SS} - 0.3 \sim 2.5$              | V     |
| PLL $V_{DD}$  | Supply Voltage | $V_{SS} - 0.3 \sim 2.1$              | V     |
| IO $V_{DD}$   | Supply Voltage | $V_{SS} - 0.3 \sim 4.0$              | V     |
| $V_{IN}$      | Input Voltage  | $V_{SS} - 0.3 \sim IO\ V_{DD} + 0.5$ | V     |
| $V_{OUT}$     | Output Voltage | $V_{SS} - 0.3 \sim IO\ V_{DD} + 0.5$ | V     |

Table 6-2: Recommended Operating Conditions

| Symbol        | Parameter             | Condition             | Min      | Typ | Max          | Units |
|---------------|-----------------------|-----------------------|----------|-----|--------------|-------|
| Core $V_{DD}$ | Supply Voltage        | $V_{SS} = 0\text{ V}$ | 1.65     | 1.8 | 1.95         | V     |
| PLL $V_{DD}$  | Supply Voltage        | $V_{SS} = 0\text{ V}$ | 1.65     | 1.8 | 1.95         | V     |
| HIO $V_{DD}$  | Supply Voltage        | $V_{SS} = 0\text{ V}$ | 2.75     | 3.0 | 3.25         | V     |
| PIO $V_{DD}$  | Supply Voltage        | $V_{SS} = 0\text{ V}$ | 2.75     | 3.0 | 3.25         | V     |
| CIO $V_{DD}$  | Supply Voltage        | $V_{SS} = 0\text{ V}$ | 2.75     | 3.0 | 3.25         | V     |
| $V_{IN}$      | Input Voltage         |                       | $V_{SS}$ |     | HIO $V_{DD}$ | V     |
|               |                       |                       | $V_{SS}$ |     | PIO $V_{DD}$ |       |
|               |                       |                       | $V_{SS}$ |     | CIO $V_{DD}$ |       |
| $T_{OPR}$     | Operating Temperature |                       | -40      | 25  | 85           | °C    |

## D.C. Characteristics

Table 6-3: Electrical Characteristics for  $V_{DD} = 3.0V$  typical

| Symbol      | Parameter                      | Condition                               | Min               | Typ | Max  | Units     |
|-------------|--------------------------------|-----------------------------------------|-------------------|-----|------|-----------|
| $I_{DDSH}$  | IO Quiescent Current           | Quiescent Conditions                    |                   | 10  |      | $\mu A$   |
| $I_{DDSL}$  | CORE Quiescent Current         | Quiescent Conditions                    |                   | 10  |      | $\mu A$   |
| $I_{IZ}$    | Input Leakage Current          |                                         | -5                |     | 5    | $\mu A$   |
| $I_{OZ}$    | Output Leakage Current         |                                         | -5                |     | 5    | $\mu A$   |
| $HIOV_{OH}$ | High Level Output Voltage      | $HIOV_{DD} = \min$<br>$I_{OH} = -3.6mA$ | $HIOV_{DD} - 0.4$ |     |      | V         |
| $CIOV_{OH}$ | High Level Output Voltage      | $CIOV_{DD} = \min$<br>$I_{OH} = -3.6mA$ | $CIOV_{DD} - 0.4$ |     |      | V         |
| $PIOV_{OH}$ | High Level Output Voltage      | $PIOV_{DD} = \min$<br>$I_{OH} = -3.6mA$ | $PIOV_{DD} - 0.4$ |     |      | V         |
| $HIOV_{OL}$ | Low Level Output Voltage       | $HIOV_{DD} = \min$<br>$I_{OL} = 3.6mA$  |                   |     | 0.4  | V         |
| $CIOV_{OL}$ | Low Level Output Voltage       | $CIOV_{DD} = \min$<br>$I_{OL} = 3.6mA$  |                   |     | 0.4  | V         |
| $PIOV_{OL}$ | Low Level Output Voltage       | $PIOV_{DD} = \min$<br>$I_{OL} = 3.6mA$  |                   |     | 0.4  | V         |
| $HIOV_{IH}$ | High Level Input Voltage       | LVC MOS Level, $V_{DD} = \max$          | 1.95              |     |      | V         |
| $CIOV_{IH}$ | High Level Input Voltage       | LVC MOS Level, $V_{DD} = \max$          | 1.95              |     |      | V         |
| $PIOV_{IH}$ | High Level Input Voltage       | LVC MOS Level, $V_{DD} = \max$          | 1.95              |     |      | V         |
| $HIOV_{IL}$ | Low Level Input Voltage        | LVC MOS Level, $V_{DD} = \min$          |                   |     | 0.85 | V         |
| $CIOV_{IL}$ | Low Level Input Voltage        | LVC MOS Level, $V_{DD} = \min$          |                   |     | 0.85 | V         |
| $PIOV_{IL}$ | Low Level Input Voltage        | LVC MOS Level, $V_{DD} = \min$          |                   |     | 0.85 | V         |
| $HIOV_{T+}$ | Positive Trigger Voltage       | LVC MOS Schmitt                         | 1.35              |     | 2.5  | V         |
| $CIOV_{T+}$ | Positive Trigger Voltage       | LVC MOS Schmitt                         | 1.35              |     | 2.5  | V         |
| $PIOV_{T+}$ | Positive Trigger Voltage       | LVC MOS Schmitt                         | 1.35              |     | 2.5  | V         |
| $HIOV_{T-}$ | Negative Trigger Voltage       | LVC MOS Schmitt                         | 0.7               |     | 1.6  | V         |
| $CIOV_{T-}$ | Negative Trigger Voltage       | LVC MOS Schmitt                         | 0.7               |     | 1.6  | V         |
| $PIOV_{T-}$ | Negative Trigger Voltage       | LVC MOS Schmitt                         | 0.7               |     | 1.6  | V         |
| $R_{PD}$    | Pull Down Resistance           | $V_{IN} = V_{DD}$                       | 30                | 60  | 144  | $k\Omega$ |
| $R_{PU}$    | Pull Up Resistance             | $V_{IN} = V_{DD}$                       | 30                | 60  | 144  | $k\Omega$ |
| $C_I$       | Input Pin Capacitance          | $f = 1MHz, V_{DD} = 0V$                 | -                 | -   | 8    | pF        |
| $C_O$       | Output Pin Capacitance         | $f = 1MHz, V_{DD} = 0V$                 | -                 | -   | 8    | pF        |
| $C_{IO}$    | Bi-Directional Pin Capacitance | $f = 1MHz, V_{DD} = 0V$                 | -                 | -   | 8    | pF        |

## 7 A.C. Characteristics

Conditions: IO  $V_{DD} = 3.0V \pm 0.25V$

$T_A = -40^\circ C$  to  $85^\circ C$

$T_{rise}$  and  $T_{fall}$  for all inputs except CLKI must be  $\leq 50$  ns (10% ~ 90%)

$C_L = 15pF$  (Host Interface)

$C_L = 15pF$  (Camera Interface)

$C_L = 30pF$  (LCD Panel/GPIO Interface)

### 7.1 Clock Timing

#### 7.1.1 Input Clocks

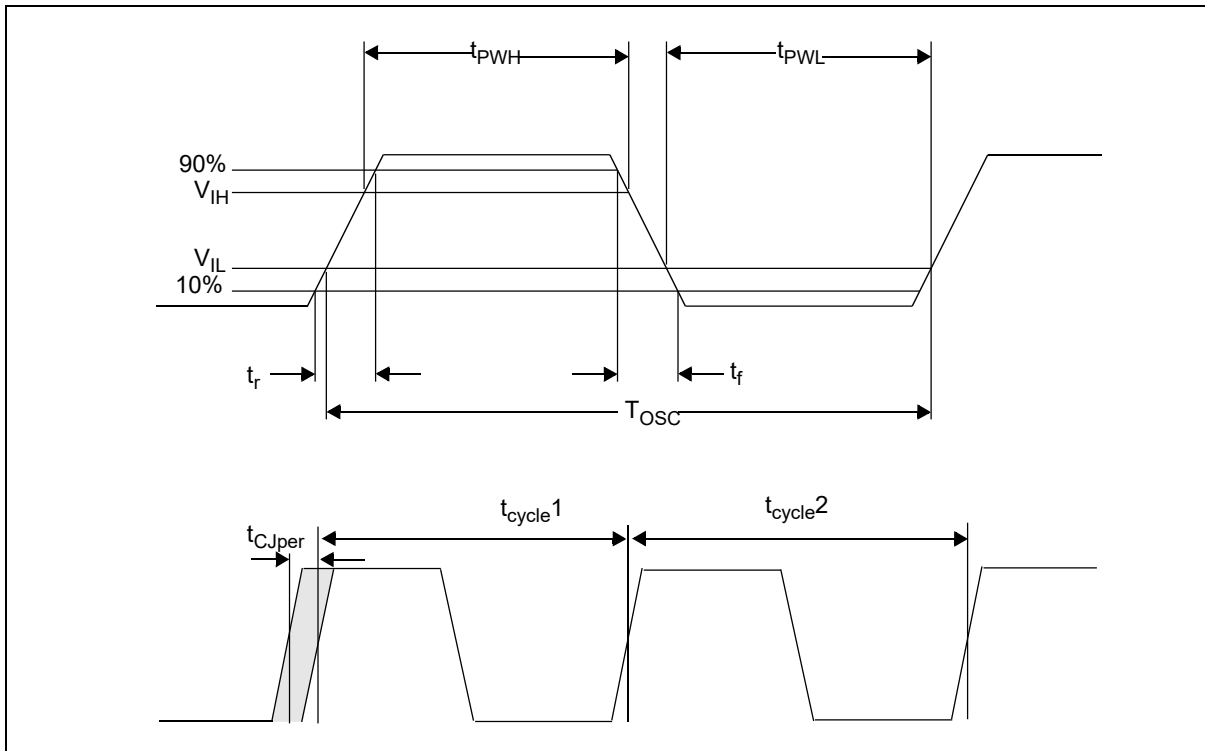


Figure 7-1: Clock Input Requirements (PLL)

## A.C. Characteristics

Table 7-1: Clock Input Requirements (PLL)

| Symbol                        | Parameter                                     | Min  | Typ         | Max | Units |
|-------------------------------|-----------------------------------------------|------|-------------|-----|-------|
| $f_{OSC}$                     | Input clock frequency                         | 30   | 32.768      | 64  | KHz   |
| $T_{OSC}$                     | Input clock period                            |      | $1/f_{OSC}$ |     | us    |
| $t_{PWH}$                     | Input clock pulse width high                  | 5    |             |     | us    |
| $t_{PWL}$                     | Input clock pulse width low                   | 5    |             |     | us    |
| $t_r$                         | Input clock rising time (10% - 90%)           |      |             | 5   | us    |
| $t_f$                         | Input clock falling time (10% - 90%)          |      |             | 5   | us    |
| $t_{CJper}$                   | Input clock period jitter (see notes 2 and 4) | -100 |             | 100 | ns    |
| $t_{CJcycle}$<br>(see note 1) | Input clock cycle jitter (see notes 3 and 4)  | -100 |             | 100 | ns    |

1.  $t_{CJcycle} = t_{cycle1} - t_{cycle2}$
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the  $t_{CJper}$  and  $t_{CJcycle}$  characteristics.

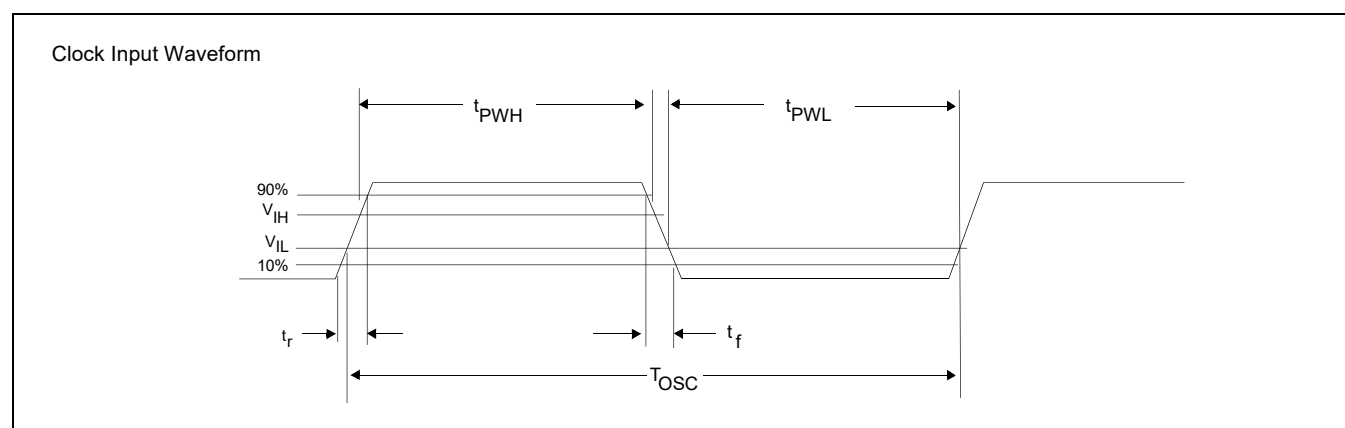


Figure 7-2: Clock Input Requirements (PLL bypassed)

Table 7-2: Clock Input Requirements (PLL bypassed)

| Symbol    | Parameter                            | Min          | Max | Units |
|-----------|--------------------------------------|--------------|-----|-------|
| $f_{OSC}$ | Input Clock Frequency (CLKI)         |              | 55  | MHz   |
| $T_{OSC}$ | Input Clock period (CLKI)            | $1/f_{OSC}$  |     | ns    |
| $t_{PWH}$ | Input Clock Pulse Width High (CLKI)  | $0.4T_{OSC}$ |     | ns    |
| $t_{PWL}$ | Input Clock Pulse Width Low (CLKI)   | $0.4T_{OSC}$ |     | ns    |
| $t_r$     | Input clock rising time (10% - 90%)  |              | 5   | ns    |
| $t_f$     | Input clock falling time (10% - 90%) |              | 5   | ns    |

### 7.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

For example, if noise with a 2KHz frequency modulation is added on PLLVDD, the jitter on the PLL clock output may fluctuate. Measures must be taken to avoid noise within the range of 1KHz to 3KHz.

The specific design should be confirmed to determine the jitter value of a clock. This is because the actual jitter characteristics are affected by a combination of factors, such as the jitter frequency spectrum of CLKI, and amplitude and frequency of the noise on the supplied power. If the jitter of a clock exceeds the requirement of a module, an external oscillator should be used instead of using the internal PLL circuitry.

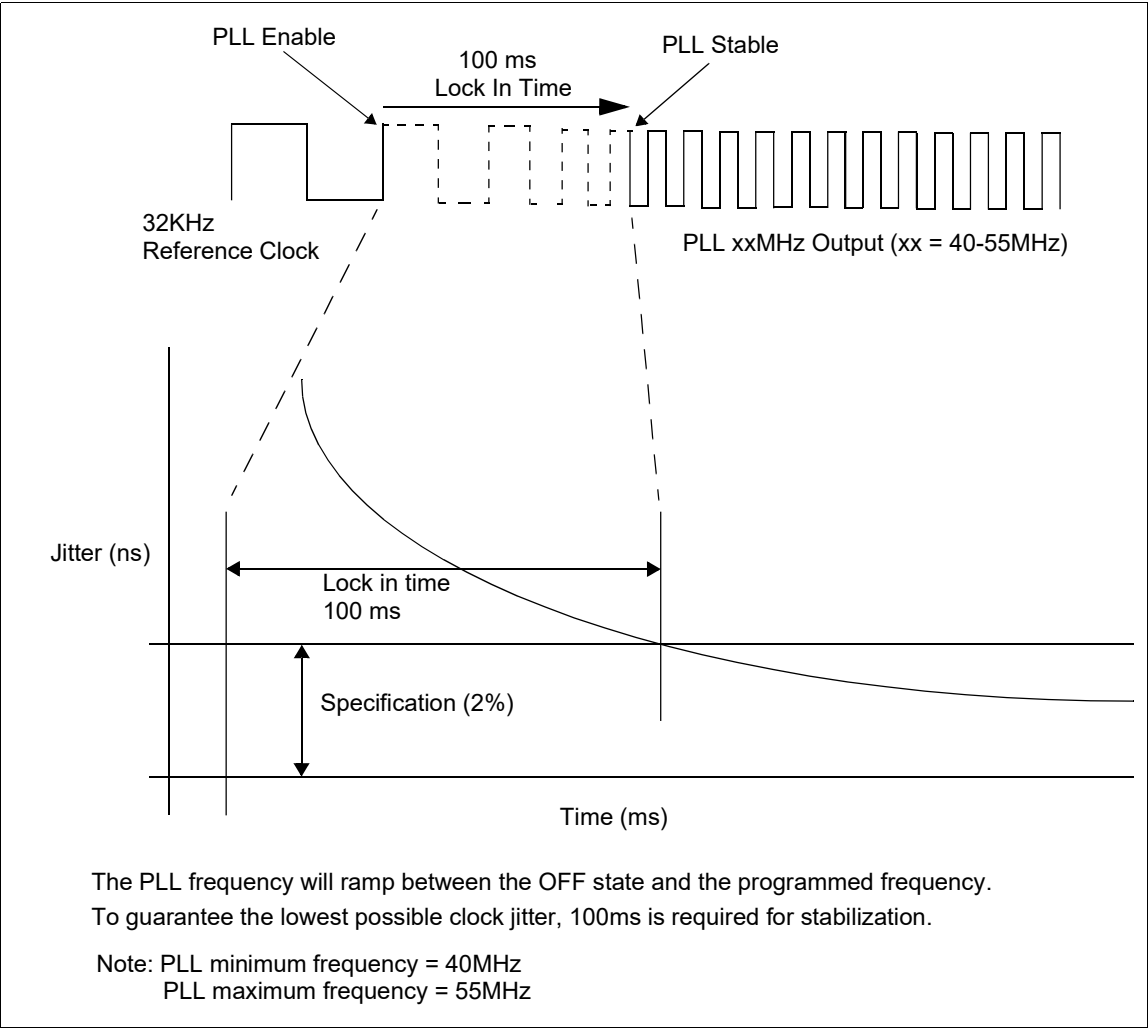


Figure 7-3: PLL Start-Up Time

7.1.3 Internal Clocks

Table 7-3: Internal Clock Requirements

| Symbol           | Parameter                               | Min | Max | Units |
|------------------|-----------------------------------------|-----|-----|-------|
| f <sub>SYS</sub> | Internal Clock Frequency (System Clock) |     | 55  | MHz   |

## 7.2 Power Supply Sequence

### 7.2.1 Power-On Sequence

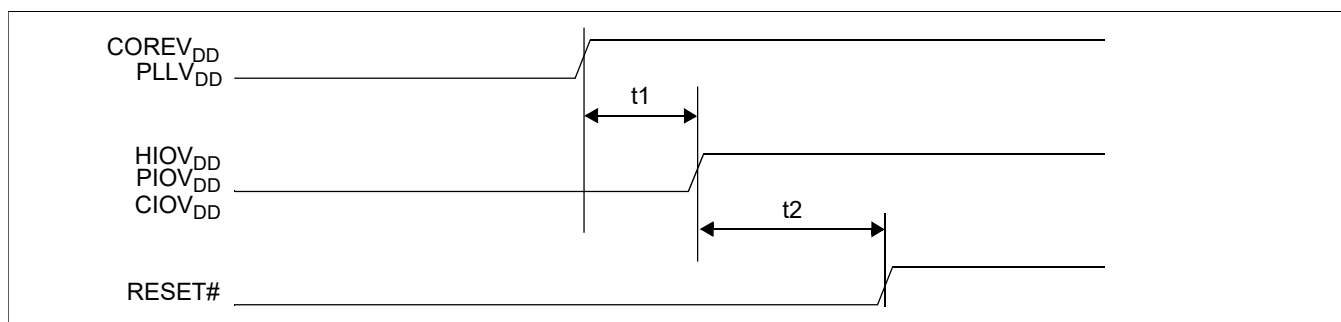


Figure 7-4: Power-On Sequence

Table 7-4: Power-On Sequence

| Symbol | Parameter                                                                   | Min | Max | Units |
|--------|-----------------------------------------------------------------------------|-----|-----|-------|
| t1     | IOV <sub>DD</sub> on delay from COREV <sub>DD</sub> / PLLV <sub>DD</sub> on | 0   |     | ns    |
| t2     | RESET# width period                                                         | 1   |     | CLKI  |

### 7.2.2 Power-Off Sequence

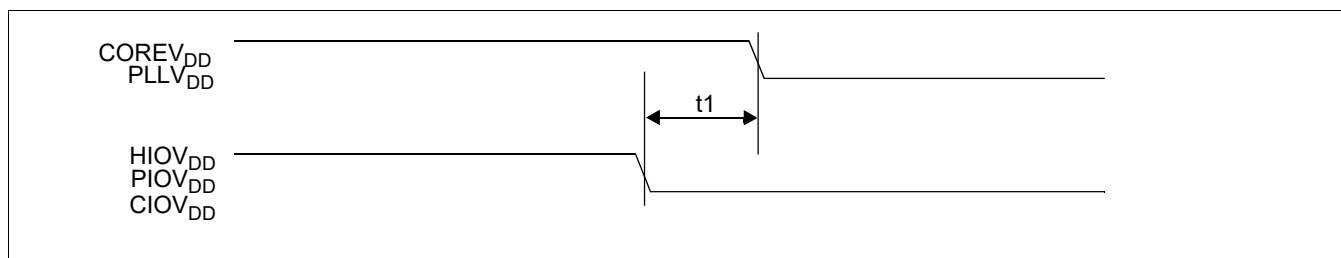


Figure 7-5: Power-Off Sequence

Table 7-5: Power-Off Sequence

| Symbol | Parameter                                                                     | Min | Max | Units |
|--------|-------------------------------------------------------------------------------|-----|-----|-------|
| t1     | COREV <sub>DD</sub> / PLLV <sub>DD</sub> off delay from IOV <sub>DD</sub> off | 0   |     | ns    |

## 7.3 Host Interface Timing

### 7.3.1 Direct 80 Type 1

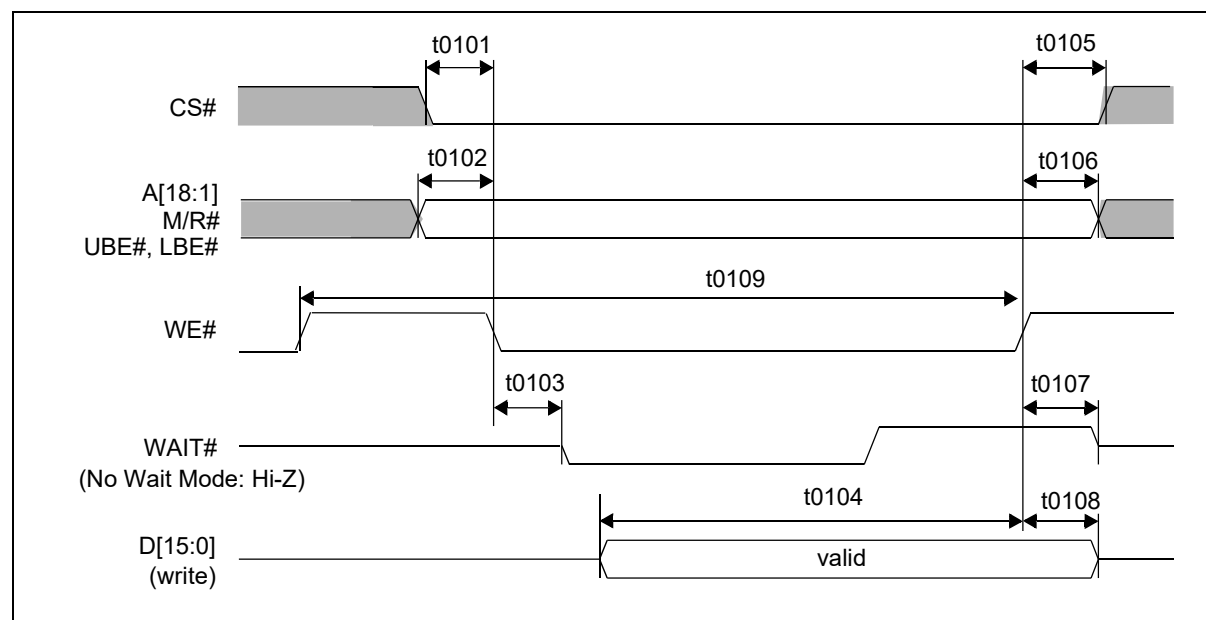


Figure 7-6: Direct 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-6: Direct 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                                | 3.0 Volt |     | Units |
|--------|----------------------------------------------------------|----------|-----|-------|
|        |                                                          | Min      | Max |       |
| t0101  | CS# setup time                                           | 5        |     | ns    |
| t0102  | A[18:1], M/R#, UBE#, LBE# setup time                     | 5        |     | ns    |
| t0103  | WE# falling edge to WAIT# driven low                     |          | 12  | ns    |
| t0104  | D[15:0] setup time to WE# rising edge                    | 15       |     | ns    |
| t0105  | CS# hold time from WE# rising edge                       | 3        |     | ns    |
| t0106  | A[18:1], M/R#, UBE#, LBE# hold time from WE# rising edge | 3        |     | ns    |
| t0107  | WE# rising edge to WAIT# high impedance                  |          | 7   | ns    |
| t0108  | D[15:0] hold time from WE# rising edge                   | 5        |     | ns    |
| t0109  | Cycle time (No wait mode only)                           | Note2,3  |     | Ts    |

1. Ts = System clock period.

2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

3. t0109min= WAIT Length + 3 Ts

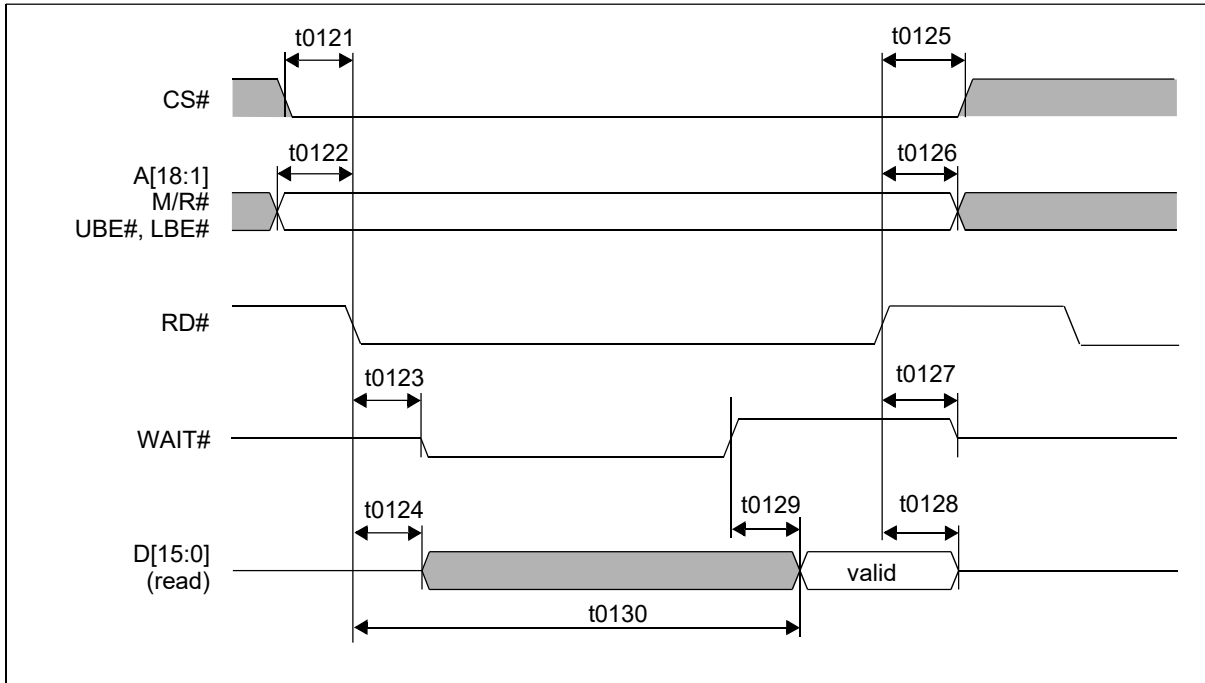


Figure 7-7: Direct 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Table 7-7: Direct 80 Type 1 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                                | 3.0 Volt |     | Units |
|--------|----------------------------------------------------------|----------|-----|-------|
|        |                                                          | Min      | Max |       |
| t0121  | CS# setup time                                           | 5        |     | ns    |
| t0122  | A[18:1], M/R#, UBE#, LBE# setup time                     | 5        |     | ns    |
| t0123  | RD# falling edge to WAIT# driven low                     |          | 12  | ns    |
| t0124  | RD# falling edge to D[15:0] driven                       | 4        |     | ns    |
| t0125  | CS# hold time from RD# rising edge                       | 2        |     | ns    |
| t0126  | A[18:1], M/R#, UBE#, LBE# hold time from RD# rising edge | 2        |     | ns    |
| t0127  | RD# rising edge to WAIT# high impedance                  |          | 7   | ns    |
| t0128  | D[15:0] hold time from RD# rising edge.                  | 2        | 8   | ns    |
| t0129  | WAIT# rising edge to valid Data if WAIT# is asserted     |          | 10  | ns    |
| t0130  | RD# falling edge to valid Data if WAIT# is NOT asserted  |          | 17  | ns    |

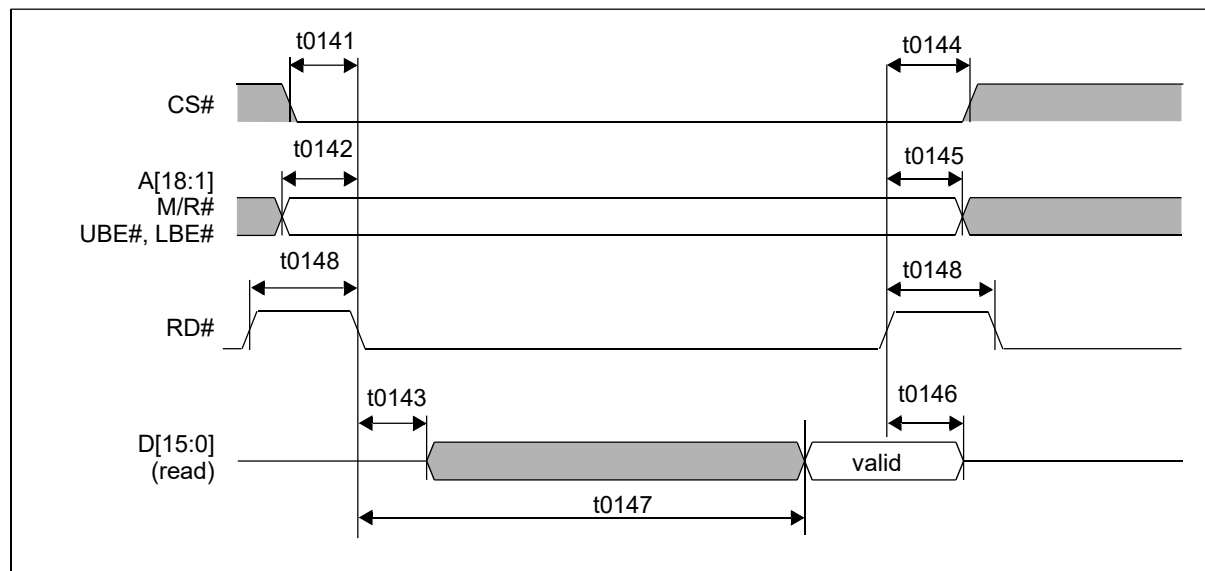


Figure 7-8: Direct 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Table 7-8: Direct 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                              | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                        | Min      | Max     |       |
| t0141  | CS# setup time                                                         | 0        |         | ns    |
| t0142  | A[18:1], M/R#, UBE#, LBE# setup time                                   | 0        |         | ns    |
| t0143  | RD# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t0144  | CS# hold time from RD# rising edge                                     | 0        |         | ns    |
| t0145  | A[18:1], M/R#, UBE#, LBE# hold time from RD# rising edge               | 0        |         | ns    |
| t0146  | D[15:0] hold time from RD# rising edge                                 | 2        | 8       | ns    |
| t0147  | RD# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t0148  | RD# pulse width high                                                   | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t0147_{max} = \text{WAIT Length} + 25 \text{ ns}$

Table 7-9: Direct 80 Type 1 Host Interface Truth Table for Little Endian

| WE# | RD# | UBE# | LBE# | D[15:8] | D[7:0] | Comments                                                        |
|-----|-----|------|------|---------|--------|-----------------------------------------------------------------|
| 0   | 1   | 0    | 0    | valid   | valid  | 16-bit write                                                    |
| 0   | 1   | 1    | 0    | -       | valid  | 8-bit write; data on low byte (even byte address <sup>1</sup> ) |
| 0   | 1   | 0    | 1    | valid   | -      | 8-bit write; data on high byte (odd byte address <sup>1</sup> ) |
| 1   | 0   | 0    | 0    | valid   | valid  | 16-bit read                                                     |
| 1   | 0   | 1    | 0    | -       | valid  | 8-bit read; data on low byte (even byte address <sup>1</sup> )  |
| 1   | 0   | 0    | 1    | valid   | -      | 8-bit read; data on high byte (odd byte address <sup>1</sup> )  |

Table 7-10: Direct 80 Type 1 Host Interface Truth Table for Big Endian

| WE# | RD# | UBE# | LBE# | D[15:8] | D[7:0] | Comments                                                         |
|-----|-----|------|------|---------|--------|------------------------------------------------------------------|
| 0   | 1   | 0    | 0    | valid   | valid  | 16-bit write                                                     |
| 0   | 1   | 1    | 0    | -       | valid  | 8-bit write; data on low byte (odd byte address <sup>1</sup> )   |
| 0   | 1   | 0    | 1    | valid   | -      | 8-bit write; data on high byte (even byte address <sup>1</sup> ) |
| 1   | 0   | 0    | 0    | valid   | valid  | 16-bit read                                                      |
| 1   | 0   | 1    | 0    | -       | valid  | 8-bit read; data on low byte (odd byte address <sup>1</sup> )    |
| 1   | 0   | 0    | 1    | valid   | -      | 8-bit read; data on high byte (even byte address <sup>1</sup> )  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

## 7.3.2 Direct 80 Type 2

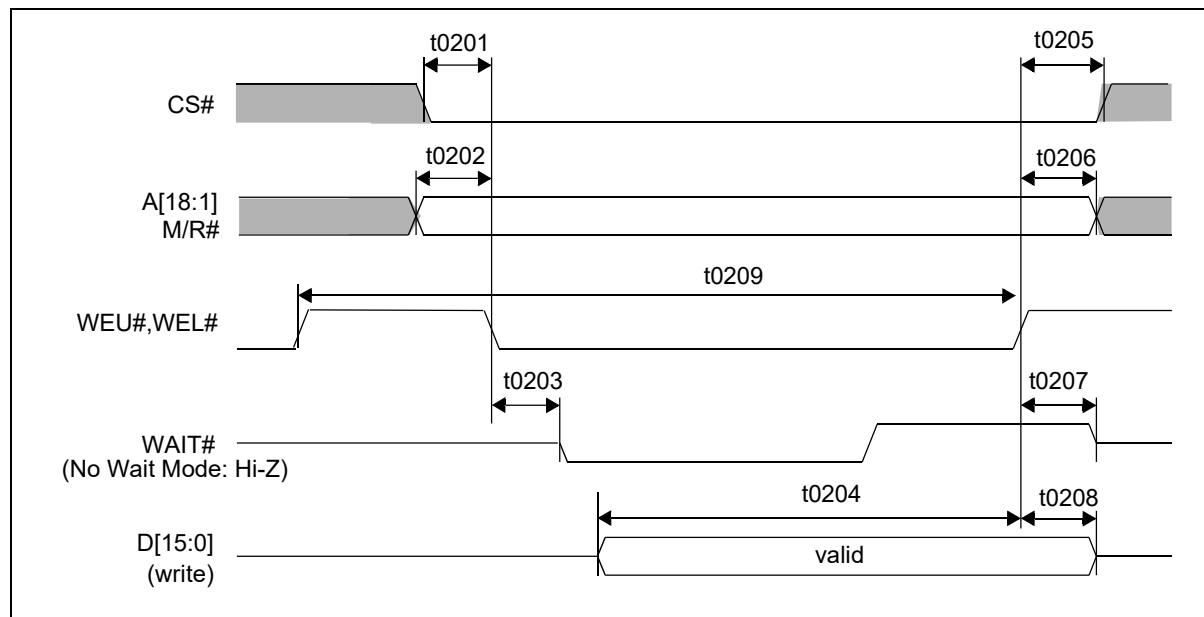


Figure 7-9: Direct 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-11: Direct 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                          | 3.0 Volt |     | Units |
|--------|----------------------------------------------------|----------|-----|-------|
|        |                                                    | Min      | Max |       |
| t0201  | CS# setup time                                     | 5        |     | ns    |
| t0202  | A[18:1], M/R# setup time                           | 5        |     | ns    |
| t0203  | WEU#,WEL# falling edge to WAIT# driven low         |          | 12  | ns    |
| t0204  | D[15:0] setup time to WEU#,WEL# rising edge        | 15       |     | ns    |
| t0205  | CS# hold time from WEU#,WEL# rising edge           | 3        |     | ns    |
| t0206  | A[18:1], M/R# hold time from WEU#,WEL# rising edge | 3        |     | ns    |
| t0207  | WEU#,WEL# rising edge to WAIT# high impedance      |          | 7   | ns    |
| t0208  | D[15:0] hold time from WEU#,WEL# rising edge       | 5        |     | ns    |
| t0209  | Cycle time (No wait mode only)                     | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period.

2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

3.  $t_{0209min} = \text{WAIT Length} + 3 T_s$

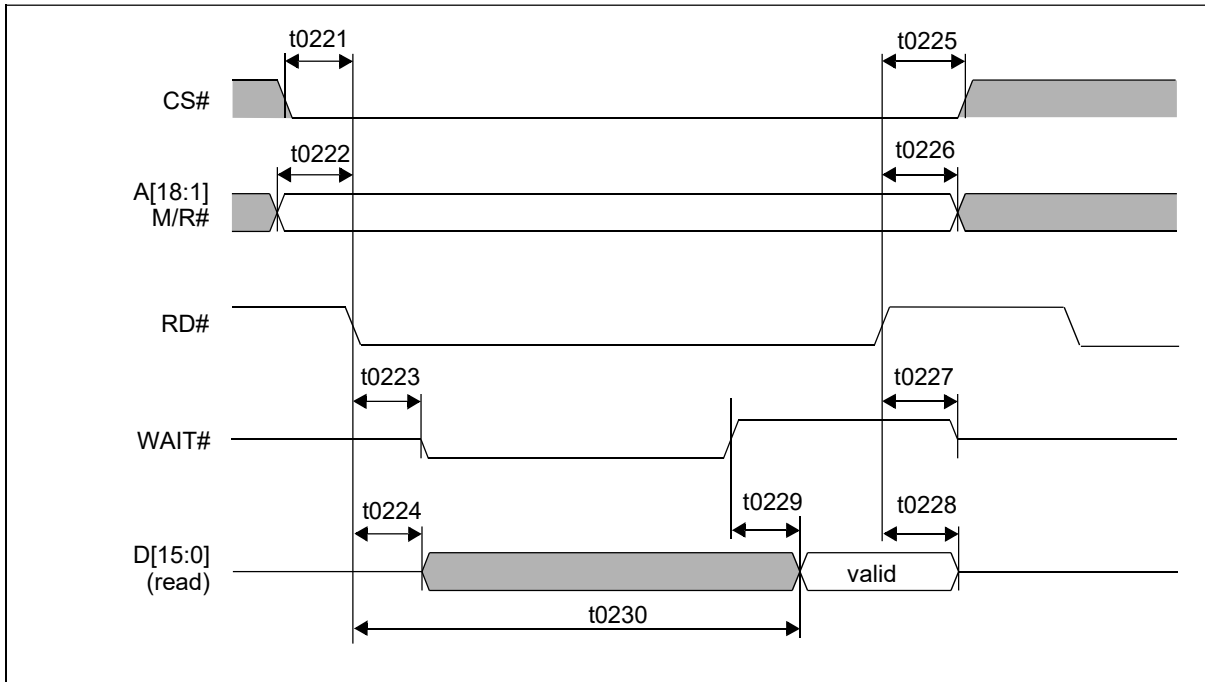


Figure 7-10: Direct 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Table 7-12: Direct 80 Type 2 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                               | 3.0 Volt |     | Units |
|--------|---------------------------------------------------------|----------|-----|-------|
|        |                                                         | Min      | Max |       |
| t0221  | CS# setup time                                          | 5        |     | ns    |
| t0222  | A[18:1], M/R# setup time                                | 5        |     | ns    |
| t0223  | RD# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t0224  | RD# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t0225  | CS# hold time from RD# rising edge                      | 2        |     | ns    |
| t0226  | A[18:1], M/R# hold time from RD# rising edge            | 2        |     | ns    |
| t0227  | RD# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t0228  | D[15:0] hold time from RD# rising edge.                 | 2        | 8   | ns    |
| t0229  | WAIT# rising edge to valid Data if WAIT# is asserted    |          | 10  | ns    |
| t0230  | RD# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

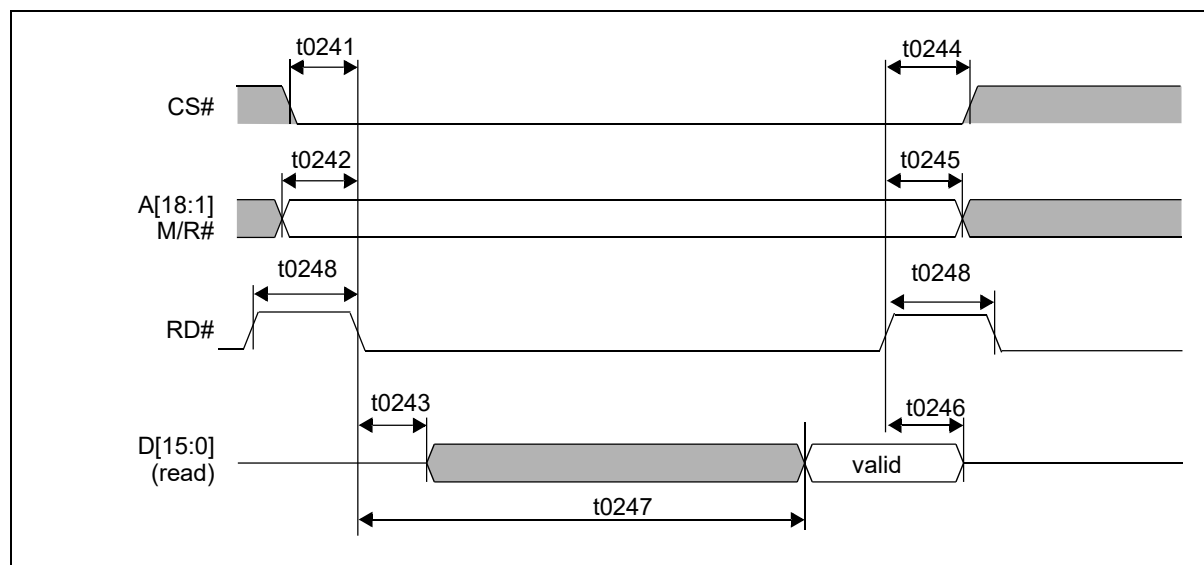


Figure 7-11: Direct 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Table 7-13: Direct 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                              | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                        | Min      | Max     |       |
| t0241  | CS# setup time                                                         | 0        |         | ns    |
| t0242  | A[18:1], M/R# setup time                                               | 0        |         | ns    |
| t0243  | RD# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t0244  | CS# hold time from RD# rising edge                                     | 0        |         | ns    |
| t0245  | A[18:1], M/R# hold time from RD# rising edge                           | 0        |         | ns    |
| t0246  | D[15:0] hold time from RD# rising edge                                 | 2        | 8       | ns    |
| t0247  | RD# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t0248  | RD# pulse width high                                                   | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t0247_{max} = \text{WAIT Length} + 25 \text{ ns}$

Table 7-14: Direct 80 Type 2 Host Interface Truth Table for Little Endian

| RD# | WEU# | WEL# | D[15:8] | D[7:0] | Comments                                                        |
|-----|------|------|---------|--------|-----------------------------------------------------------------|
| 1   | 0    | 0    | valid   | valid  | 16-bit write                                                    |
| 1   | 1    | 0    | -       | valid  | 8-bit write; data on low byte (even byte address <sup>1</sup> ) |
| 1   | 0    | 1    | valid   | -      | 8-bit write; data on high byte (odd byte address <sup>1</sup> ) |
| 0   | 1    | 1    | valid   | valid  | 16-bit read                                                     |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.3 Direct 80 Type 3

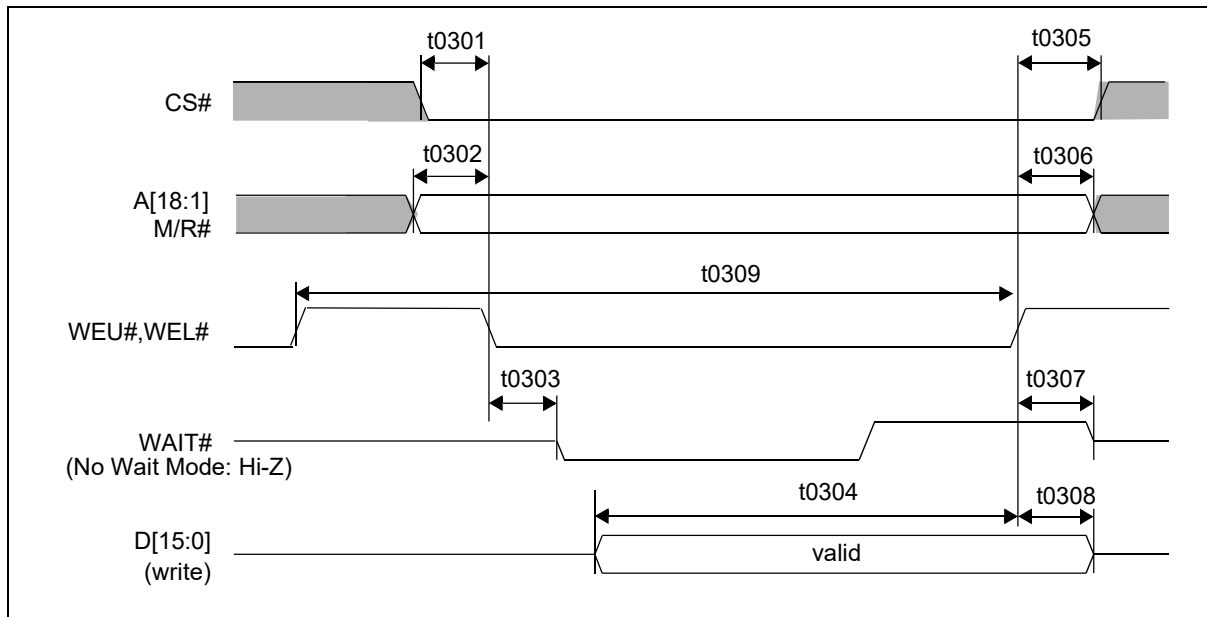


Figure 7-12: Direct 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-15: Direct 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                          | 3.0 Volt |     | Units |
|--------|----------------------------------------------------|----------|-----|-------|
|        |                                                    | Min      | Max |       |
| t0301  | CS# setup time                                     | 5        |     | ns    |
| t0302  | A[18:1], M/R# setup time                           | 5        |     | ns    |
| t0303  | WEU#,WEL# falling edge to WAIT# driven low         |          | 12  | ns    |
| t0304  | D[15:0] setup time to WEU#,WEL# rising edge        | 15       |     | ns    |
| t0305  | CS# hold time from WEU#,WEL# rising edge           | 3        |     | ns    |
| t0306  | A[18:1], M/R# hold time from WEU#,WEL# rising edge | 3        |     | ns    |
| t0307  | WEU#,WEL# rising edge to WAIT# high impedance      |          | 7   | ns    |
| t0308  | D[15:0] hold time from WEU#,WEL# rising edge       | 5        |     | ns    |
| t0309  | Cycle time (No wait mode only)                     | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t0309_{min} = \text{WAIT Length} + 3 T_s$

## A.C. Characteristics

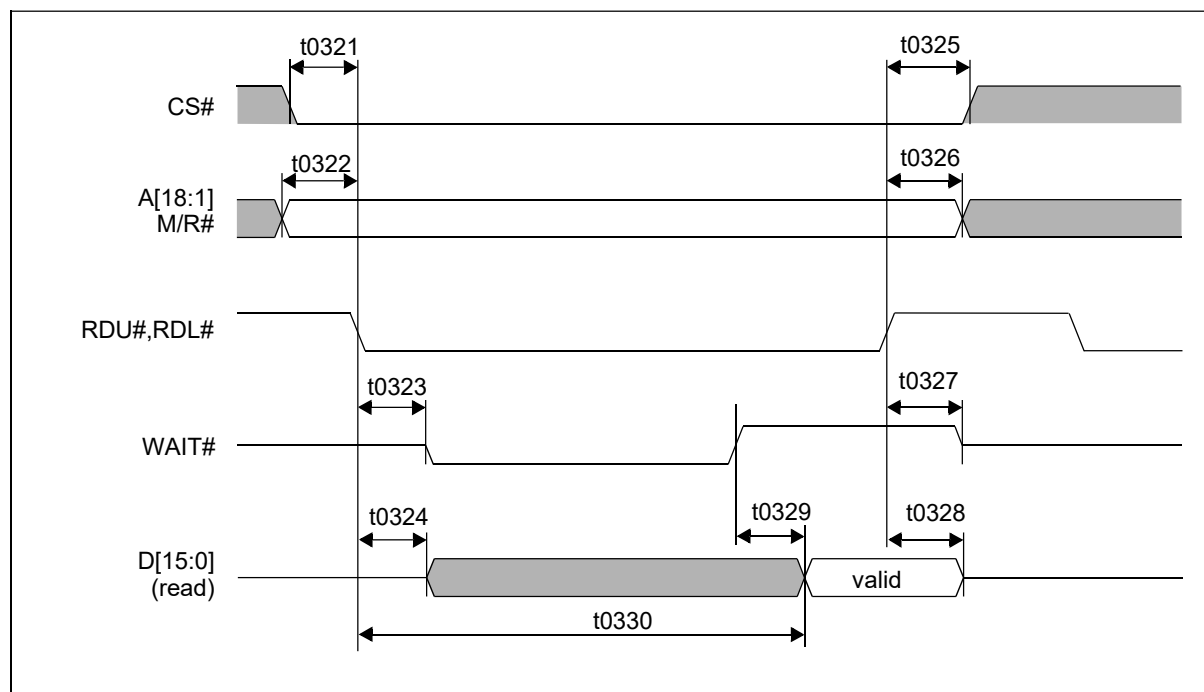


Figure 7-13: Direct 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Table 7-16: Direct 80 Type 3 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                                     | 3.0 Volt |     | Units |
|--------|---------------------------------------------------------------|----------|-----|-------|
|        |                                                               | Min      | Max |       |
| t0321  | CS# setup time                                                | 5        |     | ns    |
| t0322  | A[18:1], M/R# setup time                                      | 5        |     | ns    |
| t0323  | RDU#,RDL# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t0324  | RDU#,RDL# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t0325  | CS# hold time from RDU#,RDL# rising edge                      | 2        |     | ns    |
| t0326  | A[18:1], M/R# hold time from RDU#,RDL# rising edge            | 2        |     | ns    |
| t0327  | RDU#,RDL# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t0328  | D[15:0] hold time from RDU#,RDL# rising edge.                 | 2        | 8   | ns    |
| t0329  | WAIT# rising edge to valid Data if WAIT# is asserted          |          | 10  | ns    |
| t0330  | RDU#,RDL# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

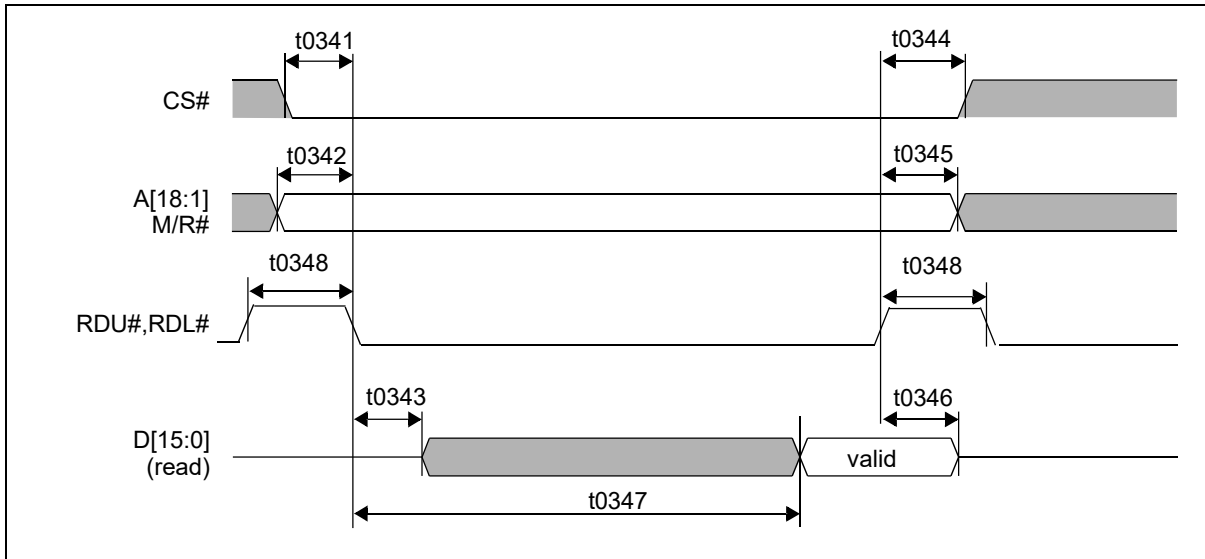


Figure 7-14: Direct 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Table 7-17: Direct 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                                    | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                              | Min      | Max     |       |
| t0341  | CS# setup time                                                               | 0        |         | ns    |
| t0342  | A[18:1], M/R# setup time                                                     | 0        |         | ns    |
| t0343  | RDU#,RDL# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t0344  | CS# hold time from RDU#,RDL# rising edge                                     | 0        |         | ns    |
| t0345  | A[18:1], M/R# hold time from RDU#,RDL# rising edge                           | 0        |         | ns    |
| t0346  | D[15:0] hold time from RDU#,RDL# rising edge                                 | 2        | 8       | ns    |
| t0347  | RDU#,RDL# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t0348  | RDU#, RDL# pulse width high                                                  | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
2.  $t0347_{max} = \text{WAIT Length} + 25 \text{ ns}$

*Table 7-18: Direct 80 Type 3 Host Interface Truth Table for Little Endian*

| WEU# | WEL# | RDU# | RDL# | D[15:8] | D[7:0] | Comments                                                        |
|------|------|------|------|---------|--------|-----------------------------------------------------------------|
| 0    | 0    | 1    | 1    | valid   | valid  | 16-bit write                                                    |
| 1    | 0    | 1    | 1    | -       | valid  | 8-bit write; data on low byte (even byte address <sup>1</sup> ) |
| 0    | 1    | 1    | 1    | valid   | -      | 8-bit write; data on high byte (odd byte address <sup>1</sup> ) |
| 1    | 1    | 0    | 0    | valid   | valid  | 16-bit read                                                     |
| 1    | 1    | 1    | 0    | -       | valid  | 8-bit read; data on low byte (even byte address <sup>1</sup> )  |
| 1    | 1    | 0    | 1    | valid   | -      | 8-bit read; data on high byte (odd byte address <sup>1</sup> )  |

*Table 7-19: Direct 80 Type 3 Host Interface Truth Table for Big Endian*

| WEU# | WEL# | RDU# | RDL# | D[15:8] | D[7:0] | Comments                                                         |
|------|------|------|------|---------|--------|------------------------------------------------------------------|
| 0    | 0    | 1    | 1    | valid   | valid  | 16-bit write                                                     |
| 1    | 0    | 1    | 1    | -       | valid  | 8-bit write; data on low byte (odd byte address <sup>1</sup> )   |
| 0    | 1    | 1    | 1    | valid   | -      | 8-bit write; data on high byte (even byte address <sup>1</sup> ) |
| 1    | 1    | 0    | 0    | valid   | valid  | 16-bit read                                                      |
| 1    | 1    | 1    | 0    | -       | valid  | 8-bit read; data on low byte (odd byte address <sup>1</sup> )    |
| 1    | 1    | 0    | 1    | valid   | -      | 8-bit read; data on high byte (even byte address <sup>1</sup> )  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.4 Direct 68

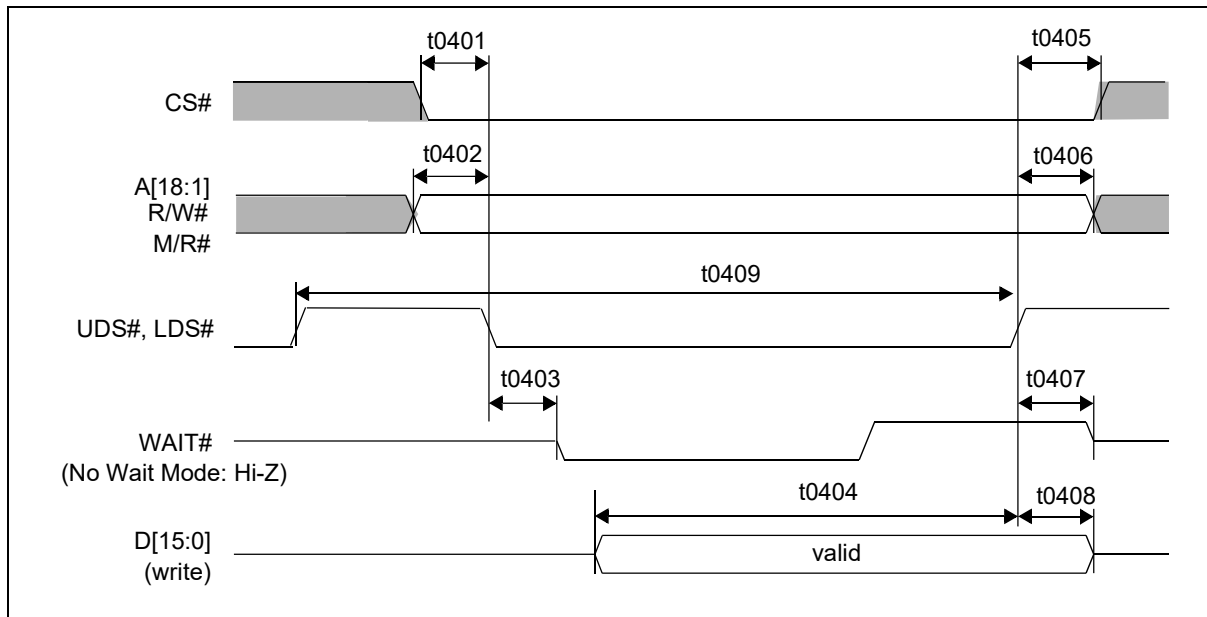


Figure 7-15: Direct 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-20: Direct 68 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                                 | 3.0 Volt |     | Units |
|--------|-----------------------------------------------------------|----------|-----|-------|
|        |                                                           | Min      | Max |       |
| t0401  | CS# setup time                                            | 5        |     | ns    |
| t0402  | AB[18:1], R/W#, M/R# setup time                           | 5        |     | ns    |
| t0403  | UDS#, LDS# falling edge to WAIT# driven low               |          | 12  | ns    |
| t0404  | D[15:0] setup time to UDS#, LDS# rising edge              | 15       |     | ns    |
| t0405  | CS# hold time from UDS#, LDS# rising edge                 | 3        |     | ns    |
| t0406  | A[18:1], R/W#, M/R# hold time from UDS#, LDS# rising edge | 3        |     | ns    |
| t0407  | UDS#, LDS# rising edge to WAIT# high impedance            |          | 7   | ns    |
| t0408  | D[15:0] hold time from UDS#, LDS# rising edge             | 5        |     | ns    |
| t0409  | Cycle time (No wait mode only)                            | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t0409_{min} = \text{WAIT Length} + 3 T_s$

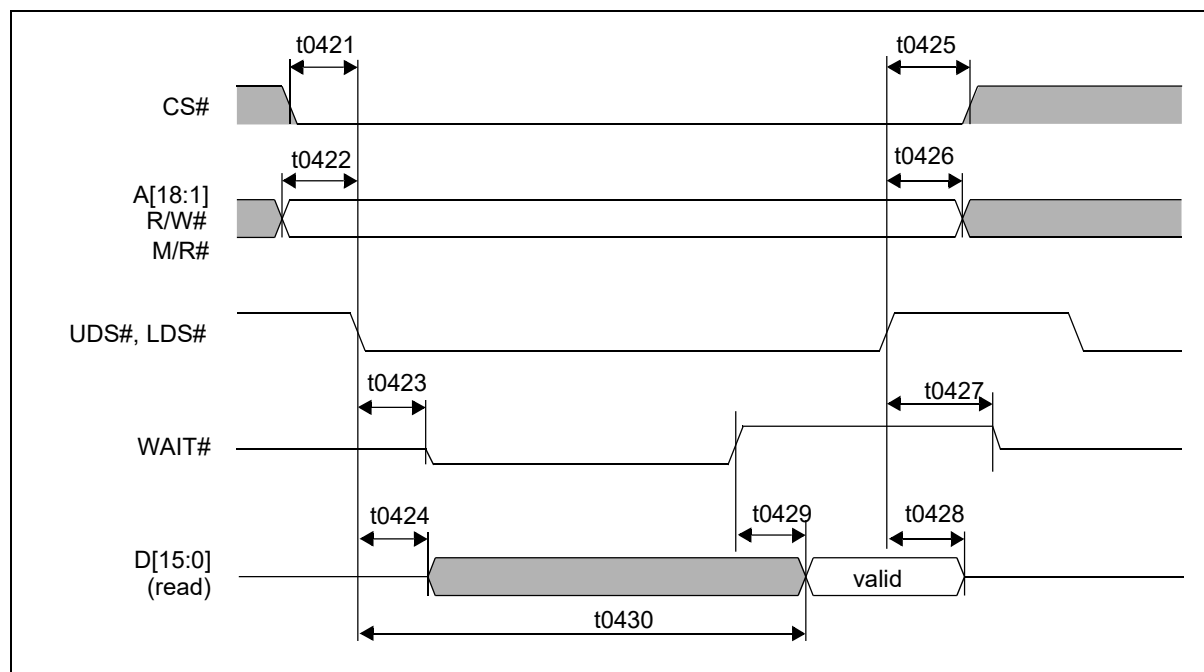


Figure 7-16: Direct 68 Interface Read Cycle Timing (Wait Mode)

Table 7-21: Direct 68 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                                      | 3.0 Volt |     | Units |
|--------|----------------------------------------------------------------|----------|-----|-------|
|        |                                                                | Min      | Max |       |
| t0421  | CS# setup time                                                 | 5        |     | ns    |
| t0422  | AB[18:1], R/W#, M/R# setup time                                | 5        |     | ns    |
| t0423  | UDS#, LDS# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t0424  | UDS#, LDS# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t0425  | CS# hold time from UDS#, LDS# rising edge                      | 2        |     | ns    |
| t0426  | A[18:1], R/W#, M/R# hold time from UDS#, LDS# rising edge      | 2        |     | ns    |
| t0427  | UDS#, LDS# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t0428  | D[15:0] hold time from UDS#, LDS# rising edge                  | 2        | 8   | ns    |
| t0429  | WAIT# rising edge to valid Data if WAIT# is asserted           |          | 10  | ns    |
| t0430  | UDS#, LDS# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

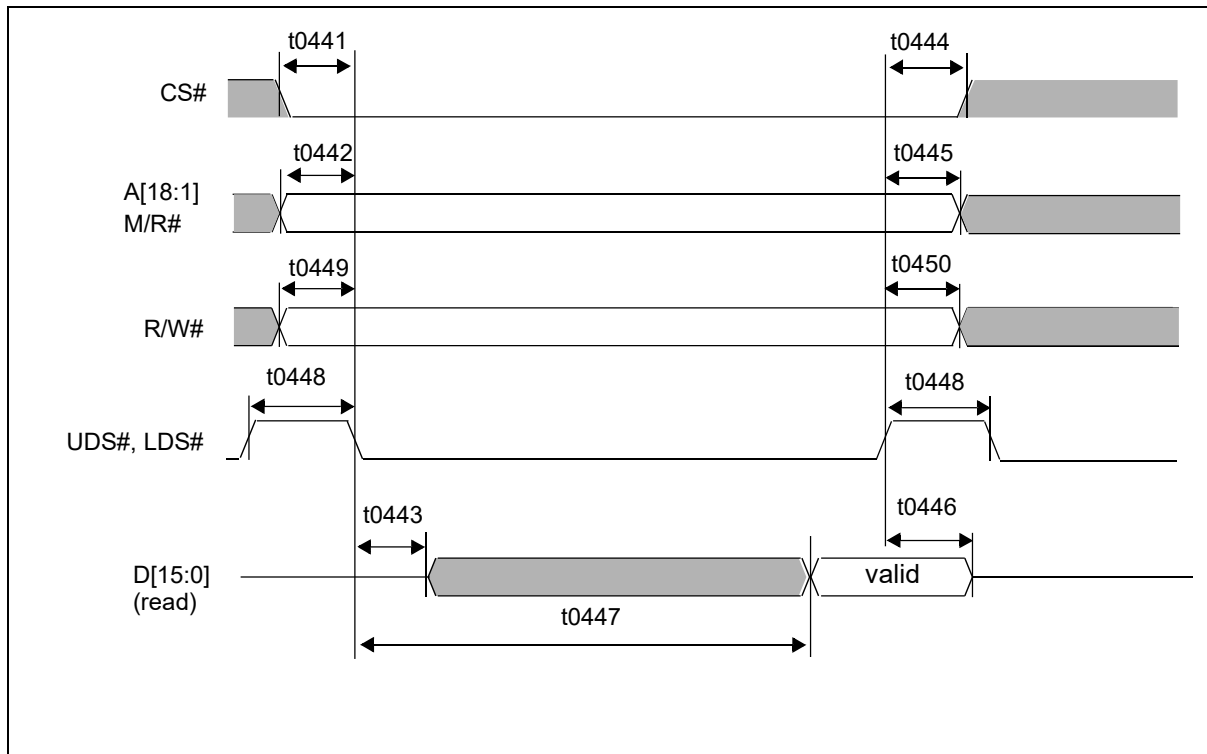


Figure 7-17: Direct 68 Interface Read Cycle Timing (No Wait Mode)

Table 7-22: Direct 68 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                                     | 3.0 Volt |         | Units |
|--------|-------------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                               | Min      | Max     |       |
| t0441  | CS# setup time                                                                | 0        |         | ns    |
| t0442  | A[18:1], M/R# setup time                                                      | 0        |         | ns    |
| t0443  | UDS#, LDS# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t0444  | CS# hold time from UDS#, LDS# rising edge                                     | 0        |         | ns    |
| t0445  | A[18:1], M/R# hold time from UDS#, LDS# rising edge                           | 0        |         | ns    |
| t0446  | D[15:0] hold time from UDS#, LDS# rising edge                                 | 2        | 8       | ns    |
| t0447  | UDS#, LDS# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t0448  | UDS#, LDS# pulse width high                                                   | 8        |         | ns    |
| t0449  | R/W# setup time                                                               | 5        |         | ns    |
| t0450  | R/W# hold time from UDS#, LDS# rising edge                                    | 2        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t_{0447max} = \text{WAIT Length} + 25 \text{ ns}$

*Table 7-23: Direct 68 Host Interface Truth Table for Little Endian*

| R/W# | UDS# | LDS# | D[15:8] | D[7:0] | Comments                                                        |
|------|------|------|---------|--------|-----------------------------------------------------------------|
| 0    | 0    | 0    | valid   | valid  | 16-bit write                                                    |
| 0    | 1    | 0    | -       | valid  | 8-bit write; data on low byte (even byte address <sup>1</sup> ) |
| 0    | 0    | 1    | valid   | -      | 8-bit write; data on high byte (odd byte address <sup>1</sup> ) |
| 1    | 0    | 0    | valid   | valid  | 16-bit read                                                     |
| 1    | 1    | 0    | -       | valid  | 8-bit read; data on low byte (even byte address <sup>1</sup> )  |
| 1    | 0    | 1    | valid   | -      | 8-bit read; data on high byte (odd byte address <sup>1</sup> )  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.5 Indirect 80 Type 1

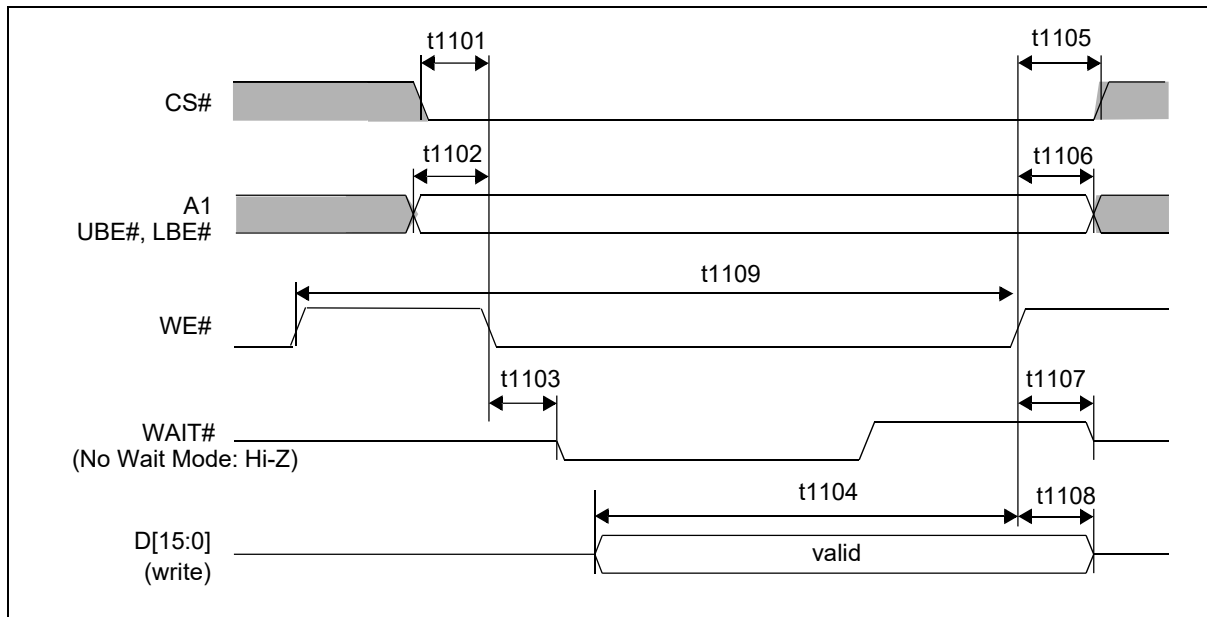


Figure 7-18: Indirect 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-24: Indirect 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                     | 3.0 Volt |     | Units |
|--------|-----------------------------------------------|----------|-----|-------|
|        |                                               | Min      | Max |       |
| t1101  | CS# setup time                                | 5        |     | ns    |
| t1102  | A1, UBE#, LBE# setup time                     | 5        |     | ns    |
| t1103  | WE# falling edge to WAIT# driven low          |          | 12  | ns    |
| t1104  | D[15:0] setup time to WE# rising edge         | 15       |     | ns    |
| t1105  | CS# hold time from WE# rising edge            | 3        |     | ns    |
| t1106  | A1, UBE#, LBE# hold time from WE# rising edge | 3        |     | ns    |
| t1107  | WE# rising edge to WAIT# high impedance       |          | 7   | ns    |
| t1108  | D[15:0] hold time from WE# rising edge        | 5        |     | ns    |
| t1109  | Cycle time (No wait mode only)                | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t1109_{min} = \text{WAIT Length} + 3 T_s$

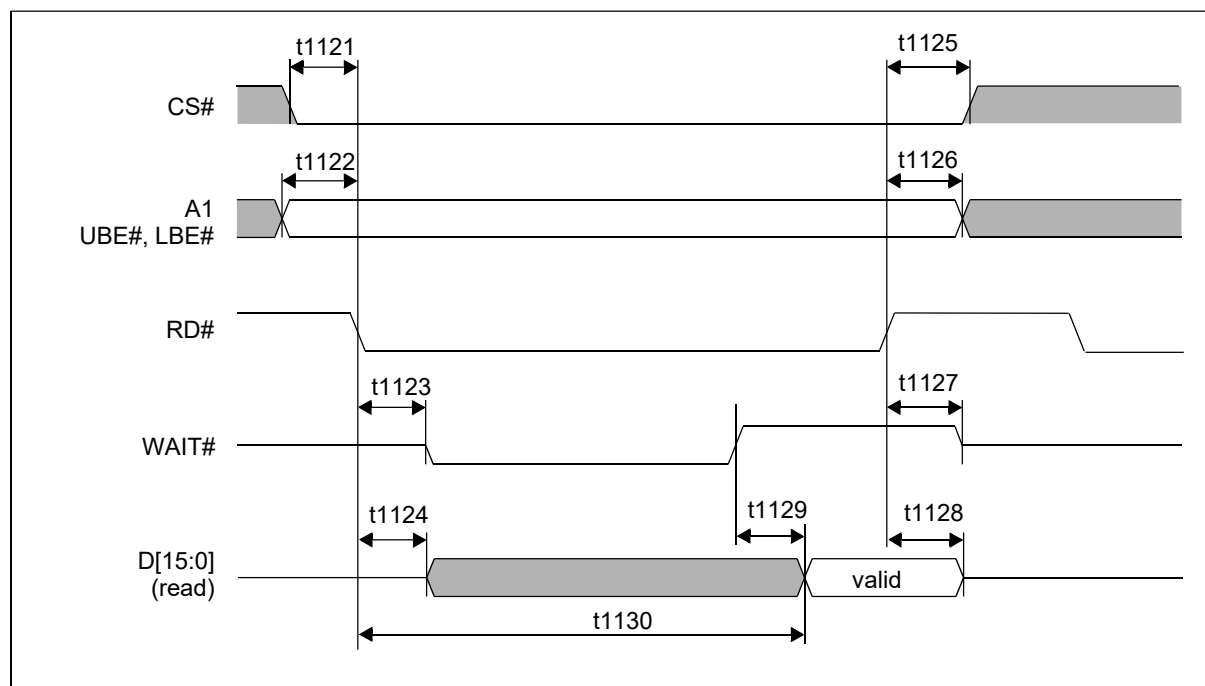


Figure 7-19: Indirect 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Table 7-25: Indirect 80 Type 1 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                               | 3.0 Volt |     | Units |
|--------|---------------------------------------------------------|----------|-----|-------|
|        |                                                         | Min      | Max |       |
| t1121  | CS# setup time                                          | 5        |     | ns    |
| t1122  | A1, UBE#, LBE# setup time                               | 5        |     | ns    |
| t1123  | RD# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t1124  | RD# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t1125  | CS# hold time from RD# rising edge                      | 2        |     | ns    |
| t1126  | A1, UBE#, LBE# hold time from RD# rising edge           | 2        |     | ns    |
| t1127  | RD# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t1128  | D[15:0] hold time from RD# rising edge.                 | 2        | 8   | ns    |
| t1129  | WAIT# rising edge to valid Data if WAIT# is asserted    |          | 10  | ns    |
| t1130  | RD# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

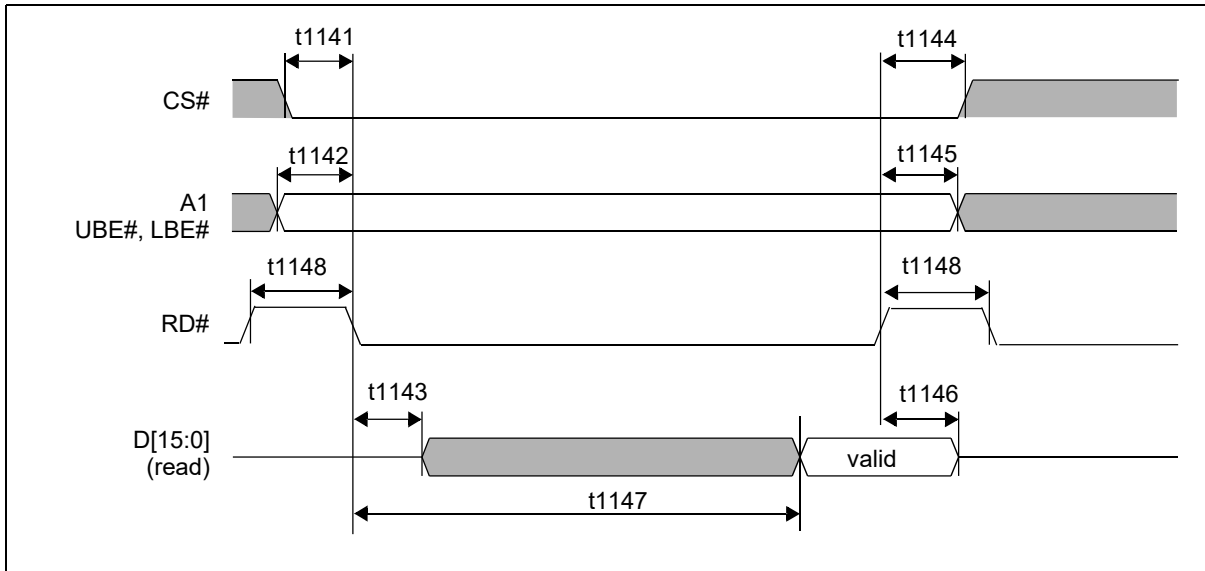


Figure 7-20: Indirect 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Table 7-26: Indirect 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                              | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                        | Min      | Max     |       |
| t1141  | CS# setup time                                                         | 0        |         | ns    |
| t1142  | A1, UBE#, LBE# setup time                                              | 0        |         | ns    |
| t1143  | RD# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t1144  | CS# hold time from RD# rising edge                                     | 0        |         | ns    |
| t1145  | A1, UBE#, LBE# hold time from RD# rising edge                          | 0        |         | ns    |
| t1146  | D[15:0] hold time from RD# rising edge                                 | 2        | 8       | ns    |
| t1147  | RD# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t1148  | RD# pulse width high                                                   | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t1147_{max} = \text{WAIT Length} + 25 \text{ ns}$

Table 7-27: Indirect 80 Type 1 Host Interface Truth Table for Little Endian

| WE# | RD# | UBE# | LBE# | D[15:8] | D[7:0] | Comments                                                                      |
|-----|-----|------|------|---------|--------|-------------------------------------------------------------------------------|
| 0   | 1   | 0    | 0    | valid   | valid  | 16-bit command write or data write                                            |
| 0   | 1   | 1    | 0    | -       | valid  | 8-bit data write (memory); data on low byte (even byte address <sup>1</sup> ) |
| 0   | 1   | 0    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (odd byte address <sup>1</sup> ) |
| 1   | 0   | 0    | 0    | valid   | valid  | 16-bit data read                                                              |
| 1   | 0   | 1    | 0    | -       | valid  | 8-bit data read (memory); data on low byte (even byte address <sup>1</sup> )  |
| 1   | 0   | 0    | 1    | valid   | -      | 8-bit data read (memory); data on high byte (odd byte address <sup>1</sup> )  |

Table 7-28: Indirect 80 Type 1 Host Interface Truth Table for Big Endian

| WE# | RD# | UBE# | LBE# | D[15:8] | D[7:0] | Comments                                                                       |
|-----|-----|------|------|---------|--------|--------------------------------------------------------------------------------|
| 0   | 1   | 0    | 0    | valid   | valid  | 16-bit command write or data write                                             |
| 0   | 1   | 1    | 0    | -       | valid  | 8-bit data write (memory); data on low byte (odd byte address <sup>1</sup> )   |
| 0   | 1   | 0    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (even byte address <sup>1</sup> ) |
| 1   | 0   | 0    | 0    | valid   | valid  | 16-bit data read                                                               |
| 1   | 0   | 1    | 0    | -       | valid  | 8-bit data read (memory); data on low byte (odd byte address <sup>1</sup> )    |
| 1   | 0   | 0    | 1    | valid   | -      | 8-bit data read (memory); data on high byte (even byte address <sup>1</sup> )  |

Table 7-29: Indirect 80 Type 1 Host Interface Function Selection

| A1 | WE# | RD# | Comments                                                  |
|----|-----|-----|-----------------------------------------------------------|
| 0  | 0   | 1   | 16-bit Command Write (register address)                   |
| 1  | 0   | 1   | Data Write (16-bit register data or 8/16-bit memory data) |
| 1  | 1   | 0   | Data Read (16-bit register data or 8/16-bit memory data)  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.6 Indirect 80 Type 2

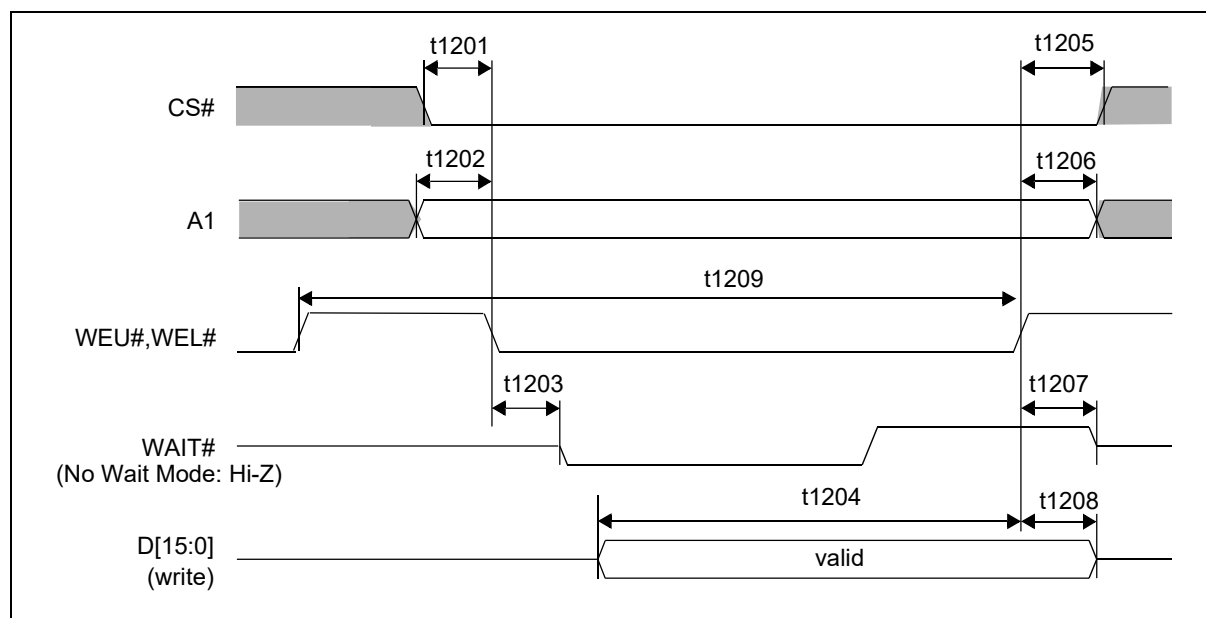


Figure 7-21: Indirect 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-30: Indirect 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                     | 3.0 Volt |     | Units |
|--------|-----------------------------------------------|----------|-----|-------|
|        |                                               | Min      | Max |       |
| t1201  | CS# setup time                                | 5        |     | ns    |
| t1202  | A1 setup time                                 | 5        |     | ns    |
| t1203  | WEU#,WEL# falling edge to WAIT# driven low    |          | 12  | ns    |
| t1204  | D[15:0] setup time to WEU#,WEL# rising edge   | 15       |     | ns    |
| t1205  | CS# hold time from WEU#,WEL# rising edge      | 3        |     | ns    |
| t1206  | A1 hold time from WEU#,WEL# rising edge       | 3        |     | ns    |
| t1207  | WEU#,WEL# rising edge to WAIT# high impedance |          | 7   | ns    |
| t1208  | D[15:0] hold time from WEU#,WEL# rising edge  | 5        |     | ns    |
| t1209  | Cycle time (No wait mode only)                | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t1209_{min} = \text{WAIT Length} + 3 T_s$

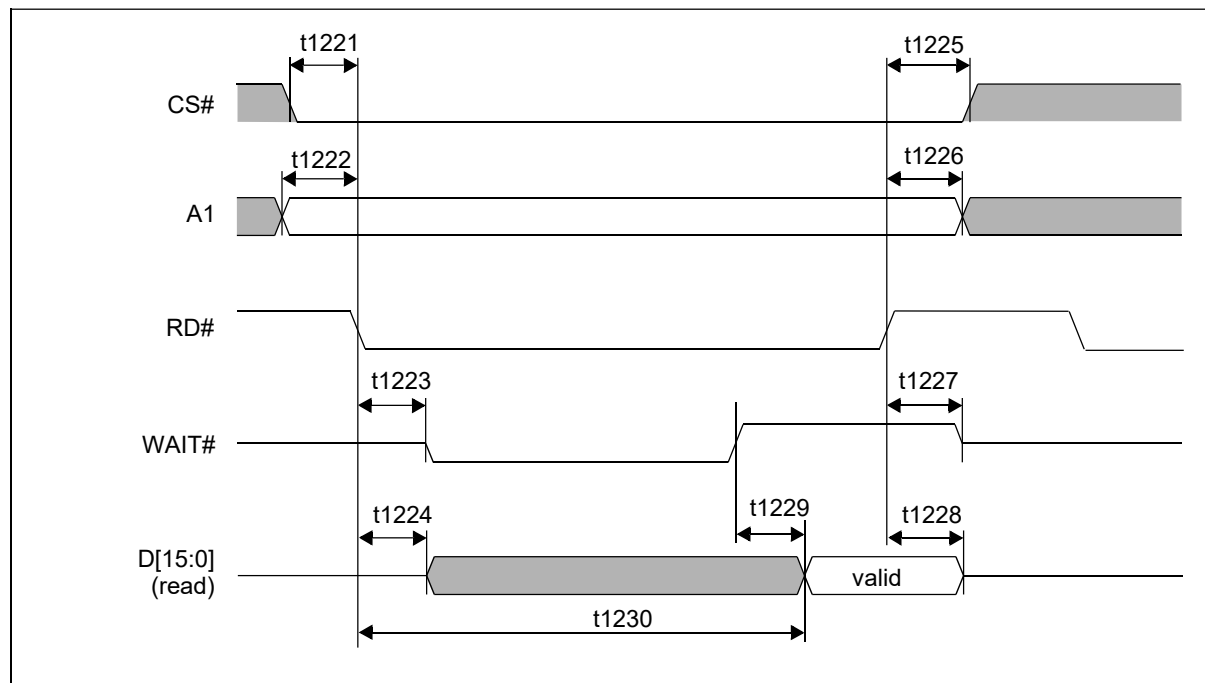


Figure 7-22: Indirect 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Table 7-31: Indirect 80 Type 2 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                               | 3.0 Volt |     | Units |
|--------|---------------------------------------------------------|----------|-----|-------|
|        |                                                         | Min      | Max |       |
| t1221  | CS# setup time                                          | 5        |     | ns    |
| t1222  | A1 setup time                                           | 5        |     | ns    |
| t1223  | RD# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t1224  | RD# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t1225  | CS# hold time from RD# rising edge                      | 2        |     | ns    |
| t1226  | A1 hold time from RD# rising edge                       | 2        |     | ns    |
| t1227  | RD# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t1228  | D[15:0] hold time from RD# rising edge.                 | 2        | 8   | ns    |
| t1229  | WAIT# rising edge to valid Data if WAIT# is asserted    |          | 10  | ns    |
| t1230  | RD# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

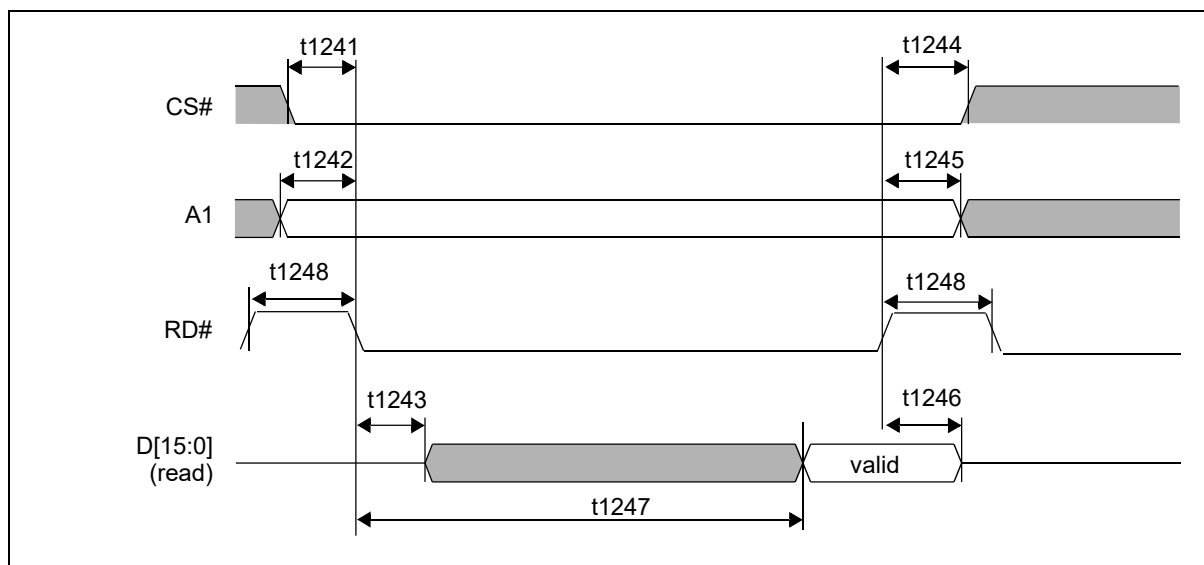


Figure 7-23: Indirect 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Table 7-32: Indirect 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                              | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                        | Min      | Max     |       |
| t1241  | CS# setup time                                                         | 0        |         | ns    |
| t1242  | A1 setup time                                                          | 0        |         | ns    |
| t1243  | RD# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t1244  | CS# hold time from RD# rising edge                                     | 0        |         | ns    |
| t1245  | A1 hold time from RD# rising edge                                      | 0        |         | ns    |
| t1246  | D[15:0] hold time from RD# rising edge                                 | 2        | 8       | ns    |
| t1247  | RD# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t1248  | RD# pulse width high                                                   | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t1247_{max} = \text{WAIT Length} + 25 \text{ ns}$

*Table 7-33: Indirect 80 Type 2 Host Interface Truth Table for Little Endian*

| RD# | WEU# | WEL# | D[15:8] | D[7:0] | Comments                                                                       |
|-----|------|------|---------|--------|--------------------------------------------------------------------------------|
| 1   | 0    | 0    | valid   | valid  | 16-bit command write or data write                                             |
| 1   | 1    | 0    | -       | valid  | 8-bit data write (memory); data on high byte (odd byte address <sup>1</sup> )  |
| 1   | 0    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (even byte address <sup>1</sup> ) |
| 0   | 1    | 1    | valid   | valid  | 16-bit data read                                                               |

*Table 7-34: Indirect 80 Type 2 Host Interface Function Selection*

| A1 | WEU#/WEL# | RD# | Comments                                                  |
|----|-----------|-----|-----------------------------------------------------------|
| 0  | 0         | 1   | 16-bit Command Write (register address)                   |
| 1  | 0         | 1   | Data Write (16-bit register data or 8/16-bit memory data) |
| 1  | 1         | 0   | Data Read (16-bit register data or 16-bit memory data)    |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.7 Indirect 80 Type 3

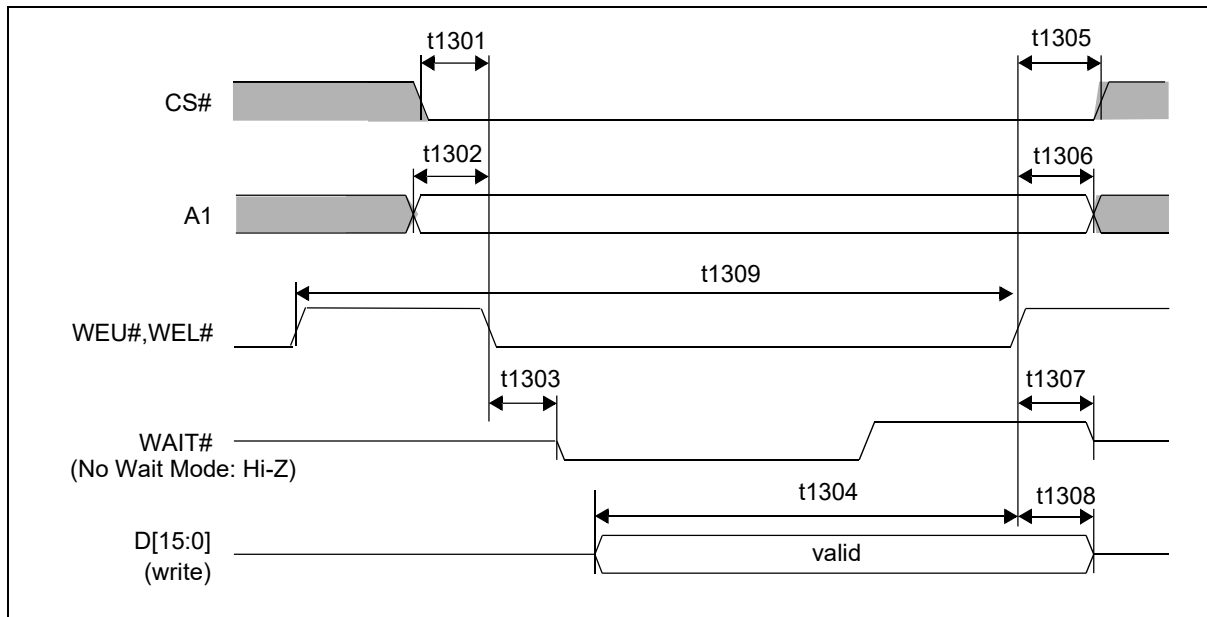


Figure 7-24: Indirect 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-35: Indirect 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                     | 3.0 Volt |     | Units |
|--------|-----------------------------------------------|----------|-----|-------|
|        |                                               | Min      | Max |       |
| t1301  | CS# setup time                                | 5        |     | ns    |
| t1302  | A1 setup time                                 | 5        |     | ns    |
| t1303  | WEU#,WEL# falling edge to WAIT# driven low    |          | 12  | ns    |
| t1304  | D[15:0] setup time to WEU#,WEL# rising edge   | 15       |     | ns    |
| t1305  | CS# hold time from WEU#,WEL# rising edge      | 3        |     | ns    |
| t1306  | A1 hold time from WEU#,WEL# rising edge       | 3        |     | ns    |
| t1307  | WEU#,WEL# rising edge to WAIT# high impedance |          | 7   | ns    |
| t1308  | D[15:0] hold time from WEU#,WEL# rising edge  | 5        |     | ns    |
| t1309  | Cycle time (No wait mode only)                | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t1309_{min} = \text{WAIT Length} + 3 T_s$

## A.C. Characteristics

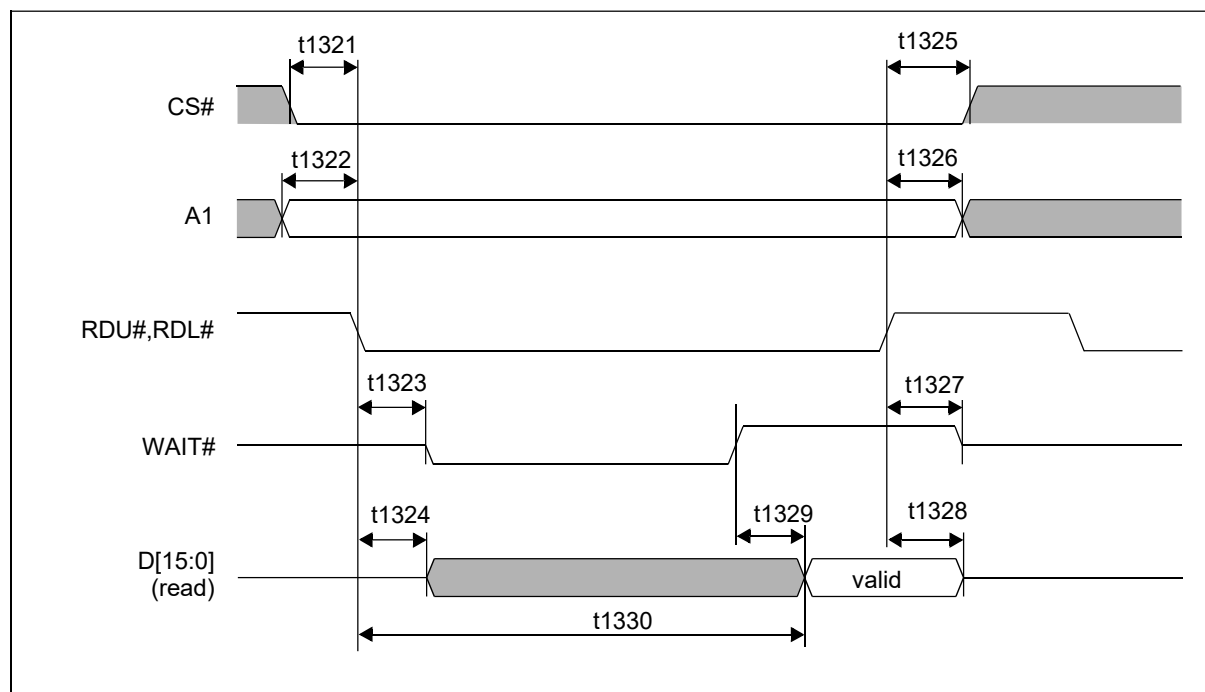


Figure 7-25: Indirect 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Table 7-36: Indirect 80 Type 3 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                                     | 3.0 Volt |     | Units |
|--------|---------------------------------------------------------------|----------|-----|-------|
|        |                                                               | Min      | Max |       |
| t1321  | CS# setup time                                                | 5        |     | ns    |
| t1322  | A1 setup time                                                 | 5        |     | ns    |
| t1323  | RDU#,RDL# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t1324  | RDU#,RDL# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t1325  | CS# hold time from RDU#,RDL# rising edge                      | 2        |     | ns    |
| t1326  | A1 hold time from RDU#,RDL# rising edge                       | 2        |     | ns    |
| t1327  | RDU#,RDL# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t1328  | D[15:0] hold time from RDU#,RDL# rising edge.                 | 2        | 8   | ns    |
| t1329  | WAIT# rising edge to valid Data if WAIT# is asserted          |          | 10  | ns    |
| t1330  | RDU#,RDL# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

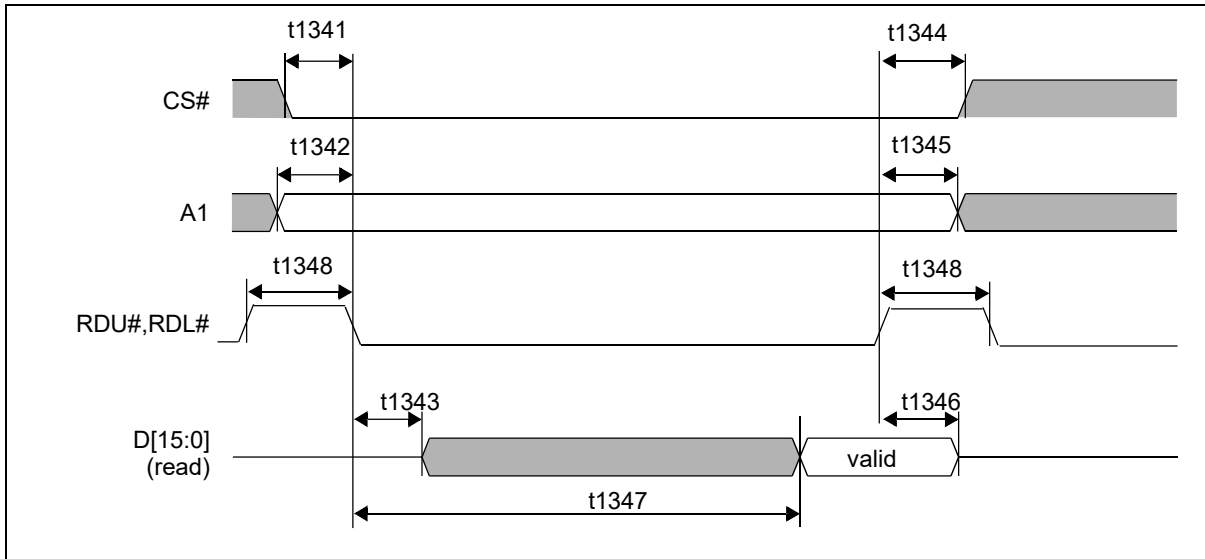


Figure 7-26: Indirect 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Table 7-37: Indirect 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                                    | 3.0 Volt |         | Units |
|--------|------------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                              | Min      | Max     |       |
| t1341  | CS# setup time                                                               | 0        |         | ns    |
| t1342  | A1 setup time                                                                | 0        |         | ns    |
| t1343  | RDU#,RDL# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t1344  | CS# hold time from RDU#,RDL# rising edge                                     | 0        |         | ns    |
| t1345  | A1 hold time from RDU#,RDL# rising edge                                      | 0        |         | ns    |
| t1346  | D[15:0] hold time from RDU#,RDL# rising edge                                 | 2        | 8       | ns    |
| t1347  | RDU#,RDL# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t1348  | RDU#, RDL# pulse width high                                                  | 8        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
2.  $t1347_{max} = \text{WAIT Length} + 25 \text{ ns}$

Table 7-38: Indirect 80 Type 3 Host Interface Truth Table for Little Endian

| WEU# | WEL# | RDU# | RDL# | D[15:8] | D[7:0] | Comments                                                                      |
|------|------|------|------|---------|--------|-------------------------------------------------------------------------------|
| 0    | 0    | 1    | 1    | valid   | valid  | 16-bit command write or data write                                            |
| 1    | 0    | 1    | 1    | -       | valid  | 8-bit data write (memory); data on low byte (even byte address <sup>1</sup> ) |
| 0    | 1    | 1    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (odd byte address <sup>1</sup> ) |
| 1    | 1    | 0    | 0    | valid   | valid  | 16-bit data read                                                              |
| 1    | 1    | 1    | 0    | -       | valid  | 8-bit data read (memory); data on low byte (even byte address <sup>1</sup> )  |
| 1    | 1    | 0    | 1    | valid   | -      | 8-bit data read (memory); data on high byte (odd byte address <sup>1</sup> )  |

Table 7-39: Indirect 80 Type 3 Host Interface Truth Table for Big Endian

| WEU# | WEL# | RDU# | RDL# | D[15:8] | D[7:0] | Comments                                                                       |
|------|------|------|------|---------|--------|--------------------------------------------------------------------------------|
| 0    | 0    | 1    | 1    | valid   | valid  | 16-bit command write or data write                                             |
| 1    | 0    | 1    | 1    | -       | valid  | 8-bit data write (memory); data on low byte (odd byte address <sup>1</sup> )   |
| 0    | 1    | 1    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (even byte address <sup>1</sup> ) |
| 1    | 1    | 0    | 0    | valid   | valid  | 16-bit data read                                                               |
| 1    | 1    | 1    | 0    | -       | valid  | 8-bit data read (memory); data on low byte (odd byte address <sup>1</sup> )    |
| 1    | 1    | 0    | 1    | valid   | -      | 8-bit data read (memory); data on high byte (even byte address <sup>1</sup> )  |

Table 7-40: Indirect 80 Type 3 Host Interface Function Select

| A1 | WEU# / WEL# | RDU# / RDL# | Comments                                                  |
|----|-------------|-------------|-----------------------------------------------------------|
| 0  | 0           | 1           | 16-bit Command Write (register address)                   |
| 1  | 0           | 1           | Data Write (16-bit register data or 8/16-bit memory data) |
| 1  | 1           | 0           | Data Read (16-bit register data or 8/16-bit memory data)  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.8 Indirect 68

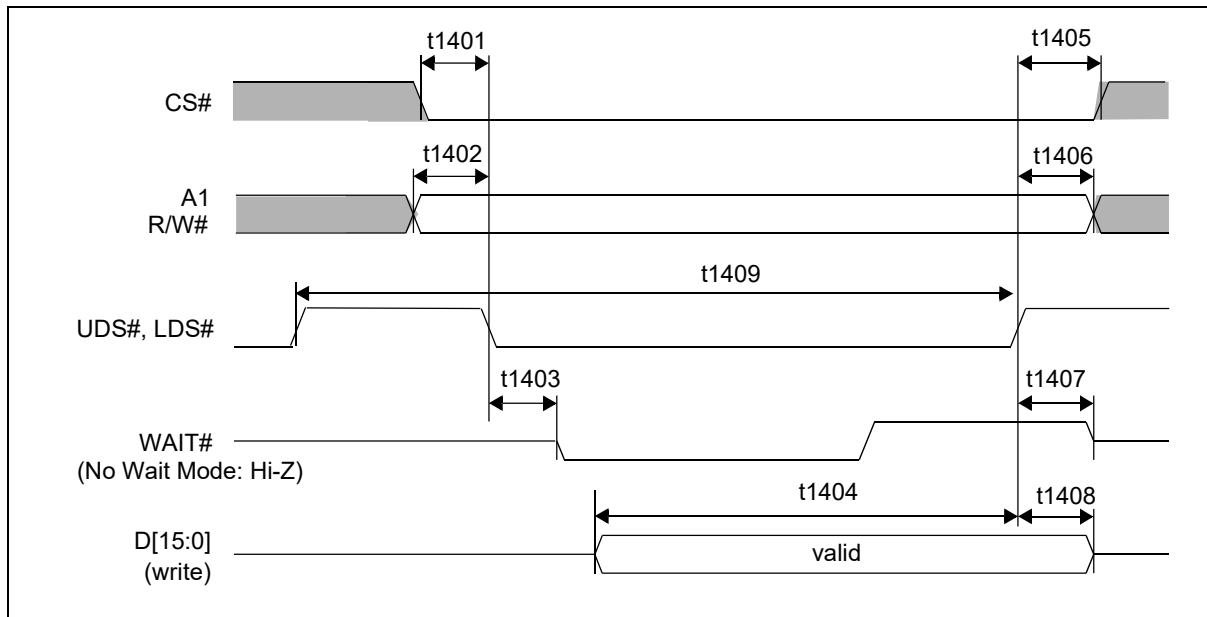


Figure 7-27: Indirect 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-41: Indirect 68 Interface Write Cycle Timing (Wait/No Wait Mode)

| Symbol | Parameter                                      | 3.0 Volt |     | Units |
|--------|------------------------------------------------|----------|-----|-------|
|        |                                                | Min      | Max |       |
| t1401  | CS# setup time                                 | 5        |     | ns    |
| t1402  | A1, R/W# setup time                            | 5        |     | ns    |
| t1403  | UDS#, LDS# falling edge to WAIT# driven low    |          | 12  | ns    |
| t1404  | D[15:0] setup time to UDS#, LDS# rising edge   | 15       |     | ns    |
| t1405  | CS# hold time from UDS#, LDS# rising edge      | 3        |     | ns    |
| t1406  | A1, R/W# hold time from UDS#, LDS# rising edge | 3        |     | ns    |
| t1407  | UDS#, LDS# rising edge to WAIT# high impedance |          | 7   | ns    |
| t1408  | D[15:0] hold time from UDS#, LDS# rising edge  | 5        |     | ns    |
| t1409  | Cycle time (No wait mode only)                 | Note2,3  |     | Ts    |

1.  $T_s$  = System clock period
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.
3.  $t1409_{min} = \text{WAIT Length} + 3 T_s$

## A.C. Characteristics

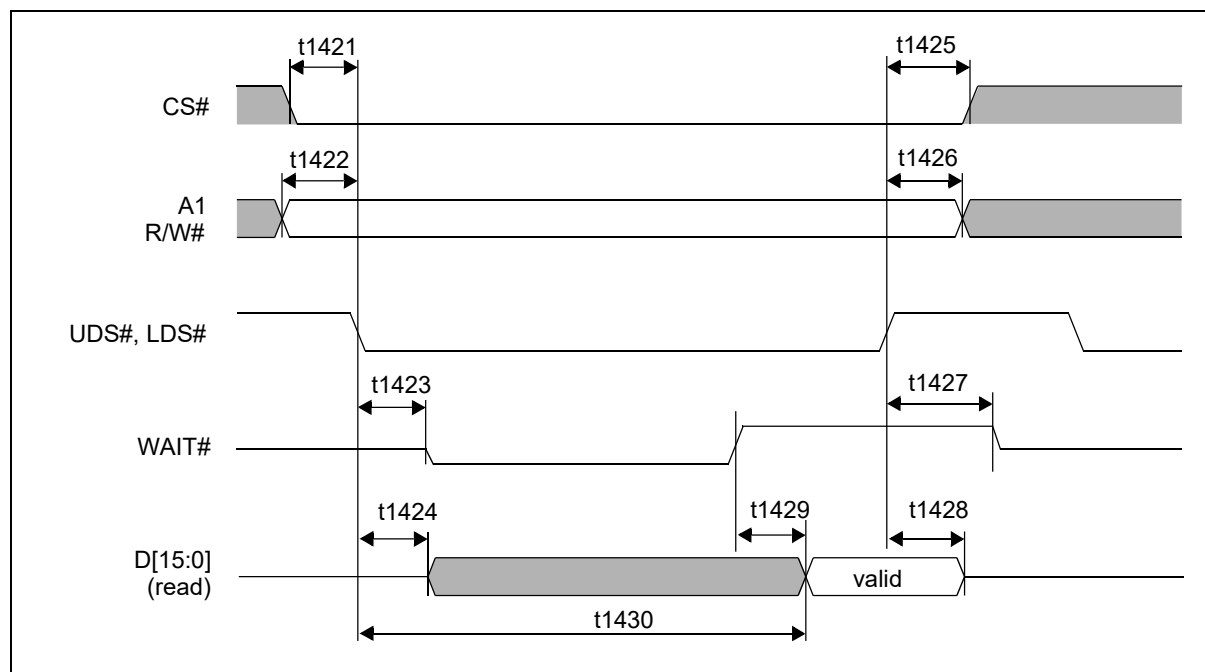


Figure 7-28: Indirect 68 Interface Read Cycle Timing (Wait Mode)

Table 7-42: Indirect 68 Interface Read Cycle Timing (Wait Mode)

| Symbol | Parameter                                                      | 3.0 Volt |     | Units |
|--------|----------------------------------------------------------------|----------|-----|-------|
|        |                                                                | Min      | Max |       |
| t1421  | CS# setup time                                                 | 5        |     | ns    |
| t1422  | A1, R/W# setup time                                            | 5        |     | ns    |
| t1423  | UDS#, LDS# falling edge to WAIT# driven low                    |          | 12  | ns    |
| t1424  | UDS#, LDS# falling edge to D[15:0] driven                      | 4        |     | ns    |
| t1425  | CS# hold time from UDS#, LDS# rising edge                      | 2        |     | ns    |
| t1426  | A1, R/W# hold time from UDS#, LDS# rising edge                 | 2        |     | ns    |
| t1427  | UDS#, LDS# rising edge to WAIT# high impedance                 |          | 7   | ns    |
| t1428  | D[15:0] hold time from UDS#, LDS# rising edge                  | 2        | 8   | ns    |
| t1429  | WAIT# rising edge to valid Data if WAIT# is asserted           |          | 10  | ns    |
| t1430  | UDS#, LDS# falling edge to valid Data if WAIT# is NOT asserted |          | 17  | ns    |

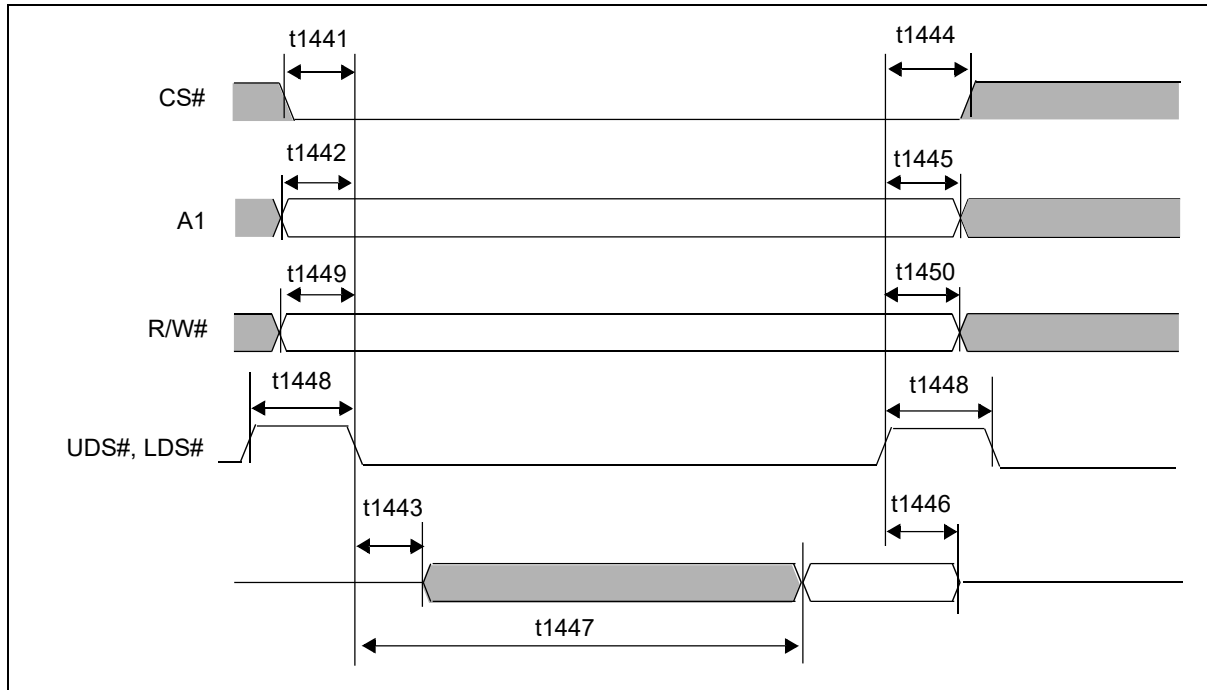


Figure 7-29: Indirect 68 Interface Read Cycle Timing (No Wait Mode)

Table 7-43: Indirect 68 Interface Read Cycle Timing (No Wait Mode)

| Symbol | Parameter                                                                     | 3.0 Volt |         | Units |
|--------|-------------------------------------------------------------------------------|----------|---------|-------|
|        |                                                                               | Min      | Max     |       |
| t1441  | CS# setup time                                                                | 0        |         | ns    |
| t1442  | A1 setup time                                                                 | 0        |         | ns    |
| t1443  | UDS#, LDS# falling edge to D[15:0] driven                                     | 4        |         | ns    |
| t1444  | CS# hold time from UDS#, LDS# rising edge                                     | 0        |         | ns    |
| t1445  | A1 hold time from UDS#, LDS# rising edge                                      | 0        |         | ns    |
| t1446  | D[15:0] hold time from UDS#, LDS# rising edge                                 | 2        | 8       | ns    |
| t1447  | UDS#, LDS# falling edge to valid Data if there are no internal delayed cycles |          | Note1,2 | ns    |
| t1448  | UDS#, LDS# pulse width high                                                   | 8        |         | ns    |
| t1449  | R/W# setup time                                                               | 5        |         | ns    |
| t1450  | R/W# hold time from UDS#, LDS# rising edge                                    | 2        |         | ns    |

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, "WAIT Length" on page 91.

2.  $t1447_{max} = \text{WAIT Length} + 25 \text{ ns}$

*Table 7-44: Indirect 68 Host Interface Truth Table for Little Endian*

| R/W# | UDS# | LDS# | D[15:8] | D[7:0] | Comments                                                                      |
|------|------|------|---------|--------|-------------------------------------------------------------------------------|
| 0    | 0    | 0    | valid   | valid  | 16-bit command write or data write                                            |
| 0    | 1    | 0    | -       | valid  | 8-bit data write (memory); data on low byte (even byte address <sup>1</sup> ) |
| 0    | 0    | 1    | valid   | -      | 8-bit data write (memory); data on high byte (odd byte address <sup>1</sup> ) |
| 1    | 0    | 0    | valid   | valid  | 16-bit data read                                                              |
| 1    | 1    | 0    | -       | valid  | 8-bit data read (memory); data on low byte (even byte address <sup>1</sup> )  |
| 1    | 0    | 1    | valid   | -      | 8-bit data read (memory); data on high byte (odd byte address <sup>1</sup> )  |

*Table 7-45: Indirect 68 Host Interface Function Select*

| A1 | R/W# | Comments                                                  |
|----|------|-----------------------------------------------------------|
| 0  | 0    | 16-bit Command Write (register address)                   |
| 1  | 0    | Data Write (16-bit register data or 8/16-bit memory data) |
| 1  | 1    | Data Read (16-bit register data or 8/16-bit memory data)  |

1. Because A0 is not used, all addresses are seen by the S1D13715 as even addresses (16-bit word address aligned on even byte addresses).

### 7.3.9 WAIT Length

The Host CPU interfaces of the S1D13715 are asynchronous. However, the CPU signals are latched internally, synchronous to the system clock. The following table shows the WAIT# length based on the system clock.

In the table, “Single” access means there is enough idle time between accesses. The minimum idle time to guarantee a single access is six system clocks from the rising edge of WE# of the current access to the rising edge of WE# of the next access. “Continuous” access means there is not enough idle time between accesses.

If Host CPU cycles are assumed to be a minimum of  $x$  clocks in length, the actual cycle length will be “ $x$  + the value in the following table”.

Table 7-46: Wait Length

| Description                                                                                 | Min           | Typ<br>(Note 4) | Max            | Unit          |
|---------------------------------------------------------------------------------------------|---------------|-----------------|----------------|---------------|
| Single Write to the registers, except the JPEG Codec registers                              |               | 0               |                | Ts<br>(Note1) |
| Continuous Write to the registers, except the JPEG Codec registers                          |               | 5               |                | Ts            |
| Single Write to the JPEG Codec registers                                                    |               | 0               |                | Ts            |
| Continuous Write to the JPEG Codec registers                                                | 4<br>(Note 3) |                 | 6<br>(Note 2)  | Ts            |
| Single Write to the display buffer                                                          |               | 0               |                | Ts            |
| Continuous Write to the display buffer                                                      |               | 4               |                | Ts            |
| Single Write to the JPEG FIFO (REG09A6h)                                                    |               | 0               |                | Ts            |
| Continuous Write to the JPEG FIFO (REG09A6h)                                                |               | 5               |                | Ts            |
| Single/Continuous Read from the registers, except the JPEG Codec registers                  |               | 5               |                | Ts            |
| Read from the registers after a Write, except the JPEG Codec registers                      |               | 8               |                | Ts            |
| Single/Continuous Read from the JPEG Codec registers, except the JPEG Codec Table registers | 5<br>(Note 3) |                 | 7<br>(Note 2)  | Ts            |
| Read from the JPEG Codec registers after a Write, except the JPEG Codec Table registers     | 8<br>(Note 3) |                 | 10<br>(Note 2) | Ts            |
| Single/Continuous Read from the display buffer                                              |               | 5               |                | Ts            |
| Read from the display buffer after a Write                                                  |               | 7               |                | Ts            |
| 1st access of a JPEG FIFO continuous read                                                   |               | 4               |                | Ts            |
| Last 2 accesses of a JPEG FIFO continuous read                                              |               | 4               |                | Ts            |
| Accesses of JPEG FIFO continuous read, except above                                         |               | 0               |                | Ts            |

1. Ts = System Clock Period
2. Memory arbitration (Camera and JPEG modules are enabled)
3. No memory arbitration (Camera and JPEG modules are disabled)
4. These are typical values. Actual WAIT lengths may be larger than specified when multiple blocks of the S1D13715 are enabled.

7.4 Panel Interface Timing

7.4.1 Generic TFT Panel Timing

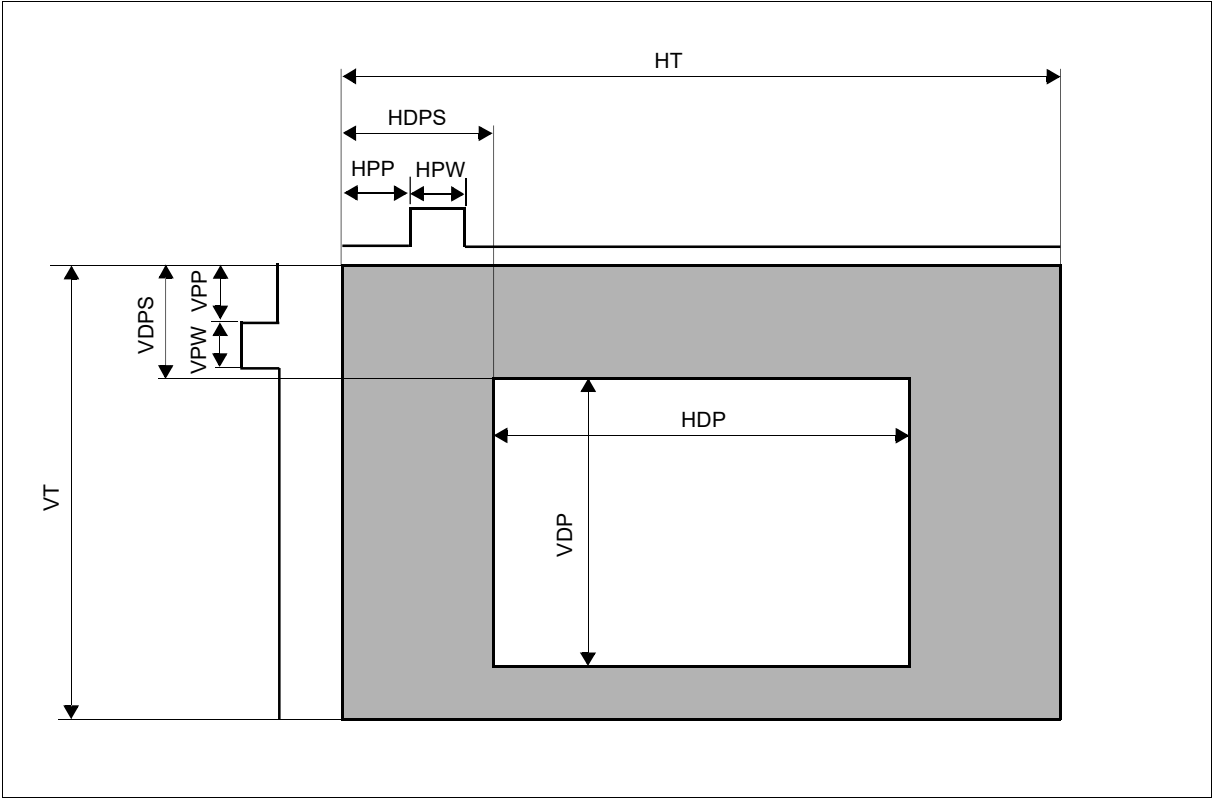


Figure 7-30: Generic TFT Panel Timing

Table 7-47: Generic TFT Panel Timing

| Symbol | Description                                   | Derived From                    | Units |
|--------|-----------------------------------------------|---------------------------------|-------|
| HT     | LCD1 Horizontal total                         | ((REG[0040h] bits 6-0) + 1) x 8 | Ts    |
| HDP    | LCD1 Display Period                           | ((REG[0042h] bits 9-1) + 1) x 2 |       |
| HDPS   | LCD1 Horizontal Display Period Start Position | ((REG[0044h] bits 9-0) + 9      |       |
| HPW    | LCD1 FPLINE Pulse Width                       | (REG[0046h] bits 6-0) + 1       |       |
| HPP    | LCD1 FPLINE Pulse Position (see note 2)       | (REG[0048h] bits 9-0) + 1       |       |
| VT     | LCD1 Vertical Total                           | (REG[004Ah] bits 9-0) + 1       | Lines |
| VDP    | LCD1 Vertical Display Period                  | (REG[004Ch] bits 9-0) + 1       |       |
| VDPS   | LCD1 Vertical Display Period Start Position   | REG[004Eh] bits 9-0             |       |
| VPW    | LCD1 FPFRAME Pulse Width                      | (REG[50h] bits 2-0) + 1         |       |
| VPP    | LCD1 FPFRAME Pulse Position (see note 2)      | REG[0052h] bits 9-0             |       |

1. The following formulas must be valid for all panel timings:  
HDPS + HDP < HT  
VDPS + VDP < VT
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. These values may be used to configure extended TFT types as required.

## Generic RGB Type Interface Panel Horizontal Timing

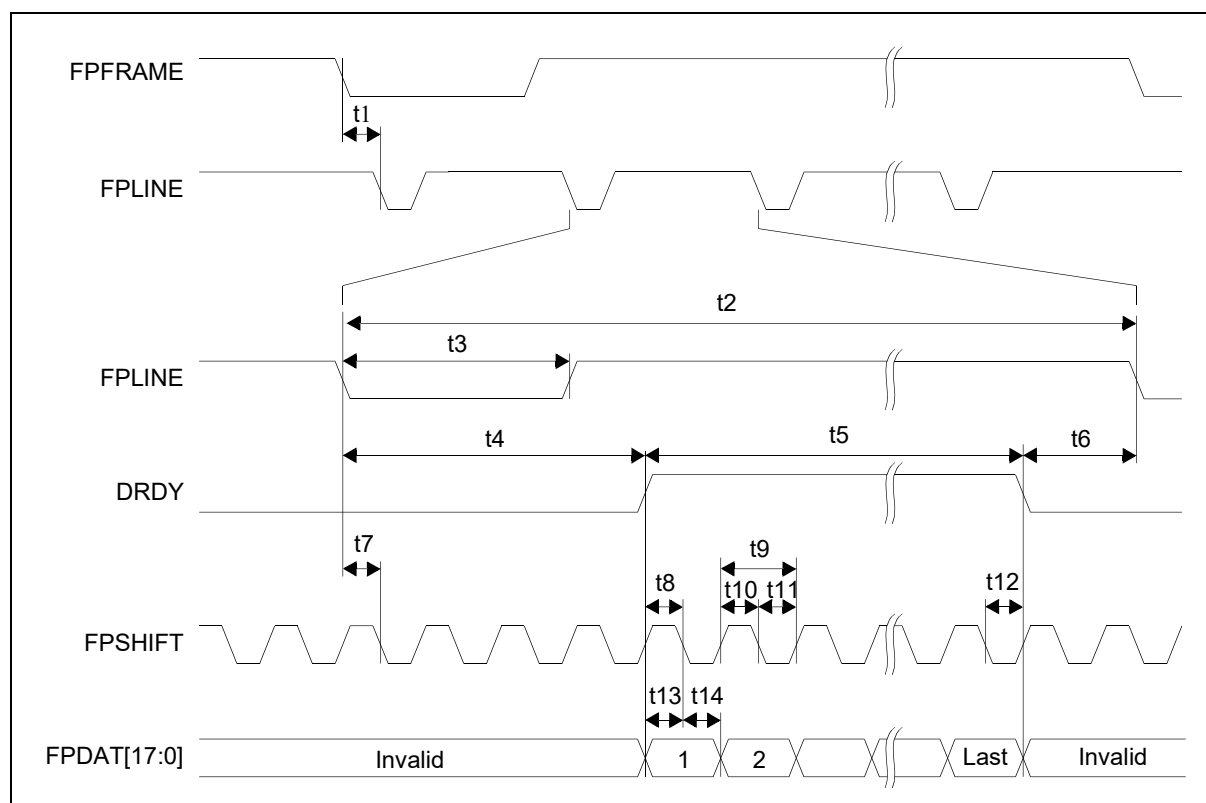


Figure 7-31: Generic RGB Type Interface Panel Horizontal Timing

Table 7-48: Generic RGB Type Interface Panel Horizontal Timing

| Symbol | Parameter                                   | Min | Typ             | Max | Units       |
|--------|---------------------------------------------|-----|-----------------|-----|-------------|
| t1     | FPFRAME falling edge to FPLINE falling edge |     | HPP<br>(note 2) |     | Ts (note 1) |
| t2     | Horizontal total period                     |     | HT              |     | Ts          |
| t3     | FPLINE pulse width                          |     | HPW             |     | Ts          |
| t4     | FPLINE falling edge to DRDY active          |     | HDPS            |     | Ts          |
| t5     | Horizontal display period                   |     | HDP             |     | Ts          |
| t6     | DRDY falling edge to FPLINE falling edge    |     | note 3          |     | Ts          |
| t7     | FPLINE setup time to FPSHIFT falling edge   |     | 0.5             |     | Ts          |
| t8     | DRDY setup to FPSHIFT falling edge          |     | 0.5             |     | Ts          |
| t9     | FPSHIFT period                              |     | 1               |     | Ts          |
| t10    | FPSHIFT pulse width high                    |     | 0.5             |     | Ts          |
| t11    | FPSHIFT pulse width low                     |     | 0.5             |     | Ts          |
| t12    | DRDY hold from FPSHIFT falling edge         |     | 0.5             |     | Ts          |
| t13    | Data setup to FPSHIFT falling edge          |     | 0.5             |     | Ts          |
| t14    | Data hold from FPSHIFT falling edge         |     | 0.5             |     | Ts          |

1. Ts = pixel clock period
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. This values may be used to configure extended TFT types as required.
3. t6typ = t2 - t4 - t5

### Note

The Generic TFT timings are based on the following:

FPFRAME Pulse Polarity bit is active low (REG[0050h] bit 7 = 0).

FPLINE Pulse Polarity bit is active low (REG[0046h] bit 7 = 0).

## Generic RGB Type Interface Panel Vertical Timing

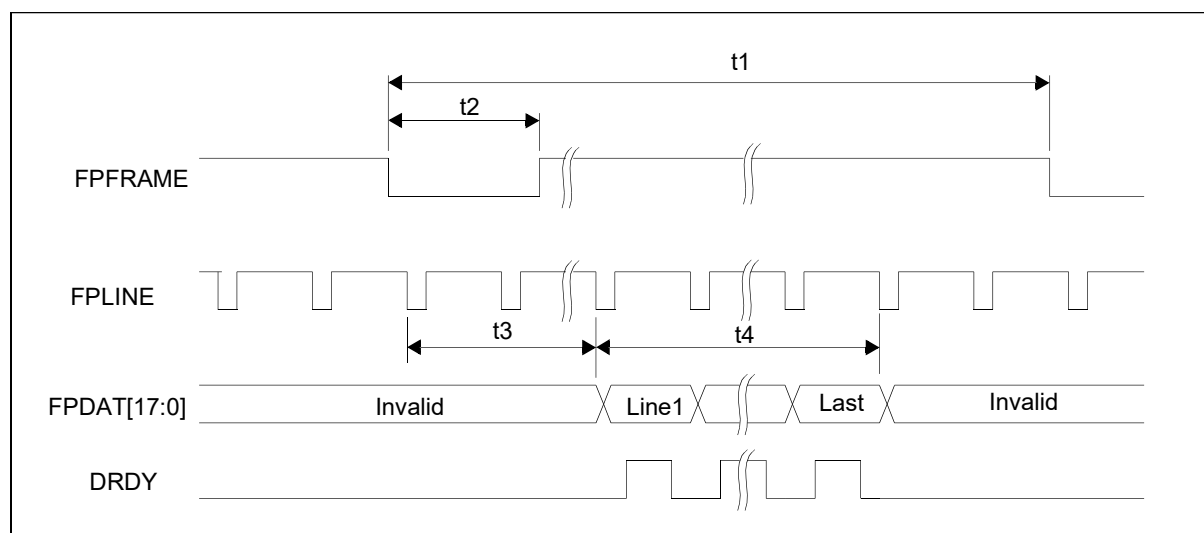


Figure 7-32: Generic RGB Type Interface Panel Vertical timing

Table 7-49: Generic RGB Type Interface Panel Vertical Timing

| Symbol | Parameter                                | Min | Typ    | Max | Units |
|--------|------------------------------------------|-----|--------|-----|-------|
| t1     | Vertical total period                    |     | VT     |     | Line  |
| t2     | FPFRAME pulse width                      |     | VPW    |     | Line  |
| t3     | Vertical display start position (note 1) |     | note 2 |     | Line  |
| t4     | Vertical display period                  |     | VDP    |     | Line  |

- t3 is measured from the first FPLINE pulse at the start of the frame to the last FPLINE pulse before FPDAT is valid.
- t3typ = VDPS - VPP (For generic TFT panel types, the VPP value must be programmed to 0. This value may be used to configure extended TFT types as required).

7.4.2 HR-TFT Panel Timing

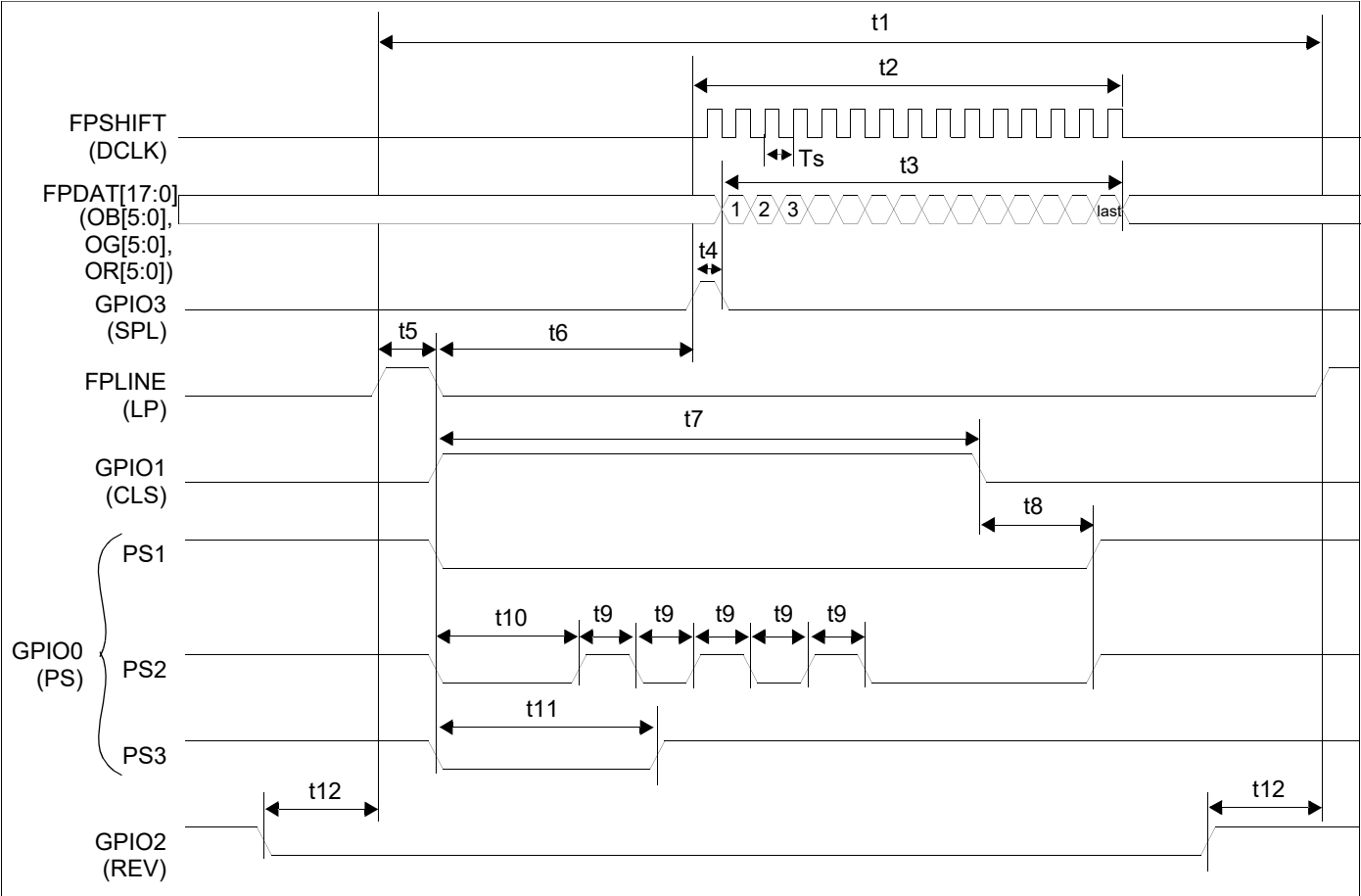


Figure 7-33: HR-TFT Panel Horizontal Timing

Table 7-50: HR-TFT Panel Horizontal Timing

| Symbol | Parameter                                                       | Min | Typ     | Max  | Units       |
|--------|-----------------------------------------------------------------|-----|---------|------|-------------|
| t1     | Horizontal total period                                         | 8   | Note 2  | 1024 | Ts (note 1) |
| t2     | FPSHIFT active                                                  | 9   | Note 3  | 1025 | Ts          |
| t3     | Horizontal display period                                       | 8   | Note 4  | 1024 | Ts          |
| t4     | GPIO3 pulse width                                               |     | 1       |      | Ts          |
| t5     | FPLINE pulse width                                              | 1   | Note 5  | 128  | Ts          |
| t6     | FPLINE falling edge to GPIO3 rising edge                        | 2   | Note 6  | -    | Ts          |
| t7     | GPIO1 pulse width                                               | 1   | Note 7  | 511  | Ts          |
| t8     | GPIO1 falling edge to GPIO0 (PS1) rising edge                   | 0   | Note 8  | 63   | Ts          |
| t9     | GPIO0 (PS2) toggle width                                        | 1   | Note 9  | 127  | Ts          |
| t10    | GPIO0 (PS2) first falling edge to GPIO0 (PS2) first rising edge | 1   | Note 10 | 255  | Ts          |
| t11    | GPIO0 (PS3) pulse width                                         | 1   | Note 11 | 127  | Ts          |
| t12    | GPIO2 (REV) toggle position to FPLINE rising edge               | 1   | Note 12 | 31   | Ts          |

1. Ts = pixel clock period
2. t1typ =  $[(\text{REG}[0040\text{h}] \text{ bits } 6-0) + 1] * 8$
3. t2typ =  $[(\text{REG}[0042\text{h}] \text{ bits } 8-0) + 1] * 2 + 1$
4. t3typ =  $[(\text{REG}[0042\text{h}] \text{ bits } 8-0) + 1] * 2$
5. t5typ =  $(\text{REG}[0046\text{h}] \text{ bits } 6-0) + 1$
6. t6typ =  $\text{REG}[0044\text{h}] \text{ bits } 9-0 - \text{REG}[0046\text{h}] \text{ bits } 6-0 + 2$
7. t7typ =  $(\text{REG}[0092\text{h}] \text{ bits } 8-0) > 0$
8. t8typ =  $(\text{REG}[0094\text{h}] \text{ bits } 5-0)$
9. t9typ =  $(\text{REG}[0098\text{h}] \text{ bits } 6-0) > 0$
10. t10typ =  $(\text{REG}[0096\text{h}] \text{ bits } 7-0) > 0$
11. t11typ =  $(\text{REG}[009A\text{h}] \text{ bits } 6-0) > 0$
12. t12typ =  $(\text{REG}[009E\text{h}] \text{ bits } 4-0) > 0$

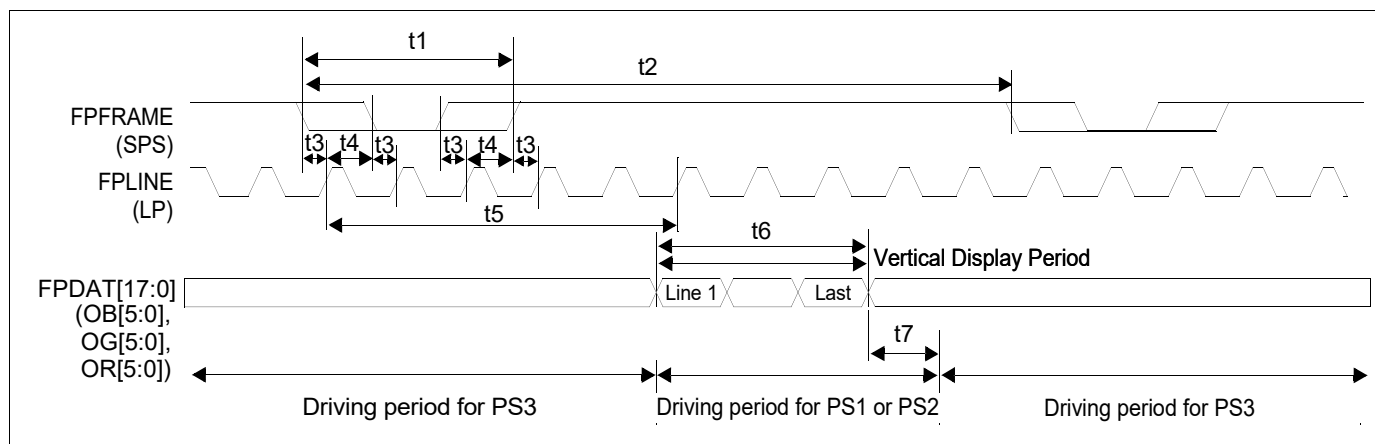


Figure 7-34: HR-TFT Panel Vertical Timing

Table 7-51: HR-TFT Panel Vertical Timing

| Symbol | Parameter                                        | Min | Typ           | Max  | Units       |
|--------|--------------------------------------------------|-----|---------------|------|-------------|
| t1     | FFRAME pulse width                               | 1   | Note 2        | 8    | Lines       |
| t2     | Vertical total period                            | 1   | Note 3        | 1024 | Lines       |
| t3     | FFRAME rising/falling edge to FPLINE rising edge |     | 1<br>(Note 4) |      | Ts (Note 1) |
| t4     | FPLINE rising edge to FFRAME rising/falling edge | 0   | Note 4        | 1023 | Ts          |
| t5     | Vertical display start position                  | 0   | Note 5        | 1023 | Lines       |
| t6     | Vertical display period                          | 1   | Note 6        | 1024 | Lines       |
| t7     | Extra driving period for PS1/2                   | 0   | Note 7        | 7    | Lines       |

1. Ts = pixel clock period
2. t1typ = (REG[0050h] bits 2-0) + 1
3. t2typ = (REG[004Ah] bits 9-0) + 1
4. t3typ The FFRAME (SPS) rising/falling edge can occur before or after FPLINE (LP) rising edge depending on the value stored in the FPLINE Pulse Start Position bits (REG[0048h] bits 9-0). To obtain the case indicated by t3, set the FPLINE Pulse Start Position bits to 0 and the FFRAME (SPS) rising/falling edge will occur 1 Ts before the FPLINE (LP) rising edge. To obtain the case indicated by t4, set the FPLINE Pulse Start Position bits to a value between 1 and the Horizontal Total - 1. Then t4 = (Horizontal Total Period - 1) - (REG[0048h] bits 9-0)
5. When REG[0048h] bits 9-0 > 4, t5typ = REG[004Eh] bits 9-0 - REG[0052h] bits 9-0  
When 0 ≤ REG[0048h] bits 9-0 ≤ 4, t5typ = REG[004Eh] bits 9-0 - REG[0052h] bits 9-0 + 1
6. t6typ = (REG[004Ch] bits 9-0) + 1
7. t7typ = (REG[00A0h] bits 2-0)

### 7.4.3 Casio TFT Panel Timing

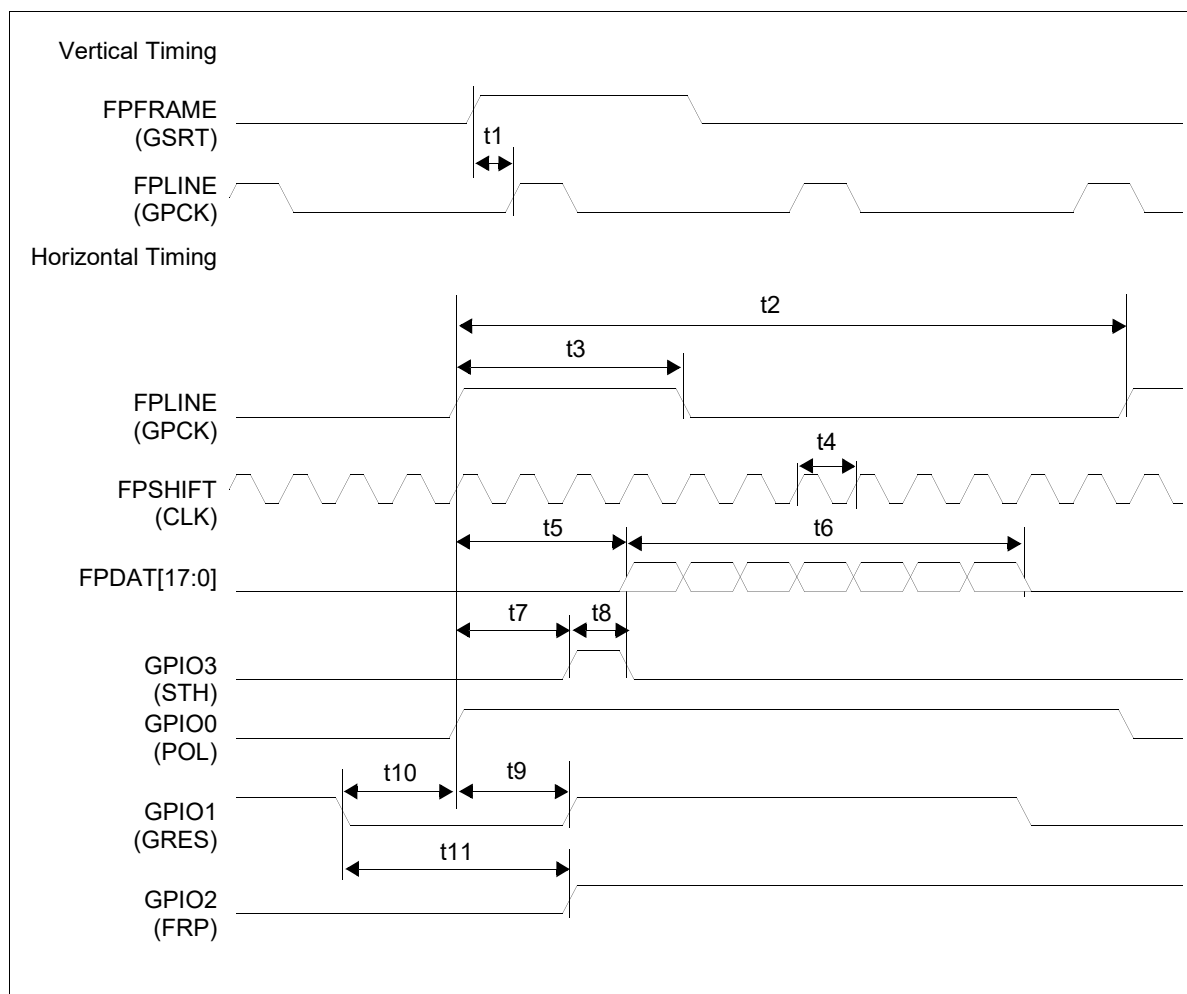


Figure 7-35: Casio TFT Horizontal Timing

Table 7-52: Casio TFT Horizontal Timing

| Symbol | Parameter                                 | Min | Typ     | Max  | Units       |
|--------|-------------------------------------------|-----|---------|------|-------------|
| t1     | Horizontal pulse start position           | 1   | Note 2  | 1024 | Ts          |
| t2     | Horizontal total                          | 8   | Note 3  | 1024 | Ts          |
| t3     | Horizontal pulse width                    | 1   | Note 4  | 128  | Ts          |
| t4     | Pixel clock period                        |     | Note 5  |      | Ts (Note 1) |
| t5     | Horizontal display period start position  | 4   | Note 6  | 1027 | Ts          |
| t6     | Horizontal display period                 | 8   | Note 7  | 1024 | Ts          |
| t7     | FPLINE rising edge to GPIO3 rising edge   | 0   | Note 8  | 63   | Ts          |
| t8     | GPIO3 pulse width                         |     | 1       |      | Ts          |
| t9     | FPLINE rising edge to GPIO1 rising edge   | 0   | Note 9  | 63   | Ts          |
| t10    | GPOIO1 falling edge to FPLINE rising edge | 1   | Note 10 | 64   | Ts          |
| t11    | FPLINE falling edge to GPIO2 toggle point | 0   | Note 11 | 127  | Ts          |

1. Ts = Pixel clock period
2. t1typ = [(REG[0048h] bits 9-0) + 1]
3. t2typ = [(REG[0040h] bits 6-0) + 1] \* 8
4. t3typ = [(REG[0046h] bits 6-0) + 1]
5. t4typ = depends on the pixel clock (PCLK)
6. t5typ = (REG[0044h] bits 9-0) + 4
7. t6typ = [(REG[0042h] bits 8-0) + 1] \* 2
8. t7typ = (REG[00A6h] bits 13-8)
9. t9typ = (REG[00A4h] bits 5-0)
10. t10typ = (REG[00A4h] bits 13-8)+1
11. t11typ = (REG[00A6h] bits 6-0)

### Note

For Casio Panels set the following:

FPPFRAME Pulse Polarity bit to active high (REG[0050h] bit 8 = 1).

FPLINE Pulse Polarity bit to active high (REG[0046h] bit 8 = 1).

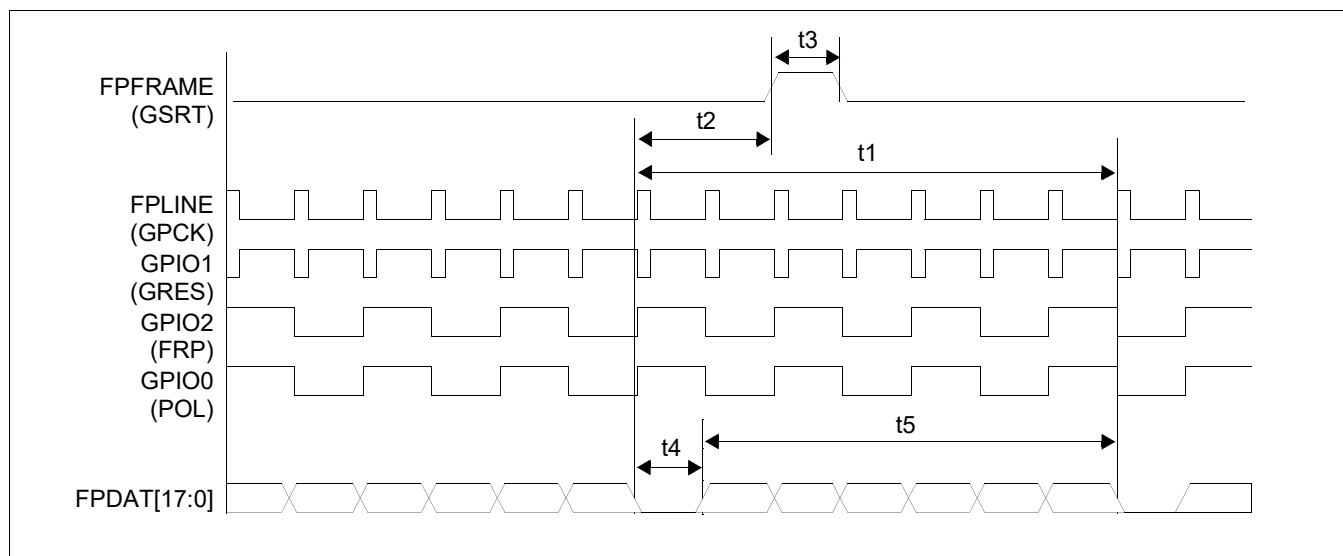


Figure 7-36: Casio TFT Vertical Timing

Table 7-53: Casio TFT Vertical Timing

| Symbol | Parameter                              | Min | Typ    | Max  | Units |
|--------|----------------------------------------|-----|--------|------|-------|
| $t_1$  | Vertical total                         | 1   | Note 1 | 1024 | Lines |
| $t_2$  | Vertical pulse start                   | 0   | Note 2 | 1023 | Lines |
| $t_3$  | Vertical pulse width                   | 1   | Note 3 | 8    | Lines |
| $t_4$  | Vertical display period start position | 1   | Note 4 | 1024 | Lines |
| $t_5$  | Vertical display period                | 1   | Note 5 | 1024 | Lines |

1.  $t_{1typ} = (\text{REG}[004Ah] \text{ bits } 9-0) + 1$
2.  $t_{2typ} = (\text{REG}[0052h] \text{ bits } 9-0) - 1$
3.  $t_{3typ} = (\text{REG}[0050h] \text{ bits } 2-0) + 1$
4.  $t_{4typ} = (\text{REG}[004Eh] \text{ bits } 9-0) + 1$
5.  $t_{5typ} = (\text{REG}[004Ch] \text{ bits } 9-0) + 1$
6.  $t_2 < t_4$

7.4.4  $\alpha$ -TFT Panel Timing

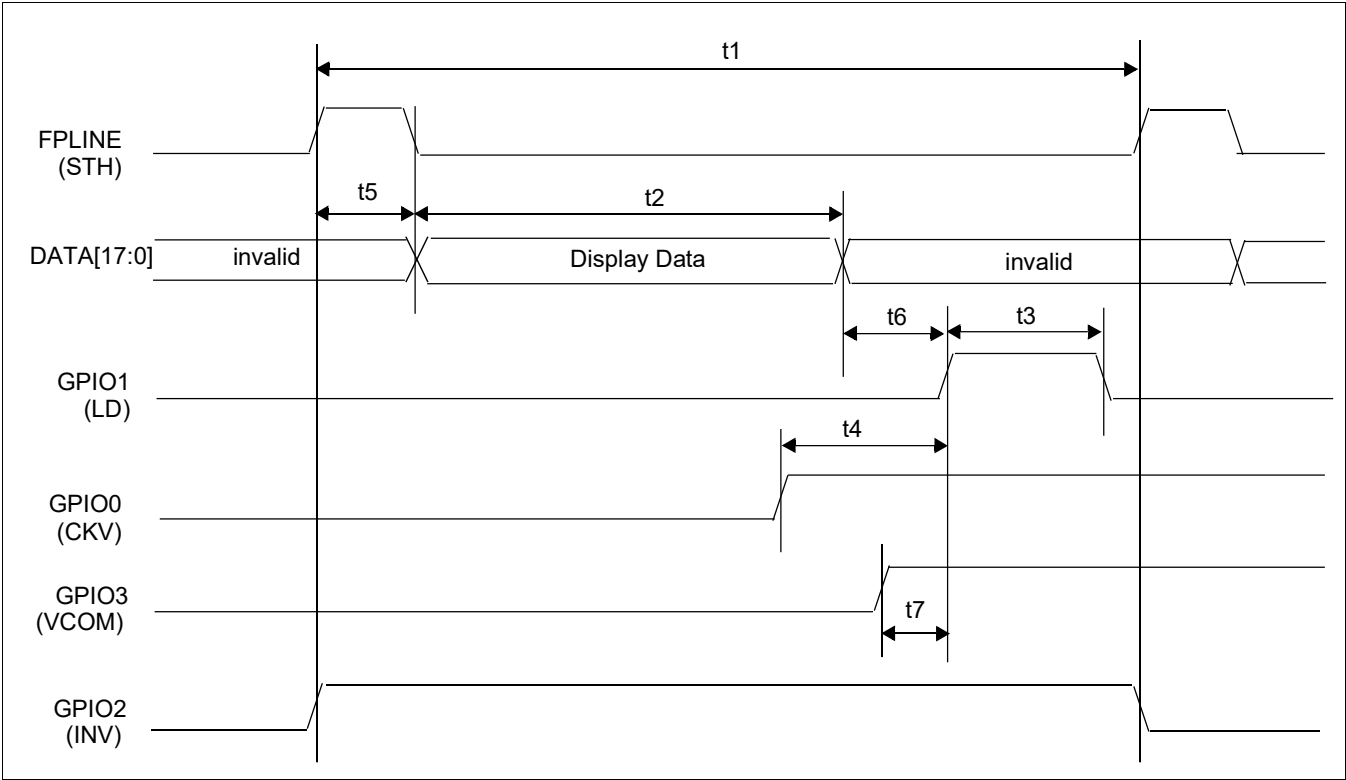


Figure 7-37:  $\alpha$ -TFT Panel Horizontal Timing

Table 7-54:  $\alpha$ -TFT Panel Horizontal Timing

| Symbol | Parameter                         | Min | Typ             | Max  | Units       |
|--------|-----------------------------------|-----|-----------------|------|-------------|
| t1     | Horizontal total period           |     | 282<br>(Note 2) | 1024 | Ts (Note 1) |
| t2     | Horizontal Display period         |     | 240<br>(Note 3) | 1014 | Ts          |
| t3     | GPIO1 (LD) pulse width            | 1   | 4<br>(Note 4)   | 8    | Ts          |
| t4     | GPIO0 (CKV) rise edge position    | 0   | 28<br>(Note 5)  | 127  | Ts          |
| t5     | FPLINE (STH) pulse width          | 1   | 1<br>(Note 6)   | 8    | Ts          |
| t6     | GPIO1 (LD) rising edge            | 0   | 1<br>(Note 7)   | 3    | Ts          |
| t7     | GPIO3 (VCOM) rising edge position | 0   | 11<br>(Note 8)  | 63   | Ts          |

1. Ts = pixel clock period
2. t1typ = REG[0080h] bits 9-0
3. t2typ = (REG[0042h] bits 8-0 + 1) x 2
4. t3typ = REG[0088h] bits 10-8 + 1
5. t4typ = t2 + t5 + t6 - (REG[0084h] bits 9-0) + 8
6. t5typ = REG[0088h] bits 2-0 + 1
7. t6typ = (REG[0082h] bits 9-0) - t2 - t5 - 8
8. t7typ = t2 + t5 + t6 - (REG[0086h] bits 9-0) + 8

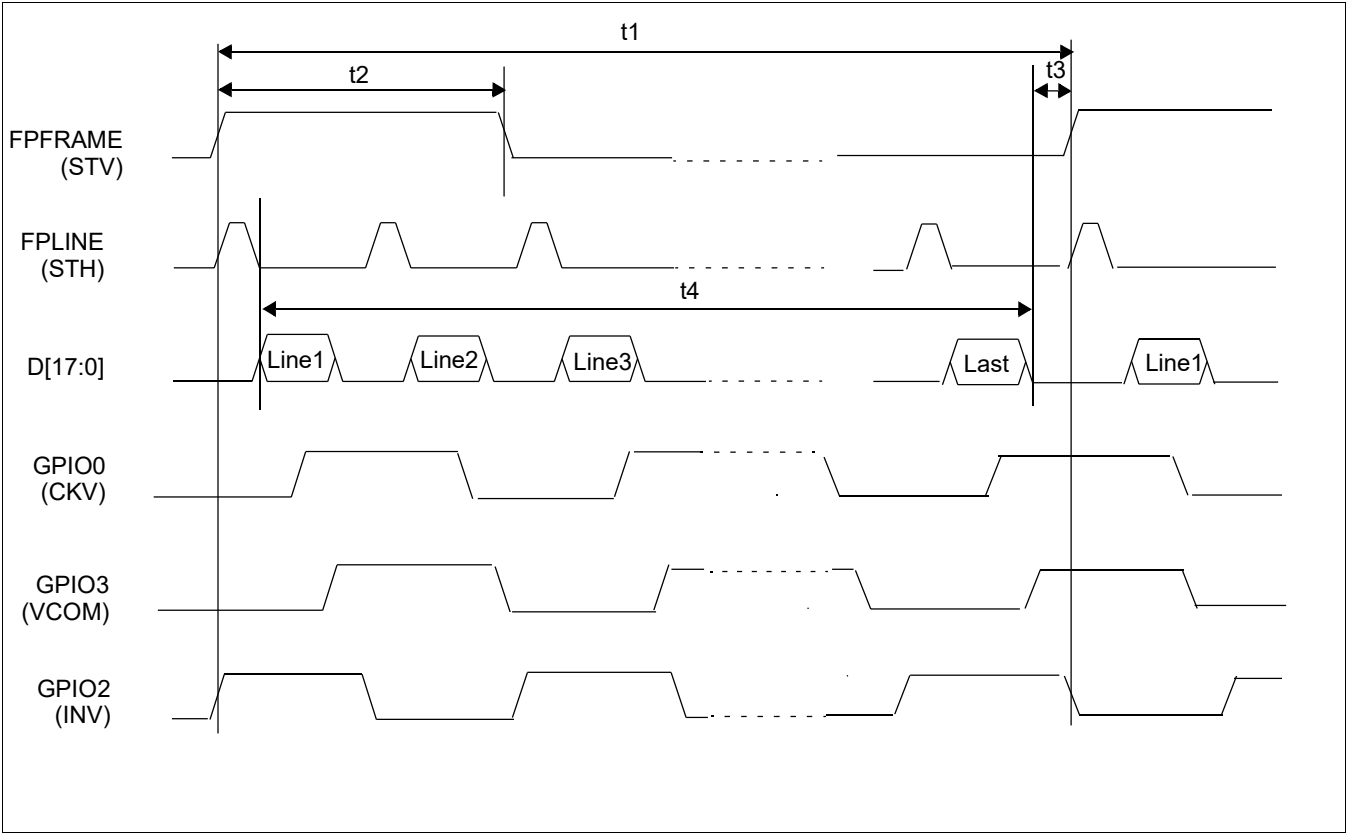


Figure 7-38:  $\alpha$ -TFT Panel Vertical Timing

Table 7-55:  $\alpha$ -TFT Panel Vertical Timing

| Symbol | Parameter                 | Min | Typ             | Max  | Units |
|--------|---------------------------|-----|-----------------|------|-------|
| t1     | Vertical total period     |     | 327<br>(Note 1) | 1024 | Lines |
| t2     | FPFRAME (STV) pulse width | 1   | 2<br>(Note 2)   |      | Lines |
| t3     | FPFRAME Hold Lines        | 1   | 7<br>(Note 3)   |      | Lines |
| t4     | Vertical display period   |     | 320<br>(Note 4) | 1022 | Lines |

- 1. t1typ = REG[004Ah] bits 9-0 + 1
- 2. t2typ = REG[0050h] bits 2-0 + 1
- 3. t3typ = t1 - t4
- 4. t4typ = REG[004Ch] bits 9-0 + 1

**Note**  
REG[004Eh] bits 9-0 must be set to zero when using the  $\alpha$ -TFT panel.

### 7.4.5 TFT Type 2 Panel Timing

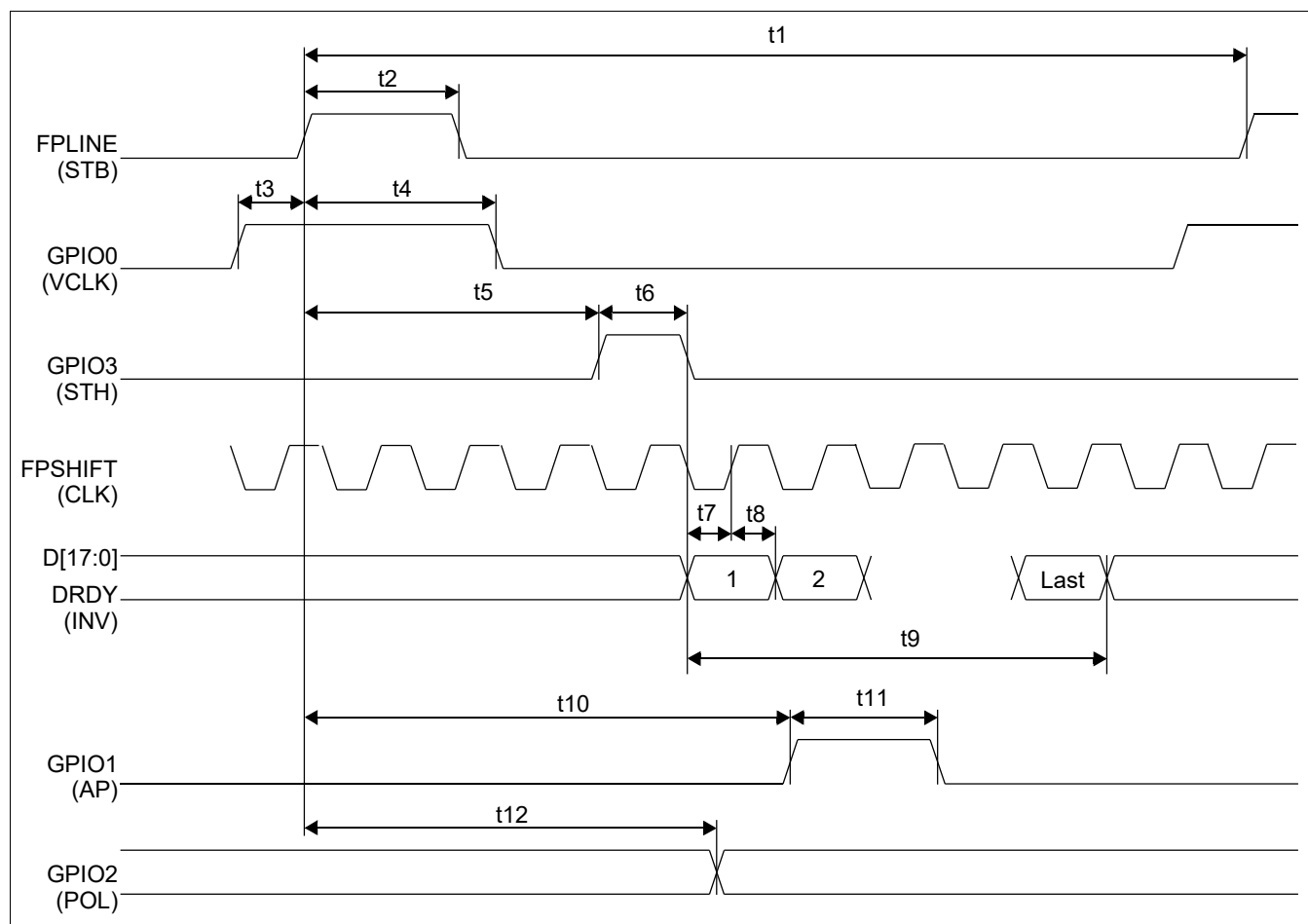


Figure 7-39: TFT Type 2 Horizontal Timing

Table 7-56: TFT Type 2 Horizontal Timing

| Symbol | Parameter                                   | Min | Typ    | Max  | Units       |
|--------|---------------------------------------------|-----|--------|------|-------------|
| t1     | Horizontal total period                     | 16  | Note 2 | 1024 | Ts (Note 1) |
| t2     | FPLINE pulse width                          |     | 5      |      | Ts          |
| t3     | GPIO0 rising edge to FPLINE rising edge     | 7   | Note 3 | 16   | Ts          |
| t4     | FPLINE rising edge to GPIO0 falling edge    | 7   | Note 4 | 16   | Ts          |
| t5     | FPLINE rising edge to GPIO3 rising edge     |     | Note 5 |      | Ts          |
| t6     | GPIO3 pulse width                           |     | 1      |      | Ts          |
| t7     | Data setup time                             | 0.5 |        |      | Ts          |
| t8     | Data hold time                              | 0.5 |        |      | Ts          |
| t9     | Horizontal display period                   | 8   | Note 6 | 1024 | Ts          |
| t10    | FPLINE rising edge to GPIO1 rising edge     | 40  | Note 7 | 90   | Ts          |
| t11    | GPIO1 pulse width                           | 20  | Note 8 | 270  | Ts          |
| t12    | FPLINE rising edge to GPIO2 toggle position |     | 10     |      | Ts          |

1. Ts = pixel clock period
2. t1typ = (REG[0040h] bits 6-0 + 1) x 8
3. t3typ = Selected from 7, 9, 12 or 16 Ts using REG[00A2h] bits 1-0
4. t4typ = Selected from 7, 9, 12 or 16 Ts using REG[00A2h] bits 4-3
5. t5typ = REG[0044h] bits 9-0 + 3
6. t9typ = (REG[0042h] bits 8-0 + 1) x 2
7. t10typ = Selected from 40, 52, 68 or 90 Ts using REG[00A2h] bits 9-8
8. t11typ = Selected from 20, 40, 80, 120, 150, 190, 240 or 270 Ts using REG[00A2h] bits 13-11

## Note

For TFT Type 2 Panels set the following:

FPFRAME Pulse Polarity bit to active high (REG[0050h] bit 7 = 1).

FPLINE Pulse Polarity bit to active high (REG[0046h] bit 7 = 1).

FPFRAME Pulse Position bits to zero (REG[0052h] bits 9-0 = 000h).

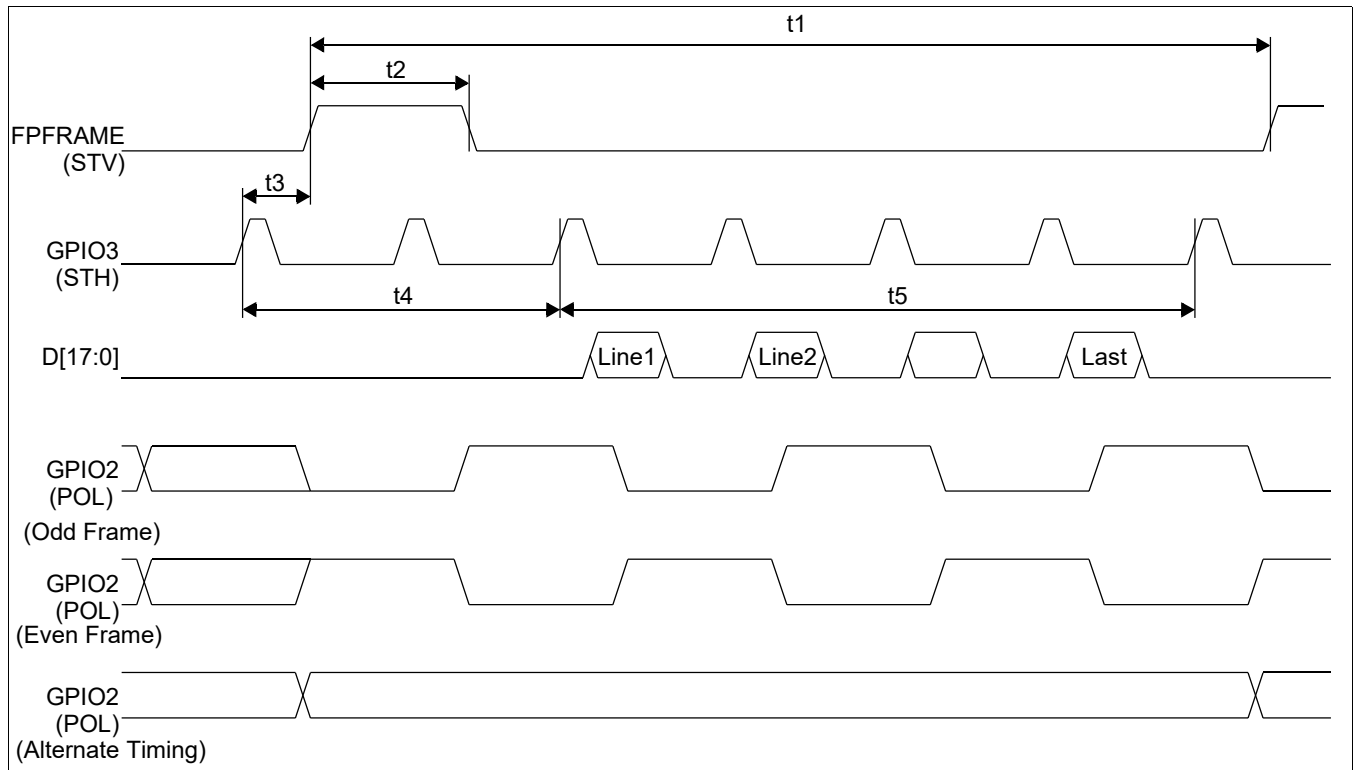


Figure 7-40: TFT Type 2 Vertical Timing

Table 7-57: TFT Type 2 Vertical Timing

| Symbol | Parameter                                | Min | Typ    | Max  | Units       |
|--------|------------------------------------------|-----|--------|------|-------------|
| $t_1$  | Vertical total period                    | 8   | Note 2 | 1024 | Lines       |
| $t_2$  | FPFRAME pulse width                      |     | 1      |      | Lines       |
| $t_3$  | GPIO3 rising edge to FPFRAME rising edge |     | 0      |      | Ts (Note 1) |
| $t_4$  | Vertical display start position          | 0   | Note 3 | 1024 | Lines       |
| $t_5$  | Vertical display period                  | 1   | Note 4 | 1024 | Ts          |

1. Ts = pixel clock period
2.  $t_{1typ}$  = REG[004Ah] bits 9-0 + 1
3.  $t_{4typ}$  = REG[004Eh] bits 9-0
4.  $t_{5typ}$  = REG[004Ch] bits 9-0 + 1

7.4.6 LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

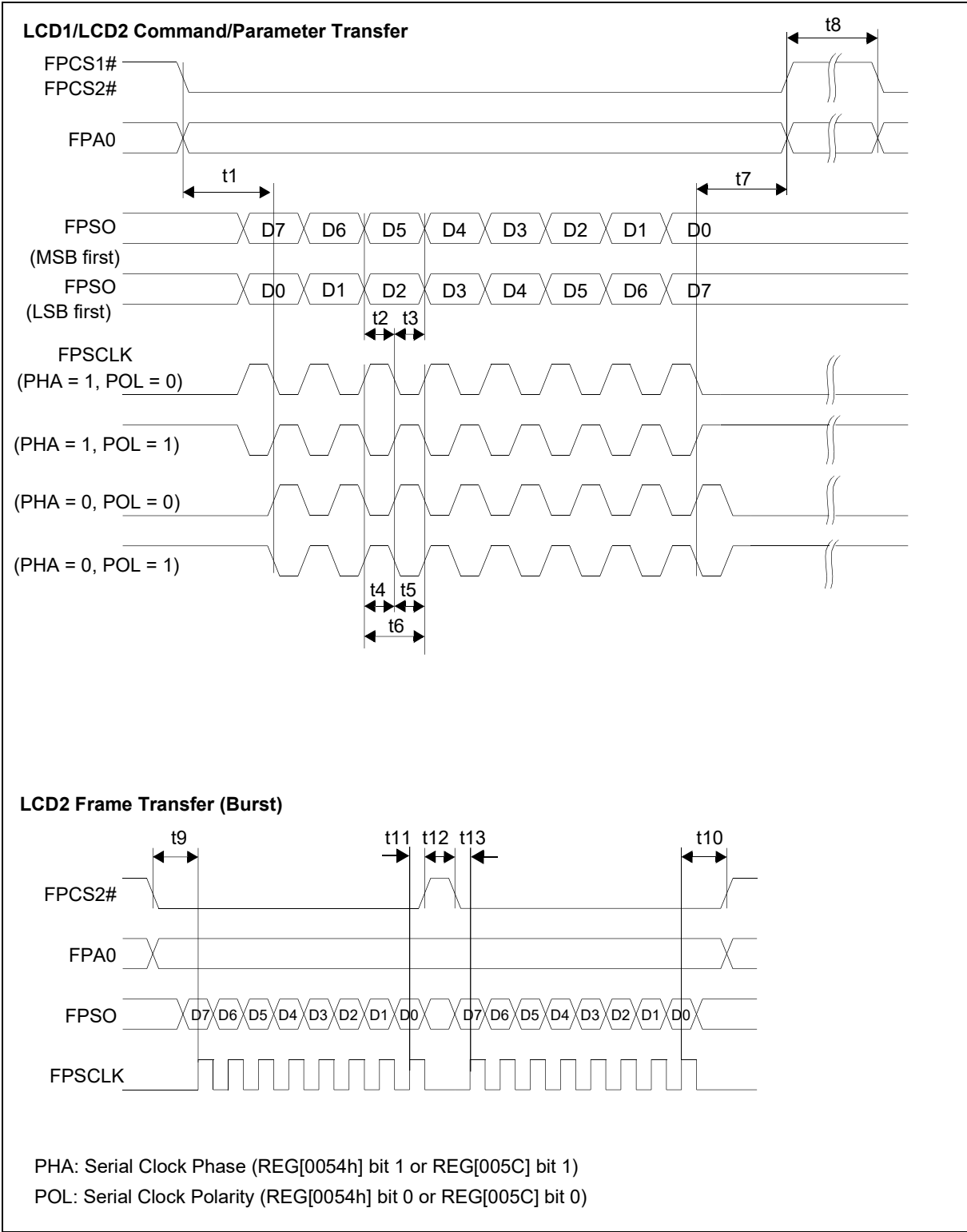


Figure 7-41: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

Table 7-58: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

| Symbol | Parameter                                            | Min | Typ | Max | Units       |
|--------|------------------------------------------------------|-----|-----|-----|-------------|
| t1     | Chip select setup time                               |     | 1.5 |     | Ts (Note 1) |
| t2     | Data setup time                                      |     | 0.5 |     | Ts          |
| t3     | Data hold time                                       |     | 0.5 |     | Ts          |
| t4     | Serial clock pulse width low (high)                  |     | 0.5 |     | Ts          |
| t5     | Serial clock pulse width high (low)                  |     | 0.5 |     | Ts          |
| t6     | Serial clock period                                  |     | 1   |     | Ts          |
| t7     | Chip select hold time for command/parameter transfer |     | 1.5 |     | Ts          |
| t8     | Chip select de-assert to reassert                    |     | 1   |     | Ts          |
| t9     | Chip select setup time at beginning of burst mode    |     | 1.5 |     |             |
| t10    | Chip select hold time at end of burst mode           |     | 2.5 |     | Ts          |
| t11    | Chip select hold time during burst mode              |     | 0.5 |     | Ts          |
| t12    | Chip select interval in burst mode                   |     | 1   |     | Ts          |
| t13    | Chip select setup time during burst mode             |     | 0.5 |     | Ts          |

1. Ts = Serial clock period

7.4.7 LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

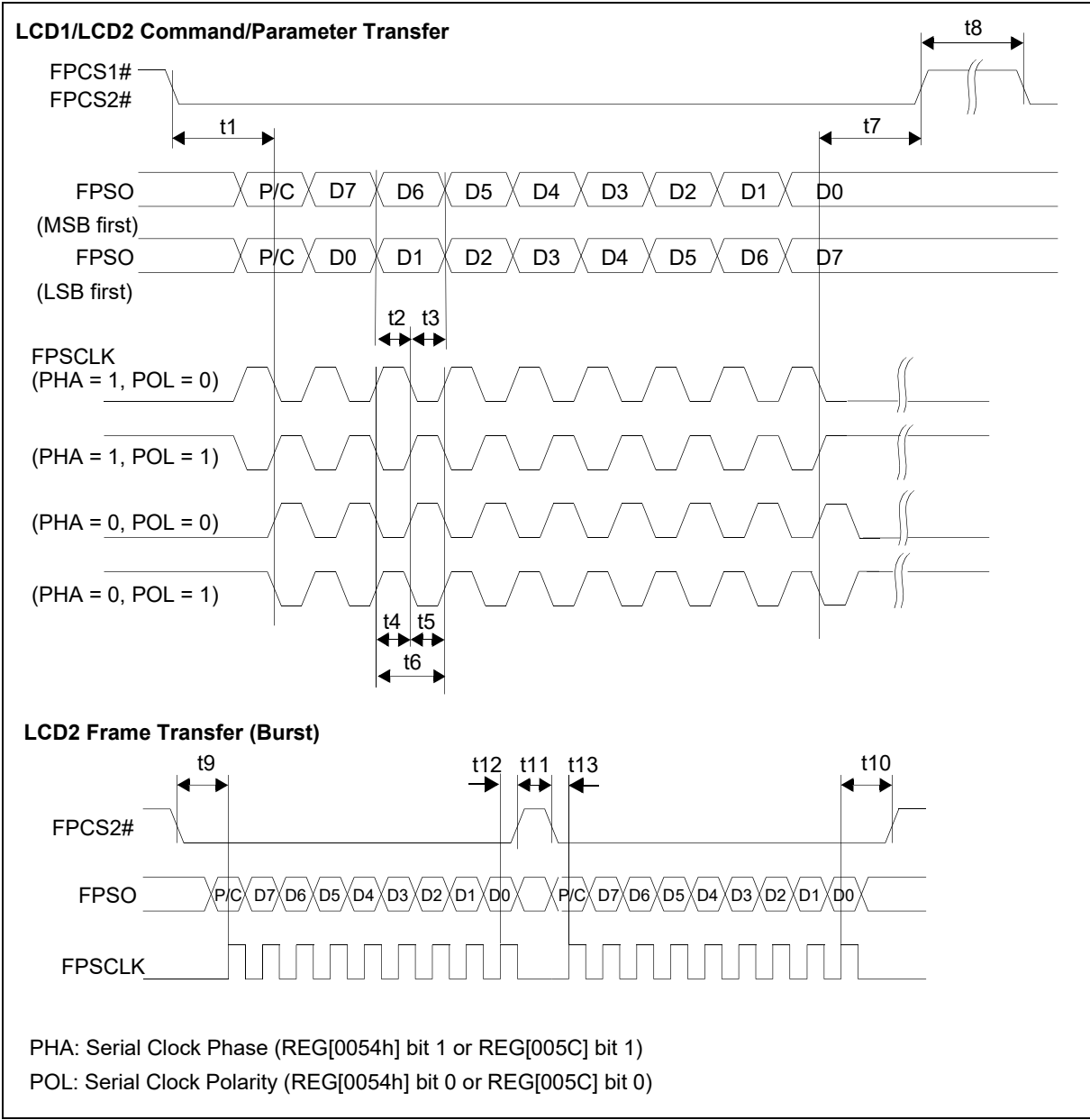


Figure 7-42: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

Table 7-59: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

| Symbol | Parameter                                         | Min | Typ | Max | Units       |
|--------|---------------------------------------------------|-----|-----|-----|-------------|
| t1     | Chip select setup time                            |     | 1.5 |     | Ts (Note 1) |
| t2     | Data setup time                                   |     | 0.5 |     | Ts          |
| t3     | Data hold time                                    |     | 0.5 |     | Ts          |
| t4     | Serial clock pulse width low (high)               |     | 0.5 |     | Ts          |
| t5     | Serial clock pulse width high (low)               |     | 0.5 |     | Ts          |
| t6     | Serial clock period                               |     | 1   |     | Ts          |
| t7     | Chip select hold time                             |     | 1.5 |     | Ts          |
| t8     | Chip select de-assert to reassert                 |     | 1   |     | Ts          |
| t9     | Chip select setup time at beginning of burst mode |     | 1.5 |     |             |
| t10    | Chip select hold time at end of burst mode        |     | 1.5 |     | Ts          |
| t11    | Chip select interval in burst mode                |     | 1   |     | Ts          |
| t12    | Chip select hold time during burst mode           |     | 0.5 |     | Ts          |
| t13    | Chip select setup time during burst mode          |     | 0.5 |     | Ts          |

1. Ts = Serial clock period

#### 7.4.8 LCD1 a-Si TFT Serial Interface Timing

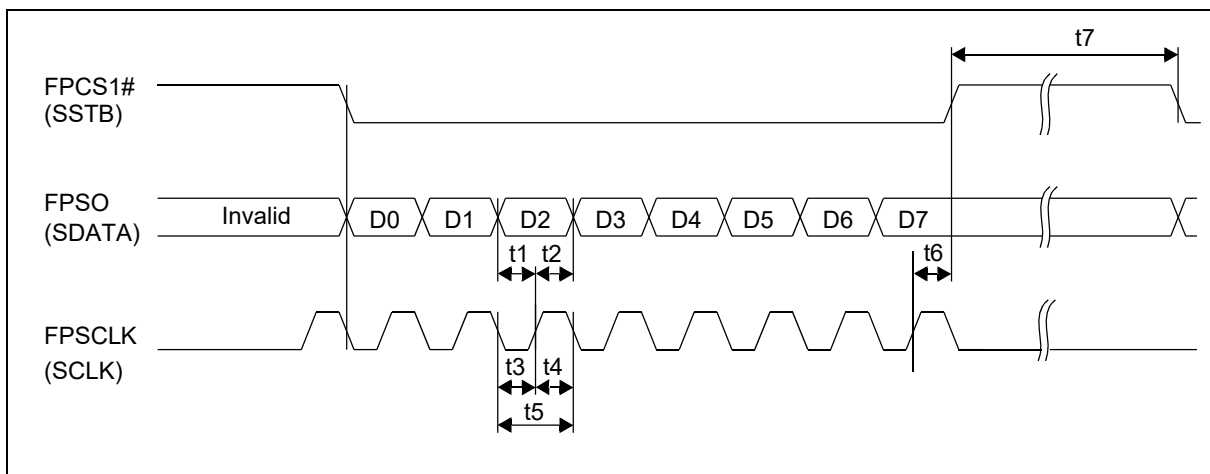


Figure 7-43: LCD1 a-Si TFT Serial Interface Timing

Table 7-60: LCD1 a-Si TFT Serial Interface Timing

| Symbol | Parameter                         | Min | Typ    | Max | Units       |
|--------|-----------------------------------|-----|--------|-----|-------------|
| t1     | Data Setup Time                   |     | 0.5    |     | Ts (Note 1) |
| t2     | Data Hold Time                    |     | 0.5    |     | Ts          |
| t3     | Serial clock plus low period      |     | 0.5    |     | Ts          |
| t4     | Serial clock pulse high period    |     | 0.5    |     | Ts          |
| t5     | Serial clock period               |     | 1      |     | Ts          |
| t6     | Chip select hold time             |     | 1.5    |     | Ts          |
| t7     | Chip select de-assert to reassert |     | Note 2 |     | Ts          |

1. Ts = Serial clock period
2. This setting depends on software

7.4.9 LCD1 uWIRE Serial Interface Timing

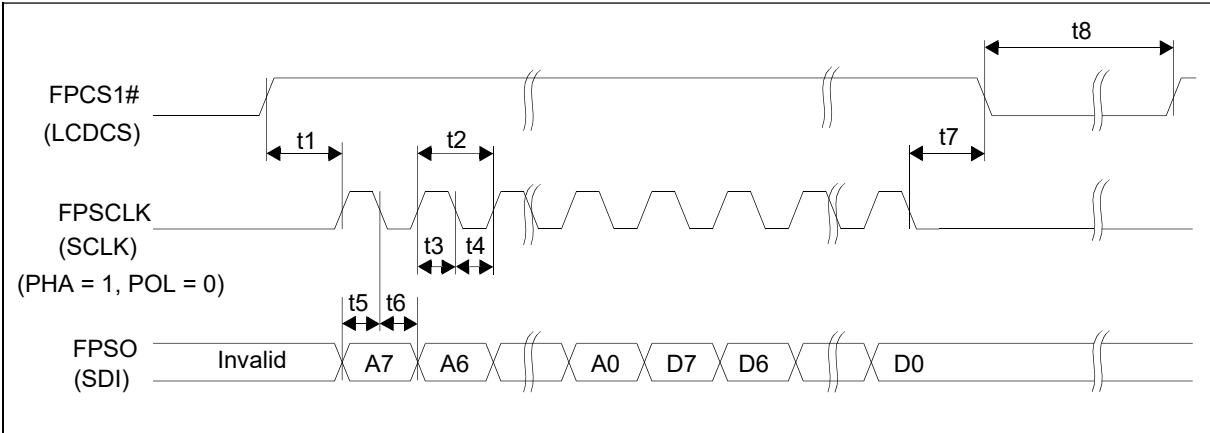


Figure 7-44: LCD1 uWIRE Serial Interface Timing

Table 7-61: LCD1 uWIRE Serial Interface Timing

| Symbol | Parameter                         | Min | Typ    | Max | Units       |
|--------|-----------------------------------|-----|--------|-----|-------------|
| t1     | Chip select setup time            |     | 1      |     | Ts (Note 1) |
| t2     | Serial Clock Period               |     | 1      |     | Ts          |
| t3     | Serial clock pulse width low      |     | 0.5    |     | Ts          |
| t4     | Serial clock pulse width high     |     | 0.5    |     | Ts          |
| t5     | Data setup time                   |     | 0.5    |     | Ts          |
| t6     | Data hold time                    |     | 0.5    |     | Ts          |
| t7     | Chip select hold time             |     | 1      |     | Ts          |
| t8     | Chip select de-assert to reassert |     | Note 2 |     | Ts          |

- 1. Ts = Serial clock period
- 2. This setting depends on software

**Note**  
When a uWire panel is selected (REG[0054h] bits 7-5 = 10x), FPCS1# idles high until the first uWire transfer is started. After the first transfer, FPCS1# idles low.

### 7.4.10 LCD1, LCD2 Parallel Interface Timing (80)

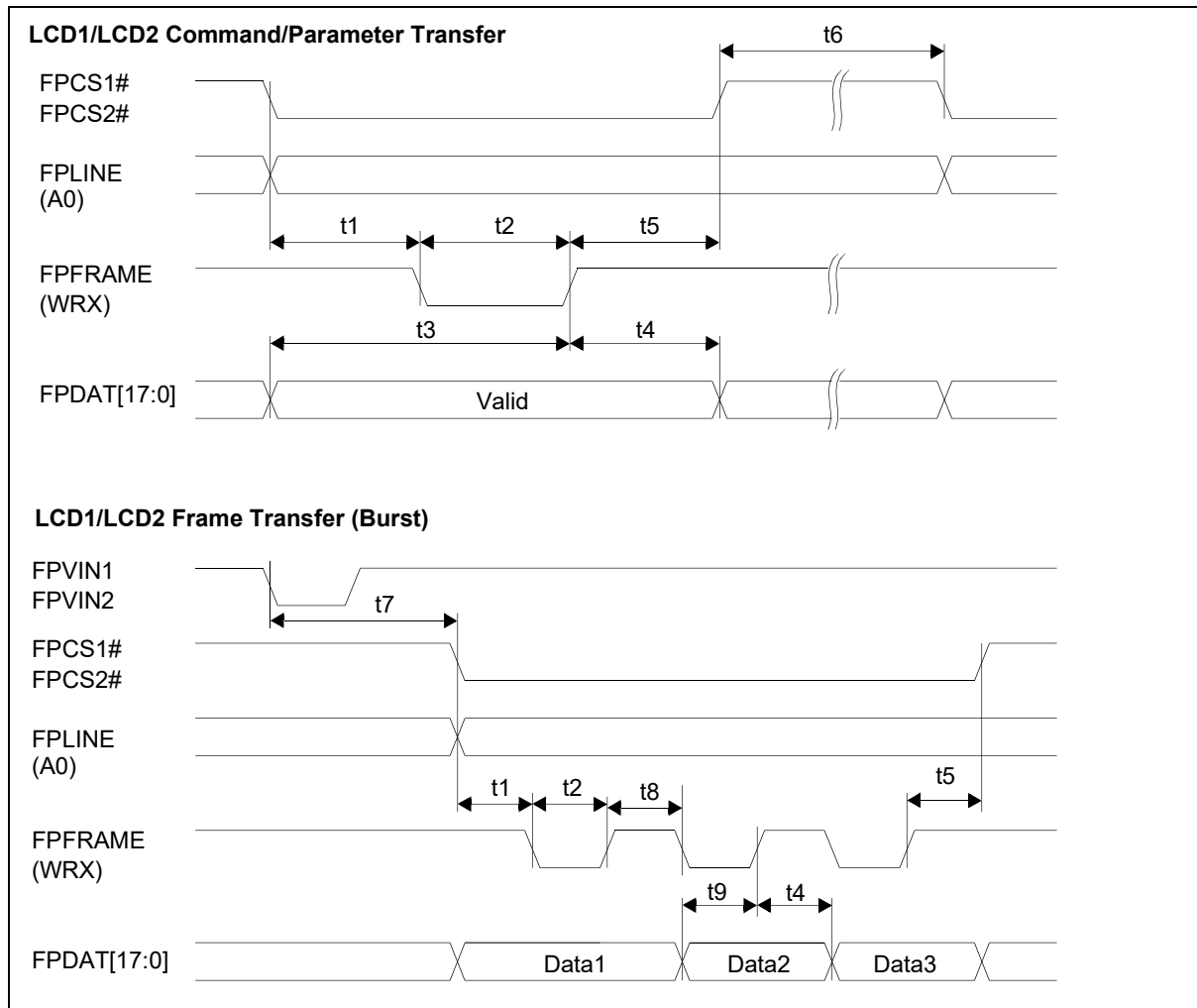


Figure 7-45: LCD1, LCD2 Parallel Interface Timing (80)

Table 7-62: LCD1, LCD2 Parallel Interface Timing (80)

| Symbol | Parameter                                                    | Min | Typ | Max | Units          |
|--------|--------------------------------------------------------------|-----|-----|-----|----------------|
| $t_1$  | Chip select falling edge to FPFAME (WRX) falling edge        |     | 1   |     | $T_s$ (Note 1) |
| $t_2$  | FPFAME (WRX) low period                                      |     | 1   |     | $T_s$          |
| $t_3$  | Data setup time for command/parameter transfers              |     | 1   |     | $T_s$          |
| $t_4$  | Data hold time                                               |     | 1   |     | $T_s$          |
| $t_5$  | Write signal rising edge to chip select rising edge          |     | 1   |     | $T_s$          |
| $t_6$  | Chip select de-assert to reassert                            |     | 0   |     | $T_s$          |
| $t_7$  | Vertical sync input falling edge to chip select falling edge |     |     | 51  | $T_s$          |
| $t_8$  | Write signal high period in burst cycle                      |     | 1   |     | $T_s$          |
| $t_9$  | Data setup time for frame transfers                          |     | 1   |     | $T_s$          |

1.  $T_s$  = Pixel clock period

## 7.4.11 LCD1, LCD2 Parallel Interface Timing (68)

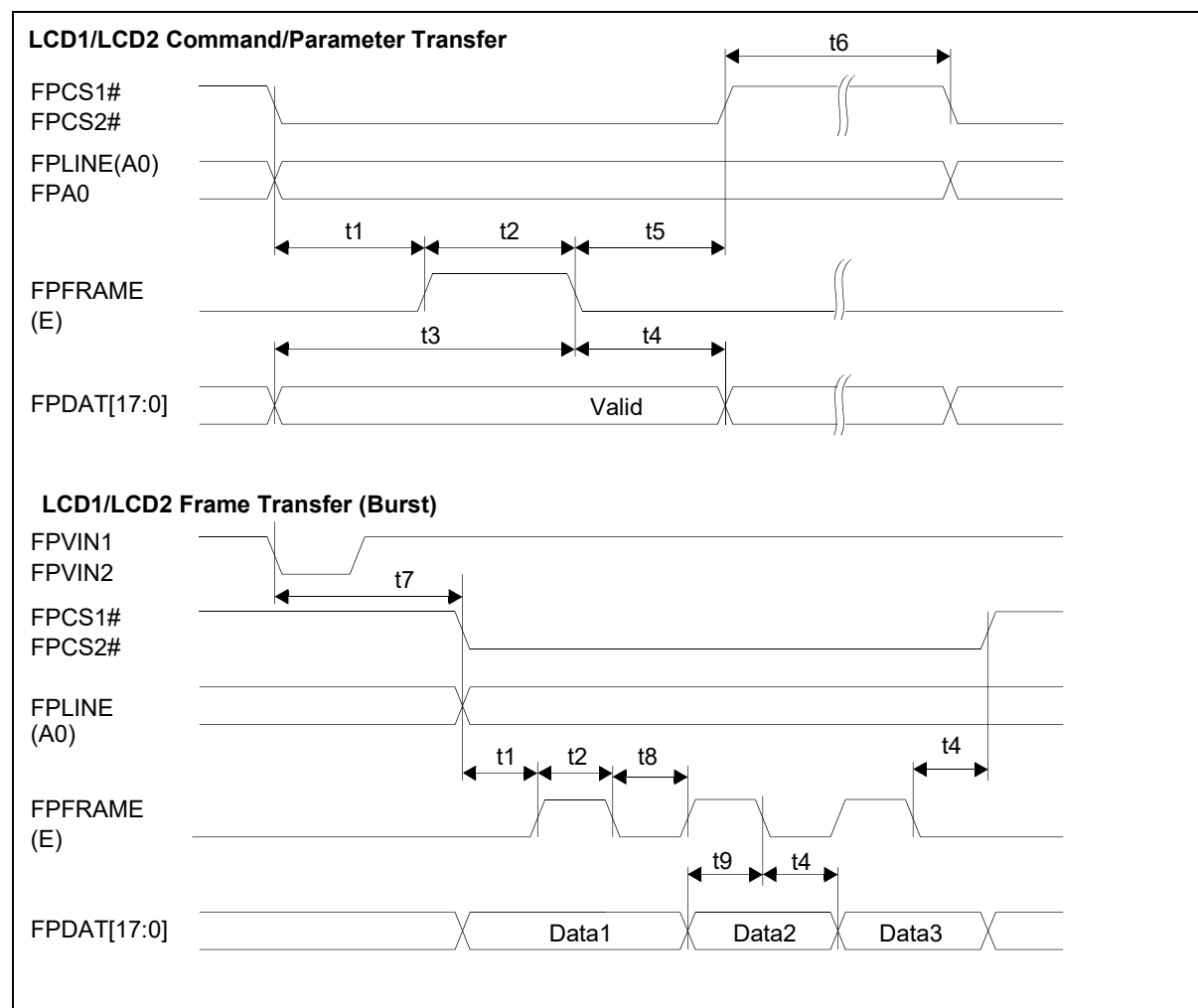


Figure 7-46: LCD1, LCD2 Parallel Interface Timing (68)

Table 7-63: LCD1, LCD2 Parallel Interface Timing (68)

| Symbol | Parameter                                                    | Min | Typ | Max | Units       |
|--------|--------------------------------------------------------------|-----|-----|-----|-------------|
| t1     | Chip select falling edge to FPFRAME (E) rising edge          |     | 1   |     | Ts (Note 1) |
| t2     | FPFRAME (E) high period                                      |     | 1   |     | Ts          |
| t3     | Data setup time for command/parameter transfers              |     | 1   |     | Ts          |
| t4     | Data hold time                                               |     | 1   |     |             |
| t5     | FPFRAME (E) falling edge to Chip select rising edge          |     | 1   |     | Ts          |
| t6     | Chip select deassert to reassert                             |     | 0   |     | Ts          |
| t7     | Vertical sync input falling edge to chip select falling edge |     |     | 51  | Ts          |
| t8     | Enable signal low period in burst cycle                      |     | 1   |     | Ts          |
| t9     | Data setup time for frame transfers                          |     | 1   |     | Ts          |

1. Ts = Pixel clock period

## 7.5 Camera Interface Timing

### 7.5.1 S1D13715B00B Camera Interface Timing

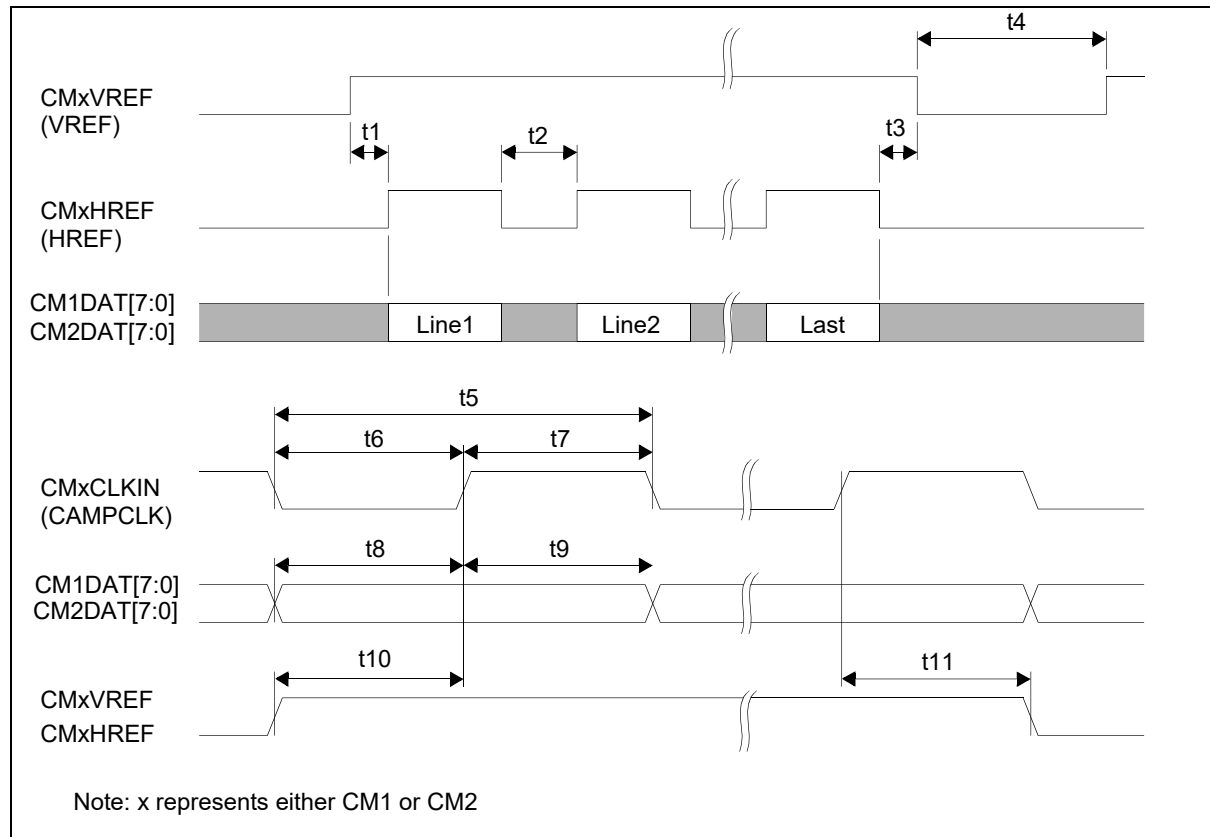


Figure 7-47: S1D13715B00B Camera Interface Timing

Table 7-64: S1D13715B00B Camera Interface Timing

| Symbol | Parameter                                    | Min | Max | Units       |
|--------|----------------------------------------------|-----|-----|-------------|
| t1     | CMxVREF rising edge to CMxHREF rising edge   | 0   |     | Tc (note 1) |
| t2     | Horizontal blank period                      | 4   |     | Tc          |
| t3     | CMxHREF falling edge to CMxVREF falling edge | 0   |     | Tc          |
| t4     | Vertical blank period                        | 1   |     | Line        |
| t5     | Camera input clock period                    | 3   |     | Ts (note 2) |
| t6     | Camera input clock pulse width low           | 1.5 |     | Ts          |
| t7     | Camera input clock pulse width high          | 1.5 |     | Ts          |
| t8     | Data setup time                              | 6   |     | ns          |
| t9     | Data hold time                               | 6   |     | ns          |
| t10    | CMxVREF, CMxHREF setup time                  | 10  |     | ns          |
| t11    | CMxVREF, CMxHREF hold time                   | 10  |     | ns          |

1. Ts = System clock period
2. Tc = Camera block input clock period

## 7.5.2 S1D13715F01A Camera Interface Timing

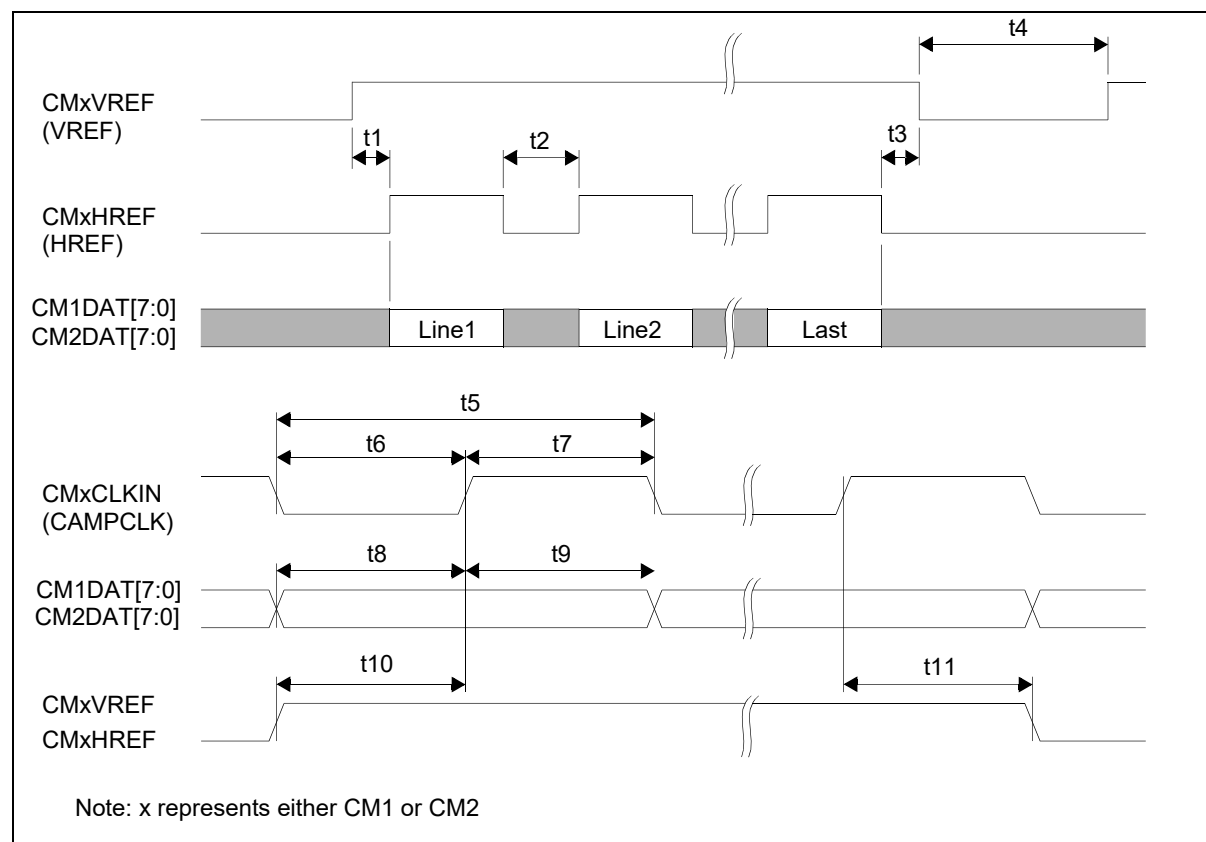


Figure 7-48: S1D13715F01A Camera Interface Timing

Table 7-65: S1D13715F01A Camera Interface Timing

| Symbol | Parameter                                    | Min | Max | Units       |
|--------|----------------------------------------------|-----|-----|-------------|
| t1     | CMxVREF rising edge to CMxHREF rising edge   | 0   |     | Tc (note 1) |
| t2     | Horizontal blank period                      | 4   |     | Tc          |
| t3     | CMxHREF falling edge to CMxVREF falling edge | 0   |     | Tc          |
| t4     | Vertical blank period                        | 1   |     | Line        |
| t5     | Camera input clock period                    | 2.2 |     | Ts (note 2) |
| t6     | Camera input clock pulse width low           | 10  |     | ns          |
| t7     | Camera input clock pulse width high          | 10  |     | ns          |
| t8     | Data setup time                              | 6   |     | ns          |
| t9     | Data hold time                               | 6   |     | ns          |
| t10    | CMxVREF, CMxHREF setup time                  | 10  |     | ns          |
| t11    | CMxVREF, CMxHREF hold time                   | 10  |     | ns          |

1. Ts = System clock period
2. Tc = Camera block input clock period

### 7.5.3 MPEG Codec Interface Timing

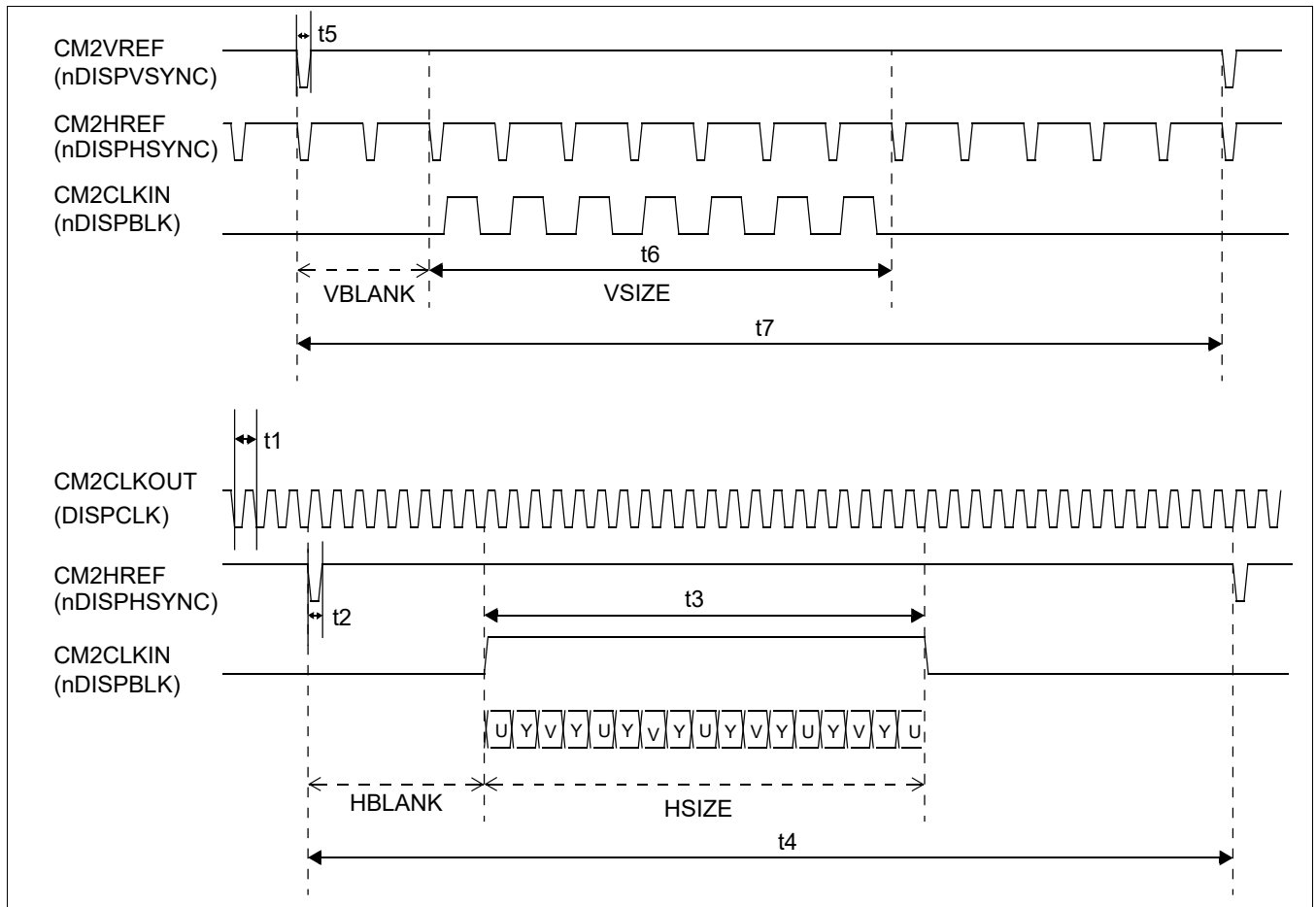


Figure 7-49: MPEG Codec Interface Timing

Table 7-66: MPEG Codec Interface Timing

| Symbol | Parameter                   | Min | Typ                     | Max  | Units       |
|--------|-----------------------------|-----|-------------------------|------|-------------|
| t1     | Camera Clock Cycle          | 4   |                         | 32   | Ts (Note 1) |
| t2     | Horizontal Sync Pulse Width |     | 1                       |      | Tc (Note 2) |
| t3     | Horizontal Display Period   | 1   |                         | 1024 | Pixel       |
| t4     | Horizontal Total            |     | REG[012Ah] bits 9-0 + 1 |      | Pixel       |
| t5     | Vertical Sync Pulse Width   |     | 1                       |      | Tc          |
| t6     | Vertical Display Period     | 1   |                         | 512  | Line        |
| t7     | Vertical Total              |     | REG[0128h] bits 9-0 + 1 |      | Line        |

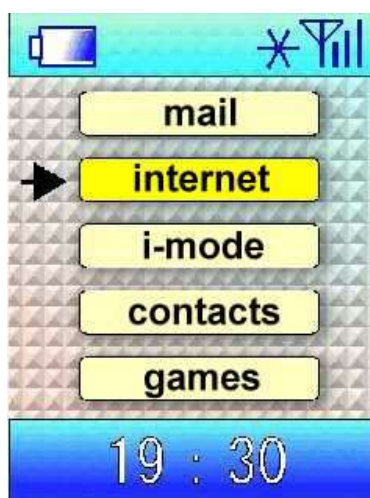
1. Ts = System clock period
2. Tc = Camera block input clock period
3. Tc should be equal or more than 4Ts
4. Tc = t1
5. 1Pixel = 2Tc

## 8 Memory Allocation

### 8.1 Main Window Case 1

#### 8.1.1 Environment

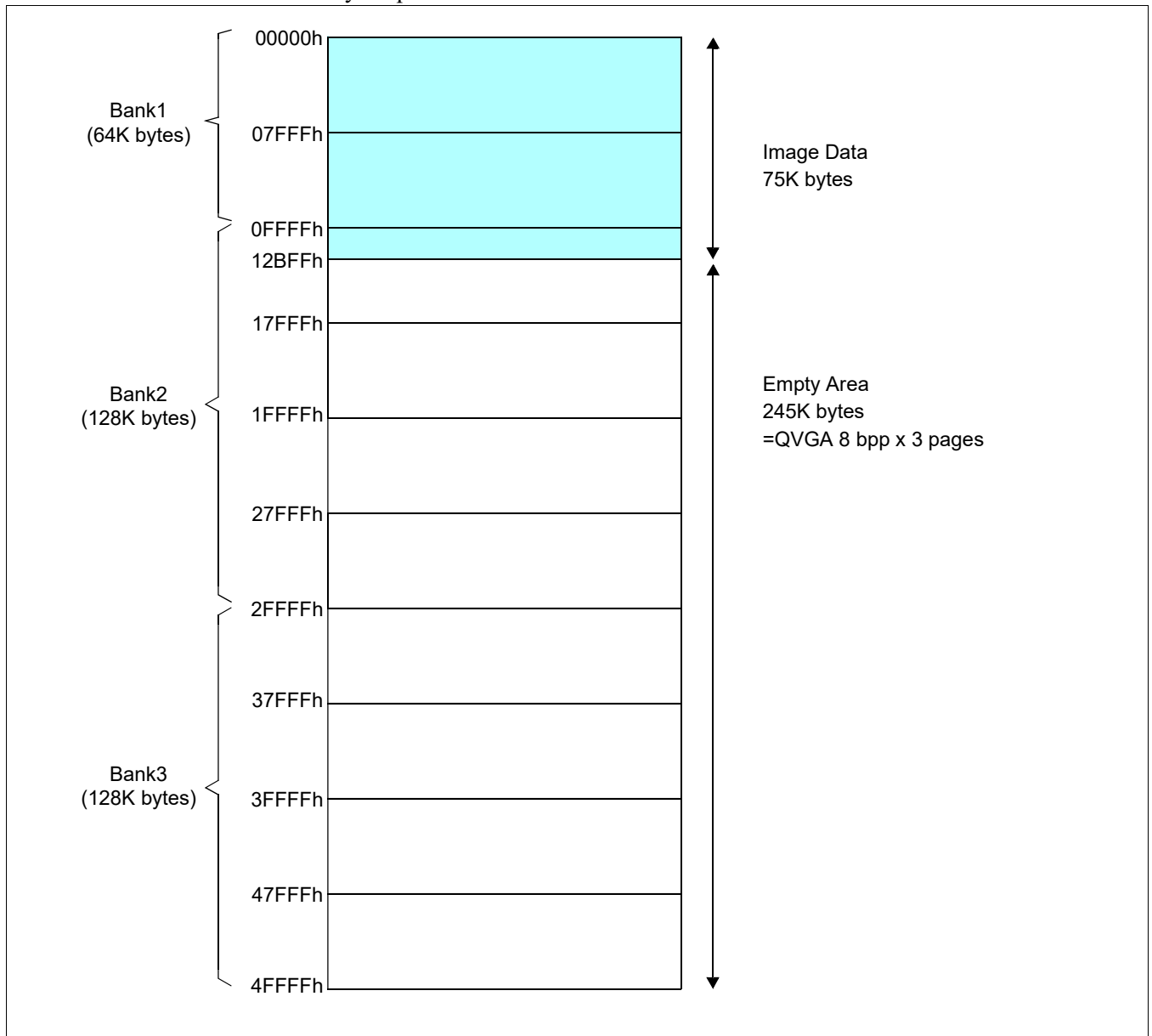
- Resolution: QVGA (240x320)
- Color Depth: 8 bpp (LUT 1))
- Data Size: 75K bytes
- Image:



Display Image

*Figure 8-1: Main Window Case 1 Image*

## • Memory Map:

*Figure 8-2: Memory Map for Main Window Case 1*

### 8.2 Main Window Case 2

#### 8.2.1 Environment

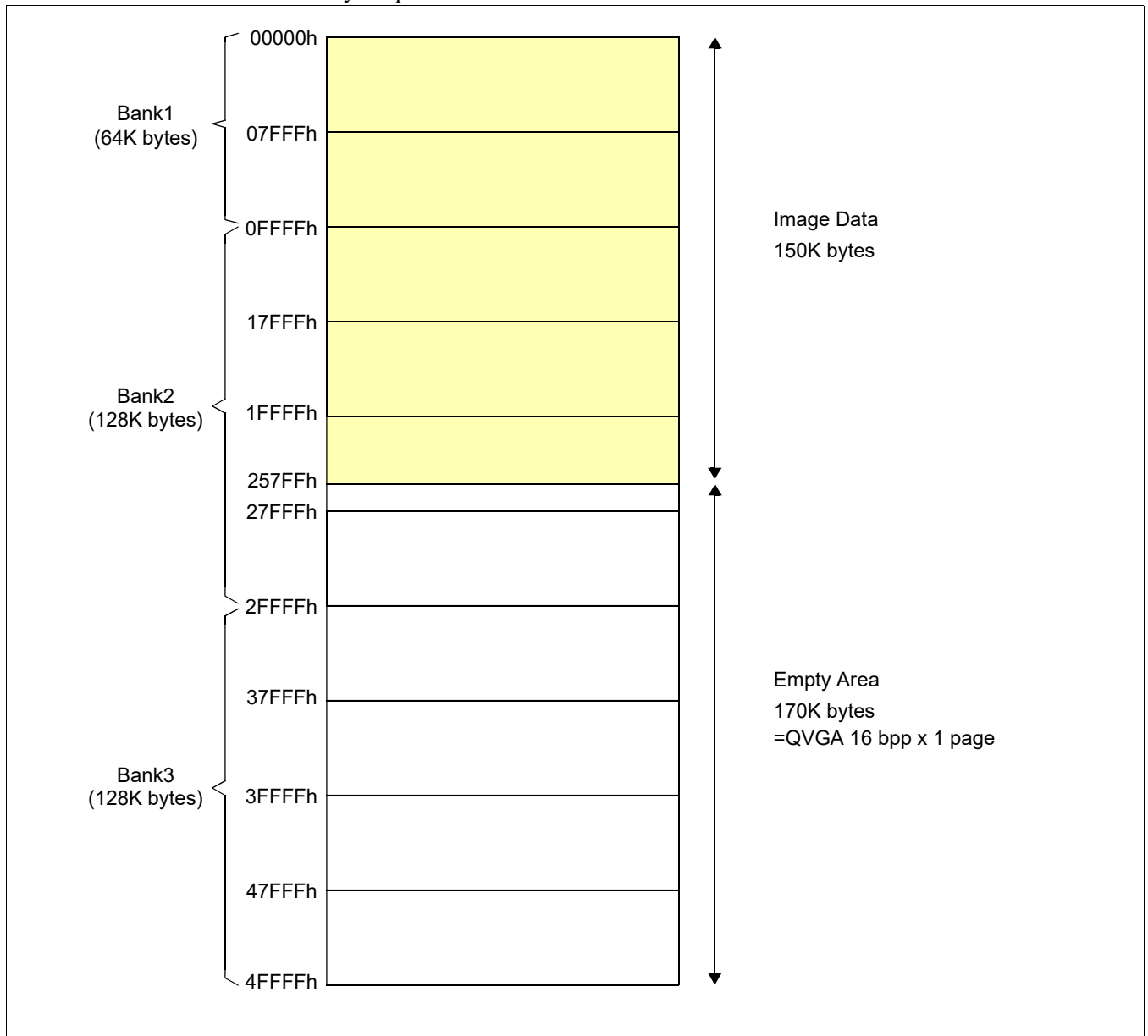
- Resolution: QVGA (240x320)
- Color Depth: 16 bpp (LUT 1)
- Data Size: 150K bytes
- Image:



Display Image

*Figure 8-3: Main Window Case 2 Image*

## • Memory Map:

*Figure 8-4: Memory Map for Main Window Case 2*

### 8.3 Main Window, PIP<sup>+</sup> Window, and Overlay Display

#### 8.3.1 Environment

- Resolution:
  - Main Window Image QVGA (240x320)
  - PIP<sup>+</sup> Window Image QVGA (240x320)
- Color Depth:
  - Main Window Image 8 bpp (LUT1)
  - PIP<sup>+</sup> Window Image 16 bpp (LUT2)
- Data Size:
  - Main Window Image 75K bytes
  - PIP<sup>+</sup> Window Image 150K bytes
- Image:

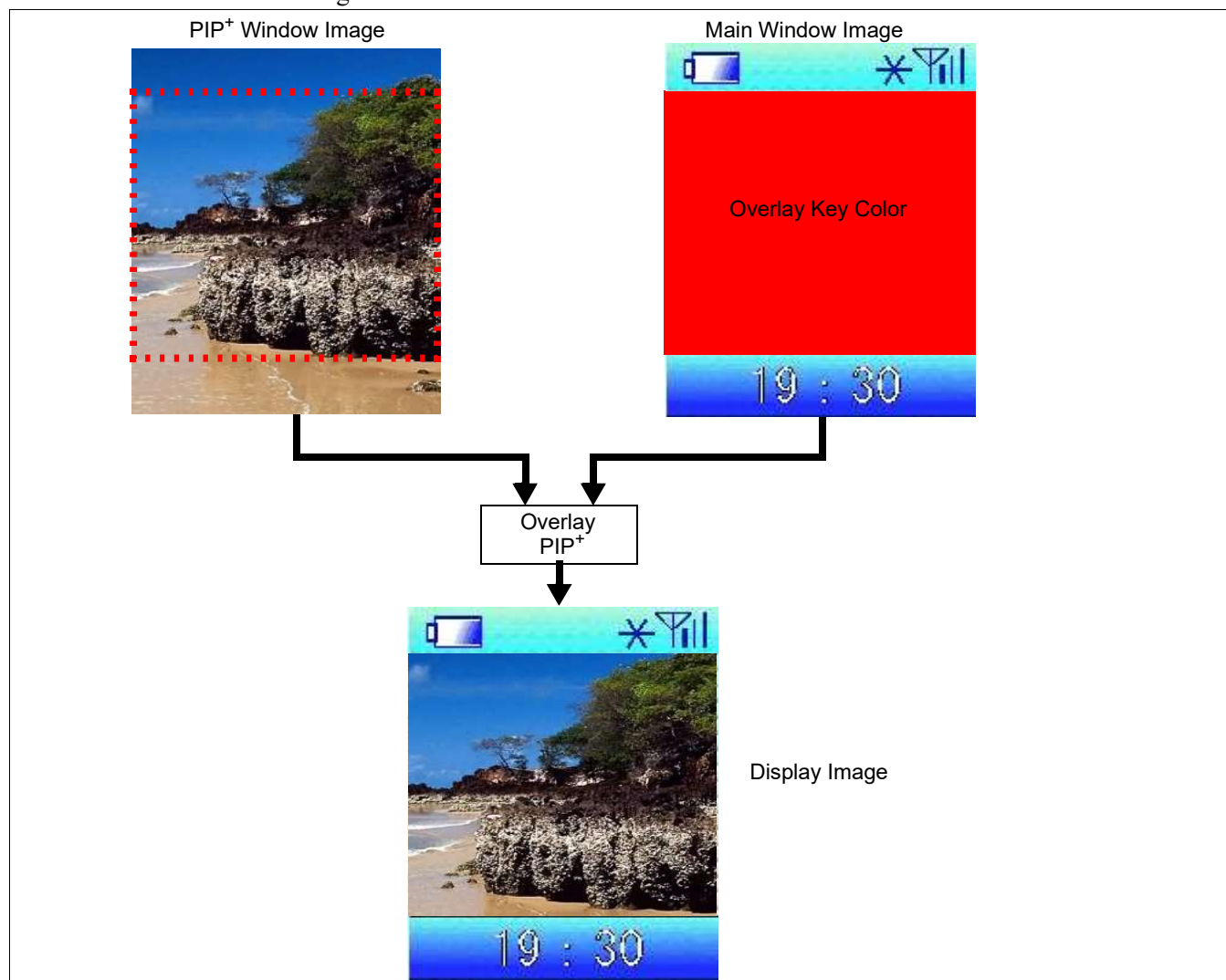
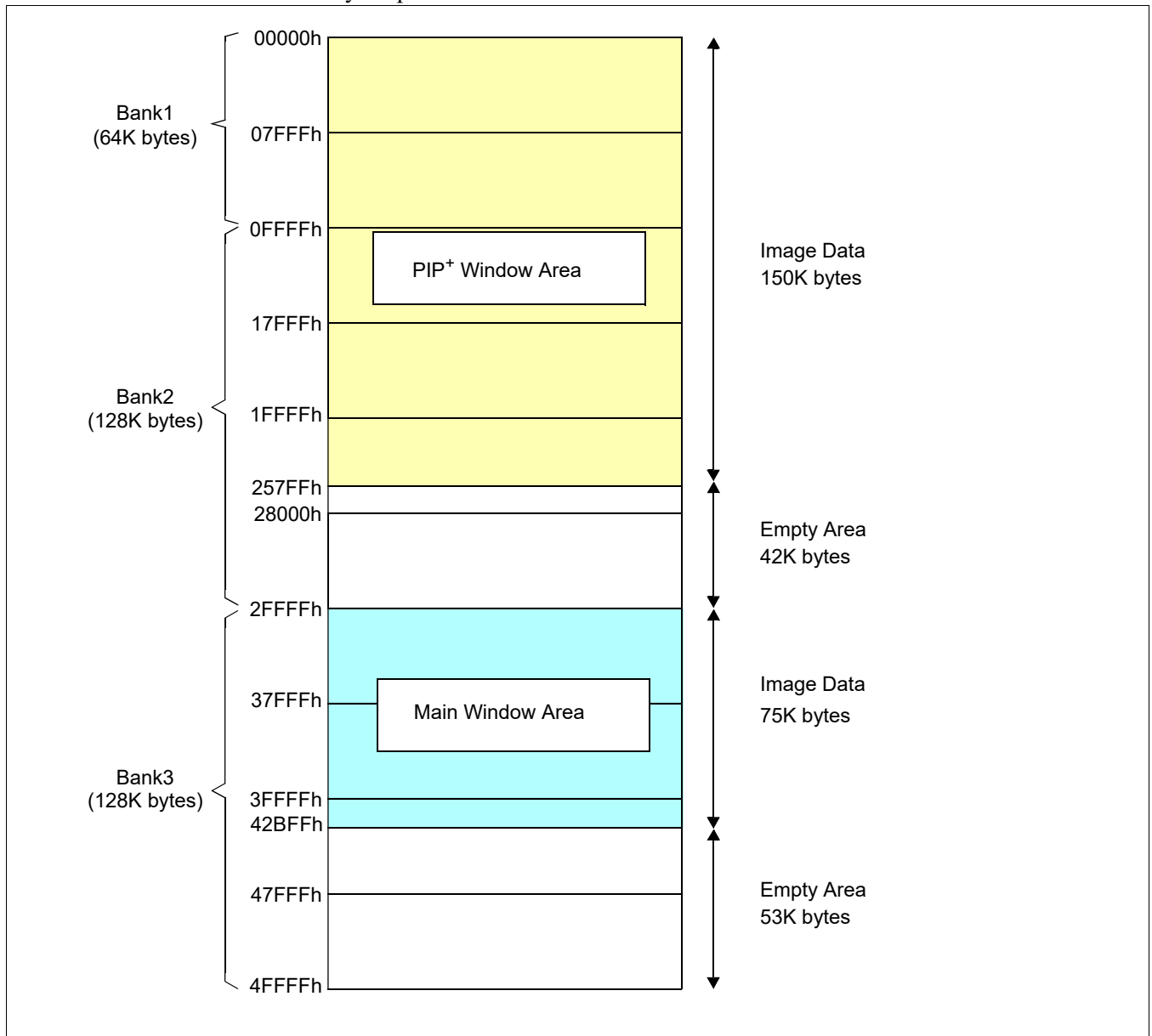


Figure 8-5: Main Window, PIP<sup>+</sup> Window, and Overlay Display

## • Memory Map:

*Figure 8-6: Memory Map for Main Window, PIP<sup>+</sup> Window, and Overlay Display*

### 8.4 Main Window, PIP<sup>+</sup> Window, Overlay, and YUV

#### 8.4.1 Environment

- Resolution:
  - Main Window Image QVGA(240x320)
  - PIP<sup>+</sup> Window Image 240x240, from Camera interface and resized
- Color Depth:
  - Main Window Image 8 bpp (LUT1)
  - PIP<sup>+</sup> Window Image 16 bpp (LUT2)
- Data Size:
  - Main Window Image 75K bytes
  - PIP<sup>+</sup> Window Image 112.5K bytes
- Image:

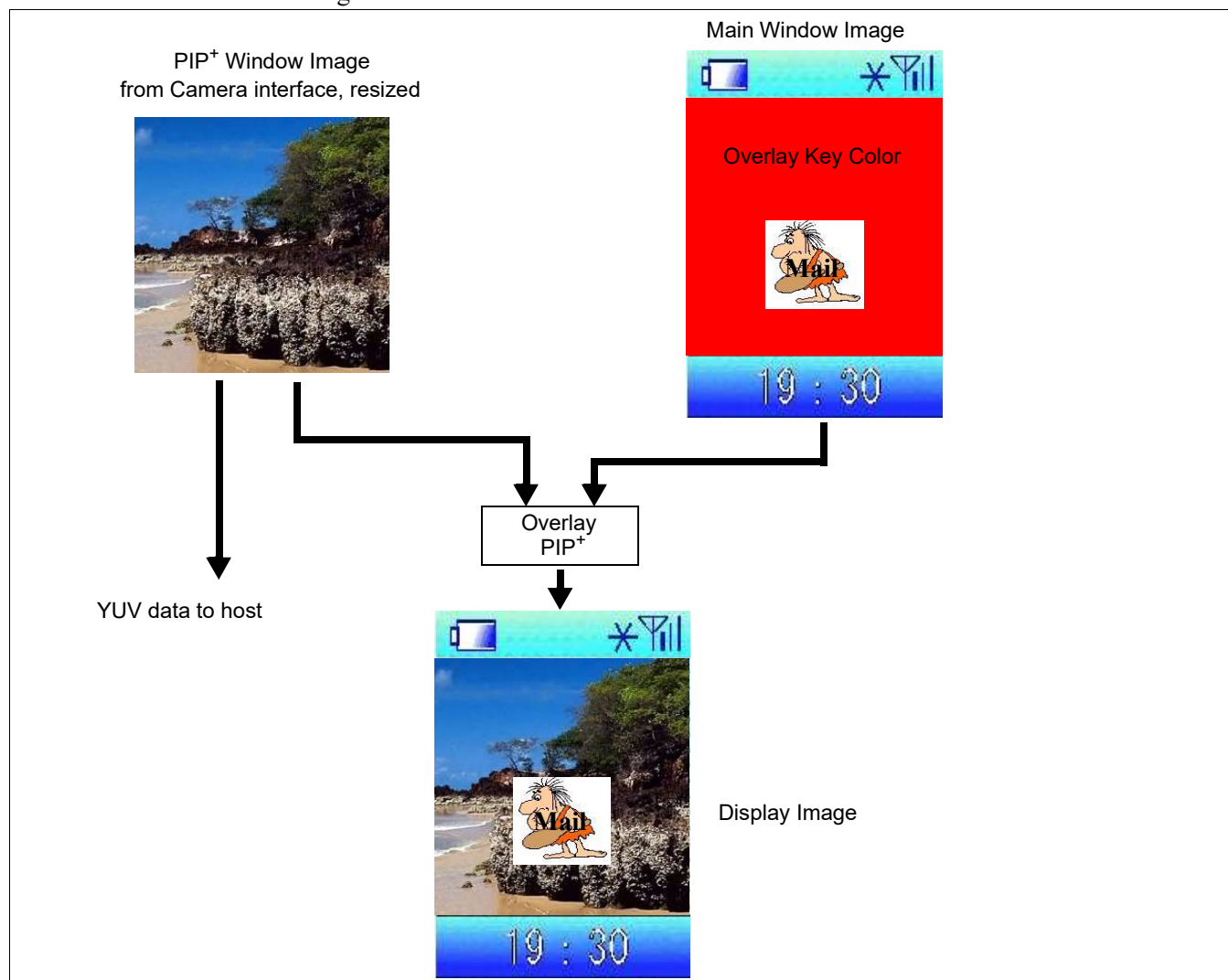


Figure 8-7: Main Window, PIP<sup>+</sup> Window, Overlay, and YUV

- Memory Map:

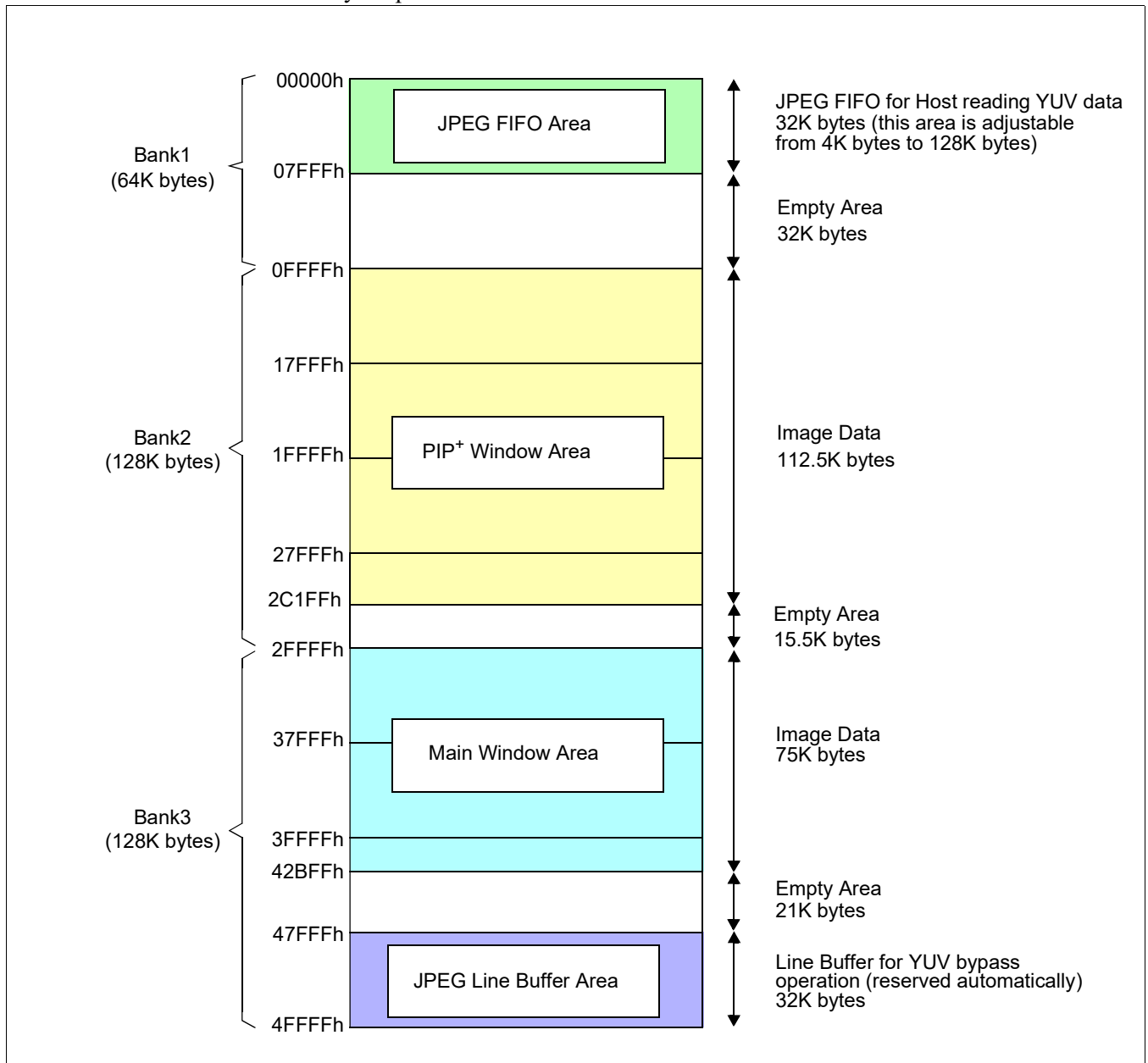


Figure 8-8: Memory Map for Main Window, PIP<sup>+</sup> Window, Overlay, and YUV

## 8.5 Main Window, PIP<sup>+</sup> Window, Overlay, and JPEG

### 8.5.1 Environment

- Resolution:
 

|                               |               |
|-------------------------------|---------------|
| Main Window Image             | QVGA(240x320) |
| PIP <sup>+</sup> Window Image | QVGA(240x240) |
- Color Depth:
 

|                               |               |
|-------------------------------|---------------|
| Main Window Image             | 8 bpp (LUT1)  |
| PIP <sup>+</sup> Window Image | 16 bpp (LUT2) |
- Data Size:
 

|                               |              |
|-------------------------------|--------------|
| Main Window Image             | 75K bytes    |
| PIP <sup>+</sup> Window Image | 112.5K bytes |
- Image:

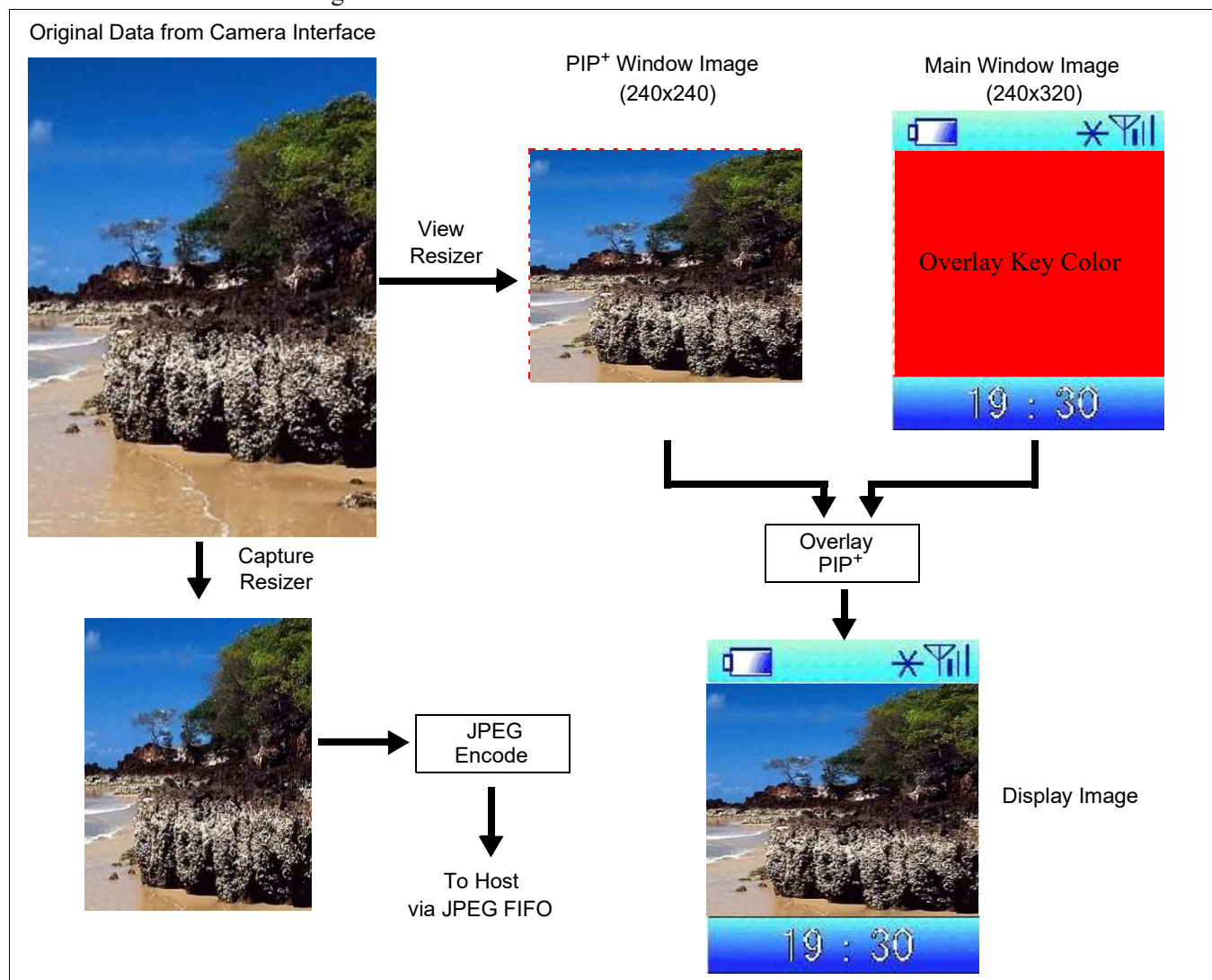


Figure 8-9: Main Window, PIP<sup>+</sup> Window, Overlay, and JPEG

• Memory Map:

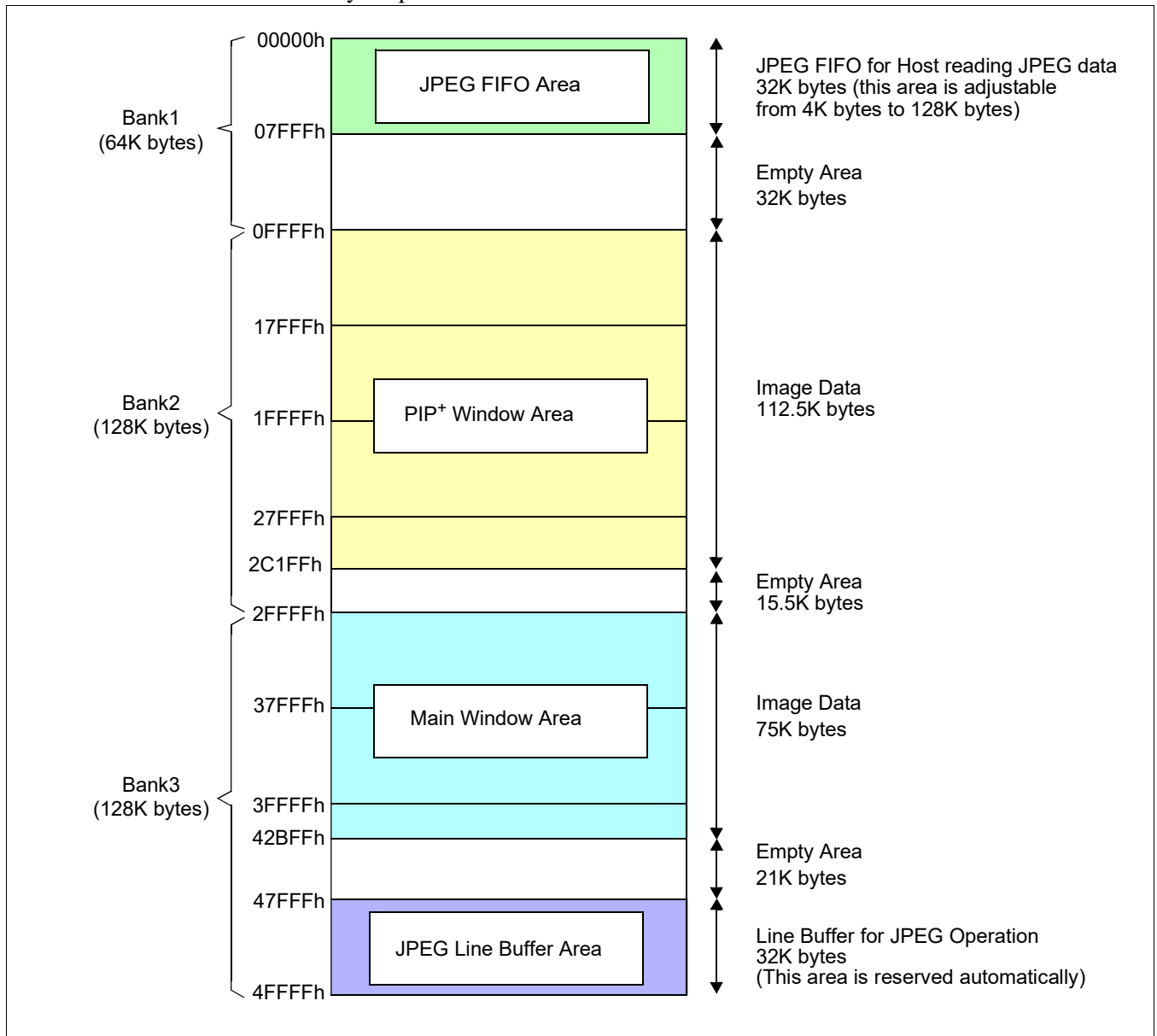


Figure 8-10: Memory Map for Main Window, PIP<sup>+</sup> Window, Overlay and JPEG

## 8.6 Main Window, PIP<sup>+</sup> Window, Overlay, RGB/YUV Converter and JPEG

### 8.6.1 Environment

- Resolution:
 

|                               |               |
|-------------------------------|---------------|
| Main Window Image             | QVGA(240x320) |
| PIP <sup>+</sup> Window Image | QVGA(240x240) |
- Color Depth:
 

|                               |               |
|-------------------------------|---------------|
| Main Window Image             | 8 bpp (LUT1)  |
| PIP <sup>+</sup> Window Image | 16 bpp (LUT2) |
- Data Size:
 

|                               |              |
|-------------------------------|--------------|
| Main Window Image             | 75K bytes    |
| PIP <sup>+</sup> Window Image | 112.5K bytes |
- Image:

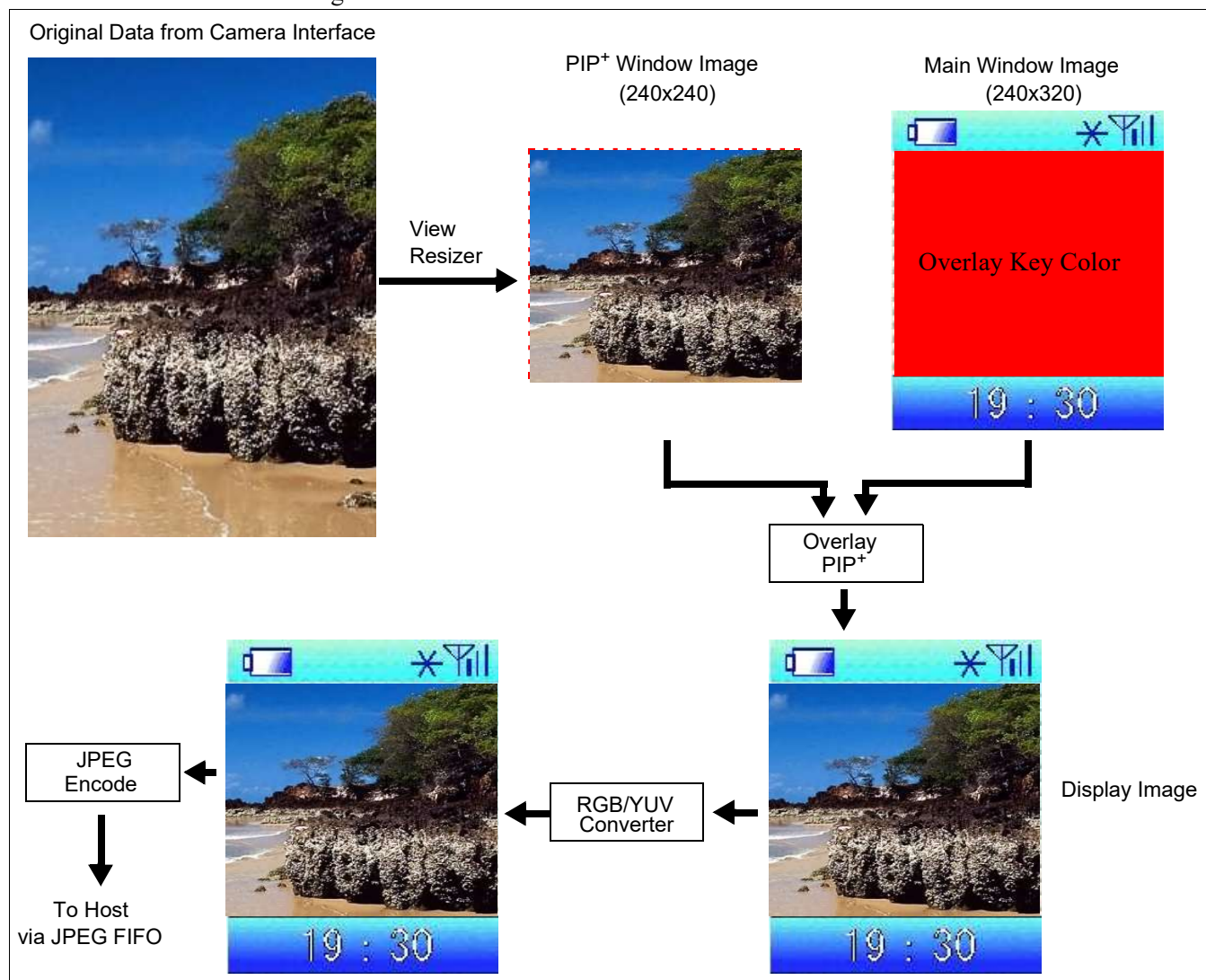


Figure 8-11: Main Window, PIP<sup>+</sup> Window, Overlay, RGB/YUV Converter and JPEG

## • Memory Map:

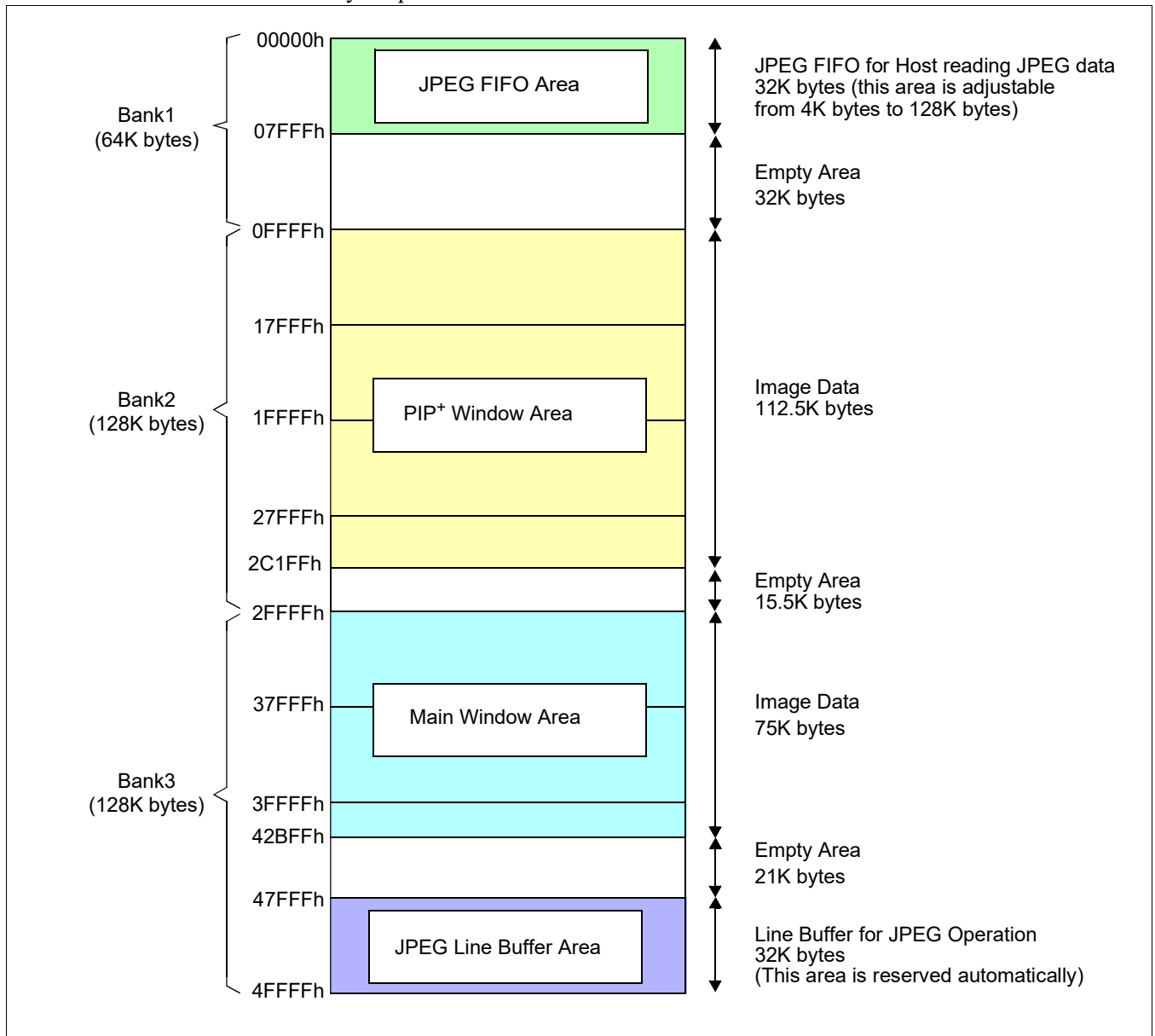


Figure 8-12: Memory Map for Main Window, PIP<sup>+</sup> Window, Overlay, RGB/YUV Converter and JPEG

# 9 Clocks

## 9.1 Clock Diagram

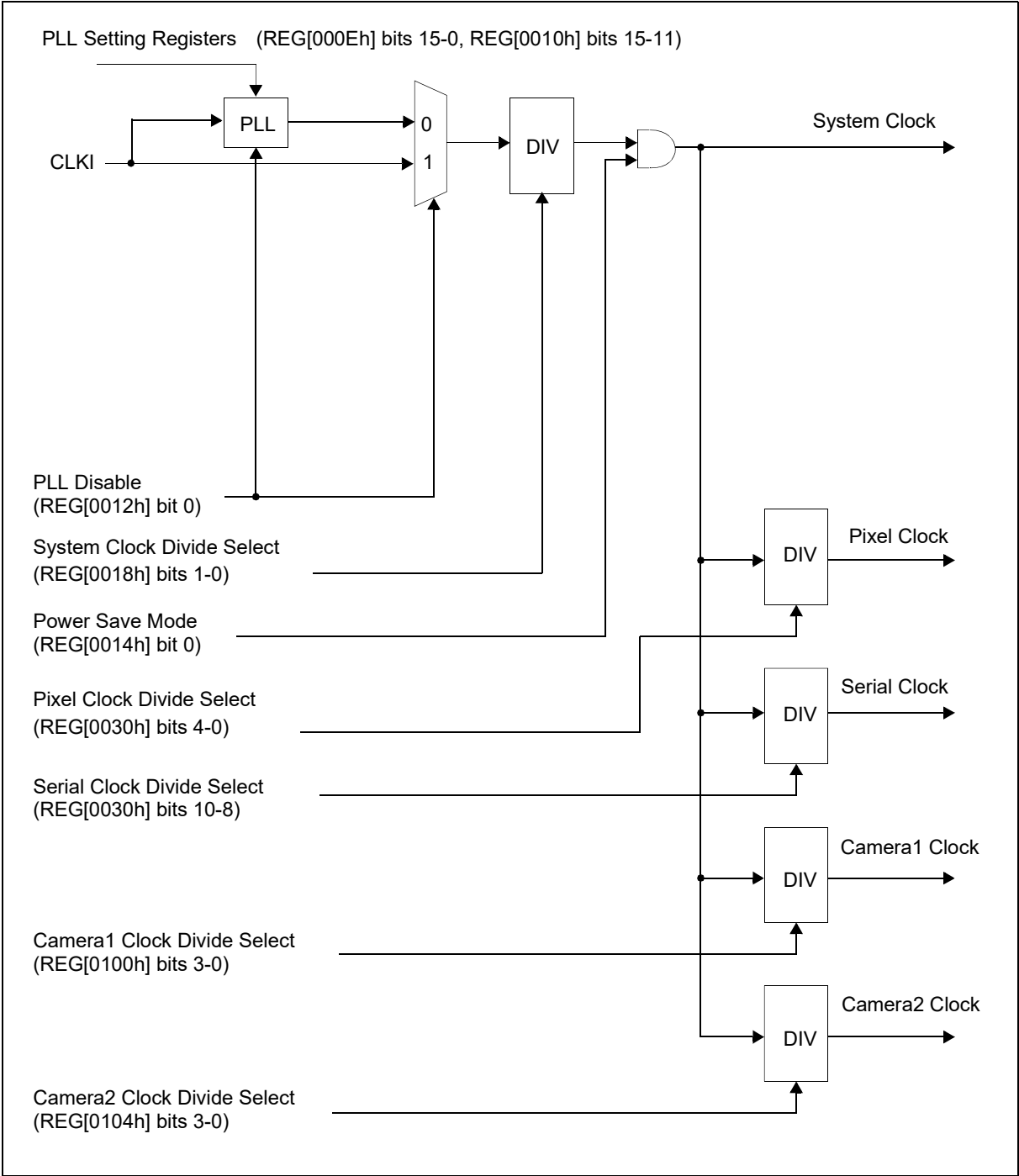


Figure 9-1: Clock Diagram

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## 9.2 Clocks

### 9.2.1 System Clock

System clock (SYSCLK) is used for the S1D13715 internal main clock. The system clock source can be selected (REG[0012h] bits 2 and 0) from either the internal PLL or an external clock input (CLKI). The System Clock Divide Select bits (REG[0018h] bits 1-0) control this clock division. The system clock can be a divided down version of the output of the PLL or the input of CLKI.

### 9.2.2 Pixel Clock

Pixel clock (PCLK) is used for the LCD1 shift clock of a RGB type panel and for the LCD1/LCD2 parallel interface timing. The pixel clock source is always the system clock and can be divided using the Pixel Clock Divide Select bits (REG[0030h] bits 4-0).

### 9.2.3 Serial Clock

Serial clock (SCLK) is used for the LCD1 and LCD2 serial interfaces. The serial clock source is always the system clock and can be divided using the Serial Clock Divide Select bits (REG[0030h] bits 10-8).

### 9.2.4 Camera1 Clock

Camera1 clock (CAM1CLK) is used for the Camera1 interface. The camera1 clock source is always the system clock and can be divided using the Camera1 Clock Divide Select bits (REG[0100h] bits 3-0).

**Note**

This clock can be output on CM1CLKOUT to be used as the master clock of an external camera module attached to the Camera1 interface.

### 9.2.5 Camera2 Clock

Camera2 clock (CAM2CLK) is used for the Camera2 interface. The camera2 clock source is always the system clock and can be divided using the Camera2 Clock Divide Select bits (REG[0104h] bits 3-0). CAM2CLK is also used for the MPEG Codec interface.

**Note**

This clock can be output on CM2CLKOUT to be used as the master clock of an external camera module attached to the Camera2 interface.

## 10 Registers

### 10.1 Register Mapping

The S1D13715 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0 (for 1 CS# mode), or CS# = 1 and M/R# = 0 (for 2 CS# mode), the registers may be accessed. The register space is decoded by AB[18:1] and BE#[1:0], and is mapped as follows.

*Table 10-1: S1D13715 Register Mapping*

| M/R# | Address          | Function                              |
|------|------------------|---------------------------------------|
| 1    | 00000h to 4FFFFh | SRAM memory                           |
| 0    | 0000h to 0003h   | System Configuration Registers        |
| 0    | 000Eh to 0019h   | Clock Setting Registers               |
| 0    | 0020h to 002Bh   | Indirect Interface Registers          |
| 0    | 0030h to 003Dh   | LCD Panel Interface Setting Registers |
| 0    | 0040h to 0057h   | LCD1 Setting Registers                |
| 0    | 0058h to 005Fh   | LCD2 Setting Registers                |
| 0    | 0080h to 00F7h   | Extended Panel Registers              |
| 0    | 0100h to 012Bh   | Camera Interface Registers            |
| 0    | 0200h to 0281h   | Display Mode Setting Registers        |
| 0    | 0300h to 030Fh   | GPIO Registers                        |
| 0    | 0310h to 0329h   | Overlay Registers                     |
| 0    | 0400h to 08FFh   | Look-Up Table Registers               |
| 0    | 0930h to 096Fh   | Resizer Operation Registers           |
| 0    | 0980h to 098Fh   | JPEG Module Registers                 |
| 0    | 09A0h to 09BEh   | JPEG FIFO Setting Registers           |
| 0    | 09C0h to 09E1h   | JPEG Line Buffer Setting Registers    |
| 0    | 0A00h to 0A11h   | Interrupt Control Registers           |
| 0    | 1000h to 17A3h   | JPEG Codec Registers                  |
| 0    | 8000h to 8033h   | 2D BitBLT Registers                   |
| 0    | 10000h           | 2D Accelerator Data Port              |

## 10.2 Register Set

The S1D13715 registers are listed in the following table.

Table 10-2: S1D13715 Register Set

| Register                                                          | Pg  | Register                                                              | Pg  |
|-------------------------------------------------------------------|-----|-----------------------------------------------------------------------|-----|
| <b>Read Only Registers</b>                                        |     |                                                                       |     |
| REG[0000h] Product Information Register                           | 137 | REG[0002h] Configuration Pins Status Register                         | 138 |
| REG[0006h] Bus Timeout Setting Register                           | 138 |                                                                       |     |
| <b>Clock Setting Registers</b>                                    |     |                                                                       |     |
| REG[000Eh] PLL Setting Register 0                                 | 139 | REG[0010h] PLL Setting Register 1                                     | 141 |
| REG[0012h] PLL Setting Register 2                                 | 142 | REG[0014h] Miscellaneous Configuration Register                       | 143 |
| REG[0016h] Software Reset Register                                | 146 | REG[0018h] System Clock Setting Register                              | 146 |
| <b>Indirect Interface Registers</b>                               |     |                                                                       |     |
| REG[0020h] is Reserved                                            | 147 | REG[0022h] Indirect Interface Memory Address Register 1               | 147 |
| REG[0024h] Indirect Interface Memory Address Register 2           | 147 | REG[0026h] Indirect Interface Auto Increment Register                 | 148 |
| REG[0028h] Indirect Interface Memory Access Port Register         | 148 | REG[002Ah] Indirect Interface 2D BitBLT Data Read/Write Port Register | 148 |
| <b>LCD Panel Interface Setting Registers</b>                      |     |                                                                       |     |
| REG[0030h] LCD Interface Clock Setting Register                   | 149 | REG[0032h] LCD Module Clock Setting Register                          | 151 |
| REG[0034h] LCD Interface Command Register                         | 153 | REG[0036h] LCD Interface Parameter Register                           | 154 |
| REG[0038h] LCD Interface Status Register                          | 154 | REG[003Ah] LCD Interface Frame Transfer Register                      | 155 |
| REG[003Ch] LCD Interface Transfer Setting Register                | 155 |                                                                       |     |
| <b>LCD1 Setting Registers</b>                                     |     |                                                                       |     |
| REG[0040h] LCD1 Horizontal Total Register                         | 157 | REG[0042h] LCD1 Horizontal Display Period Register                    | 158 |
| REG[0044h] LCD1 Horizontal Display Period Start Position Register | 158 | REG[0046h] LCD1 FPLINE Register                                       | 159 |
| REG[0048h] LCD1 FPLINE Pulse Position Register                    | 159 | REG[004Ah] LCD1 Vertical Total Register                               | 160 |
| REG[004Ch] LCD1 Vertical Display Period Register                  | 160 | REG[004Eh] LCD1 Vertical Display Period Start Position Register       | 160 |
| REG[0050h] LCD1 FPFRAME Register                                  | 161 | REG[0052h] LCD1 FPFRAME Pulse Position Register                       | 161 |
| REG[0054h] LCD1 Serial Interface Setting Register                 | 162 | REG[0056h] LCD1 Parallel Interface Setting Register                   | 163 |
| <b>LCD2 Setting Registers</b>                                     |     |                                                                       |     |
| REG[0058h] LCD2 Horizontal Display Period Register                | 165 | REG[005Ah] LCD2 Vertical Display Period Register                      | 165 |
| REG[005Ch] LCD2 Serial Interface Setting Register                 | 166 | REG[005Eh] LCD2 Parallel Interface Setting Register                   | 167 |

Table 10-2: S1D13715 Register Set

| Register                                                               | Pg  | Register                                                             | Pg  |
|------------------------------------------------------------------------|-----|----------------------------------------------------------------------|-----|
| <b>Extended Panel Registers</b>                                        |     |                                                                      |     |
| REG[0070h] is Reserved                                                 | 169 | REG[0080h] Samsung a-TFT Horizontal Total Register                   | 169 |
| REG[0082h] Samsung a-TFT LD Rising Edge Register                       | 169 | REG[0084h] Samsung a-TFT CKV Toggle Point Register                   | 170 |
| REG[0086h] Samsung a-TFT VCOM Toggle Point Register                    | 170 | REG[0088h] Samsung a-TFT Pulse Width Register                        | 170 |
| REG[008Ah] through REG[008Eh] are Reserved                             | 171 | REG[0090h] HR-TFT Configuration Register                             | 171 |
| REG[0092h] HR-TFT CLS Width Register                                   | 171 | REG[0094h] HR-TFT PS1 Rising Edge Register                           | 172 |
| REG[0096h] HR-TFT PS2 Rising Edge Register                             | 172 | REG[0098h] HR-TFT PS2 Toggle Width Register                          | 172 |
| REG[009Ah] HR-TFT PS3 Signal Width Register                            | 173 | REG[009Eh] HR-TFT REV Toggle Point Register                          | 173 |
| REG[00A0h] HR-TFT PS1/2 End Register                                   | 173 | REG[00A2h] Type 2 TFT Configuration Register 0                       | 174 |
| REG[00A4h] Casio TFT Timing Register 0                                 | 175 | REG[00A6h] Casio TFT Timing Register 1                               | 176 |
| REG[00A8h] Type 2 TFT Configuration Register 1                         | 176 | REG[00AAh] through REG[00ECh] are Reserved                           | 176 |
| REG[00EEh] Partial Drive Area0 Start Line Register                     | 177 | REG[00F0h] Partial Drive Area0 End Line Register                     | 178 |
| REG[00F2h] Partial Drive Area1 Start Line Register                     | 178 | REG[00F4h] Partial Drive Area1 End Line Register                     | 179 |
| REG[00F6h] through REG[00FCh] are Reserved                             | 179 | REG[00FEh] LCD Interface ID Register                                 | 180 |
| <b>Camera Interface Setting Registers</b>                              |     |                                                                      |     |
| REG[0100h] Camera1 Clock Setting Register                              | 181 | REG[0102h] Camera1 Signal Setting Register                           | 182 |
| REG[0104h] Camera2 Clock Divide Select Register                        | 183 | REG[0106h] Camera2 Input Signal Format Select Register               | 184 |
| REG[0108h] through REG[010Eh] are Reserved                             | 185 | REG[0110h] Camera Mode Setting Register                              | 185 |
| REG[0112h] Camera Frame Setting Register                               | 188 | REG[0114h] Camera Control Register                                   | 189 |
| REG[0116h] Camera Status Register                                      | 190 | REG[0120h] Strobe Line Delay Register                                | 192 |
| REG[0122h] Strobe Pulse Width Register                                 | 192 | REG[0124h] Strobe Control Register                                   | 193 |
| REG[0128h] MPEG Interface VSYNC Width register                         | 194 | REG[012Ah] MPEG Interface HSYNC Width register                       | 194 |
| REG[012Ch] through REG[012Fh] are Reserved                             | 195 |                                                                      |     |
| <b>Display Mode Setting Registers</b>                                  |     |                                                                      |     |
| REG[0200h] Display Mode Setting Register 0                             | 195 | REG[0202h] Display Mode Setting Register 1                           | 198 |
| REG[0204h] Transparent Overlay Key Color Red Data Register             | 201 | REG[0206h] Transparent Overlay Key Color Green Data Register         | 201 |
| REG[0208h] Transparent Overlay Key Color Blue Data Register            | 202 | REG[0210h] Main Window Display Start Address Register 0              | 202 |
| REG[0212h] Main Window Display Start Address Register 1                | 202 | REG[0214h] Main Window Start Address Status Register                 | 203 |
| REG[0216h] Main Window Line Address Offset Register                    | 204 | REG[0218h] PIP+ Display Start Address Register 0                     | 206 |
| REG[021Ah] PIP+ Display Start Address Register 1                       | 206 | REG[021Ch] PIP+ Window Start Address Status Register                 | 206 |
| REG[021Eh] PIP+ Window Line Address Offset Register                    | 207 | REG[0220h] PIP+ X Start Positions Register                           | 209 |
| REG[0222h] PIP+ Y Start Positions Register                             | 209 | REG[0224h] PIP+ X End Positions Register                             | 210 |
| REG[0226h] PIP+ Y End Positions Register                               | 210 | REG[0228h] is Reserved                                               | 210 |
| REG[022Ah] Back Buffer Display Start Address Register 0                | 211 | REG[022Ch] Back Buffer Display Start Address Register 1              | 211 |
| REG[0240h] YUV/RGB Translate Mode Register                             | 211 | REG[0242h] YUV/RGB Converter Write Start Address 0 Register 0        | 215 |
| REG[0244h] YUV/RGB Converter Write Start Address 0 Register 1          | 215 | REG[0246h] YUV/RGB Converter Write Start Address 1 Register 0        | 216 |
| REG[0248h] YUV/RGB Converter Write Start Address 1 Register 1          | 216 | REG[024Ah] UV Data Fix Register                                      | 216 |
| REG[024Ch] YRC Rectangle Pixel Width Register                          | 216 | REG[024Eh] YRC Rectangular Line Address Offset Register              | 217 |
| REG[0260h] RGB/YUV Converter Configuration Register                    | 217 | REG[0262h] is Reserved                                               | 218 |
| REG[0264h] Memory Image JPEG Encode Horizontal Display Period Register | 219 | REG[0266h] Memory Image JPEG Encode Vertical Display Period Register | 219 |
| REG[0268h] is Reserved                                                 | 219 | REG[0270h] Host Image JPEG Encode Control Register                   | 220 |
| REG[0272h] Host Image JPEG Encode Horizontal Pixel Count Register      | 221 | REG[0274h] Host Image JPEG Encode Vertical Line Count Register       | 221 |

Table 10-2: S1D13715 Register Set

| Register                                                | Pg  | Register                                                 | Pg  |
|---------------------------------------------------------|-----|----------------------------------------------------------|-----|
| REG[0276h] Host Image JPEG Encode RGB Data Register 0   | 222 | REG[0278h] Host Image JPEG Encode RGB Data Register 1    | 222 |
| REG[0280h] is Reserved                                  | 222 |                                                          |     |
| <b>GPIO Registers</b>                                   |     |                                                          |     |
| REG[0300h] GPIO Status and Control Register 0           | 223 | REG[0302h] GPIO Status and Control Register 1            | 223 |
| REG[0304h] GPIO Status and Control Register 2           | 223 | REG[0306h] GPIO Status and Control Register 3            | 223 |
| REG[0308h] GPIO Pull Down Control Register 0            | 224 | REG[030Ah] GPIO Pull Down Control Register 1             | 224 |
| REG[030Ch] GPIO Status and Control Register 4           | 224 | REG[030Eh] GPIO Status and Control Register 5            | 224 |
| <b>Overlay Registers</b>                                |     |                                                          |     |
| REG[0310h] Average Overlay Key Color Red Data Register  | 225 | REG[0312h] Average Overlay Key Color Green Data Register | 226 |
| REG[0314h] Average Overlay Key Color Blue Data Register | 226 | REG[0316h] AND Overlay Key Color Red Data Register       | 227 |
| REG[0318h] AND Overlay Key Color Green Data Register    | 227 | REG[031Ah] AND Overlay Key Color Blue Data Register      | 228 |
| REG[031Ch] OR Overlay Key Color Red Data Register       | 228 | REG[031Eh] OR Overlay Key Color Green Data Register      | 229 |
| REG[0320h] OR Overlay Key Color Blue Data Register      | 229 | REG[0322h] INV Overlay Key Color Red Data Register       | 230 |
| REG[0324h] INV Overlay Key Color Green Data Register    | 230 | REG[0326h] INV Overlay Key Color Blue Data Register      | 231 |
| REG[0328h] Overlay Miscellaneous Register               | 231 |                                                          |     |
| <b>LUT Registers</b>                                    |     |                                                          |     |
| REG[0400 - 07FCh] LUT1 Data Register 0                  | 234 | REG[0402 - 07FEh] LUT1 Data Register 1                   | 234 |
| REG[0800 - 08FCh] LUT2 Data Register 0                  | 235 | REG[0802 - 08FEh] LUT2 Data Register 1                   | 235 |
| <b>Resizer Operation Registers</b>                      |     |                                                          |     |
| REG[0930h] Global Resizer Control Register              | 236 | REG[0932h] through REG[093Eh] are Reserved               | 238 |
| REG[0940h] View Resizer Control Register                | 239 | REG[0944h] View Resizer Start X Position Register        | 239 |
| REG[0946h] View Resizer Start Y Position Register       | 240 | REG[0948h] View Resizer End X Position Register          | 240 |
| REG[094Ah] View Resizer End Y Position Register         | 240 | REG[094Ch] View Resizer Operation Setting Register 0     | 240 |
| REG[094Eh] View Resizer Operation Setting Register 1    | 243 | REG[0960h] Capture Resizer Control Register              | 244 |
| REG[0964h] Capture Resizer Start X Position Register    | 245 | REG[0966h] Capture Resizer Start Y Position Register     | 245 |
| REG[0968h] Capture Resizer End X Position Register      | 245 | REG[096Ah] Capture Resizer End Y Position Register       | 246 |
| REG[096Ch] Capture Resizer Operation Setting Register 0 | 246 | REG[096Eh] Capture Resizer Operation Setting Register 1  | 248 |
| <b>JPEG Module Registers</b>                            |     |                                                          |     |
| REG[0980h] JPEG Control Register                        | 249 | REG[0982h] JPEG Status Flag Register                     | 254 |
| REG[0984h] JPEG Raw Status Flag Register                | 258 | REG[0986h] JPEG Interrupt Control Register               | 261 |
| REG[0988h] is Reserved                                  | 262 | REG[098Ah] JPEG Code Start/Stop Control Register         | 263 |
| REG[098Ch] through REG[098Eh] are Reserved              | 263 |                                                          |     |

Table 10-2: S1D13715 Register Set

| Register                                                | Pg  | Register                                                 | Pg  |
|---------------------------------------------------------|-----|----------------------------------------------------------|-----|
| <b>JPEG FIFO Setting Registers</b>                      |     |                                                          |     |
| REG[09A0h] JPEG FIFO Control Register                   | 264 | REG[09A2h] JPEG FIFO Status Register                     | 265 |
| REG[09A4h] JPEG FIFO Size Register                      | 266 | REG[09A6h] JPEG FIFO Read/Write Port Register            | 267 |
| REG[09A8h] JPEG FIFO Valid Data Size Register           | 267 | REG[09AAh] JPEG FIFO Read Pointer Register               | 267 |
| REG[09ACh] JPEG FIFO Write Pointer Register             | 268 | REG[09B0h] Encode Size Limit Register 0                  | 268 |
| REG[09B2h] Encode Size Limit Register 1                 | 268 | REG[09B4h] Encode Size Result Register 0                 | 269 |
| REG[09B6h] Encode Size Result Register 1                | 269 | REG[09B8h] JPEG File Size Register 0                     | 269 |
| REG[09BAh] JPEG File Size Register 1                    | 269 | REG[09BCh] is Reserved                                   | 269 |
| REG[09C0h] JPEG Line Buffer Status Flag Register        | 270 | REG[09C2h] JPEG Line Buffer Raw Status Flag Register     | 271 |
| REG[09C4h] JPEG Line Buffer Raw Current Status Register | 272 | REG[09C6h] JPEG Line Buffer Interrupt Control Register   | 272 |
| REG[09C8h] through REG[09CEh] are Reserved              | 273 | REG[09D0h] JPEG Line Buffer Configuration Register       | 273 |
| REG[09D2h] JPEG Line Buffer Address Offset Register     | 274 | REG[09D4h] through REG[09DEh] are Reserved               | 274 |
| REG[09E0h] JPEG Line Buffer Read/Write Port Register    | 275 |                                                          |     |
| <b>Interrupt Control Registers</b>                      |     |                                                          |     |
| REG[0A00h] Interrupt Status Register                    | 276 | REG[0A02h] Interrupt Control Register 0                  | 276 |
| REG[0A04h] Interrupt Control Register 1                 | 277 | REG[0A06h] Debug Status Register                         | 278 |
| REG[0A08h] Interrupt Control for Debug Register         | 278 | REG[0A0Ah] Host Cycle Interrupt Status Register          | 279 |
| REG[0A0Ch] Host Cycle Interrupt Control Register        | 281 | REG[0A0Eh] Cycle Time Out Control Register               | 282 |
| REG[0A10h] is Reserved                                  | 282 | REG[0A40h] Interrupt Request Status Register             | 283 |
| <b>JPEG Encode Performance Register</b>                 |     |                                                          |     |
| REG[0F00h] JPEG Encode Performance Register             | 283 |                                                          |     |
| <b>JPEG Codec Registers</b>                             |     |                                                          |     |
| REG[1000h] Operation Mode Setting Register              | 284 | REG[1002h] Command Setting Register                      | 285 |
| REG[1004h] JPEG Operation Status Register               | 286 | REG[1006h] Quantization Table Number Register            | 286 |
| REG[1008h] Huffman Table Number Register                | 286 | REG[100Ah] DRI Setting Register 0                        | 288 |
| REG[100Ch] DRI Setting Register 1                       | 288 | REG[100Eh] Vertical Pixel Size Register 0                | 289 |
| REG[1010h] Vertical Pixel Size Register 1               | 289 | REG[1012h] Horizontal Pixel Size Register 0              | 290 |
| REG[1014h] Horizontal Pixel Size Register 1             | 290 | REG[1016h] through REG[101Ah] are Reserved               | 290 |
| REG[101Ch] RST Marker Operation Setting Register        | 291 | REG[101Eh] RST Marker Operation Status Register          | 292 |
| REG[1020 - 1066h] Insertion Marker Data Register        | 293 | REG[1200 - 127Eh] Quantization Table No. 0 Register      | 293 |
| REG[1280 - 12FEh] Quantization Table No. 1 Register     | 293 | REG[1400 - 141Eh] DC Huffman Table No. 0 Register 0      | 294 |
| REG[1420 - 1436h] DC Huffman Table No. 0 Register 1     | 294 | REG[1440 - 145Eh] AC Huffman Table No. 0 Register 0      | 295 |
| REG[1460 - 15A2h] AC Huffman Table No. 0 Register 1     | 295 | REG[1600 - 161Eh] DC Huffman Table No. 1 Register 0      | 297 |
| REG[1620 - 1636h] DC Huffman Table No. 1 Register 1     | 297 | REG[1640 - 165Eh] AC Huffman Table No. 1 Register 0      | 298 |
| REG[1660 - 17A2h] AC Huffman Table No. 1 Register 1     | 298 |                                                          |     |
| <b>2D BitBLT Registers</b>                              |     |                                                          |     |
| REG[8000h] BitBLT Control Register 0                    | 300 | REG[8002h] BitBLT Control Register 1                     | 300 |
| REG[8004h] BitBLT Status Register 0                     | 301 | REG[8006h] BitBLT Status Register 1                      | 302 |
| REG[8008h] BitBLT Command Register 0                    | 302 | REG[800Ah] BitBLT Command Register 1                     | 303 |
| REG[800Ch] BitBLT Source Start Address Register 0       | 304 | REG[800Eh] BitBLT Source Start Address Register 1        | 304 |
| REG[8010h] BitBLT Destination Start Address Register 0  | 305 | REG[8012h] BitBLT Destination Start Address Register 1   | 305 |
| REG[8014h] BitBLT Memory Address Offset Register        | 305 | REG[8018h] BitBLT Width Register                         | 305 |
| REG[801Ch] BitBLT Height Register                       | 306 | REG[8020h] BitBLT Background Color Register              | 306 |
| REG[8024h] BitBLT Foreground Color Register             | 306 | REG[8030h] BitBLT Interrupt Status Register              | 306 |
| REG[8032h] BitBLT Interrupt Control Register            | 307 | REG[10000h] 2D BitBLT Data Memory Mapped Region Register | 307 |

## 10.3 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

Some registers are only accessible when certain conditions exist. Any attempts to read/write in-accessible registers are invalid. The following restrictions apply to all registers.

- REG[0000h] - REG[0018h] and REG[0300h] - REG[030Eh] are always accessible.
- REG[0000h] - REG[0018h] are not reset by a Software Reset.
- When power save mode is enabled (REG[0014h] bit 0 = 1), REG[0030h] - REG[0A0Eh] are not accessible.
- When the JPEG Codec is disabled (REG[0980h] bit 0 = 0), REG[1000h] - REG[17A2h] are not accessible.

## 10.4 Register Description

### 10.4.1 System Configuration Registers

| REG[0000h] Product Information Register |    |    |    |    |    |                        |   |
|-----------------------------------------|----|----|----|----|----|------------------------|---|
| Default = 5058h                         |    |    |    |    |    |                        |   |
| Read Only                               |    |    |    |    |    |                        |   |
| Display Buffer Size bits 7-0            |    |    |    |    |    |                        |   |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9                      | 8 |
| Product Code bits 5-0                   |    |    |    |    |    | Revision Code bits 1-0 |   |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1                      | 0 |

- bits 15-8      Display Buffer Size bits [7:0] (Read Only)  
 These bits indicate the size of the SRAM display buffer measured in 4K byte increments. The S1D13715 display buffer is 320K bytes and these bits return a value of 80 (50h).  
 REG[0000h] bits 15-8      = display buffer size ÷ 4K bytes  
                                      = 320K bytes ÷ 4K bytes  
                                      = 80 (50h)
- bits 7-2      Product Code bits [5:0] (Read Only)  
 These bits indicate the product code. The product code for the S1D13715 is 010110 (16h).
- bits 1-0      Revision Code bits [1:0] (Read Only)  
 These bits indicate the revision code. The revision code is 00.

| REG[0002h] Configuration Pins Status Register |                 |    |    |    |    |   |   |
|-----------------------------------------------|-----------------|----|----|----|----|---|---|
| Default = 0000h                               |                 |    |    |    |    |   |   |
| Read Only                                     |                 |    |    |    |    |   |   |
| 15                                            | 14              | 13 | 12 | 11 | 10 | 9 | 8 |
| n/a                                           | CNF[6:0] Status |    |    |    |    |   |   |
| 7                                             | 6               | 5  | 4  | 3  | 2  | 1 | 0 |

bits 6-0

CNF[6:0] Status (Read Only)

These status bits return the status of the configuration pins CNF[6:0]. CNF[6:0] are latched at the rising edge of RESET#. For a functional description of each configuration bit (CNF[6:0]), see Section 5.4, “Summary of Configuration Options” on page 43.

| REG[0006h] Bus Timeout Setting Register |    |    |    |    |                                         |                           |                                     |
|-----------------------------------------|----|----|----|----|-----------------------------------------|---------------------------|-------------------------------------|
| Default = 0000h                         |    |    |    |    |                                         |                           |                                     |
| Read/Write                              |    |    |    |    |                                         |                           |                                     |
| 15                                      | 14 | 13 | 13 | 11 | 10                                      | 9                         | 8                                   |
| n/a                                     |    |    |    |    | Bus Timeout Reset Interrupt Status (RO) | Bus Timeout Reset Disable | Bus Timeout Reset Interrupt Disable |
| 7                                       | 6  | 5  | 4  | 3  | 2                                       | 1                         | 0                                   |

bit 2

Bus Timeout Reset Interrupt Status (Read Only).

This is the status bit for the bus timeout reset function. Bus timeout reset occurs when the WAIT# signal is active for 2 or 3 cycles.

This is the status bit for the bus timeout function.

When this bit = 1, a bus timeout has occurred.

When this bit = 0, a bus timeout has not occurred.

This flag is cleared by the Bus Timeout Reset Interrupt Disable bit (REG[0006h] bit 0).

bit 1

Bus Timeout Reset Disable

This bit controls the Bus Timeout Reset function of the S1D13715. If a bus timeout occurs, the Bus Timeout Reset Interrupt Status is set (REG[0006h] bit 2) and the chip is reset.

When this bit = 0, the bus timeout reset function is enabled (default).

When this bit = 1, the bus timeout reset function is disabled.

## Note

When the internal PLL is disabled (REG[0012h] bit 0 = 1), the Bus Timeout function must be disabled (REG[0006h] bit 1 = 1).

bit 0

Bus Timeout Reset Interrupt Disable

This bit controls the bus timeout reset interrupt and is used to clear the Bus Timeout Reset Interrupt Status (REG[0006h] bit 2).

When this bit = 0, the Bus Timeout Interrupt is enabled (default).

When this bit = 1, the Bus Timeout Interrupt is disabled.

When this bit is written as 1, the Bus Timeout Flag (REG[0006h] bit 2) is cleared.

## 10.4.2 Clock Setting Registers

| REG[000Eh] PLL Setting Register 0 |    |    |    |                    |    |   |   | Read/Write |
|-----------------------------------|----|----|----|--------------------|----|---|---|------------|
| Default = 1BE8h                   |    |    |    |                    |    |   |   |            |
| N-Counter bits 3-0                |    |    |    | L-Counter bits 9-6 |    |   |   |            |
| 15                                | 14 | 13 | 12 | 11                 | 10 | 9 | 8 |            |
| L-Counter bits 5-0                |    |    |    | V-Divider bits 1-0 |    |   |   |            |
| 7                                 | 6  | 5  | 4  | 3                  | 2  | 1 | 0 |            |

### Note

Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: “Power-On/Power-Off Sequence,” on page 308 or Figure 11-2: “Power Save Modes,” on page 309.

bits 15-12

N-Counter bits [3:0]

bits 11-2

L-Counter bits [9:0]

These bits are used together to configure the PLL Output (in MHz) and must be set according to the following formula.

$$\begin{aligned}\text{PLL Output} &= (\text{N-Counter} + 1) \times (\text{L-Counter} + 1) \times \text{CLKI} \\ &= \text{NN} \times \text{LL} \times \text{CLKI}\end{aligned}$$

Where:

PLL Output is the desired PLL output frequency in MHz (55MHz max)

N-Counter is the value in bits 15-12

L-Counter is the value in bits 11-2

CLKI is the PLL reference frequency (should always be 32.768kHz)

Table 10-3: PLL Setting Example

| Target Freq. (MHz) | NN | LL  | NN x LL | REG[000Eh] | POUT (MHz) |
|--------------------|----|-----|---------|------------|------------|
| 40                 | 4  | 305 | 1220    | 34C0h      | 39.98      |
| 45                 | 6  | 229 | 1374    | 5390h      | 45.02      |
| 48.76              | 16 | 93  | 1488    | F194h      | 48.76      |
| 50                 | 15 | 122 | 1830    | E1E4h      | 49.97      |
| 54                 | 16 | 103 | 1648    | F198h      | 54.00      |
| 55                 | 2  | 839 | 1678    | 1D18h      | 54.98      |

### Note

To optimize power consumption, use the largest NN value possible.

bits 1-0

V-Divider bits [1:0]  
These bits are used to fine tune the PLL output jitter. The V-Divider bits represent a value as shown in the following table. The V-Divider bits must be set such that the following formula is valid.

$$100\text{MHz} \leq \text{PLL Output} \times \text{V-Divider} \leq 410\text{MHz}$$

Table 10-4: V-Divider

| REG[000Eh] bits 1-0 | V-Divider |
|---------------------|-----------|
| 00                  | see note  |
| 01                  | 2         |
| 10                  | 4         |
| 11                  | 8         |

Where:  
PLL Output in MHz (55MHz max) generated by bits 15-12 (N-Counter) and bits 11-2 (L-Counter)  
V-Divide is the value from Table 10-4:

**Note**  
Setting the V-Divider value to 00 provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

| REG[0010h] PLL Setting Register 1 |    |    |    |     |    |   |   | Read/Write |
|-----------------------------------|----|----|----|-----|----|---|---|------------|
| Default = 0000h                   |    |    |    |     |    |   |   |            |
| VCO Kv Set bits 3-0               |    |    |    | n/a |    |   |   |            |
| 15                                | 14 | 13 | 12 | 11  | 10 | 9 | 8 |            |
| n/a                               |    |    |    |     |    |   |   |            |
| 7                                 | 6  | 5  | 4  | 3   | 2  | 1 | 0 |            |

**Note**

Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: “Power-On/Power-Off Sequence,” on page 308 or Figure 11-2: “Power Save Modes,” on page 309.

bits 15-12

VCO Kv Set bits [3:0]

These bits are used to fine tune the PLL output jitter. These bits should be set as follows.

If  $100\text{MHz} \leq (\text{PLL Output} \times \text{V-Divider}) \leq 200\text{MHz}$ , set these bits to 0010.

If  $200\text{MHz} < (\text{PLL Output} \times \text{V-Divider}) \leq 300\text{MHz}$ , set these bits to 0101.

If  $300\text{MHz} < (\text{PLL Output} \times \text{V-Divider}) \leq 410\text{MHz}$ , set these bits to 0111.

All other non-zero values for these bits are reserved.

Where:

PLL Output is the desired PLL output frequency in MHz and is generated using REG[000Eh] bits 15-12 and REG[000Eh] bits 11-2

V-Divide is the value from Table 10-4: and is controlled by REG[000Eh] bits 1-0

**Note**

Setting the value of these bits to 0000 provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

| REG[0012h] PLL Setting Register 2 |    |    |    |    |          |          |             |
|-----------------------------------|----|----|----|----|----------|----------|-------------|
| Default = 0001h                   |    |    |    |    |          |          |             |
| Read/Write                        |    |    |    |    |          |          |             |
| n/a                               |    |    |    |    |          |          |             |
| 15                                | 14 | 13 | 12 | 11 | 10       | 9        | 8           |
| n/a                               |    |    |    |    | Reserved | Reserved | PLL Disable |
| 7                                 | 6  | 5  | 4  | 3  | 2        | 1        | 0           |

**Note**  
For more information on the PLL and clock structure, see Section 9, “Clocks” on page 130.

- bit 2

Reserved  
The default value for this bit is 0.
- bit 1

Reserved  
The default value for this bit is 0.
- bit 0

PLL Disable  
This bit controls the internal PLL. The PLL must be configured using PLL Setting Register 0 (REG[000Eh]) and PLL Setting Register 1 (REG[0010h]) before enabling this bit. When this bit = 0, the PLL is enabled. When this option is selected, the PLL output is the source for the system clock divider.  
When this bit = 1, the PLL is disabled (default). When this option is selected, the external clock, CLKI is the source for the system clock divider.

**Note**  
There may be up to a 100ms delay before the PLL output becomes stable. The S1D13715 must not be accessed during this time.

| REG[0014h] Miscellaneous Configuration Register |                                    |     |                                                       |                           |                             |          | Read/Write        |
|-------------------------------------------------|------------------------------------|-----|-------------------------------------------------------|---------------------------|-----------------------------|----------|-------------------|
| Default = 0011h                                 |                                    |     |                                                       |                           |                             |          |                   |
| n/a                                             |                                    |     | Parallel Bypass Data Bus Width Select                 | Parallel Bit Order Select | Bypass Mode Select bits 2-0 |          |                   |
| 15                                              | 14                                 | 13  | 12                                                    | 11                        | 10                          | 9        | 8                 |
| VNDP Status (RO)                                | Memory Controller Idle Status (RO) | n/a | Serial/Parallel Input Active Pull-up/Pull-down Enable | n/a                       | Reserved                    | Reserved | Power Save Enable |
| 7                                               | 6                                  | 5   | 4                                                     | 3                         | 2                           | 1        | 0                 |

bit 12

**Parallel Bypass Data Bus Width Select**

This bit selects the data bus width for parallel bypass in Mode 2 and Mode 3. For parallel bypass pin mapping, see Table 5-15: “Serial/Parallel Bypass Pin Mapping,” on page 49. When this bit = 0, the data bus width for parallel bypass is 16-bit. In this setting GPIO20 and GPIO21 are available as GPIOs.

When this bit = 1, the data bus width for parallel bypass is 18-bit. In this setting GPIO20 and GPIO21 are used by the host cpu parallel interface and cannot be used for GPIO. GPIO register settings for these GPIOs have no effect on these signals.

**Note**

The HIOVDD and PIOVDD voltages must be compatible when using parallel bypass mode.

bit 11

**Parallel Bit Order Select**

This bit specifies the LCD data order for parallel panels when Mode 2, Mode 3, and Mode 4 are selected (see (REG[0032h] bits 1-0). However, this bit has no effect for all 24-bit parallel panels and 16/18-bit parallel panels in Mode 4.

When this bit = 0, the FPDAT0 output is the MSB.

When this bit = 1, the FPDAT0 output is the LSB.

*Table 10-5: Parallel Bit Order Selection*

| REG[0014h] bit 11 | Mode 2                | Mode 3                | Mode 4               |
|-------------------|-----------------------|-----------------------|----------------------|
| 0                 | LSB starts at FPDAT0  | LSB starts at FPDAT0  | LSB starts at FPDAT0 |
| 1                 | LSB starts at FPDAT17 | LSB starts at FPDAT17 | LSB starts at FPDAT7 |

bits 10-8

Bypass Mode Select bits [2:0]

These bits specify the bypass mode for both LCD1 and LCD2 displays. These bits must be configured before the Serial/Parallel Port Bypass Enable bit (REG[0032h] bit 8) is set. If REG[0032h] bit 8 is set to 1 when these bits = 000 or any Reserved setting, there is no hardware effect. For bypass mode pin mapping, see Table 5-15: “Serial/Parallel Bypass Pin Mapping,” on page 49.

Table 10-6: Bypass Mode Selection

| REG[0014h] bits 10-8 | Bypass Mode                                                                                                                                                                                                                    |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000                  | Serial/Parallel Bypass is disabled for both LCD1 and LCD2                                                                                                                                                                      |
| 001                  | <b>This option is for Mode 2 (REG[0032h] bits 1-0 = 10) only.</b> When Mode 2 is selected, parallel bypass of LCD1 is possible but serial bypass of LCD2 is not allowed.                                                       |
| 010                  | <b>This option is for Mode 1 (REG[0032h] bits 1-0 = 00) or Mode 2 (REG[0032h] bits 1-0 = 10) only.</b> When Mode 1 is selected, serial bypass of LCD2 is possible. When Mode 2 is selected, serial bypass of LCD2 is possible. |
| 011                  | <b>This option is for Mode 3 (REG[0032h] bits 1-0 = 11) only.</b> When Mode 3 is selected, parallel bypass of LCD1 and LCD2 is possible. Switch between LCD1 and LCD2 using SCS# and SI.                                       |
| 100                  | <b>This option is for Mode 4 (REG[0032h] bits 1-0 = 01) only.</b> When Mode 4 is selected, parallel bypass of LCD2 is possible.                                                                                                |
| 101 - 111            | Reserved                                                                                                                                                                                                                       |

### Note

If the Serial/Parallel Port Bypass Enable bit (REG[0032h] bit 8) is set to 1 and the Bypass Mode Select bits are not configured correctly, some signals may still be bypassed resulting in unpredictable results.

### Note

The HIOVDD and PIOVDD voltages must be compatible when using parallel bypass mode.

bit 7

Vertical Non-Display Period Status (Read Only)

If an RGB type panel is selected for LCD1 (Mode 1/Mode 4, see REG[0032h] bits 1-0), this status bit indicates whether the panel is in a Vertical Non-Display Period. This bit has no effect when Mode 2 or Mode 3 is selected.

When this bit = 0, the LCD panel output is in a Vertical Display Period.

When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 6

Memory Controller Idle Status (Read Only)

This bit indicates the status of the memory controller and must be checked before enabling Power Save Mode (REG[0014h] bit 0) or disabling the PLL (REG[0012h] bit 0). For further information on using this bit, see Figure 11-1: “Power-On/Power-Off Sequence,” on page 308 or Figure 11-2: “Power Save Modes,” on page 309.

When this bit = 0, the memory controller is powered up.

When this bit = 1, the memory controller is idling and the system clock source can be disabled.

- bit 4      **Serial/Parallel Input Active Pull-up/Pull-down Enable**  
 This bit controls the active pull-up/pull-down resistors on the host serial/parallel input pins (SCS#, SCLK, SA0, SI). When the serial/parallel input port is unused (Hi-Z), set this bit to 1.  
 When this bit = 0, the pull-up/pull-down resistors are inactive.  
 When this bit = 1, the pull-up/pull-down resistors are active and the pins are affected as follows (default).

*Table 10-7: Serial/Parallel Pull-up/Pull-down Resistors*

| Pin  | Type      |
|------|-----------|
| SCS# | Pull-up   |
| SCLK | Pull-down |
| SA0  | Pull-down |
| SI   | Pull-down |

**Note**

For Panel Interface Mode 3 (REG[0032h] bits 1-0 = 11) when the parallel panel on LCD2 is bypassed (REG[0014h] bits 10-8 = 011), the SI pin (PCS1#) must be pulled-up to HIOVDD and REG[0014h] bit 4 must be set to 0 at initialization.

- bit 2      **Reserved**  
 The default value for this bit is 0.

- bit 1      **Reserved**  
 The default value for this bit is 0.

- bit 0      **Power Save Mode Enable**  
 This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13715 is operating normally. When power save mode is enabled, the S1D13715 is in a power efficient state. For more information on the S1D13715 condition during Power Save Mode, see Section 11.2, “Power Save Mode Function” on page 311.  
 When this bit = 0, power save mode is disabled.  
 When this bit = 1, power save mode is enabled (default).

**Note**

For all modes except Mode 1 (see REG[0032h] bits 1-0), the LCD Output Port must be turned off (REG[0202h] bits 12-10 = 000) before enabling power save mode. For all modes, the Memory Controller Idle Status bit (REG[0014h] bit 6) must return a 1 before enabling power save mode.

| REG[0016h] Software Reset Register |    |    |    |    |    |   |   |
|------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable           |    |    |    |    |    |   |   |
| Write Only                         |    |    |    |    |    |   |   |
| Software Reset bits 15-8           |    |    |    |    |    |   |   |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Software Reset bits 7-0            |    |    |    |    |    |   |   |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

Software Reset bits [15:0] (Write Only)  
When any value is written to these bits, **all registers are reset to their default values**. A software reset via this register **does not clear the display buffer**. For further information on software reset, see Section 11.1.2, “Reset” on page 310.

| REG[0018h] System Clock Setting Register |    |    |    |    |    |                                     |   |
|------------------------------------------|----|----|----|----|----|-------------------------------------|---|
| Default = 0000h                          |    |    |    |    |    |                                     |   |
| Read/Write                               |    |    |    |    |    |                                     |   |
| n/a                                      |    |    |    |    |    |                                     |   |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9                                   | 8 |
| n/a                                      |    |    |    |    |    | System Clock Divide Select bits 1-0 |   |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1                                   | 0 |

bits 1-0

System Clock Divide Select bits [1:0]  
These bits determine the divide ratio for the system clock. The source is selectable, using REG[0012h] bit 0, between either the PLL output (see REG[000Eh]-REG[0012h]) or an external clock source (CLKI).

Table 10-8: System Clock Divide Ratio Selection

| REG[0018h] bits 1-0 | System Clock Divide Ratio |
|---------------------|---------------------------|
| 00                  | 1:1                       |
| 01                  | 2:1                       |
| 10                  | 3:1                       |
| 11                  | 4:1                       |

**Note**  
For more information on clocks, see Section 9, “Clocks” on page 130.

### 10.4.3 Indirect Interface Registers

These registers are used for the Indirect Interface only. The indirect interface is selected at RESET# using the configuration bits CNF[4:2] (see Table 5-9: “Summary of Power-On/Reset Options,” on page 43). For examples using the Indirect Interface, see Section 21, “Indirect Host Interface” on page 399.

#### REG[0020h] is Reserved

This register is Reserved and should not be written.

| REG[0022h] Indirect Interface Memory Address Register 1 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                         |    |    |    |    |    |   |   |            |
| Indirect Interface Memory Address bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Indirect Interface Memory Address bits 7-1              |    |    |    |    |    |   |   | n/a        |
| 7                                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[0024h] Indirect Interface Memory Address Register 2 |    |    |    |    |                                              |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----|----------------------------------------------|---|---|------------|
| Default = 0000h                                         |    |    |    |    |                                              |   |   |            |
| n/a                                                     |    |    |    |    |                                              |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11 | 10                                           | 9 | 8 |            |
| n/a                                                     |    |    |    |    | Indirect Interface Memory Address bits 18-16 |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3  | 2                                            | 1 | 0 |            |

REG[0024h] bits 2-0

REG[0022h] bits 15-1 Indirect Interface Memory Address bits [18:1]

**This register is used for Indirect Interface modes only.**

These bits determine the memory start address for each memory access. After a completed memory access, this register is incremented automatically.

#### Note

Only 16-bit memory accesses are possible when an indirect interface is selected.

| REG[0026h] Indirect Interface Auto Increment Register |    |    |    |    |    |                                            |   |
|-------------------------------------------------------|----|----|----|----|----|--------------------------------------------|---|
| Default = 0000h                                       |    |    |    |    |    |                                            |   |
| Read/Write                                            |    |    |    |    |    |                                            |   |
| 15                                                    | 14 | 13 | 12 | 11 | 10 | 9                                          | 8 |
| n/a                                                   |    |    |    |    |    | Indirect Interface Auto Increment bits 1-0 |   |
| 7                                                     | 6  | 5  | 4  | 3  | 2  | 1                                          | 0 |

bits 1-0

Indirect Interface Auto Increment bits [1:0]

**This register is used for Indirect Interface modes only.**

These bits determine the method used to auto increment the memory address stored in the Indirect Interface Memory Address registers (REG[0024h]-[0022h]). The Indirect Interface Memory Address registers must be auto incremented after each memory access based on the type of memory accesses being done (byte or word).

Table 10-9: Indirect Interface Auto Increment Selection

| REG[0026h] bits 1-0 | Indirect Interface Auto Increment                                                          |
|---------------------|--------------------------------------------------------------------------------------------|
| 00 (default)        | Increment when a high byte access or word access takes place                               |
| 01                  | Increment only when a word access takes place (no increment takes place for byte accesses) |
| 10                  | Never increment (Auto increment is disabled)                                               |
| 11                  | Reserved                                                                                   |

| REG[0028h] Indirect Interface Memory Access Port Register |    |    |    |    |    |   |   |
|-----------------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                                  |    |    |    |    |    |   |   |
| Read/Write                                                |    |    |    |    |    |   |   |
| Indirect Interface Memory Access Port bits 15-8           |    |    |    |    |    |   |   |
| 15                                                        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Indirect Interface Memory Access Port bits 7-0            |    |    |    |    |    |   |   |
| 7                                                         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

Indirect Interface Memory Access Port bits [15:0]

**This register is used for Indirect Interface modes only.**

These bits are the memory read/write port for the Indirect Interface. An Index Write to this register begins (or triggers) a burst read/write to memory.

| REG[002Ah] Indirect Interface 2D BitBLT Data Read/Write Port Register |    |    |    |    |    |   |   |
|-----------------------------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                                              |    |    |    |    |    |   |   |
| Read/Write                                                            |    |    |    |    |    |   |   |
| Indirect Interface 2D BitBLT Data Read/Write Port bits 15-8           |    |    |    |    |    |   |   |
| 15                                                                    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Indirect Interface 2D BitBLT Data Read/Write Port bits 7-0            |    |    |    |    |    |   |   |
| 7                                                                     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

Indirect Interface 2D BitBLT Data Read/Write Port bits [15:0]

**This register is used for Indirect Interface modes only.**

These bits are the read/write port for 2D BitBLT data when using the Indirect Interface (instead of REG[10000h] for direct addressing).

## 10.4.4 LCD Panel Interface Generic Setting Register

| REG[0030h] LCD Interface Clock Setting Register |    |    |                                    |                                     |    |   |   | Read/Write |
|-------------------------------------------------|----|----|------------------------------------|-------------------------------------|----|---|---|------------|
| Default = 0000h                                 |    |    |                                    |                                     |    |   |   |            |
| n/a                                             |    |    |                                    | Serial Clock Divide Select bits 2-0 |    |   |   |            |
| 15                                              | 14 | 13 | 12                                 | 11                                  | 10 | 9 | 8 |            |
| n/a                                             |    |    | Pixel Clock Divide Select bits 4-0 |                                     |    |   |   |            |
| 7                                               | 6  | 5  | 4                                  | 3                                   | 2  | 1 | 0 |            |

bits 10-8

Serial Clock Divide Select bits[2:0]

These bits specify the divide ratio for the serial clock. The clock source for the serial clock is the system clock (see Figure 9-1: “Clock Diagram,” on page 130). If LCD1 or LCD2 is not a serial interface type LCD panel (REG[0032h] bits 1-0) or if Serial Port Bypass is enabled (REG[0032h] bit 8 = 1), these bits are ignored.

Table 10-10: Serial Clock Divide Ratio Selection

| REG[0030h] bits 10-8 | Serial Clock Divide Ratio |
|----------------------|---------------------------|
| 000                  | 2:1                       |
| 001                  | 4:1                       |
| 010                  | 6:1                       |
| 011                  | 8:1                       |
| 100                  | 10:1                      |
| 101                  | 12:1                      |
| 110                  | 14:1                      |
| 111                  | 16:1                      |

bits 4-0

Pixel Clock Divide Select bits[4:0]

These bits specify the divide ratio for the pixel clock. The clock source for the pixel clock is the system clock (see Figure 9-1: “Clock Diagram,” on page 130). When LCD1 is an RGB type panel (REG[0032h] bits 1-0 = 00b or 01b), the pixel clock is the same as the shift clock. When LCD1 or LCD2 is a parallel interface type panel (REG[0032h] bits 1-0 = 10b or 11b), the pixel clock is used for the parallel data output timing clock.

*Table 10-11: Pixel Clock Divide Selection*

| REG[0030h] bits 4-0 | Pixel Clock Divide Ratio |
|---------------------|--------------------------|
| 00000               | 2:1 (see Note)           |
| 00001               | 4:1                      |
| 00010               | 6:1                      |
| 00011               | 8:1                      |
| 00100               | 10:1                     |
| 00101               | 12:1                     |
| 00110               | 14:1                     |
| 00111               | 16:1                     |
| 01000               | 18:1                     |
| 01001               | 20:1                     |
| 01010               | 22:1                     |
| 01011               | 24:1                     |
| 01100               | 26:1                     |
| 01101               | 28:1                     |
| 01110               | 30:1                     |
| 01111               | 32:1                     |
| 10000               | 34:1                     |
| 10001               | 36:1                     |
| 10010               | 38:1                     |
| 10011               | 40:1                     |
| 10100               | 42:1                     |
| 10101               | 44:1                     |
| 10110               | 46:1                     |
| 10111               | 48:1                     |
| 11000 - 11111       | Reserved                 |

**Note**

SwivelView should not be used when the 2:1 Pixel Clock Divide Ratio is used (REG[0202h] bits 5-4 = 00b and bits 1-0 = 00b).

| REG[0032h] LCD Module Clock Setting Register |                                             |    |    |     |    |                             |                                           |
|----------------------------------------------|---------------------------------------------|----|----|-----|----|-----------------------------|-------------------------------------------|
| Default = 0000h                              |                                             |    |    |     |    |                             |                                           |
| RGB Panel Type bits 5-0                      |                                             |    |    |     |    | n/a                         | Serial/<br>Parallel Port<br>Bypass Enable |
| 15                                           | 14                                          | 13 | 12 | 11  | 10 | 9                           | 8                                         |
| FPSHIFT Polarity<br>Select                   | RGB Interface Panel Data Bus Width bits 2-0 |    |    | n/a |    | Panel Interface<br>bits 1-0 |                                           |
| 7                                            | 6                                           | 5  | 4  | 3   | 2  | 1                           | 0                                         |

bits 15-10

RGB Panel Type bits [5:0]

When the panel interface for LCD1 is RGB (REG[0032h] bits 1-0 = 00), these bits determine the RGB panel type. When LCD1 is not an RGB interface (REG[0032h] bits 1-0 = 10 or 11), these bit are ignored.

Table 10-12: RGB Panel Type Selection

| REG[0032h] bits 15-10 | RGB Panel Type (LCD1) |
|-----------------------|-----------------------|
| 000000                | General TFT, ND-TFD   |
| 000001                | HR-TFT                |
| 000010                | Casio TFT             |
| 000011                | TFT Type 2            |
| 000100                | TFT Type 3            |
| 000101 - 101111       | Reserved              |
| 110000                | $\alpha$ -TFT         |
| 110001 - 111111       | Reserved              |

bit 8

## Serial/Parallel Port Bypass Enable

This bit controls the serial/parallel port bypass function. Before enabling Serial/Parallel Port Bypass, the Bypass Mode must be configured using the Bypass Mode Select bits (REG[0014h] bits 10-8) or there will be no hardware effect.

When the serial/parallel port bypass is enabled, the host can drive the LCD2 serial/parallel interface directly via the Host serial/parallel interface. When the serial/parallel port bypass is disabled, the LCD2 serial/parallel interface is controlled by the S1D13715. For serial/parallel bypass pin mapping and input/output port assignments, see Table 5-15: “Serial/Parallel Bypass Pin Mapping,” on page 49.

When this bit = 0, the serial/parallel port bypass is disabled.

When this bit = 1, the serial/parallel port bypass is enabled.

### Note

When power save mode is enabled (REG[0014h] bit 0 = 1), the host can drive the LCD2 serial interface directly via the host serial interface automatically. In this situation, the Serial/Parallel Port Bypass Enable bit does not need to be set, however, the Bypass Mode Select bits (REG[0014h] bits 10-8) must be set according to the selected mode.

bit 7

## FPSHIFT Polarity Select

This bit sets the polarity of the shift clock for RGB type panels (inverts FPSHIFT).

When this bit = 0, all panel interface signals change at the rising edge of FPSHIFT.

When this bit = 1, all panel interface signals change at the falling edge of FPSHIFT.

bits 6-4

## RGB Interface Panel Data Bus Width bits [2:0]

These bits only have an effect when a RGB interface panel is selected (REG[0032h] bits 1-0 = 00 or 01). These bits determine the RGB Interface Panel Data Bus size. Unused FPDAT[17:0] pins are forced low and unused GPIO[9:4] pins are used as GPIOs.

*Table 10-13: RGB Interface Panel Data Bus Width Selection*

| REG[0032h] bits 6-4 | RGB Interface Panel Data Bus Width (LCD1) |
|---------------------|-------------------------------------------|
| 000                 | 9-bit                                     |
| 001                 | 12-bit                                    |
| 010                 | 16-bit                                    |
| 011                 | 18-bit                                    |
| 100                 | 24-bit                                    |
| 101 - 111           | Reserved                                  |

bits 1-0

Panel Interface bits[1:0]

These bits determine the LCD1 and LCD2 interface types.

Table 10-14: Panel Interface Selection

| REG[0032h] bits 1-0 | Mode | LCD1 Panel Interface                   | LCD2 Panel Interface                   |
|---------------------|------|----------------------------------------|----------------------------------------|
| 00                  | 1    | RGB Interface                          | Serial Interface<br>(RAM integrated)   |
| 01                  | 4    | RGB Interface                          | Parallel Interface<br>(RAM integrated) |
| 10                  | 2    | Parallel Interface<br>(RAM integrated) | Serial Interface<br>(RAM integrated)   |
| 11                  | 3    | Parallel Interface<br>(RAM integrated) | Parallel Interface<br>(RAM integrated) |

**REG[0034h] LCD Interface Command Register**

Default = 0000h

Read/Write

| LCD Interface Command Register bits 15-8 |    |    |    |    |    |   |   |
|------------------------------------------|----|----|----|----|----|---|---|
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LCD Interface Command Register bits 7-0  |    |    |    |    |    |   |   |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 15-0

LCD Interface Command Register bits [15:0]

**These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels.** These bits form the command register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), the command transfer starts when this register is written. When the command transfer starts, the FPA0 pin is driven low or high depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

**Note**

If the LCD1 serial data type is set to uWIRE or TFT Type 5 (REG[0054h] bits 7-5 = 10x or 11x), the upper byte of REG[0034h] is used for A[7:0] and the lower byte is used for D[7:0].

| REG[0036h] LCD Interface Parameter Register |    |    |    |    |    |   |   |
|---------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                             |    |    |    |    |    |   |   |
| Read/Write                                  |    |    |    |    |    |   |   |
| LCD Interface Parameter Register bits 15-8  |    |    |    |    |    |   |   |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LCD Interface Parameter Register bits 7-0   |    |    |    |    |    |   |   |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 15-0

LCD Interface Parameter Register bits [15:0]

**These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels.** These bits form the parameter register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), data transfer starts when this register is written. When the data transfer starts, the FPA0 pin is driven high or low depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

Note

If the LCD1 serial data type is set to uWIRE or TFT Type 5 (REG[0054h] bits 7-5 = 10x or 11x), the upper byte of REG[0036h] is used for A[7:0] and the lower byte is used for D[7:0].

| REG[0038h] LCD Interface Status Register |    |    |    |    |    |   |                      |
|------------------------------------------|----|----|----|----|----|---|----------------------|
| Default = 0000h                          |    |    |    |    |    |   |                      |
| Read Only                                |    |    |    |    |    |   |                      |
| n/a                                      |    |    |    |    |    |   |                      |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8                    |
| n/a                                      |    |    |    |    |    |   | LCD Interface Status |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0                    |

bit 0

LCD Interface Status (Read Only)

This bit indicates the status of the LCD1 or LCD2 serial/parallel interface. When this bit = 0, the LCD1 or LCD2 serial/parallel interface is not busy (or ready). When this bit = 1, the LCD1 or LCD2 serial/parallel interface is busy.

| REG[003Ah] LCD Interface Frame Transfer Register |    |    |    |     |    |    |   | Read/Write                           |
|--------------------------------------------------|----|----|----|-----|----|----|---|--------------------------------------|
| Default = 0000h                                  |    |    |    |     |    |    |   |                                      |
| 15                                               | 14 | 13 | 12 | n/a | 11 | 10 | 9 | 8                                    |
| 7                                                | 6  | 5  | 4  | n/a | 3  | 2  | 1 | LCD Interface Frame Transfer Trigger |
|                                                  |    |    |    |     |    |    |   | 0                                    |

bit 0

LCD Interface Frame Transfer Trigger

**This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels.** This bit is the trigger to transfer 1 frame of data to the LCD interface.

When this bit is set to 1 and the LCD interface status is not busy (REG[0038h] bit 0 = 0), 1 frame of data is transferred to the LCD interface. When the data transfer is finished, this bit is cleared automatically.

When this bit is set to 1 and the LCD interface is busy (REG[0038h] bit 0 = 1), the frame transfer request is ignored. Once the LCD interface is no longer busy, this bit is cleared without transferring any data.

**Note**

When LCD Interface Auto Transfer is enabled (REG[003Ch] bit 0 = 1), this bit remains high (1).

| REG[003Ch] LCD Interface Transfer Setting Register |     |    |    |     |    |    |   | Read/Write                               |
|----------------------------------------------------|-----|----|----|-----|----|----|---|------------------------------------------|
| Default = 0000h                                    |     |    |    |     |    |    |   |                                          |
| 15                                                 | 14  | 13 | 12 | n/a | 11 | 10 | 9 | 8                                        |
| P/C Polarity Invert Enable                         | n/a |    |    |     |    |    |   | LCD Interface Auto Frame Transfer Enable |
| 7                                                  | 6   | 5  | 4  |     | 3  | 2  | 1 | 0                                        |

bit 7

Parameter/Command Polarity Invert Enable

**This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels.** During an LCD Interface Command (REG[0034h]) or LCD Interface Parameter (REG[0036h]) transfer, FPA0 is driven high or low based on the setting of this bit. When LCD1 is a ND-TFD 9-bit panel (REG[0054h] bits 7-5 = 001) or LCD2 is a 9-bit serial panel (REG[005Ch] bit 5 = 1), this bit determines the MSB of the 9-bit data on FPSO.

Table 10-15: Parameter/Command Invert Setting

| REG[003Ch] bit 7 | FPA0 Signal Output |           |
|------------------|--------------------|-----------|
|                  | Command            | Parameter |
| 0                | Low                | High      |
| 1                | High               | Low       |

bit 0

LCD Interface Auto Frame Transfer Enable

**This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels.** This bit controls the automatic frame transfer of one frame of display memory to the LCD interface. The frame transfer is triggered and synchronized by the camera interface vertical sync signal (CM1VREF or CM2VREF). All camera input signals are required to trigger the frame transfer.

When this bit = 0, auto frame transfer is disabled.

When this bit = 1, auto frame transfer is enabled.

When this bit = 1, the LCD Interface Status bit (REG[0038h] bit 0) is always busy. When busy, command/parameter and frame transfers cannot be sent manually. This bit should be disabled before camera input is disabled.

**Note**

While auto transfer is enabled, the following condition must be met or no frame transfers will take place.

1 Frame transfer cycle (time) < 1 CMVREF period (time)

**Note**

While auto transfer is enabled, do not vary the PCLK and CM1CLKOUT/CM2CLKOUT frequencies

### 10.4.5 LCD1 Setting Register

| REG[0040h] LCD1 Horizontal Total Register |    |                                |    |    |    |          |            |
|-------------------------------------------|----|--------------------------------|----|----|----|----------|------------|
| Default = 0001h                           |    |                                |    |    |    |          |            |
|                                           |    |                                |    |    |    |          | Read/Write |
| n/a                                       |    |                                |    |    |    | Reserved |            |
| 15                                        | 14 | 13                             | 12 | 11 | 10 | 9        | 8          |
| Reserved                                  |    | LCD1 Horizontal Total bits 6-0 |    |    |    |          |            |
| 7                                         | 6  | 5                              | 4  | 3  | 2  | 1        | 0          |

bits 9-7                      Reserved  
 These bits default to 0

bits 6-0                      LCD1 Horizontal Total bits [6:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the LCD1 Horizontal Total period, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period. The maximum Horizontal Total is 1024 pixels. These bits must not be set to 0.  

$$\text{REG}[0040\text{h}] \text{ bits } 6-0 = (\text{Horizontal Total in pixels} \div 8) - 1$$

**Note**

This register must be programmed such that the following formula is valid.  

$$\text{HT} \geq \text{HDP} + \text{HNDP}$$

| REG[0042h] LCD1 Horizontal Display Period Register |    |    |     |    |    |   | Read/Write     |
|----------------------------------------------------|----|----|-----|----|----|---|----------------|
| Default = 0000h                                    |    |    |     |    |    |   |                |
| 15                                                 | 14 | 13 | n/a | 11 | 10 | 9 | LCD1 HDP bit 8 |
| LCD1 Horizontal Display Period bits 7-0            |    |    |     |    |    |   | 8              |
| 7                                                  | 6  | 5  | 4   | 3  | 2  | 1 | 0              |

bits 8-0      LCD1 Horizontal Display Period bits [8:0]  
These bits specify the LCD1 Horizontal Display Period, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.

$$\text{REG[0042h] bits 8-0} = (\text{Horizontal Display Period in pixels} \div 2) - 1$$

**Note**  
For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.  
$$\text{HDP} \times \text{VDP} \geq 40 \text{ pixels.}$$

| REG[0044h] LCD1 Horizontal Display Period Start Position Register |    |    |     |    |    |   | Read/Write        |
|-------------------------------------------------------------------|----|----|-----|----|----|---|-------------------|
| Default = 0000h                                                   |    |    |     |    |    |   |                   |
| 15                                                                | 14 | 13 | n/a | 11 | 10 | 9 | LCD1 HDP bits 9-8 |
| LCD1 Horizontal Display Period bits 7-0                           |    |    |     |    |    |   | 8                 |
| 7                                                                 | 6  | 5  | 4   | 3  | 2  | 1 | 0                 |

bits 9-0      LCD1 Horizontal Display Period Start Position bits [9:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the LCD1 Horizontal Display Period Start Position in 1 pixel resolution.

$$\text{REG[0044h] bits 9-0} = \text{Horizontal Display Period Start Position in pixels} - 9$$

| REG[0046h] LCD1 FPLINE Register |                             |    |     |    |    |   | Read/Write |
|---------------------------------|-----------------------------|----|-----|----|----|---|------------|
| Default = 0000h                 |                             |    |     |    |    |   |            |
|                                 |                             |    | n/a |    |    |   |            |
| 15                              | 14                          | 13 | 12  | 11 | 10 | 9 | 8          |
| FPLINE Polarity                 | FPLINE Pulse Width bits 6-0 |    |     |    |    |   |            |
| 7                               | 6                           | 5  | 4   | 3  | 2  | 1 | 0          |

- bit 7 FPLINE Pulse Polarity  
**This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and has no effect when a serial or parallel interface panel is selected.** This bit selects the polarity of the horizontal sync signal (FPLINE).  
 When this bit = 0, the horizontal sync signal (FPLINE) is active low.  
 When this bit = 1, the horizontal sync signal (FPLINE) is active high.
- bits 6-0 FPLINE Pulse Width bits [6:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the width of the horizontal sync signal (FPLINE), in 1 pixel resolution.  
 REG[0046h] bits 6-0 = FPLINE Pulse Width in pixels - 1

| REG[0048h] LCD1 FPLINE Pulse Position Register |    |    |     |    |    |                                | Read/Write |
|------------------------------------------------|----|----|-----|----|----|--------------------------------|------------|
| Default = 0000h                                |    |    |     |    |    |                                |            |
|                                                |    |    | n/a |    |    | FPLINE Pulse Position bits 9-8 |            |
| 15                                             | 14 | 13 | 12  | 11 | 10 | 9                              | 8          |
| FPLINE Pulse Position bits 7-0                 |    |    |     |    |    |                                |            |
| 7                                              | 6  | 5  | 4   | 3  | 2  | 1                              | 0          |

- bits 9-0 FPLINE Pulse Position bits [9:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the position of the FPLINE pulse.  
 REG[0048h] bits 9-0 = FPFAME edge to FPLINE edge in pixels - 1

| REG[004Ah] LCD1 Vertical Total Register |    |    |    |    |    |   | Read/Write                   |  |
|-----------------------------------------|----|----|----|----|----|---|------------------------------|--|
| Default = 0000h                         |    |    |    |    |    |   |                              |  |
| n/a                                     |    |    |    |    |    |   | LCD1 Vertical Total bits 9-8 |  |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8                            |  |
| LCD1 Vertical Total bits 7-0            |    |    |    |    |    |   |                              |  |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0                            |  |

bits 9-0

LCD1 Vertical Total bits [9:0]

**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the LCD1 Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

REG[004Ah] bits 9-0 = Vertical Total in lines - 1

| REG[004Ch] LCD1 Vertical Display Period Register |    |    |    |    |    |   | Read/Write                       |  |
|--------------------------------------------------|----|----|----|----|----|---|----------------------------------|--|
| Default = 0000h                                  |    |    |    |    |    |   |                                  |  |
| n/a                                              |    |    |    |    |    |   | Vertical Display Period bits 9-8 |  |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9 | 8                                |  |
| Vertical Display Period bits 7-0                 |    |    |    |    |    |   |                                  |  |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1 | 0                                |  |

bits 9-0

Vertical Display Period bits [9:0]

These bits specify the LCD1 Vertical Display period, in 1 line resolution. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[004Ch] bits 9-0 = Vertical Display Period in lines - 1

## Note

For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

$$\text{HDP} \times \text{VDP} \geq 40 \text{ pixels}$$

| REG[004Eh] LCD1 Vertical Display Period Start Position Register |    |    |    |    |    |   | Read/Write                                      |  |
|-----------------------------------------------------------------|----|----|----|----|----|---|-------------------------------------------------|--|
| Default = 0000h                                                 |    |    |    |    |    |   |                                                 |  |
| n/a                                                             |    |    |    |    |    |   | Vertical Display Period Start Position bits 9-8 |  |
| 15                                                              | 14 | 13 | 12 | 11 | 10 | 9 | 8                                               |  |
| Vertical Display Period Start Position bits 7-0                 |    |    |    |    |    |   |                                                 |  |
| 7                                                               | 6  | 5  | 4  | 3  | 2  | 1 | 0                                               |  |

bits 9-0

LCD1 Vertical Display Period Start Position bits [9:0]

**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the LCD1 Vertical Display Period Start Position in 1 line resolution.

| REG[0050h] LCD1 FPFRAME Register |     |    |    |    |                              |   |   |
|----------------------------------|-----|----|----|----|------------------------------|---|---|
| Default = 0000h                  |     |    |    |    |                              |   |   |
| Read/Write                       |     |    |    |    |                              |   |   |
| n/a                              |     |    |    |    |                              |   |   |
| 15                               | 14  | 13 | 12 | 11 | 10                           | 9 | 8 |
| FPFRAME Polarity                 | n/a |    |    |    | FPFRAME Pulse Width bits 2-0 |   |   |
| 7                                | 6   | 5  | 4  | 3  | 2                            | 1 | 0 |

bit 7 FPFRAME Pulse Polarity  
**This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and has no effect when a serial or parallel interface panel is selected.** This bit selects the polarity of the vertical sync signal (FPFRAME).  
 When this bit = 0, the vertical sync signal (FPFRAME) is active low.  
 When this bit = 1, the vertical sync signal (FPFRAME) is active high.

bits 2-0 FPFRAME Pulse Width bits [2:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the width of the panel vertical sync signal (FPFRAME), in 1 line resolution.  
 REG[0050h] bits 2-0 = FPFRAME Pulse Width in lines - 1

| REG[0052h] LCD1 FPFRAME Pulse Position Register |    |    |    |    |    |                                 |   |
|-------------------------------------------------|----|----|----|----|----|---------------------------------|---|
| Default = 0000h                                 |    |    |    |    |    |                                 |   |
| Read/Write                                      |    |    |    |    |    |                                 |   |
| n/a                                             |    |    |    |    |    | FPFRAME Pulse Position bits 9-8 |   |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9                               | 8 |
| FPFRAME Pulse Position bits 7-0                 |    |    |    |    |    |                                 |   |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1                               | 0 |

bits 9-0 FPFRAME Pulse Position bits [9:0]  
**These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00 or 01) and have no effect when a serial or parallel interface panel is selected.** These bits specify the start position of the FPFRAME signal, in 1 line resolution.

| REG[0054h] LCD1 Serial Interface Setting Register |    |    |                            |     |    |                         |                            |
|---------------------------------------------------|----|----|----------------------------|-----|----|-------------------------|----------------------------|
| Default = 0001h                                   |    |    |                            |     |    |                         |                            |
| Read/Write                                        |    |    |                            |     |    |                         |                            |
| n/a                                               |    |    |                            |     |    |                         |                            |
| 15                                                | 14 | 13 | 12                         | 11  | 10 | 9                       | 8                          |
| LCD1 Serial Data Type bits 2-0                    |    |    | LCD1 Serial Data Direction | n/a |    | LCD1 Serial Clock Phase | LCD1 Serial Clock Polarity |
| 7                                                 | 6  | 5  | 4                          | 3   | 2  | 1                       | 0                          |

bit 7-5                      LCD1 Serial Data Type bits [2:0]  
These bits determine the LCD1 Serial Data Type for RGB displays requiring initialization through a serial interface.

Table 10-16: LCD1 Serial Data Type Selection

| REG[0054h] bits 7-5 | LCD1 Serial Data Type        |
|---------------------|------------------------------|
| 000                 | ND-TFD 4 pins (8-bit Serial) |
| 001                 | ND-TFD 3 pins (9-bit Serial) |
| 01x                 | a-Si TFT (8-bit Serial)      |
| 10x                 | uWIRE (16-bit Serial)        |
| 11x                 | Reserved                     |

**Note**  
For Mode 2 and Mode 3 configurations (see REG[0032h] bits 1-0), these bits must be set to 000.

bit 4                      LCD1 Serial Data Direction  
This bit determines the LCD1 serial data direction for RGB displays requiring initialization through a serial interface.  
When this bit = 0, the MSB is first.  
When this bit = 1, the LSB is first.

bit 1                      LCD1 Serial Clock Phase  
This bit specifies the serial clock phase for RGB displays requiring initialization through a serial interface. See Table 10-17: “LCD1 Serial Clock Polarity and Phase Selection”.

**Note**  
For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing” on page 108.

bit 0 LCD1 Serial Clock Polarity  
This bit determines the LCD1 serial data format for RGB displays requiring initialization through a serial interface.

Table 10-17: LCD1 Serial Clock Polarity and Phase Selection

| REG[0054h] bit 1 | REG[0054h] bit 0 | Serial Data Output Changes   | Idling Status of Clock |
|------------------|------------------|------------------------------|------------------------|
| 0                | 0                | falling edge of Serial Clock | Low                    |
|                  | 1                | rising edge of Serial Clock  | High                   |
| 1                | 0                | rising edge of Serial Clock  | Low                    |
|                  | 1                | falling edge of Serial Clock | High                   |

**Note**

For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing” on page 108.

| REG[0056h] LCD1 Parallel Interface Setting Register |                           |                  |                 |     |                                    |            |   |
|-----------------------------------------------------|---------------------------|------------------|-----------------|-----|------------------------------------|------------|---|
| Default = 0000h                                     |                           |                  |                 |     |                                    | Read/Write |   |
| n/a                                                 |                           | LCD1 Pin Control | LCD1 CS Control | n/a |                                    | Reserved   |   |
| 15                                                  | 14                        | 13               | 12              | 11  | 10                                 | 9          | 8 |
| LCD1 VSYNC Input Enable                             | LCD1 Parallel Type Select | n/a              |                 |     | LCD1 Parallel Data Format bits 2-0 |            |   |
| 7                                                   | 6                         | 5                | 4               | 3   | 2                                  | 1          | 0 |

bit 13 LCD1 Pin Control  
This bit controls the parallel interface data output buffer for LCD1.  
When this bit = 0 and REG[005Eh] bit 13 = 0, FPDAT[17:0] are always output buffers and do not tristate. All other pins are not affected.  
When this bit = 1, FPDAT[17:0] are tristated, except during LCD1 control/display data output when FPDAT[17:0] become output buffers. GPIO[2:1], which are used to read 2-bits of data from the LCD1 panel, are forced to inputs.

bit 12 LCD1 CS Control  
**This bit is only valid when LCD1 Pin Control is enabled (REG[0056h] bit 13 = 1).**  
When this bit = 0, the LCD1 chip select signal, output on FPCS1#, is automatically generated by the S1D13715.  
When this bit = 1, the LCD1 chip select signal, output on FPCS1#, is derived from a logical AND of the original signal and GPIO0 (REG[030Ch] bit 0). GPIO0 is forced to an output.

**Note**

The panel read signal must be generated by a GPIO (i.e. GPIO3). Read data must be input from GPIO[2:1].

- bits 9-8      Reserved  
These bits are reserved and default to 0.
- bit 7      LCD1 VSYNC Input Enable  
**This bit is not used for RGB type panels.**  
This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN1). When a manual transfer has been initiated, the LCD1 data output will occur on the next falling edge of FPVIN1.  
When this bit = 1, the LCD1 data output is synchronous with an external VSYNC input.  
When this bit = 0, the LCD1 data output is independent of an external VSYNC input.

### Note

The FPVIN1 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN1 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN1 falling edge.

### Note

Once a manual frame transfer has been initiated (REG[003Ah] bit 0 = 1), the LCD1 VSYNC Input Enable bit must not be disabled before the next VSYNC signal has occurred or the LCD interface will always be busy and subsequent transfers will not occur.

- bit 6      LCD1 Parallel Type Select  
This bit determines the LCD1 parallel interface type.  
When this bit = 0, the parallel interface is type 80.  
When this bit = 1, the parallel interface is type 68.
- bit 2-0      LCD1 Parallel Data Format bits [2:0]  
These bits determine the LCD1 parallel data format. **These bits are not used for RGB Type Panels (REG[0032h] bits 1-0 = 00 or 01).** For further information on available parallel data formats, see Section 13.4, "Parallel Data Format" on page 320.

Table 10-18: LCD1 Parallel Data Format Selection

| REG[0056h] bits 2-0 | LCD1 Parallel Data Format |                                    |
|---------------------|---------------------------|------------------------------------|
|                     | Data Bus Width            | Data Format                        |
| 000                 | 8-bit                     | RGB = 3:3:2<br>(1 cycle/pixel)     |
| 001                 |                           | RGB = 4:4:4<br>(3 cycle / 2 pixel) |
| 010                 | 16-bit                    | RGB = 8:8:8<br>(3 cycle/2 pixel)   |
| 011                 | 8-bit                     | RGB = 8:8:8<br>(3 cycle/pixel)     |
| 100                 | 24-bit                    | RGB = 8:8:8<br>(1 cycle/pixel)     |
| 101                 | 16-bit                    | RGB = 4:4:4<br>(1 cycle/pixel)     |
| 110                 |                           | RGB = 5:6:5<br>(1 cycle/pixel)     |
| 111                 | 18-bit                    | RGB = 6:6:6<br>(1 cycle/pixel)     |

## 10.4.6 LCD2 Setting Registers

| REG[0058h] LCD2 Horizontal Display Period Register |    |    |    |    |    |   | Read/Write     |
|----------------------------------------------------|----|----|----|----|----|---|----------------|
| Default = 0000h                                    |    |    |    |    |    |   |                |
| n/a                                                |    |    |    |    |    |   | LCD2 HDP bit 8 |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9 | 8              |
| LCD2 Horizontal Display Period bits 7-0            |    |    |    |    |    |   |                |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1 | 0              |

bits 8-0

LCD2 Horizontal Display Period bits [8:0]

These bits specify the LCD2 Horizontal Display Period, in 2 pixel resolution.

REG[0058h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

**Note**

For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

$$\text{HDP} \times \text{VDP} \geq 40 \text{ pixels.}$$

| REG[005Ah] LCD2 Vertical Display Period Register |    |    |    |    |    |   | Read/Write                            |
|--------------------------------------------------|----|----|----|----|----|---|---------------------------------------|
| Default = 0000h                                  |    |    |    |    |    |   |                                       |
| n/a                                              |    |    |    |    |    |   | LCD2 Vertical Display Period bits 9-8 |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9 | 8                                     |
| LCD2 Vertical Display Period bits 7-0            |    |    |    |    |    |   |                                       |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1 | 0                                     |

bits 9-0

Vertical Display Period bits [9:0]

These bits specify the LCD2 Vertical Display Period, in 1 line resolution.

REG[005Ah] bits 9-0 = Vertical Display Period in lines - 1

**Note**

For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

$$\text{HDP} \times \text{VDP} \geq 40 \text{ pixels.}$$

| REG[005Ch] LCD2 Serial Interface Setting Register |    |                       |                            |                                  |    |                         |                            |
|---------------------------------------------------|----|-----------------------|----------------------------|----------------------------------|----|-------------------------|----------------------------|
| Default = 0001h                                   |    |                       |                            |                                  |    |                         |                            |
| Read/Write                                        |    |                       |                            |                                  |    |                         |                            |
| n/a                                               |    |                       |                            |                                  |    |                         |                            |
| 15                                                | 14 | 13                    | 12                         | 11                               | 10 | 9                       | 8                          |
| n/a                                               |    | LCD2 Serial Data Type | LCD2 Serial Data Direction | LCD2 Serial Data Format bits 1-0 |    | LCD2 Serial Clock Phase | LCD2 Serial Clock Polarity |
| 7                                                 | 6  | 5                     | 4                          | 3                                | 2  | 1                       | 0                          |

bit 5 LCD2 Serial Data Type  
This bit determines the LCD2 serial data type.

Table 10-19: LCD2 Serial Data Type Selection

| REG[005Ch] bit 5 | LCD2 Serial Data Type |
|------------------|-----------------------|
| 0                | 4 pins (8-bit)        |
| 1                | 3 pins (9-bit)        |

bit 4 LCD2 Serial Data Direction  
This bit determines the LCD2 serial data direction.  
When this bit = 0, the MSB is first.  
When this bit = 1, the LSB is first.

bit 3-2 LCD2 Serial Data Format bits[1:0]  
These bits determine the LCD2 serial data format. For further information on available serial data formats, see Section 13.5, “Serial Data Format” on page 327.

Table 10-20: LCD2 Serial Data Format Selection

| REG[005Ch] bits 3-2 | LCD2 Serial Data Format |                                     |
|---------------------|-------------------------|-------------------------------------|
|                     | Data Length             | Data Format                         |
| 00                  | 8-bit                   | RGB=3.3.2<br>(1 transfer / pixel)   |
| 01                  |                         | RGB=4.4.4<br>(3 transfer / 2 pixel) |
| 10                  | Reserved                |                                     |
| 11                  |                         |                                     |

bit 1 LCD2 Serial Clock Phase  
This bit specifies the LCD2 serial clock phase. See Table 10-21: “LCD2 Serial Clock Polarity and Phase Selection”.

## Note

For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing” on page 108.

bit 0 LCD2 Serial Clock Polarity  
This bit determines the LCD2 serial clock polarity.

Table 10-21: LCD2 Serial Clock Polarity and Phase Selection

| REG[005Ch] bit 1 | REG[005Ch] bit 0 | Serial Data Output Changes   | Clock Idling Status |
|------------------|------------------|------------------------------|---------------------|
| 0                | 0                | falling edge of Serial Clock | Low                 |
|                  | 1                | rising edge of Serial Clock  | High                |
| 1                | 0                | rising edge of Serial Clock  | Low                 |
|                  | 1                | falling edge of Serial Clock | High                |

**Note**

For details on timing, see Section 7.4.6, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing” on page 108.

| REG[005Eh] LCD2 Parallel Interface Setting Register |                           |                  |                 |     |                                    |   |            |
|-----------------------------------------------------|---------------------------|------------------|-----------------|-----|------------------------------------|---|------------|
| Default = 0000h                                     |                           |                  |                 |     |                                    |   | Read/Write |
| n/a                                                 |                           | LCD2 Pin Control | LCD2 CS Control | n/a |                                    |   |            |
| 15                                                  | 14                        | 13               | 12              | 11  | 10                                 | 9 | 8          |
| LCD2 VSYNC Input Enable                             | LCD2 Parallel Type Select | n/a              |                 |     | LCD2 Parallel Data Format bits 2-0 |   |            |
| 7                                                   | 6                         | 5                | 4               | 3   | 2                                  | 1 | 0          |

bit 13 LCD2 Pin Control  
This bit controls the parallel interface data output buffer for LCD1.  
When this bit = 0 and REG[0056h] bit 13 = 0, FPDAT[17:0] are always output buffers and do not tristate. All other pins are not affected.  
When this bit = 1, FPDAT[17:0] are tristated, except during LCD2 control/display data output when FPDAT[17:0] become output buffers. GPIO[2:1], which are used to read 2-bits of data from the LCD2 panel, are forced to inputs.

bit 12 LCD2 CS Control  
**This bit is only valid when LCD2 Pin Control is enabled (REG[005Eh] bit 13 = 1).**  
When this bit = 0, the LCD2 chip select signal from the FPCS2 is automatically generated by the S1D13715.  
When this bit = 1, the LCD1 chip select signal, output on FPCS1#, is derived from a logical AND of the original signal and GPIO0 (REG[030Ch] bit 0). GPIO0 is forced to an output.

**Note**

The panel read signal must be generated by a GPIO (i.e. GPIO3). Read data must be input from GPIO[2:1].

bit 7 LCD2 VSYNC Input Enable  
 This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN2). When a manual transfer has been initiated, the LCD1 data output will occur on the next falling edge of FPVIN1.  
 When this bit = 1, the LCD2 data output is synchronous with an external VSYNC input.  
 When this bit = 0, the LCD2 data output is independent of an external VSYNC input.

**Note**

The FPVIN2 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN2 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN2 falling edge.

bit 6 LCD2 Parallel Type Select  
 This bit determines the LCD2 parallel interface type.  
 When this bit = 0, the parallel interface is type 80.  
 When this bit = 1, the parallel interface is type 68.

bits 2-0 LCD2 Parallel Data Format bits[2:0]  
 These bits determine the LCD2 Parallel Data Format. For further information on available parallel data formats, see Section 13.4, “Parallel Data Format” on page 320.

*Table 10-22: LCD2 Parallel Data Format Selection*

| REG[005Eh] bits 2-0 | LCD2 Parallel Data Format |                                  |
|---------------------|---------------------------|----------------------------------|
|                     | Data Bus Width            | Data Format                      |
| 000                 | 8-bit                     | RGB=3.3.2<br>(1 cycle/pixel)     |
| 001                 |                           | RGB=4.4.4<br>(3 cycle / 2 pixel) |
| 011                 |                           | RGB=8.8.8<br>(3 cycle/pixel)     |
| 101                 | 16-bit                    | RGB=4.4.4<br>(1 cycle/pixel)     |
| 110                 |                           | RGB=5.6.5<br>(1 cycle/pixel)     |
| 111                 | 18-bit                    | RGB=6.6.6<br>(1 cycle/pixel)     |
| 010                 | 16-bit                    | RGB=8.8.8<br>(3 cycle/2 pixel)   |
| 100                 | 24-bit                    | RGB=8.8.8<br>(1 cycle/1 pixel)   |

## 10.4.7 Extended Panel Registers

### REG[0070h] is Reserved

This register is Reserved and should not be written.

| REG[0080h] Samsung $\alpha$ -TFT Horizontal Total Register |    |    |    |    |    |  | Read/Write                              |   |
|------------------------------------------------------------|----|----|----|----|----|--|-----------------------------------------|---|
| Default = 0000h                                            |    |    |    |    |    |  |                                         |   |
| n/a                                                        |    |    |    |    |    |  | $\alpha$ -TFT Horizontal Total bits 9-8 |   |
| 15                                                         | 14 | 13 | 12 | 11 | 10 |  | 9                                       | 8 |
| $\alpha$ -TFT Horizontal Total bits 7-0                    |    |    |    |    |    |  |                                         |   |
| 7                                                          | 6  | 5  | 4  | 3  | 2  |  | 1                                       | 0 |

bits 9-0

$\alpha$ -TFT Horizontal Total bits [9:0]

**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000) and have no effect for any other panel type.** These bits specify the Horizontal Total period for Samsung a-TFT panels as follows.

REG[0080] Bits [9:0] =  $\alpha$ -TFT Horizontal Total - 1  
and must have a value greater than 8.

| REG[0082h] Samsung $\alpha$ -TFT LD Rising Edge Register |    |    |    |    |    |  | Read/Write                            |   |
|----------------------------------------------------------|----|----|----|----|----|--|---------------------------------------|---|
| Default = 0000h                                          |    |    |    |    |    |  |                                       |   |
| n/a                                                      |    |    |    |    |    |  | $\alpha$ -TFT LD Rising Edge bits 9-8 |   |
| 15                                                       | 14 | 13 | 12 | 11 | 10 |  | 9                                     | 8 |
| $\alpha$ -TFT LD Rising Edge bits 7-0                    |    |    |    |    |    |  |                                       |   |
| 7                                                        | 6  | 5  | 4  | 3  | 2  |  | 1                                     | 0 |

bits 9-0

$\alpha$ -TFT LD Rising Edge bits [9:0]

**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000) and have no effect for any other panel type.** These bits specify the LD rising edge position from the STH rising edge.

LD Rising Edge Position = (STH Pulse Width + HDP + LD Rising Edge) + 8

| REG[0084h] Samsung $\alpha$ -TFT CKV Toggle Point Register |    |    |    |    |    |                                         |   |
|------------------------------------------------------------|----|----|----|----|----|-----------------------------------------|---|
| Default = 0000h                                            |    |    |    |    |    |                                         |   |
| n/a                                                        |    |    |    |    |    | Read/Write                              |   |
| 15                                                         | 14 | 13 | 12 | 11 | 10 | $\alpha$ -TFT CKV Toggle Point bits 9-8 |   |
|                                                            |    |    |    |    |    | 9                                       | 8 |
| $\alpha$ -TFT CKV Toggle Point bits 7-0                    |    |    |    |    |    |                                         |   |
| 7                                                          | 6  | 5  | 4  | 3  | 2  | 1                                       | 0 |

bits 9-0

$\alpha$ -TFT CKV Toggle Point bits [9:0]

**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000) and have no effect for any other panel type.** These bits specify the CKV toggle point from the STH rising edge.

CKV Toggle Position = (STH Pulse Width + HDP + LD Rising Edge - (CKV Toggle Position to LD Rising Edge period)) + 8

## Note

CKV Toggle Position to LD Rising Edge period is shown in Section 7.4.4, “a-TFT Panel Timing” on page 102.

| REG[0086h] Samsung $\alpha$ -TFT VCOM Toggle Point Register |    |    |    |    |    |                                          |   |
|-------------------------------------------------------------|----|----|----|----|----|------------------------------------------|---|
| Default = 0000h                                             |    |    |    |    |    |                                          |   |
| n/a                                                         |    |    |    |    |    | Read/Write                               |   |
| 15                                                          | 14 | 13 | 12 | 11 | 10 | $\alpha$ -TFT VCOM Toggle Point bits 9-8 |   |
|                                                             |    |    |    |    |    | 9                                        | 8 |
| $\alpha$ -TFT VCOM Toggle Point bits 7-0                    |    |    |    |    |    |                                          |   |
| 7                                                           | 6  | 5  | 4  | 3  | 2  | 1                                        | 0 |

bits 9-0

$\alpha$ -TFT VCOM Toggle Point bits [9:0]

**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000) and have no effect for any other panel type.** These bits specify the VCOM toggle point from the STH rising edge.

VCOM Rising Edge Position = (STH Pulse Width + HDP + LD Rising Edge - (VCOM Toggle Position to LD Rising Edge period)) + 8

## Note

VCOM Toggle Position to LD Rising Edge period is shown in Section 7.4.4, “a-TFT Panel Timing” on page 102.

| REG[0088h] Samsung $\alpha$ -TFT Pulse Width Register |    |    |    |    |    |                                        |   |
|-------------------------------------------------------|----|----|----|----|----|----------------------------------------|---|
| Default = 0000h                                       |    |    |    |    |    |                                        |   |
| n/a                                                   |    |    |    |    |    | Read/Write                             |   |
| 15                                                    | 14 | 13 | 12 | 11 | 10 | $\alpha$ -TFT LD Pulse Width bits 2-0  |   |
|                                                       |    |    |    |    |    | 9                                      | 8 |
| n/a                                                   |    |    |    |    |    | $\alpha$ -TFT STH Pulse Width bits 2-0 |   |
| 7                                                     | 6  | 5  | 4  | 3  | 2  | 1                                      | 0 |

bits 10-8

$\alpha$ -TFT LD Pulse Width bits [2:0]

**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 = 110000) and have no effect for any other panel type.** These bits specify the LD pulse width.

LD Pulse Width = (REG[0088h] bits 10-8) - 1

bits 2-0  $\alpha$ -TFT STH Pulse Width bits [2:0]  
**These bits are for Samsung a-TFT panels only (REG[0032h] bits 15-10 bits 1-0 = 110000) and have no effect for any other panel type.** These bits specify the STH pulse width.  

$$\text{STH Pulse Width} = (\text{REG}[0088\text{h}] \text{ bits 2-0}) - 1$$

### REG[008Ah] through REG[008Eh] are Reserved

These registers are Reserved and should not be written.

| REG[0090h] HR-TFT Configuration Register |    |    |    |    |          |                |          | Read/Write |
|------------------------------------------|----|----|----|----|----------|----------------|----------|------------|
| Default = 0000h                          |    |    |    |    |          |                |          |            |
| n/a                                      |    |    |    |    |          |                |          |            |
| 15                                       | 14 | 13 | 12 | 11 | 10       | 9              | 8        |            |
| n/a                                      |    |    |    |    | Reserved | HR-TFT PS Mode | Reserved |            |
| 7                                        | 6  | 5  | 4  | 3  | 2        | 1              | 0        |            |

bit 2 Reserved  
The default value for this bit is 0.

bit 1 HR-TFT PS Mode  
**This bit is for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and has no effect for any other panel type.** This bit selects the timing used for the PS signal. The alternate PS timings (PS1, PS2, PS3) result in additional power saving on the HR-TFT Panel.  
When this bit = 0, the PS signal uses PS1 timing.  
When this bit = 1, the PS signal uses PS2 timing.

bit 0 Reserved  
The default value for this bit is 0.

| REG[0092h] HR-TFT CLS Width Register |    |    |    |    |    |   |                       | Read/Write |
|--------------------------------------|----|----|----|----|----|---|-----------------------|------------|
| Default = 012Ch                      |    |    |    |    |    |   |                       |            |
| n/a                                  |    |    |    |    |    |   | CLS Pulse Width bit 8 |            |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8                     |            |
| CLS Pulse Width bits 7-0             |    |    |    |    |    |   |                       |            |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0                     |            |

bit 8-0 CLS Pulse Width bits [8:0]  
**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the width of the CLS signal in PCLKs.

#### Note

This register must be programmed such that the following formula is valid.

$$(\text{REG}[0092\text{h}] \text{ bits 8-0}) > 0$$

## REG[0094h] HR-TFT PS1 Rising Edge Register

Default = 0032h

Read/Write

|     |    |    |    |                          |    |   |   |
|-----|----|----|----|--------------------------|----|---|---|
| n/a |    |    |    |                          |    |   |   |
| 15  | 14 | 13 | 12 | 11                       | 10 | 9 | 8 |
| n/a |    |    |    | PS1 Rising Edge bits 5-0 |    |   |   |
| 7   | 6  | 5  | 4  | 3                        | 2  | 1 | 0 |

bit 5-0

PS1 Rising Edge bits [5:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the number of PCLKs between the CLS falling edge and the PS1 rising edge.

## REG[0096h] HR-TFT PS2 Rising Edge Register

Default = 0064h

Read/Write

|                          |    |    |    |    |    |   |   |
|--------------------------|----|----|----|----|----|---|---|
| n/a                      |    |    |    |    |    |   |   |
| 15                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PS2 Rising Edge bits 7-0 |    |    |    |    |    |   |   |
| 7                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 7-0

PS2 Rising Edge bits [7:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the number of PCLKs between the LP falling edge and the first PS2 rising edge.

### Note

This register must be programmed such that the following formula is valid.  
 $(\text{REG}[0096\text{h}] \text{ bits } 7-0) > 0$

## REG[0098h] HR-TFT PS2 Toggle Width Register

Default = 000Ah

Read/Write

|                           |    |    |    |    |    |   |   |
|---------------------------|----|----|----|----|----|---|---|
| n/a                       |    |    |    |    |    |   |   |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PS2 Toggle Width bits 6-0 |    |    |    |    |    |   |   |
| n/a                       | 7  | 6  | 5  | 4  | 3  | 2 | 1 |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 6-0

PS2 Toggle Width bits [6:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the width of the PS2 signal before toggling (in PCLKs).

### Note

This register must be programmed such that the following formula is valid.  
 $(\text{REG}[0098\text{h}] \text{ bits } 6-0) > 0$

| REG[009Ah] HR-TFT PS3 Signal Width Register |                           |    |    |     |    |    |   | Read/Write |
|---------------------------------------------|---------------------------|----|----|-----|----|----|---|------------|
| Default = 0064h                             |                           |    |    |     |    |    |   |            |
| 15                                          | 14                        | 13 | 12 | n/a | 11 | 10 | 9 | 8          |
| n/a                                         | PS3 Signal Width bits 6-0 |    |    |     |    |    |   |            |
| 7                                           | 6                         | 5  | 4  | 3   | 2  | 1  | 0 |            |

bit 6-0

PS3 Signal Width bits [6:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the width of the PS3 signal in PCLKs.

**Note**

This register must be programmed such that the following formula is valid.  
 $(\text{REG}[009\text{Ah}] \text{ bits } 6-0) > 0$

| REG[009Eh] HR-TFT REV Toggle Point Register |                     |    |    |     |    |    |   | Read/Write |
|---------------------------------------------|---------------------|----|----|-----|----|----|---|------------|
| Default = 000Ah                             |                     |    |    |     |    |    |   |            |
| 15                                          | 14                  | 13 | 12 | n/a | 11 | 10 | 9 | 8          |
| n/a                                         | REV Toggle bits 4-0 |    |    |     |    |    |   |            |
| 7                                           | 6                   | 5  | 4  | 3   | 2  | 1  | 0 |            |

bit 4-0

REV Toggle bits [4:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register determines the width in PCLKs to toggle the REV signal prior to the LP rising edge.

$\text{REG}[009\text{E}] \text{ bits}[4:0] = \text{REV toggle position in PCLKs}$

**Note**

This register must be programmed such that the following formula is valid.  
 $(\text{REG}[009\text{Eh}] \text{ bits } 4-0) > 0$

| REG[00A0h] HR-TFT PS1/2 End Register |                    |    |    |     |    |    |   | Read/Write |
|--------------------------------------|--------------------|----|----|-----|----|----|---|------------|
| Default = 0007h                      |                    |    |    |     |    |    |   |            |
| 15                                   | 14                 | 13 | 12 | n/a | 11 | 10 | 9 | 8          |
| n/a                                  | PS1/2 End bits 2-0 |    |    |     |    |    |   |            |
| 7                                    | 6                  | 5  | 4  | 3   | 2  | 1  | 0 |            |

bit 2-0

PS1/2 End bits [2:0]

**These bits are for HR-TFT panels only (REG[0032h] bits 15-10 = 000001) and have no effect for any other panel type.** This register allows the PS signal to continue into the vertical non-display period (in lines).

**Note**

This register must be programmed such that the following formula is valid.  
 $\text{VT} > (\text{REG}[00\text{A}0\text{h}] \text{ bits } 2-0) + \text{VDP} + \text{VPS} + 1$

| REG[00A2h] Type 2 TFT Configuration Register 0 |     |                         |    |    |     |                             | Read/Write |
|------------------------------------------------|-----|-------------------------|----|----|-----|-----------------------------|------------|
| Default = 0000h                                |     |                         |    |    |     |                             |            |
| POL Type                                       | n/a | AP Pulse Width bits 2-0 |    |    | n/a | AP Rising Position bits 1-0 |            |
| 15                                             | 14  | 13                      | 12 | 11 | 10  | 9                           | 8          |
| n/a                                            |     | VCLK Hold bits 1-0      |    |    | n/a | VCLK Setup bits 1-0         |            |
| 7                                              | 6   | 5                       | 4  | 3  | 2   | 1                           | 0          |

bit 15

POL Type

**This bit is for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011) and has no effect for any other panel type.** This bit selects how often the POL signal is toggled. The GPIO2 pin controls the POL signal used for the TFT Type 2 Interface.

When this bit = 0, the POL signal is toggled every line.

When this bit = 1, the POL signal is toggled every frame.

bits 13-11

AP Pulse Width bits [2:0]

**These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011) and have no effect for any other panel type.** These bits specify the AP Pulse Width used for the TFT Type 2 Interface. The GPIO1 pin controls the AP signal for the TFT Type 2 Interface.

Table 10-23: AP Pulse Width

| REG[00A2h] bits 13-11 | AP Pulse Width (in PCLKs) |
|-----------------------|---------------------------|
| 000                   | 20                        |
| 001                   | 40                        |
| 010                   | 80                        |
| 011                   | 120                       |
| 100                   | 150                       |
| 101                   | 190                       |
| 110                   | 240                       |
| 111                   | 270                       |

bits 9-8

AP Rising Position bits [1:0]

**These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011) and have no effect for any other panel type.** These bits specify the TFT Type 2 AC timing parameter from the rising edge of FPLINE (STB) to the rising edge of GPIO1 (AP). The parameter is selected as follows.

Table 10-24: AP Rising Position

| REG[00A2h] bits 9-8 | AP Rising Position (in PCLKs) |
|---------------------|-------------------------------|
| 00                  | 40                            |
| 01                  | 52                            |
| 10                  | 68                            |
| 11                  | 90                            |

bits 4-3

VCLK Hold bits [1:0]

**These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011) and have no effect for any other panel type.** These bits specify the TFT Type 2 AC timing parameter from the rising edge of FPLINE (STB) to the falling edge of GPIO0 (VCLK). The parameter is selected as follows.

Table 10-25: VCLK Hold

| REG[00A2h] bits 4-3 | VCLK Hold (in PCLKs) |
|---------------------|----------------------|
| 00                  | 7                    |
| 01                  | 9                    |
| 10                  | 12                   |
| 11                  | 16                   |

bits 1-0

VCLK Setup bits [1:0]

**These bits are for Type 2 TFT panels only (REG[0032h] bits 15-10 = 000011) and have no effect for any other panel type.** These bits specify the TFT Type 2 AC timing parameter from the rising edge of GPIO0 (VCLK) to the rising edge of FPLINE (STB). The parameter is selected as follows.

Table 10-26: VCLK Setup

| REG[00A2h] bits 1-0 | VCLK Setup (in PCLKs) |
|---------------------|-----------------------|
| 00                  | 7                     |
| 01                  | 9                     |
| 10                  | 12                    |
| 11                  | 16                    |

| REG[00A4h] Casio TFT Timing Register 0 |    |                                                |    |    |    |   |   | Read/Write |  |
|----------------------------------------|----|------------------------------------------------|----|----|----|---|---|------------|--|
| Default = 0E09h                        |    |                                                |    |    |    |   |   |            |  |
| n/a                                    |    | GRES Falling Edge to GPCK Rising Edge bits 5-0 |    |    |    |   |   |            |  |
| 15                                     | 14 | 13                                             | 12 | 11 | 10 | 9 | 8 |            |  |
| n/a                                    |    | GPCK Rising Edge to GRES Rising Edge bits 5-0  |    |    |    |   |   |            |  |
| 7                                      | 6  | 5                                              | 4  | 3  | 2  | 1 | 0 |            |  |

bits 13-8

GRES Falling Edge to GPCK Rising Edge bits[5:0]

**These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010) and have no effect for any other panel type.** These bits determine the number of PCLKs from GRES falling edge to GPCK rising edge.

$$\text{GRES falling edge to GPCK rising edge} = (\text{REG}[00A4h] \text{ bits } 13-8) + 1$$

bits 5-0

GPCK Rising Edge to GRES Rising Edge bits[5:0]

**These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010) and have no effect for any other panel type.** These bits determine the number of PCLKs from GPCK rising edge to GRES rising edge.

## Registers

| REG[00A6h] Casio TFT Timing Register 1 |    |                                                |    |    |    |   |   |
|----------------------------------------|----|------------------------------------------------|----|----|----|---|---|
| Default = 0918h                        |    |                                                |    |    |    |   |   |
| Read/Write                             |    |                                                |    |    |    |   |   |
| n/a                                    |    | GPCK Rising Edge to STH Pulse bits 5-0         |    |    |    |   |   |
| 15                                     | 14 | 13                                             | 12 | 11 | 10 | 9 | 8 |
| n/a                                    |    | GRES Falling Edge to FRP Toggle Point bits 6-0 |    |    |    |   |   |
| 7                                      | 6  | 5                                              | 4  | 3  | 2  | 1 | 0 |

bits 13-8 GPCK Rising Edge to STH Pulse bits[5:0]  
**These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010) and have no effect for any other panel type.** These bits determine the number of PCLKs from GPCK rising edge to STH pulse.

bits 6-0 GRES Falling Edge to FRP Toggle Point bits[6:0]  
**These bits are for Casio TFT panels only (REG[0032h] bits 15-10 = 000010) and have no effect for any other panel type.** These bits determine the number of PCLKs from GRES falling edge to FRP Toggle point.

| REG[00A8h] Type 2 TFT Configuration Register 1 |    |    |    |    |    |   |                            |
|------------------------------------------------|----|----|----|----|----|---|----------------------------|
| Default = 0000h                                |    |    |    |    |    |   |                            |
| Read/Write                                     |    |    |    |    |    |   |                            |
| n/a                                            |    |    |    |    |    |   |                            |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9 | 8                          |
| n/a                                            |    |    |    |    |    |   | Data Compare Invert Enable |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1 | 0                          |

bit 0 Data Compare Invert Enable  
 This bit can be used to lower power consumption for TFT Type 2 Interfaces. The Data Compare and Invert function reduces the amount of data toggled by counting the number of bits that are changed (1 to 0 **or** 0 to 1) from the previous pixel data. If more than half of the bits are changed the data is inverted and the lesser amount of bits are toggled. For all other panel interfaces it has no effect.  
 When this bit = 0, the Data Compare and Invert functions are disabled.  
 When this bit = 1, the Data Compare and Invert functions are enabled.

### REG[00AAh] through REG[00ECh] are Reserved

These registers are Reserved and should not be written.

| REG[00EEh] Partial Drive Area0 Start Line Register |                |                |                |           |                                  |                                         | Read/Write |  |
|----------------------------------------------------|----------------|----------------|----------------|-----------|----------------------------------|-----------------------------------------|------------|--|
| Default = 0000h                                    |                |                |                |           |                                  |                                         |            |  |
| Partial Drive Enable<br>15                         | Reserved<br>14 | Reserved<br>13 | Reserved<br>12 | n/a<br>11 | Partial Drive Area0 Enable<br>10 | Partial Drive Area0 Start Line bits 9-8 |            |  |
|                                                    |                |                |                |           |                                  | 9                                       | 8          |  |
| Partial Drive Area0 Start Line bits 7-0            |                |                |                |           |                                  |                                         |            |  |
| 7                                                  | 6              | 5              | 4              | 3         | 2                                | 1                                       | 0          |  |

- bit 15 Partial Drive Enable  
When this bit = 0, normal mode is enabled (partial drive is disabled).  
When this bit = 1, a Partial Drive cycle starts from the next frame.
- bit 14 Reserved  
The default value for this bit is 0.
- bit 13 Reserved  
The default value for this bit is 0.
- bit 12 Reserved  
The default value for this bit is 0.
- bit 10 Partial Drive Area0 Enable  
The Partial Drive Enable bit (REG[00EEh] bit 15) must be set to 1 before Partial Drive Area0 can be enabled.  
When this bit = 1, Partial Drive Area0 is enabled.  
When this bit = 0, Partial Drive Area0 is disabled.
- bits 9-0 Partial Drive Area0 Start Line bits [9:0]  
These bits specify the Partial Drive Area0 Start Line number in 1 line resolution.  
REG[00EEh] bits 9-0 = Partial Drive Start Line in lines

**Note**

Partial Drive Area0 Start Line must be set as smaller than Partial Drive Area1 Start Line Address.

**Note**

These bits must be programmed such that the following formulas are valid:

REG[00EEh] bits 9-0 > REG[004Eh] bits 9-0

REG[00EEh] bits 9-0 = Partial Area0/1 Display Start in lines + REG[004Eh]

REG[00EEh] bits 9-0 ≠ REG[0052h] bits 8-0

| REG[00F0h] Partial Drive Area0 End Line Register |    |          |          |     |    |                                       |   |
|--------------------------------------------------|----|----------|----------|-----|----|---------------------------------------|---|
| Default = 0000h                                  |    |          |          |     |    |                                       |   |
| Read/Write                                       |    |          |          |     |    |                                       |   |
| n/a                                              |    | Reserved | Reserved | n/a |    | Partial Drive Area0 End Line bits 9-8 |   |
| 15                                               | 14 | 13       | 12       | 11  | 10 | 9                                     | 8 |
| Partial Drive Area0 End Line bits 7-0            |    |          |          |     |    |                                       |   |
| 7                                                | 6  | 5        | 4        | 3   | 2  | 1                                     | 0 |

- bit 13

Reserved  
The default value for this bit is 0.
- bit 12

Reserved  
The default value for this bit is 0.
- bits 9-0

Partial Drive Area0 End Line bits [9:0]  
These bits specify the Partial Drive Area0 End Line in 1 line resolution.  
REG[00F0h] bits 9-0 = Partial Drive Area0 End Line in lines

**Note**  
The Partial Drive Area0 End Line must be set at least 1 line smaller than the Partial Drive Area1 Start Line Address.

**Note**  
The Partial Drive End Line bits indicate the line at which the partial area will end. For example, to display 30 lines at the beginning of the display, set the Start to 1 and the End to 29.

| REG[00F2h] Partial Drive Area1 Start Line Register |    |    |    |    |                            |                                         |   |
|----------------------------------------------------|----|----|----|----|----------------------------|-----------------------------------------|---|
| Default = 0000h                                    |    |    |    |    |                            |                                         |   |
| Read/Write                                         |    |    |    |    |                            |                                         |   |
| n/a                                                |    |    |    |    | Partial Drive Area1 Enable | Partial Drive Area1 Start Line bits 9-8 |   |
| 15                                                 | 14 | 13 | 12 | 11 | 10                         | 9                                       | 8 |
| Partial Drive Area1 Start Line bits 7-0            |    |    |    |    |                            |                                         |   |
| 7                                                  | 6  | 5  | 4  | 3  | 2                          | 1                                       | 0 |

- bit 10

Partial Drive Area1 Enable  
The Partial Drive Enable bit (REG[00EEh] bit 15) must be set to 1 before Partial Drive Area1 can be enabled.  
When this bit = 1, Partial Drive Area1 is enabled.  
When this bit = 0, Partial Drive Area1 is disabled.

bits 9-0

Partial Drive Area1 Start Line bits [9:0]

These bits specify the Partial Drive Area1 Start Line number in 1 line resolution.

REG[00F2h] bits 9-0 = Partial Drive Start Line in lines

**Note**

The Partial Drive Area1 Start Line must be set at least 1 line larger than the Partial Drive Area0 End Line Address.

**Note**

These bits must be programmed such that the following formulas are valid:

REG[00F2h] bits 9-0 > REG[004Eh] bits 9-0

REG[00F2h] bits 9-0 = Partial Area0/1 Display Start in lines + REG[004Eh]

REG[00F2h] bits 9-0 ≠ REG[0052h] bits 8-0

| REG[00F4h] Partial Drive Area1 End Line Register |    |    |    |    |    |  | Read/Write                            |   |
|--------------------------------------------------|----|----|----|----|----|--|---------------------------------------|---|
| Default = 0000h                                  |    |    |    |    |    |  |                                       |   |
| n/a                                              |    |    |    |    |    |  | Partial Drive Area1 End Line bits 9-8 |   |
| 15                                               | 14 | 13 | 12 | 11 | 10 |  | 9                                     | 8 |
| Partial Drive Area1 End Line bits 7-0            |    |    |    |    |    |  |                                       |   |
| 7                                                | 6  | 5  | 4  | 3  | 2  |  | 1                                     | 0 |

bits 9-0

Partial Drive Area1 End Line bits [9:0]

These bits specify the Partial Drive Area1 End Line number in 1 line resolution.

REG[00F4h] bits 9-0 = Partial Drive Area1 End Line Number in Lines

**Note**

The Partial Drive Area0 End Line must be set at least 3 lines smaller than the Partial Drive Area1 Start Line Address.

**Note**

The Partial Drive End Line bits indicate the line at which the partial area will end. For example, to display 30 lines at the beginning of the display set the Start to 1 and the End to 29.

**REG[00F6h] through REG[00FCh] are Reserved**

These registers are Reserved and should not be written.

| REG[00FEh] LCD Interface ID Register |    |    |    |    |    |   | Read/Write |
|--------------------------------------|----|----|----|----|----|---|------------|
| Default = 0001h                      |    |    |    |    |    |   |            |
| LCD Interface Address ID bits 7-0    |    |    |    |    |    |   |            |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| LCD Interface Data ID bits 7-0       |    |    |    |    |    |   |            |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0          |

- bits 15-8

LCD Interface Address ID bits [7:0]  
These bits, along with REG[0034h] bits 15-8, indicate the address for the serial command interface of the TFT Type 5 panel.
- bits 7-0

LCD Interface Data ID bits [7:0] (default = 01h)  
These bits, along with REG[0034h] bits 7-0, indicate the data for the serial command interface of the TFT Type 5 panel.

**Note**

The serial command interface consists of four bytes of data as follows:

- 1. Identify register address (REG[00FEh] bits 15-8).
- 2. Register address (REG[0034h] bits 15-8).
- 3. Identify register data (REG[00FEh] bits 7-0).
- 4. Register data (REG[0034h] bits 7-0).

REG[00FEh] is written first, then REG[0034h]. The command transfer is started after writing REG[0034h].

## 10.4.8 Camera Interface Setting Register

| REG[0100h] Camera1 Clock Setting Register |    |    |    |                                      |    |   |   | Read/Write |
|-------------------------------------------|----|----|----|--------------------------------------|----|---|---|------------|
| Default = 0000h                           |    |    |    |                                      |    |   |   |            |
| 15                                        | 14 | 13 | 12 | 11                                   | 10 | 9 | 8 |            |
| n/a                                       |    |    |    | Camera1 Clock Divide Select bits 4-0 |    |   |   |            |
| 7                                         | 6  | 5  | 4  | 3                                    | 2  | 1 | 0 |            |

bits 4-0

Camera1 Clock Divide Select bits[4:0]

These bits specify the divide ratio used to generate the Camera1 Clock from the System Clock.

Table 10-27: Camera1 Clock Divide Ratio Selection

| REG[0100h] bits 4-0 | Camera1 Clock Divide Ratio | REG[0100h] bits 4-0 | Camera1 Clock Divide Ratio |
|---------------------|----------------------------|---------------------|----------------------------|
| 00000               | 1:1                        | 10000               | 17:1                       |
| 00001               | 2:1                        | 10001               | 18:1                       |
| 00010               | 3:1                        | 10010               | 19:1                       |
| 00011               | 4:1                        | 10011               | 20:1                       |
| 00100               | 5:1                        | 10100               | 21:1                       |
| 00101               | 6:1                        | 10101               | 22:1                       |
| 00110               | 7:1                        | 10110               | 23:1                       |
| 00111               | 8:1                        | 10111               | 24:1                       |
| 01000               | 9:1                        | 11000               | 25:1                       |
| 01001               | 10:1                       | 11001               | 26:1                       |
| 01010               | 11:1                       | 11010               | 27:1                       |
| 01011               | 12:1                       | 11011               | 28:1                       |
| 01100               | 13:1                       | 11100               | 29:1                       |
| 01101               | 14:1                       | 11101               | 30:1                       |
| 01110               | 15:1                       | 11110               | 31:1                       |
| 01111               | 16:1                       | 11111               | 32:1                       |

| REG[0102h] Camera1 Signal Setting Register |                          |                           |                                         |    |                             |                             | Read/Write                     |
|--------------------------------------------|--------------------------|---------------------------|-----------------------------------------|----|-----------------------------|-----------------------------|--------------------------------|
| Default = 0000h                            |                          |                           |                                         |    |                             |                             |                                |
| 15                                         | 14                       | 13                        | 12                                      | 11 | 10                          | 9                           | 8                              |
| n/a                                        | Camera1 Interface Select | Camera1 Clock Mode Select | Camera1 YUV Data Format Select bits 1-0 |    | Camera1 HSYNC Active Select | Camera1 VSYNC Active Select | Camera1 Valid Input Clock Edge |
| 7                                          | 6                        | 5                         | 4                                       | 3  | 2                           | 1                           | 0                              |

bit 6                      Camera1 Interface Select  
This bit specifies the Camera1 Interface type.  
When this bit = 0, the Camera1 interface is configured for YUV 4:2:2 8-bit.  
When this bit = 1, the Camera1 interface is configured for YUV 4:2:2 16-bit.

bit 5                      Camera1 Clock Mode Select  
This bit determines the source of the clock used to sample incoming YUV data on the Camera1 interface.  
When this bit = 0, the external input clock (CM1CLKIN) from the camera interface is used to sample incoming YUV data (default).  
When this bit = 1, the internally divided system clock is used to sample incoming YUV data.

bits 4-3                      Camera1 YUV Data Format Select bits [1:0]  
These bits specify the YUV data format for the Camera1 interface, in bytes.

*Table 10-28: YUV Data Format Selection*

| REG[0102h] bits 4-3 | YUV Data Format (8-bit format) | YUV Data Format (16-bit format)                |
|---------------------|--------------------------------|------------------------------------------------|
| 00                  | (1st) UYVY (last)              | (1st cam1) U V (last)<br>(1st cam2) Y Y (last) |
| 01                  | (1st) VYUY (last)              | (1st cam1) V U (last)<br>(1st cam2) Y Y (last) |
| 10                  | (1st) YUYV (last)              | (1st cam1) Y Y (last)<br>(1st cam2) U V (last) |
| 11                  | (1st) YVYU (last)              | (1st cam1) Y Y (last)<br>(1st cam2) V U (last) |

bit 2                      Camera1 HSYNC Active Select  
This bit defines HYSNC for the Camera1 interface.  
When this bit = 0, the Camera1 HSYNC (CM1HREF) is active low and CM1HREF high means data is valid.  
When this bit = 1, the Camera1 HSYNC (CM1HREF) is active high and CM1HREF low means data is valid.

bit 1                      Camera1 VSYNC Active Select  
This bit defines VYSNC for the Camera1 interface.  
When this bit = 0, the Camera1 VSYNC (CM1VREF) is active low and CM1VREF high means data is valid.  
When this bit = 1, the Camera1 VSYNC (CM1VREF) is active high and CM1VREF low means data is valid.

bit 0

**Camera1 Valid Input Clock Edge**

This bit determines the edge on which Camera1 data is latched.

When this bit = 0, the S1D13715 latches input data on the rising edge of the clock (CM1CLKIN).

When this bit = 1, S1D13715 latches input data on the falling edge of the clock (CM1CLKIN).

| <b>REG[0104h] Camera2 Clock Divide Select Register</b> |    |    |                                      |    |    |   |   | Read/Write |
|--------------------------------------------------------|----|----|--------------------------------------|----|----|---|---|------------|
| Default = 0000h                                        |    |    |                                      |    |    |   |   |            |
| n/a                                                    |    |    |                                      |    |    |   |   |            |
| 15                                                     | 14 | 13 | 12                                   | 11 | 10 | 9 | 8 |            |
| n/a                                                    |    |    | Camera2 Clock Divide Select bits 4-0 |    |    |   |   |            |
| 7                                                      | 6  | 5  | 4                                    | 3  | 2  | 1 | 0 |            |

bits 4-0

**Camera2 Clock Divide Select bits[4:0]**

These bits specify the divide ratio used to generate the Camera2 Clock from the System Clock.

*Table 10-29: Camera2 Clock Divide Ratio Selection*

| REG[0102h] bits 4-0 | Camera2 Clock Divide Ratio | REG[0102h] bits 4-0 | Camera2 Clock Divide Ratio |
|---------------------|----------------------------|---------------------|----------------------------|
| 00000               | 1:1                        | 10000               | 17:1                       |
| 00001               | 2:1                        | 10001               | 18:1                       |
| 00010               | 3:1                        | 10010               | 19:1                       |
| 00011               | 4:1                        | 10011               | 20:1                       |
| 00100               | 5:1                        | 10100               | 21:1                       |
| 00101               | 6:1                        | 10101               | 22:1                       |
| 00110               | 7:1                        | 10110               | 23:1                       |
| 00111               | 8:1                        | 10111               | 24:1                       |
| 01000               | 9:1                        | 11000               | 25:1                       |
| 01001               | 10:1                       | 11001               | 26:1                       |
| 01010               | 11:1                       | 11010               | 27:1                       |
| 01011               | 12:1                       | 11011               | 28:1                       |
| 01100               | 13:1                       | 11100               | 29:1                       |
| 01101               | 14:1                       | 11101               | 30:1                       |
| 01110               | 15:1                       | 11110               | 31:1                       |
| 01111               | 16:1                       | 11111               | 32:1                       |

| REG[0106h] Camera2 Input Signal Format Select Register |    |                           |                                         |    |                             |                             | Read/Write                     |
|--------------------------------------------------------|----|---------------------------|-----------------------------------------|----|-----------------------------|-----------------------------|--------------------------------|
| Default = 0000h                                        |    |                           |                                         |    |                             |                             |                                |
| 15                                                     | 14 | 13                        | 12                                      | 11 | 10                          | 9                           | 8                              |
| Camera2 Interface Select bits 1-0                      |    | Camera2 Clock Mode Select | Camera2 YUV Data Format Select bits 1-0 |    | Camera2 HSYNC Active Select | Camera2 VSYNC Active Select | Camera2 Valid Input Clock Edge |
| 7                                                      | 6  | 5                         | 4                                       | 3  | 2                           | 1                           | 0                              |

bits 7-6 Camera2 Interface Select bits [1:0]  
These bits specify the Camera2 Interface type.

Table 10-30: YUV Data Format Selection

| REG[0106h] bits 7-6 | YUV Format           |
|---------------------|----------------------|
| 00                  | Camera Interface     |
| 01                  | MPEG Codec Interface |
| 10                  | Reserved             |
| 11                  | Reserved             |

bit 5 Camera2 Clock Mode Select  
This bit determines the source of the clock used to sample incoming YUV data on the Camera2 interface.  
When this bit = 0, the external input clock from the camera interface is used to sample incoming YUV data (default).  
When this bit = 1, the internally divided system clock (CM2CLKIN) is used to sample incoming YUV data.

bits 4-3 Camera2 YUV Data Format Select bits[1:0]  
These bits specify the YUV data format for the Camera2 interface, in bytes.

Table 10-31: YUV Data Format Selection

| REG[0106h] bits 4-3 | YUV Format        |
|---------------------|-------------------|
| 00                  | (1st) UYVY (last) |
| 01                  | (1st) VYUY (last) |
| 10                  | (1st) YUYV (last) |
| 11                  | (1st) YVYU (last) |

bit 2 Camera2 HSYNC Active Select  
This bit defines HYSNC for the Camera2 interface.  
When this bit = 0, the Camera2 HSYNC (CM2HREF) is active low and CM2HREF high means data is valid.  
When this bit = 1, the Camera2 HSYNC (CM2HREF) is active high and CM2HREF low means data is valid.

bit 1 Camera2 VSYNC Active Select  
This bit defines VYSNC for the Camera2 interface.  
When this bit = 0, the Camera2 VSYNC (CM2VREF) is active low and CM2VREF high means data is valid.  
When this bit = 1, the Camera2 VSYNC (CM2VREF) is active high and CM2VREF low means data is valid.

bit 0                      Camera2 Valid Input Clock Edge  
 This bit determines the edge on which Camera2 data is latched.  
 When this bit = 0, the S1D13715 latches input data on the rising edge of the clock (CM2CLKIN).  
 When this bit = 1, S1D13715 latches input data on the falling edge of the clock (CM2CLKIN).

### REG[0108h] through REG[010Eh] are Reserved

These registers are Reserved and should not be written.

| REG[0110h] Camera Mode Setting Register |                             |                                  |                                  |                                   |    |          | Read/Write             |
|-----------------------------------------|-----------------------------|----------------------------------|----------------------------------|-----------------------------------|----|----------|------------------------|
| Default = 0000h                         |                             |                                  |                                  |                                   |    |          |                        |
| Reserved                                | n/a                         | Camera2 Active Pull-down Disable | Camera1 Active Pull-down Disable | n/a                               |    | Reserved | YUV Data Offset Enable |
| 15                                      | 14                          | 13                               | 12                               | 11                                | 10 | 9        | 8                      |
| ITU-R BT656 Enable                      | Camera Mode Select bits 2-0 |                                  |                                  | Clock Output Port Select bits 2-0 |    |          | Camera Module Enable   |
| 7                                       | 6                           | 5                                | 4                                | 3                                 | 2  | 1        | 0                      |

bit 15                      Reserved  
 The default value for this bit is 0.

bit 13                      Camera2 Active Pull-down Disable  
 This bit controls the active pull-down resistors on the Camera2 interface.  
 When this bit = 1, the active pull-down resistors on the Camera2 interface are disabled.  
 When this bit = 0, the active pull-down resistors on the Camera2 interface are enabled.

bit 12                      Camera1 Active Pull-down Disable  
 This bit controls the active pull-down resistors on the Camera1 interface.  
 When this bit = 1, the active pull-down resistors on the Camera1 interface are disabled.  
 When this bit = 0, the active pull-down resistors on the Camera1 interface are enabled.

bit 9                        Reserved  
 The default value for this bit is 0.

bit 8

### YUV Data Offset Enable

This bit determines whether the incoming U and V data from the camera interface is internally offset. Typically, camera modules output in YUV or YCbCr offset format, therefore this bit is cleared or set to 0. If the camera data is intended for viewing after the YUV/RGB Converter (YRC), or encoding through the JPEG codec, the resulting YUV data format should be YUV or YCbCr offset.

When this bit = 0, no offset is applied to the incoming U and V camera (UV values are unmodified).

When this bit = 1, an offset is applied to the incoming U and V camera data, the incoming U and V camera data MSB are inverted.

### Note

For YUV to RGB Converter (YRC) input requirements, see the bit description for REG[0240h] bit 4.

Table 10-32: YUV/YUV Offset Enable

| REG[0110h] bits 8 | YUV Data Offset                                                        | Input Data Range       | Output Data Range      |
|-------------------|------------------------------------------------------------------------|------------------------|------------------------|
| 0                 | No offset is applied                                                   | $0 \leq Y \leq 255$    | Same as Input          |
|                   |                                                                        | $-128 \leq U \leq 127$ |                        |
|                   |                                                                        | $-128 \leq V \leq 127$ |                        |
|                   |                                                                        | $16 \leq Y \leq 235$   |                        |
|                   |                                                                        | $-113 \leq U \leq 112$ |                        |
|                   |                                                                        | $-113 \leq V \leq 112$ |                        |
| 1                 | Camera format:<br>YUV Straight range converted to YUV Offset range     | $0 \leq Y \leq 255$    | $0 \leq Y \leq 255$    |
|                   |                                                                        | $0 \leq U \leq 255$    | $-128 \leq U \leq 127$ |
|                   |                                                                        | $0 \leq V \leq 255$    | $-128 \leq V \leq 127$ |
|                   | Camera format:<br>YCbCr Straight range converted to YCbCr Offset range | $16 \leq Y \leq 235$   | $16 \leq Y \leq 235$   |
|                   |                                                                        | $16 \leq U \leq 240$   | $-113 \leq U \leq 112$ |
|                   |                                                                        | $16 \leq V \leq 240$   | $-113 \leq V \leq 112$ |

bit 7

### ITU-R BT656 Enable

This bit controls the active camera interface type and is valid when the interface type is YUV 4:2:2 8-bit (see REG[0102h] bit 6).

When this bit = 0, the normal camera interface is active. In this mode the HSYNC, VSYNC, clock, and data signals are independent.

When this bit = 1, the ITU-R BT656 camera interface is active. In this mode the HSYNC and VSYNC signals are mixed with the data signals.

bit 6-4 Camera Mode Select bits [2:0]  
These bits select the active camera mode.

*Table 10-33: Camera Mode Selection*

| REG[0110h] bits 6-4 | Active Camera Mode                                                             |
|---------------------|--------------------------------------------------------------------------------|
| 000                 | Camera1 Interface Input is Active                                              |
| 001                 | Camera2 Interface Input is Active                                              |
| 010 (see note)      | Camera1 Interface Input is Active<br>and<br>Camera2 Interface Output is Active |
| 011-111             | Reserved                                                                       |

**Note**

This camera mode must not be selected when any of the following interfaces are selected because the Camera2 data pins are already allocated.

- Camera1 interface is set for 16-bit YUV 4:2:2 (REG[0102h] bit 6 = 1)
- Camera2 interface is set for MPEG Codec Interface (REG[0106h] bits 7-6 = 10)

bit 3-1 Clock Output Select bits [2:0]  
These bits select the active clock output ports.

*Table 10-34: Clock Output Port Selection*

| REG[0110h] bits 3-1 | Active Clock Output Port                            |
|---------------------|-----------------------------------------------------|
| 000                 | Same Active Port as selected by REG[0110h] bits 6-4 |
| 001                 | Camera1 Output Port Active Only                     |
| 010                 | Camera2 Output Port Active Only                     |
| 011                 | Both Camera1 and Camera2 Output Port Active         |
| 100                 | Clock Output Inactive                               |
| 101-111             | Reserved                                            |

bit 0 Camera Module Enable  
This bit controls the camera module.  
When this bit = 1, the camera module and clock output (CM1CLKOUT/CM2CLKOUT) are enabled.  
When this bit = 0, the camera module and clock output (CM1CLKOUT/CM2CLKOUT) are disabled.

| REG[0112h] Camera Frame Setting Register |                                    |                                                     |                                 |    |    |                                         | Read/Write                            |
|------------------------------------------|------------------------------------|-----------------------------------------------------|---------------------------------|----|----|-----------------------------------------|---------------------------------------|
| Default = 0000h                          |                                    |                                                     |                                 |    |    |                                         |                                       |
| n/a                                      |                                    |                                                     |                                 |    |    |                                         |                                       |
| 15                                       | 14                                 | 13                                                  | 12                              | 11 | 10 | 9                                       | 8                                     |
| Camera Frame Capture Interrupt Control   | Camera Single Frame Capture Enable | Camera Frame Capture Interrupt Status Always Active | Frame Sampling Control bits 2-0 |    |    | Camera Frame Capture Interrupt Polarity | Camera Frame Capture Interrupt Enable |
| 7                                        | 6                                  | 5                                                   | 4                               | 3  | 2  | 1                                       | 0                                     |

bit 7

## Camera Frame Capture Interrupt Control

This bit controls when the camera frame capture interrupt is asserted and depends on the setting of the Camera Single Frame Capture Mode bit (REG[0112h] bit 6) as follows.

For continuous frame capture mode (REG[0112h] bit 6 = 0):

When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).

When this bit = 1, the interrupt is generated after a valid frame is captured and the capture is stopped.

For single frame capture mode (REG[0112h] bit 6 = 1):

When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).

When this bit = 1, the interrupt is generated when a valid frame is captured.

## Note

When this bit = 1, the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5) has no effect on camera frame interrupt generation.

bit 6

## Camera Single Frame Capture Enable

This bit controls the camera frame capture mode of the camera interface. This bit **must not** be changed while the camera module is enabled (REG[0110h] bit 0 = 1).

When this bit = 0, frames from the camera interface are continuously captured.

When this bit = 1, the next frame from the camera interface is captured when a camera frame capture start command is issued (REG[0114h] bit 2 = 1). The camera frame capture stops after a single frame is captured.

bit 5

## Camera Frame Capture Interrupt Status Always Active

When Camera Frame Capture Interrupts are enabled (REG[0112h] bit 0 = 1b) this bit enables triggering of the camera frame capture interrupt on all captured camera frames. This bit has no effect if Camera Frame Capture Interrupts are disabled

When this bit = 0, the camera frame capture interrupt flag is only active when the JPEG Start/Stop Control bit is on, REG[098Ah] bit 0 = 1.

When this bit = 1, the camera frame capture interrupt flag is active on all captured camera frames.

bits 4-2

Frame Sampling Control Bits [2:0]

These bits control the camera data sampling rate in frames.

Table 10-35: Frame Sampling Control Selection

| REG[0112h] bits 4-2 | Frame Sampling Mode                   |
|---------------------|---------------------------------------|
| 000                 | Every Frame is sampled                |
| 001                 | 1 Frame is sampled for every 2 Frames |
| 010                 | 1 Frame is sampled for every 3 Frames |
| 011                 | 1 Frame is sampled for every 4 Frames |
| 100                 | 1 Frame is sampled for every 5 Frames |
| 101                 | 1 Frame is sampled for every 6 Frames |
| 110                 | 1 Frame is sampled for every 7 Frames |
| 111                 | Reserved                              |

bit 1

Camera Frame Capture Interrupt Trigger Polarity

This bit controls the assertion timing of the camera frame capture interrupt.

When this bit = 0, the Camera Frame Capture Interrupt is asserted when VSYNC is active.

When this bit = 1, the Camera Frame Capture Interrupt is asserted when VSYNC is inactive.

bit 0

Camera Frame Capture Interrupt Enable

This bit controls whether a camera frame capture interrupt is generated or not.

When this bit = 0, the camera frame capture interrupt is disabled.

When this bit = 1, the camera frame capture interrupt is enabled.

| REG[0114h] Camera Control Register |    |    |    |                              |                               | Write Only                                        |                                   |
|------------------------------------|----|----|----|------------------------------|-------------------------------|---------------------------------------------------|-----------------------------------|
| Default = 0000h                    |    |    |    |                              |                               |                                                   |                                   |
| n/a                                |    |    |    |                              |                               | ITU-R BT656<br>Error Flag 1 Clear                 | ITU-R BT656<br>Error Flag 0 Clear |
| 15                                 | 14 | 13 | 12 | 11                           | 10                            | 9                                                 | 8                                 |
| n/a                                |    |    |    | Camera Frame<br>Capture Stop | Camera Frame<br>Capture Start | Camera Frame<br>Capture Interrupt<br>Status Clear | Camera Module<br>Software Reset   |
| 7                                  | 6  | 5  | 4  | 3                            | 2                             | 1                                                 | 0                                 |

bit 9

ITU-R BT656 Error Flag 1 Clear (Write Only)

**This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).**

Writing a 1 to this bit clears the ITU-R BT656 Error Flag 1 (REG[0116h] bit 9).

Writing a 0 to this bit has no hardware effect.

bit 8

ITU-R BT656 Error Flag 0 Clear (Write Only)

**This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).**

Writing a 1 to this bit clears the ITU-R BT656 Error Flag 0 (REG[0116h] bit 8).

Writing a 0 to this bit has no hardware effect.

bit 3

Camera Frame Capture Stop (Write Only)

This bit stops image frame capturing from the camera interface.

Writing a 1 to this bit stops image frame capturing.

Writing a 0 to this bit has no hardware effect.

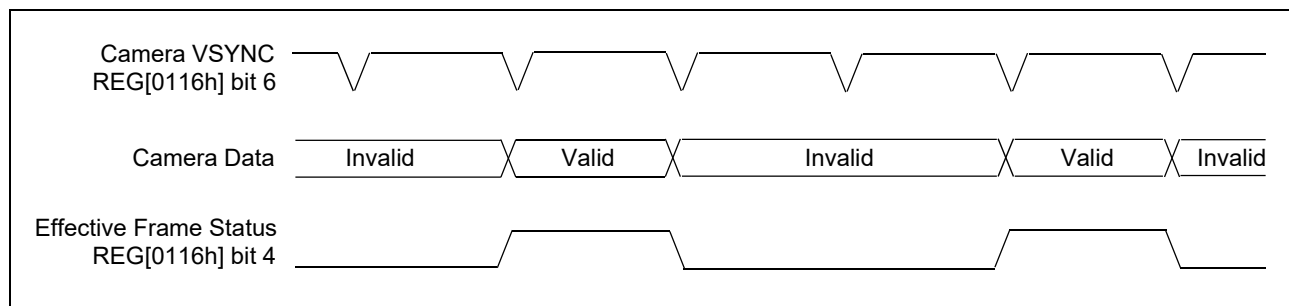
## Registers

- bit 2      Camera Frame Capture Start (Write Only)  
This bit starts image frame capturing from the camera interface.  
Writing a 1 to this bit starts image frame capturing.  
Writing a 0 to this bit has no hardware effect.
- bit 1      Camera Frame Capture Interrupt Status Clear (Write Only)  
This bit clears the Camera Frame Capture Interrupt Status bit (REG[0116h] bit 1).  
Writing a 1 to this bit clears the Camera Frame Capture Interrupt Status.  
Writing a 0 to this bit has no hardware effect.
- bit 0      Camera Module Software Reset (Write Only)  
This bit initializes the camera module logic. Camera interface registers are not affected.  
Writing a 1 to this bit initializes the camera module.  
Writing a 0 to this bit has no hardware effect.

| REG[0116h] Camera Status Register |              |                               |                        |                                  |                                      |                                       | Read Only                |
|-----------------------------------|--------------|-------------------------------|------------------------|----------------------------------|--------------------------------------|---------------------------------------|--------------------------|
| Default = 0044h                   |              |                               |                        |                                  |                                      |                                       |                          |
| n/a                               |              |                               |                        |                                  |                                      | ITU-R BT656 Error Flag 1              | ITU-R BT656 Error Flag 0 |
| 15                                | 14           | 13                            | 12                     | 11                               | 10                                   | 9                                     | 8                        |
| n/a                               | Camera Vsync | Effective Strobe Frame Status | Effective Frame Status | Camera Frame Capture Busy Status | Camera Frame Capture Start/Stop Flag | Camera Frame Capture Interrupt Status | n/a                      |
| 7                                 | 6            | 5                             | 4                      | 3                                | 2                                    | 1                                     | 0                        |

- bit 9      ITU-R BT656 Error Flag 1 (Read Only)  
**This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).**  
When this bit = 1, a 2-bit error is detected on the reference decode operation.  
When this bit = 0, no error has occurred.  
  
To clear this bit, see REG[0114h] bit 9.
- bit 8      ITU-R BT656 Error Flag 0 (Read Only)  
**This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).**  
When this bit = 1, a 1-bit error is detected on the reference decode operation.  
When this bit = 0, no error has occurred.  
  
To clear this bit, see REG[0114h] bit 8.
- bit 6      Camera VSYNC (Read Only)  
This bit indicates the current condition of VSYNC from the camera interface.  
When this bit = 1, VSYNC is currently occurring.  
When this bit = 0, VSYNC is not currently occurring.
- bit 5      Effective Strobe Frame Status (Read Only)  
This bit indicates the status of the valid data captured when the strobe is enabled (REG[0124h] bit 0 = 1). This bit goes high when the valid frame for the strobe pulse is captured. It will only remain high for one frame and then go low.  
This bit returns a 1, when the valid frame for the strobe pulse is captured. It remains high for only one frame and then goes low.  
This bit returns a 0, when there is no valid data.

- bit 4      **Effective Frame Status (Read Only)**  
 This bit indicates whether the current frame from the camera interface is an “effective” frame based on the Frame Sampling Control bits (REG[0112h] bit 4-2).  
 When this bit = 1, an effective frame is occurring.  
 When this bit = 0, an effective frame is not occurring.
- The following diagram shows an example of the Effective Frame Status bit where the Frame Sampling Control bits are set for 1 frame sampled for every 3 frames (REG[0112h] bits 4-2 = 010).



*Figure 10-1: Effective Frame Status Bit Example*

- bit 3      **Camera Frame Capture Busy Status (Read Only)**  
 This bit indicates the status of frame capturing from the camera interface.  
 When this bit = 1, frames are being captured.  
 When this bit = 0, frames are not being captured.
- bit 2      **Camera Frame Capture Start/Stop Flag (Read Only)**  
 This bit indicates the current state of the camera frame capture setting in relation to the setting of the Camera Frame Capture Start/Stop bits (REG[0114h] bits 3-2).  
 When this bit = 1, the camera frame capturing start command has been asserted.  
 When this bit = 0, camera frame capturing has been stopped.
- bit 1      **Camera Frame Capture Interrupt Status (Read Only)**  
 This bit indicates when a Camera Frame Capture Interrupt has taken place. This bit is masked by the Camera Frame Capture Interrupt Enable bit (REG[0112h] bit 0) and cleared using the Camera Frame Capture Interrupt Status Clear bit (REG[0114h] bit 1).  
 When this bit = 1, a camera frame capture interrupt has occurred.  
 When this bit = 0, a camera frame capture interrupt has not occurred.

#### Note

When the Camera Frame Capture Interrupt is enabled (REG[0112h] bit 0 = 1) and the Camera Frame Capture Interrupt Status Always Active is enabled (REG[0112h] bit 5 = 0), the camera frame capture interrupt is only set at the first camera VREF if continuous capture mode is selected (REG[0112h] bit 6 = 0).

#### Note

This bit is set regardless of whether the resizers are enabled. Therefore, the Camera Frame Capture Interrupt Status bit cannot be used as an indication that a camera frame has been written to the embedded memory or the JPEG Codec.

| REG[0120h] Strobe Line Delay Register |    |    |    |    |    |   | Read/Write |
|---------------------------------------|----|----|----|----|----|---|------------|
| Default = 0000h                       |    |    |    |    |    |   |            |
| Strobe Line Delay bits 15-8           |    |    |    |    |    |   |            |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| Strobe Line Delay bits 7-0            |    |    |    |    |    |   |            |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1 | 0          |

bit 15-0

Strobe Line Delay bits [15:0]  
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the delay, in lines of the camera interface, from the first HSYNC input of a camera frame to the beginning of the Strobe Control Signal. For details on the Strobe Control Signal, see Section 20.2, “Strobe Control Signal” on page 396.

| REG[0122h] Strobe Pulse Width Register |    |    |    |    |    |   | Read/Write |
|----------------------------------------|----|----|----|----|----|---|------------|
| Default = 0000h                        |    |    |    |    |    |   |            |
| Strobe Pulse Width bits 15-8           |    |    |    |    |    |   |            |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| Strobe Pulse Width bits 7-0            |    |    |    |    |    |   |            |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0          |

bit 15-0

Strobe Pulse Width bits [15:0]  
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the pulse width of the Strobe Control Signal, in lines of the camera interface. For details on the Strobe Control Signal, see Section 20.2, “Strobe Control Signal” on page 396.

| REG[0124h] Strobe Control Register    |    |    |    |                    |          |                                |               |
|---------------------------------------|----|----|----|--------------------|----------|--------------------------------|---------------|
| Default = 0000h                       |    |    |    |                    |          |                                |               |
| Read/Write                            |    |    |    |                    |          |                                |               |
| n/a                                   |    |    |    |                    |          |                                |               |
| 15                                    | 14 | 13 | 12 | 11                 | 10       | 9                              | 8             |
| Strobe Capture Delay Control bits 3-0 |    |    |    | Strobe Port Enable | Reserved | Strobe Control Signal Polarity | Strobe Enable |
| 7                                     | 6  | 5  | 4  | 3                  | 2        | 1                              | 0             |

bit 7-4

Strobe Capture Delay Control bits [3:0]

When the strobe is enabled (REG[0124h] bit 0 = 1) and continuous frame capture mode is enabled (REG[0112h] bit 6 = 0), these bits specify the delay, in camera frames, from when the strobe signal (GPIO20) is output until camera data is captured by the JPEG encoder. This register has no effect when the strobe is disabled or when single frame capture mode is enabled (REG[0112h] bit 6 = 1).

Table 10-36: Strobe Capture Delay Control

| REG[0124h] bits 7-4 | Delay Value |
|---------------------|-------------|
| 0000                | No Delay    |
| 0001                | 1 Frame     |
| 0010                | 2 Frames    |
| 0011                | 3 Frames    |
| 0100                | 4 Frames    |
| 0101                | 5 Frames    |
| 0110                | 6 Frames    |
| 0111                | 7 Frames    |
| 1000                | 8 Frames    |
| 1001                | 9 Frames    |
| 1010                | 10 Frames   |
| 1011                | 11 Frames   |
| 1100                | 12 Frames   |
| 1101                | 13 Frames   |
| 1110                | 14 Frames   |
| 1111                | 15 Frames   |

bit 3

Strobe Port Enable

When the strobe is enabled (REG[0124h] bit 0 = 1), this bit configures the output port used for the Strobe Control Signal.

When this bit = 1, GPIO20 is used as the output for the Strobe Control Signal.

When this bit = 0, GPIO20 is a normal general purpose IO pin.

bit 2

Reserved

The default value for this bit is 0.

bit 1

Strobe Control Signal Polarity

This bit selects output polarity of the Strobe Control Signal.

When this bit = 1, the strobe control signal is active high.

When this bit = 0, the strobe control signal is active low.

bit 0

### Strobe Enable

This bit controls the Strobe function. This bit must remain enabled for the entire duration of the delay value (REG[0124h] bits 7-4), otherwise the strobe will be disabled immediately when the Strobe Enable bit is set to 0.

When this bit = 1, the strobe function is enabled and a strobe pulse is output on GPIO20 when a JPEG encode is started (REG[098Ah] bit 0 = 1), or when the camera frame capture is stopped (REG[0114h] bit 3 = 1) in continuous capture mode, or when a single frame is captured in single frame capture mode (REG[0112h] bit 6 = 1 and REG[0114h] bit 2 = 1). When this bit = 0, the strobe function is disabled.

Typically the strobe signal controls the external camera flash and is used in conjunction with the camera interface and JPEG encoder to capture or display the optimal camera image after the camera flash has gone off. The strobe function can be used for the following:

- After a JPEG encode has been started, to delay the camera frame from being encoded as specified in REG[0126h] bits 7-4. This is only available in continuous frame capture mode.
- To memory encode the specified delayed camera image and main window image after the continuous frame capture has been stopped.
- To generate a strobe signal every time a camera frame is captured in single frame capture mode.

| REG[0128h] MPEG Interface VSYNC Width register |    |    |    |    |    |                                     |   |
|------------------------------------------------|----|----|----|----|----|-------------------------------------|---|
| Default = 0000h                                |    |    |    |    |    |                                     |   |
| n/a                                            |    |    |    |    |    | MPEG Interface VSYNC Width bits 9-8 |   |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9                                   | 8 |
| MPEG Interface VSYNC Width bits 7-0            |    |    |    |    |    |                                     |   |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1                                   | 0 |

bits 9-0

### MPEG Interface VSYNC Width bits [9:0]

When the MPEG interface is enabled, these bits specify the Vertical Total Period for a MPEG interface chip.

REG[0128h] bits 9-0 = Vertical Total -1

| REG[012Ah] MPEG Interface HSYNC Width register |    |    |    |    |    |                                     |   |
|------------------------------------------------|----|----|----|----|----|-------------------------------------|---|
| Default = 0000h                                |    |    |    |    |    |                                     |   |
| n/a                                            |    |    |    |    |    | MPEG Interface HSYNC Width bits 9-8 |   |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9                                   | 8 |
| MPEG Interface HSYNC Width bits 7-0            |    |    |    |    |    |                                     |   |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1                                   | 0 |

bits 9-0

### MPEG Interface HSYNC Width bits[9:0]

When the MPEG interface is enabled, these bits specify the Horizontal Total Period for MPEG interface chip.

REG[012Ah] bits 9-0 = Horizontal Total -1

**REG[012Ch] through REG[012Fh] are Reserved**

These registers are Reserved and should not be written.

**10.4.9 Display Mode Setting Register**

| <b>REG[0200h] Display Mode Setting Register 0</b> |                                     |                             |                           |                                 |                                      | <b>Read/Write</b>               |   |
|---------------------------------------------------|-------------------------------------|-----------------------------|---------------------------|---------------------------------|--------------------------------------|---------------------------------|---|
| Default = 0000h                                   |                                     |                             |                           |                                 |                                      |                                 |   |
| n/a                                               |                                     | Double Buffer Window Select | Double Buffer Mode Enable | n/a                             | Memory Image JPEG Encode Status (RO) | Display Mode Select bits 1-0    |   |
| 15                                                | 14                                  | 13                          | 12                        | 11                              | 10                                   | 9                               | 8 |
| LCD Software Reset (WO)                           | LCD Memory Image JPEG Encode Enable | LUT2 Bypass Enable          | LUT1 Bypass Enable        | PIP+ Window Bpp Select bits 1-0 |                                      | Main Window Bpp Select bits 1-0 |   |
| 7                                                 | 6                                   | 5                           | 4                         | 3                               | 2                                    | 1                               | 0 |

bit 13 Double Buffer Window Select  
 This bit controls which window (Main or PIP<sup>+</sup>) is affected when Double Buffer Mode is enabled (REG[0200h] bit 12 = 1).  
 When this bit = 1, the Main window area is double buffered.  
 When this bit = 0, the PIP<sup>+</sup> window area is double buffered.

bit 12 Double Buffer Mode Enable  
 This bit controls double buffer mode. When double buffer mode is enabled, the window to be double buffered must be selected using the Double Buffer Window Select bit (REG[0200h] bit 13). The corresponding Main/PIP<sup>+</sup> window area settings, such as the Display Start Address and the Line Address Offset registers, specify the front buffer display start address and line address offset. The back buffer uses the same line address offset as the front buffer, however its display start address is now controlled by the Back Buffer Display Start Address registers (REG[022Ch]-[022Ah]). The following table summarizes the possible address and offset configurations.  
 When this bit = 1, double buffer mode is enabled.  
 When this bit = 0, double buffer mode is disabled.

*Table 10-37: Double Buffer Address Registers*

| Double Buffer Window Select<br>(REG[0200h] bit 13) | Front Buffer       |            | Back Buffer        |            |
|----------------------------------------------------|--------------------|------------|--------------------|------------|
|                                                    | Start Address      | Offset     | Start Address      | Offset     |
| double buffer = Main                               | REG[0212h]-[0210h] | REG[0216h] | REG[022Ch]-[022Ah] | REG[0216h] |
| double buffer = PIP <sup>+</sup>                   | REG[021Ah]-[0218h] | REG[021Eh] | REG[022Ch]-[022Ah] | REG[021Eh] |

Double buffer mode in combination with double buffer write mode (REG[0240h] bit 5 = 1) can be used to enhance the performance of the camera interface, allowing the display to be refreshed from one buffer while the camera interface is writing data to the other buffer.

**Note**

If double buffer mode is enabled, but single buffer write mode is selected (REG[0240h] bit 5 = 0), only the back buffer image is displayed on the selected window (see REG[0200h] bit 13).

bit 10 Memory Image JPEG Encode Status (Read Only)  
 When this bit = 1, the memory image (or display frame) JPEG encode process is in progress.  
 When this bit = 0, the memory image JPEG Encode process has finished or the memory image JPEG encode mode is not enabled.

bit 9-8 Display Mode Select bits[1:0]  
 These bits determine the display mode for either LCD1 or LCD2 depending on the setting of the LCD Output Port Select bits (REG[0202h] bits 12-10).

*Table 10-38: Display Mode Selection*

| REG[0200h] bits 9-8 | Display Mode                                  |
|---------------------|-----------------------------------------------|
| 00                  | Main Window only                              |
| 01                  | Main Window and PIP <sup>+</sup>              |
| 10                  | Reserved                                      |
| 11                  | Main Window and PIP <sup>+</sup> with Overlay |

bit 7 LCD Software Reset (Write Only)  
 When this bit is set to 1, a software reset is performed on the LCD interface.  
 When this bit is set to 0, there is no hardware effect.

bit 6 LCD Memory Image JPEG Encode Enable  
 This bit controls the memory image JPEG encode function which uses the RGB to YUV Converter (RYC). When enabled, a single frame of display data that is sent to the display is also sent to the JPEG encoder. This bit must be cleared and re-enabled for each individual Memory Image JPEG Encode process.

For panels without RAM, data is sent to the JPEG encoder with the first updated frame after the mode is enabled (REG[0200h] bit 6 = 1). For panels with RAM, data is sent to the JPEG encoder using a frame forwarding trigger according to the panel type (i.e. manual transfer using REG[003Ah] bit 0 = 1).

When this bit = 1, LCD memory image JPEG encode is enabled.  
 When this bit = 0, LCD memory image JPEG encode is disabled.

bit 5 LUT2 Bypass Enable  
 LUT2 is associated with the PIP<sup>+</sup> Window. This bit determines if LUT2 is used for output to the PIP<sup>+</sup> Window. For more information on the display format when LUT2 is used or bypassed, see Section 13, “Display Data Formats” on page 316.  
 When this bit = 1, LUT2 is bypassed.  
 When this bit = 0, LUT2 is used.

bit 4 LUT1 Bypass Enable  
 LUT1 is associated with the Main Window. This bit determines if LUT1 is used for output to the Main Window. For more information on the display format when LUT1 is used or bypassed, see Section 13, “Display Data Formats” on page 316.  
 When this bit = 1, LUT1 is bypassed.  
 When this bit = 0, LUT1 is used.

bit 3-2

PIP+ Window Bits-per-pixel Select bits[1:0]

These bits determine the color depth for the PIP+ Window. For more information, see Section 13, “Display Data Formats” on page 316.

Table 10-39: LUT2 (PIP+ Window) Color Mode Selection

| REG[0200h] bits 3-2 | Color Depth | LUT2 Bypass Enable | Color                                                                                                                                                        |
|---------------------|-------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00                  | 8 bpp       | 0                  | LUT2 color format                                                                                                                                            |
|                     |             | 1                  | Data is handled as follows:<br>R_data={r2, r1, r0, r2, r2, r2, r2, r2}<br>G_data={g2, g1, g0, g2, g2, g2, g2, g2}<br>B_data={b1, b0, b1, b1, b1, b1, b1, b1} |
| 01                  | 16 bpp      | 0                  | LUT2 color format                                                                                                                                            |
|                     |             | 1                  | Data is handled as follows:<br>R_data={r4, r3, r2, r1, r0, r4, r4, r4}<br>G_data={g5, g4, g3, g2, g1, g0, g5, g5}<br>B_data={b4, b3, b2, b1, b0, b4, b4, b4} |
| 10                  | Reserved    | 0                  | Reserved                                                                                                                                                     |
|                     |             | 1                  |                                                                                                                                                              |
| 11                  | 32 bpp      | 0                  | Reserved                                                                                                                                                     |
|                     |             | 1                  | Same as Input Data Format                                                                                                                                    |

bit 1-0

Main Window Bits-per-pixel Select bits[1:0]

These bits determine the color depth for the Main Window. For more information, see Section 13, “Display Data Formats” on page 316.

Table 10-40: LUT1 (Main Window) Color Mode Selection

| REG[0200h] bits 1-0 | Color Depth | LUT1 Bypass Enable | Color                                                                                                                                                        |
|---------------------|-------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00                  | 8 bpp       | 0                  | LUT1 color format                                                                                                                                            |
|                     |             | 1                  | Data is handled as follows:<br>R_data={r2, r1, r0, r2, r2, r2, r2, r2}<br>G_data={g2, g1, g0, g2, g2, g2, g2, g2}<br>B_data={b1, b0, b1, b1, b1, b1, b1, b1} |
| 01                  | 16 bpp      | 0                  | LUT1 color format                                                                                                                                            |
|                     |             | 1                  | Data is handled as follows:<br>R_data={r4, r3, r2, r1, r0, r4, r4, r4}<br>G_data={g5, g4, g3, g2, g1, g0, g5, g5}<br>B_data={b4, b3, b2, b1, b0, b4, b4, b4} |
| 10                  | Reserved    | 0                  | Reserved                                                                                                                                                     |
|                     |             | 1                  |                                                                                                                                                              |
| 11                  | 32 bpp      | 0                  | Reserved                                                                                                                                                     |
|                     |             | 1                  | Same as Input Data Format                                                                                                                                    |

| REG[0202h] Display Mode Setting Register 1 |          |                                             |                                 |     |    |                                             | Read/Write    |  |
|--------------------------------------------|----------|---------------------------------------------|---------------------------------|-----|----|---------------------------------------------|---------------|--|
| Default = 0000h                            |          |                                             |                                 |     |    |                                             |               |  |
| Active LCD Port Status bits 2-0 (RO)       |          |                                             | LCD Output Port Select bits 2-0 |     |    | SW Video Invert                             | Display Blank |  |
| 15                                         | 14       | 13                                          | 12                              | 11  | 10 | 9                                           | 8             |  |
| PIP+ Window Mirror Enable                  | Reserved | PIP+ Window SwivelView Mode Select bits 1-0 | Main Window Mirror Enable       | n/a |    | Main Window SwivelView Mode Select bits 1-0 |               |  |
| 7                                          | 6        | 5                                           | 4                               | 3   | 2  | 1                                           | 0             |  |

bits 15-13

Active LCD Port Status bits[2:0] (Read Only)

These bits indicate the selected output port is active. Before sending any commands, parameters, or image data to the port, confirm that the desired port is active.

## Note

These bits are read only and are only changed using the LCD Output Port Select bits 2-0 (REG[0202h] bits 12-10).

Table 10-41: Active LCD Port Status

| REG[0202h] bits 15-13 | Active LCD Port |
|-----------------------|-----------------|
| 000                   | All Off         |
| 001                   | LCD1            |
| 010                   | LCD2            |
| 011 to 111            | Reserved        |

bits 12-10

LCD Output Port Select bits [2:0]

These bits specify the valid output port. Changes to these bits take effect after the end of the current frame. The auto transfer bits (REG[003Ch] bit 0) must be cleared before changing these bits.

Table 10-42: LCD Output Port Selection

| REG[0202h] bits 12-10 | LCD Output Port |
|-----------------------|-----------------|
| 000                   | All Off         |
| 001                   | LCD1            |
| 010                   | LCD2            |
| 011 - 111             | Reserved        |

bit 9

Software Video Invert

This bit determines whether the RGB type panel data output (FPDAT[17:0], GPIO[9:4]) is inverted or left unchanged (normal). This bit has an effect when the display is active and when the display is blanked (see REG[0202h] bit 8). For a summary, see Table 10-43: “LCD Interface Data Output Selection”.

When this bit = 0, the panel data output is left unchanged (normal).

When this bit = 1, the panel data output is inverted.

## Note

If the Software Video Invert bit is set to 1 when configured for an 8-bit parallel panel, the FPDAT[15:8] pins will toggle.

- bit 8**      **Display Blank**  
 This bit blanks the display of RGB Type panels by disabling the display pipe and forcing all data outputs (FPDAT[17:0], GPIO[9:4]) low (or high). For a summary, see Table 10-43: “LCD Interface Data Output Selection”.  
 When this bit = 0, the display is active.  
 When this bit = 1, display is blanked and all data outputs are forced low or high based on the setting of the Software Video Invert bit (REG[0202h] bit 9).

*Table 10-43: LCD Interface Data Output Selection*

| REG[0202h] bit 8 | REG[0202h] bit 9 | LCD Interface Data Output |
|------------------|------------------|---------------------------|
| 0                | 0                | normal                    |
|                  | 1                | inverted                  |
| 1                | 0                | forced low                |
|                  | 1                | forced high               |

**Note**

For further details, see Table 5-12: “LCD Interface Pin Mapping for Mode 1,” on page 46 and Table 5-13: “LCD Interface Pin Mapping for Modes 2/3,” on page 47.

- bit 7**      **PIP<sup>+</sup> Window Mirror Enable**  
 This bit controls the Mirror Display function for the PIP<sup>+</sup> window. Mirror display is independently controlled for the PIP<sup>+</sup> Window and the Main window (see REG[0202h] bit 3).  
 When this bit = 0, mirror display for the PIP<sup>+</sup> window is disabled.  
 When this bit = 1, mirror display for the PIP<sup>+</sup> window is enabled.
- bit 6**      **Reserved**  
 The default value for this bit is 0.
- bit 5-4**      **PIP<sup>+</sup> Window SwivelView Mode Select bits[1:0]**  
 These bits select the SwivelView mode of the PIP<sup>+</sup> window. The SwivelView mode (orientation) of the PIP<sup>+</sup> window is independently controlled for the PIP<sup>+</sup> window and the Main window (see bits 1-0). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 14, “SwivelView™” on page 334.

*Table 10-44: PIP<sup>+</sup> Window SwivelView Mode Selection*

| REG[0202h] bits 5-4 | SwivelView Mode |
|---------------------|-----------------|
| 00                  | 0° (Normal)     |
| 01                  | 90°             |
| 10                  | 180°            |
| 11                  | 270°            |

- bit 3**      **Main Window Mirror Enable**  
 This bit controls the Mirror Display function for the Main Window. Mirror display is independently controlled for the PIP<sup>+</sup> window (bit 7) and the main window.  
 When this bit = 0, mirror display for the main window is disabled.  
 When this bit = 1, mirror display for the main window is enabled.

bits 1-0                      Main Window SwivelView Mode Select bits[1:0]  
These bits select the SwivelView mode of the Main window. The SwivelView mode (orientation) of the Main window is independently controlled for the Main window and the PIP<sup>+</sup> window (see bits 5-4). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 14, “SwivelView™” on page 334.

Table 10-45: Main Window SwivelView Mode Selection

| REG[0202h] bits 1-0 | SwivelView Mode |
|---------------------|-----------------|
| 00                  | 0° (Normal)     |
| 01                  | 90°             |
| 10                  | 180°            |
| 11                  | 270°            |

| REG[0204h] Transparent Overlay Key Color Red Data Register |    |    |    |    |    |   |   | Read/Write |
|------------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                            |    |    |    |    |    |   |   |            |
| n/a                                                        |    |    |    |    |    |   |   |            |
| 15                                                         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Transparent Overlay Key Color Red Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bits 7-0

Transparent Overlay Key Color Red Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the red color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0206h] Transparent Overlay Key Color Green Data Register |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                              |    |    |    |    |    |   |   |            |
| n/a                                                          |    |    |    |    |    |   |   |            |
| 15                                                           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Transparent Overlay Key Color Green Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bits 7-0

Transparent Overlay Key Color Green Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the green color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0208h] Transparent Overlay Key Color Blue Data Register |    |    |    |    |    |   |   | Read/Write |
|-------------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                             |    |    |    |    |    |   |   |            |
| n/a                                                         |    |    |    |    |    |   |   |            |
| 15                                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Transparent Overlay Key Color Blue Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bits 7-0

Transparent Overlay Key Color Blue Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the blue color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0210h] Main Window Display Start Address Register 0 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                         |    |    |    |    |    |   |   |            |
| Main Window Display Start Address bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Main Window Display Start Address bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[0212h] Main Window Display Start Address Register 1 |    |    |    |                                              |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----------------------------------------------|----|---|---|------------|
| Default = 0000h                                         |    |    |    |                                              |    |   |   |            |
| n/a                                                     |    |    |    |                                              |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11                                           | 10 | 9 | 8 |            |
| n/a                                                     |    |    |    | Main Window Display Start Address bits 18-16 |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3                                            | 2  | 1 | 0 |            |

REG[0212h] bits 2-0

REG[0210h] bits 15-0 Main Window Display Start Address bits [18:0]

These bits specify the Main window starting address for the LCD image in the display buffer. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number. At 32 bpp, this register should be incremented by 32-bit steps.

| REG[0214h] Main Window Start Address Status Register |    |    |    |    |    |   |                                  | Read Only |
|------------------------------------------------------|----|----|----|----|----|---|----------------------------------|-----------|
| Default = 0001h                                      |    |    |    |    |    |   |                                  |           |
| n/a                                                  |    |    |    |    |    |   |                                  |           |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8                                |           |
| n/a                                                  |    |    |    |    |    |   | Main Window Start Address Status |           |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0                                |           |

bit 0

Main Window Start Address Status (Read Only)

When Double Buffer Mode is disabled (REG[0200h] bit 12 = 0), this bit indicates the current main window frame status. This bit is updated only after the Main Window Display Start Address has been changed.

When this bit = 1, the current frame is using the latest Main Window Display Start Address values (REG[0210h] - REG[0212h]).

When this bit = 0, the next frame will use the latest Main Window Display Start Address values (REG[0210h] - REG[0212h]).

When Double Buffer Mode is enabled (REG[0200h] bit 12 = 1) and the Main Window is used for the front buffer (REG[0200h] bit 13 = 1), this bit indicates which buffer is currently displayed.

When this bit = 1, the front buffer which corresponds to the Main window area (REG[0210h] - REG[0212h]) is being displayed.

When this bit = 0, the back buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.

| REG[0216h] Main Window Line Address Offset Register |    |                                                  |                                                    |                                           |    |   |   |
|-----------------------------------------------------|----|--------------------------------------------------|----------------------------------------------------|-------------------------------------------|----|---|---|
| Default = 0000h                                     |    |                                                  |                                                    |                                           |    |   |   |
| Read/Write                                          |    |                                                  |                                                    |                                           |    |   |   |
| n/a                                                 |    | Main Window<br>Vertical Pixel<br>Doubling Enable | Main Window<br>Horizontal Pixel<br>Doubling Enable | Main Window Line Address Offset bits 11-8 |    |   |   |
| 15                                                  | 14 | 13                                               | 12                                                 | 11                                        | 10 | 9 | 8 |
| Main Window Line Address Offset bits 7-0            |    |                                                  |                                                    |                                           |    |   |   |
| 7                                                   | 6  | 5                                                | 4                                                  | 3                                         | 2  | 1 | 0 |

bit 13

Main Window Pixel Doubling Vertical Enable

This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubles for a 320 pixel high panel).

When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When this bit = 0, there is no hardware effect.

When vertical pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.

For SwivelView 0°

Address = 0

For SwivelView 90°

Address = (main window height - (bpp/8))

For SwivelView 180°

Address = ((main window height - 1) x (main window width)) - (bpp/8)

For SwivelView 270°

Address = main window line offset x ((main window width ÷ 2) - 1)

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 12    | <p><b>Main Window Pixel Doubling Horizontal Enable</b></p> <p>This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubles for a 320 pixel wide panel)</p> <p>When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.</p> <p>When this bit = 0, there is no hardware effect.</p> <p>When horizontal pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.</p> <p>For SwivelView 0°</p> <p style="padding-left: 20px;">Address = 0</p> <p>For SwivelView 90°</p> <p style="padding-left: 20px;">Address = (main window height - (bpp/8))</p> <p>For SwivelView 180°</p> <p style="padding-left: 20px;">Address = ((main window height - 1) x (main window width)) - (bpp/8)</p> <p>For SwivelView 270°</p> <p style="padding-left: 20px;">Address = main window line offset x ((main window width ÷ 2) - 1)</p> |
| bits 11-0 | <p><b>Main Window Line Address Offset bits [11:0]</b></p> <p>These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the main window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number. At 32 bpp, these bits should be incremented by 32-bit steps.</p> <p>Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).</p> <p style="padding-left: 20px;">REG[0216h] bits 11-0 = Line width in pixels x bpp ÷ 8</p>                                                                                                                                                                                                                                                                                                                |

| REG[0218h] PIP <sup>+</sup> Display Start Address Register 0 |    |    |    |    |    |   |   |
|--------------------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                              |    |    |    |    |    |   |   |
| Read/Write                                                   |    |    |    |    |    |   |   |
| PIP <sup>+</sup> Display Start Address bits 15-8             |    |    |    |    |    |   |   |
| 15                                                           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PIP <sup>+</sup> Display Start Address bits 7-0              |    |    |    |    |    |   |   |
| 7                                                            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

| REG[021Ah] PIP <sup>+</sup> Display Start Address Register 1 |    |    |    |    |                                                   |   |   |
|--------------------------------------------------------------|----|----|----|----|---------------------------------------------------|---|---|
| Default = 0000h                                              |    |    |    |    |                                                   |   |   |
| Read/Write                                                   |    |    |    |    |                                                   |   |   |
| n/a                                                          |    |    |    |    |                                                   |   |   |
| 15                                                           | 14 | 13 | 12 | 11 | 10                                                | 9 | 8 |
| n/a                                                          |    |    |    |    | PIP <sup>+</sup> Display Start Address bits 18-16 |   |   |
| 7                                                            | 6  | 5  | 4  | 3  | 2                                                 | 1 | 0 |

REG[021Ah] bits 2-0

REG[0218h] bits 15-0 PIP<sup>+</sup> Display Start Address bits [18:0]

These bits specify the PIP<sup>+</sup> window starting address for the LCD image in the display buffer. When the PIP<sup>+</sup> function is disabled (REG[0200h] bits 9-8 = 00), this register is ignored. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number. At 32 bpp, this register should be incremented by 32-bit steps.

| REG[021Ch] PIP <sup>+</sup> Window Start Address Status Register |    |    |    |    |    |   |                                              |
|------------------------------------------------------------------|----|----|----|----|----|---|----------------------------------------------|
| Default = 0001h                                                  |    |    |    |    |    |   |                                              |
| Read Only                                                        |    |    |    |    |    |   |                                              |
| n/a                                                              |    |    |    |    |    |   |                                              |
| 15                                                               | 14 | 13 | 12 | 11 | 10 | 9 | 8                                            |
| n/a                                                              |    |    |    |    |    |   | PIP <sup>+</sup> Window Start Address Status |
| 7                                                                | 6  | 5  | 4  | 3  | 2  | 1 | 0                                            |

bit 0

PIP<sup>+</sup> Window Start Address Status (Read Only)

When Double Buffer Mode is disabled (REG[0200h] bit 12 = 0), this bit indicates the current PIP<sup>+</sup> window frame status. This bit is updated only after the PIP<sup>+</sup> Window Display Start Address has been changed.

When this bit = 1, the current frame is using the latest PIP<sup>+</sup> Window Display Start Address values (REG[0218h] - REG[021Ah]).

When this bit = 0, the next frame will use the latest PIP<sup>+</sup> Window Display Start Address values (REG[0218h] - REG[021Ah]).

When Double Buffer Mode is enabled (REG[0200h] bit 12 = 1) and the PIP<sup>+</sup> Window is used for the front buffer (REG[0200h] bit 13 = 0), this bit indicates which buffer is currently displayed.

When this bit = 1, the front buffer which corresponds to the PIP<sup>+</sup> window area (REG[0218h] - REG[021Ah]) is being displayed.

When this bit = 0, the back buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.

| REG[021Eh] PIP <sup>+</sup> Window Line Address Offset Register |    |                                                        |                                                          |                                                       |    |   |   |
|-----------------------------------------------------------------|----|--------------------------------------------------------|----------------------------------------------------------|-------------------------------------------------------|----|---|---|
| Default = 0000h                                                 |    |                                                        |                                                          |                                                       |    |   |   |
| Read/Write                                                      |    |                                                        |                                                          |                                                       |    |   |   |
| n/a                                                             |    | PIP <sup>+</sup> Window Pixel Doubling Vertical Enable | PIP <sup>+</sup> Window Pixel Doubling Horizontal Enable | PIP <sup>+</sup> Window Line Address Offset bits 11-8 |    |   |   |
| 15                                                              | 14 | 13                                                     | 12                                                       | 11                                                    | 10 | 9 | 8 |
| PIP <sup>+</sup> Window Line Address Offset bits 7-0            |    |                                                        |                                                          |                                                       |    |   |   |
| 7                                                               | 6  | 5                                                      | 4                                                        | 3                                                     | 2  | 1 | 0 |

bit 13

**PIP<sup>+</sup> Window Pixel Doubling Vertical Enable**

This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubles for a 320 pixel high panel).

When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When this bit = 0, there is no hardware effect.

When vertical pixel doubling of the PIP<sup>+</sup> window is enabled, the PIP<sup>+</sup> window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.

For SwivelView 0°

$$\text{Address} = 0$$

For SwivelView 90°

$$\text{Address} = (\text{PIP}^+ \text{ window height} - (\text{bpp}/8))$$

For SwivelView 180°

$$\text{Address} = ((\text{PIP}^+ \text{ window height} - 1) \times (\text{PIP}^+ \text{ window width})) - (\text{bpp}/8)$$

For SwivelView 270°

$$\text{Address} = \text{PIP}^+ \text{ window line offset} \times ((\text{PIP}^+ \text{ window width} \div 2) - 1)$$

bit 12

### PIP<sup>+</sup> Window Pixel Doubling Horizontal Enable

This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubles for a 320 pixel wide panel)

When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.

When this bit = 0, there is no hardware effect.

When horizontal pixel doubling of the PIP<sup>+</sup> window is enabled, the PIP<sup>+</sup> window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.

For SwivelView 0°

$$\text{Address} = 0$$

For SwivelView 90°

$$\text{Address} = (\text{PIP}^+ \text{ window height} - (\text{bpp}/8))$$

For SwivelView 180°

$$\text{Address} = ((\text{PIP}^+ \text{ window height} - 1) \times (\text{PIP}^+ \text{ window width})) - (\text{bpp}/8)$$

For SwivelView 270°

$$\text{Address} = \text{PIP}^+ \text{ window line offset} \times ((\text{PIP}^+ \text{ window width} \div 2) - 1)$$

bits 11-0

### PIP<sup>+</sup> Window Line Address Offset bits [11:0]

This register specifies the offset from the beginning of one display line to the beginning of the next display line in the memory of the PIP<sup>+</sup> window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number. At 32 bpp, these bits should be incremented by 32-bit steps.

Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

$$\text{REG}[021\text{Eh}] \text{ bits } 11-0 = \text{Line width in pixels} \times \text{bpp} \div 8$$

### Note

When the camera image is being displayed in the PIP<sup>+</sup> window, the PIP<sup>+</sup> window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

| REG[0220h] PIP <sup>+</sup> X Start Positions Register |    |    |    |    |    |  | Read/Write                                 |   |
|--------------------------------------------------------|----|----|----|----|----|--|--------------------------------------------|---|
| Default = 0000h                                        |    |    |    |    |    |  |                                            |   |
| n/a                                                    |    |    |    |    |    |  | PIP <sup>+</sup> X Start Position bits 9-8 |   |
| 15                                                     | 14 | 13 | 12 | 11 | 10 |  | 9                                          | 8 |
| PIP <sup>+</sup> X Start Position bits 7-0             |    |    |    |    |    |  |                                            |   |
| 7                                                      | 6  | 5  | 4  | 3  | 2  |  | 1                                          | 0 |

bits 9-0

PIP<sup>+</sup> Window X Start Position bits [9:0]

These bits determine the X start position of the PIP<sup>+</sup> window in relation to the origin of the panel (in pixels).

**Note**

When the camera image is being displayed in the PIP<sup>+</sup> window, the PIP<sup>+</sup> window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

| REG[0222h] PIP <sup>+</sup> Y Start Positions Register |    |    |    |    |    |  | Read/Write                                 |   |
|--------------------------------------------------------|----|----|----|----|----|--|--------------------------------------------|---|
| Default = 0000h                                        |    |    |    |    |    |  |                                            |   |
| n/a                                                    |    |    |    |    |    |  | PIP <sup>+</sup> Y Start Position bits 9-8 |   |
| 15                                                     | 14 | 13 | 12 | 11 | 10 |  | 9                                          | 8 |
| PIP <sup>+</sup> Y Start Position bits 7-0             |    |    |    |    |    |  |                                            |   |
| 7                                                      | 6  | 5  | 4  | 3  | 2  |  | 1                                          | 0 |

bits 9-0

PIP<sup>+</sup> Window Y Start Position bits [9:0]

These bits determine the Y start position of the PIP<sup>+</sup> window in relation to the origin of the panel (in pixels).

**Note**

When the camera image is being displayed in the PIP<sup>+</sup> window, the PIP<sup>+</sup> window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

| REG[0224h] PIP <sup>+</sup> X End Positions Register |    |    |    |    |    |                                          |   |
|------------------------------------------------------|----|----|----|----|----|------------------------------------------|---|
| Default = 0000h                                      |    |    |    |    |    |                                          |   |
| n/a                                                  |    |    |    |    |    | Read/Write                               |   |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | PIP <sup>+</sup> X End Position bits 9-8 |   |
|                                                      |    |    |    |    |    | 9                                        | 8 |
| PIP <sup>+</sup> X End Position bits 7-0             |    |    |    |    |    |                                          |   |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1                                        | 0 |

bits 9-0                      PIP<sup>+</sup> Window X End Position bits [9:0]  
These bits determine the X end position of the PIP<sup>+</sup> window in relation to the origin of the panel (in pixels).

**Note**  
These bits must be set such that the following formula is valid.  
REG[0224h] bits 9-0 < Horizontal Display Period

**Note**  
When the camera image is being displayed in the PIP<sup>+</sup> window, the PIP<sup>+</sup> window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

| REG[0226h] PIP <sup>+</sup> Y End Positions Register |    |    |    |    |    |                                          |   |
|------------------------------------------------------|----|----|----|----|----|------------------------------------------|---|
| Default = 0000h                                      |    |    |    |    |    |                                          |   |
| n/a                                                  |    |    |    |    |    | Read/Write                               |   |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | PIP <sup>+</sup> Y End Position bits 9-8 |   |
|                                                      |    |    |    |    |    | 9                                        | 8 |
| PIP <sup>+</sup> Y End Position bits 7-0             |    |    |    |    |    |                                          |   |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1                                        | 0 |

bits 9-0                      PIP<sup>+</sup> Window Y End Position bits [9:0]  
These bits determine the Y end position of the PIP<sup>+</sup> window in relation to the origin of the panel (in pixels).

**Note**  
These bits must be set such that the following formula is valid.  
REG[0226h] bits 9-0 < Vertical Display Period

**Note**  
When the camera image is being displayed in the PIP<sup>+</sup> window, the PIP<sup>+</sup> window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

**REG[0228h] is Reserved**

This register is Reserved and should not be written.

| REG[022Ah] Back Buffer Display Start Address Register 0 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                         |    |    |    |    |    |   |   |            |
| Back Buffer Display Start Address bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Back Buffer Display Start Address bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[022Ch] Back Buffer Display Start Address Register 1 |    |    |    |                                              |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----------------------------------------------|----|---|---|------------|
| Default = 0000h                                         |    |    |    |                                              |    |   |   |            |
| n/a                                                     |    |    |    |                                              |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11                                           | 10 | 9 | 8 |            |
| n/a                                                     |    |    |    | Back Buffer Display Start Address bits 18-16 |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3                                            | 2  | 1 | 0 |            |

REG[022Ch] bits 2-0

REG[022Ah] bits 15-0 Back Buffer Display Start Address bits [18:0]

These bits specify the Back Buffer window starting address for the LCD image in the display buffer. When the Double Buffer function is disabled (REG[0200h] bits 12 = 0), this register is ignored.

| REG[0240h] YUV/RGB Translate Mode Register |                                       |                                  |                            |                                |                                |     |                               | Read/Write |
|--------------------------------------------|---------------------------------------|----------------------------------|----------------------------|--------------------------------|--------------------------------|-----|-------------------------------|------------|
| Default = 0405h                            |                                       |                                  |                            |                                |                                |     |                               |            |
| YUV/RGB Converter Bypass Enable            | YUV/RGB Converter Reset               | UV Fix bits 1-0                  |                            | YRC Output Bpp Select bits 1-0 |                                | n/a | YUV Output Data Format Select |            |
| 15                                         | 14                                    | 13                               | 12                         | 11                             | 10                             | 9   | 8                             |            |
| Reserved                                   | YUV/RGB Rectangular Write Mode Enable | Frame Buffer Writing Mode Select | YUV Input Data Type Select | n/a                            | YUV/RGB Transfer Mode bits 2-0 |     |                               |            |
| 7                                          | 6                                     | 5                                | 4                          | 3                              | 2                              | 1   | 0                             |            |

bit 15

YUV/RGB Converter Bypass Enable

When YUV/RGB Converter (YRC) bypass mode is enabled, YUV data from the camera interface or JPEG decoder, or Host goes directly into the internal memory. When the YRC is enabled (bypass mode is disabled), incoming YUV data is converted to RGB format and stored in the display buffer to be displayed by the LCD panel.

When this bit = 0, YUV/RGB Converter bypass mode is disabled (default).

When this bit = 1, YUV/RGB Converter bypass mode is enabled.

#### Note

The YUV/RGB converter swaps the incoming byte data when it is disabled. To change the YUV data back to normal, set the YRC Output Data Format Select bit (REG[0240h] bit 8) to 1. Disabling the YRC is useful for cameras that can output RGB data.

bit 14

YUV/RGB Converter Reset

This bit resets the YUV/RGB Converter (YRC). It has no effect on the YRC registers. The YRC should be reset after any changes are made to the Resizer Operation registers (REG[0930h]-[096Eh]) and before performing a Memory Image JPEG Encode operation. When this bit is set to 1, the YUV/RGB Converter is reset. This bit must be set back to 0 before the YUV/RGB Converter can be used again.

When this bit is set to 0, the YRC is available for use.

bits 13-12                      UV Fix Select bits [1:0]  
These bits control the UV input to the YUV/RGB Converter (YRC). The setting of these bits has an effect on the UV data even when the YRC is disabled (REG[0240h] bit 15 = 1)..

Table 10-46: UV Fix Selection

| REG[0240h] bits 13-12 | UV Input to the YUV/RGB Converter                           |
|-----------------------|-------------------------------------------------------------|
| 00                    | Original U data, original V data                            |
| 01                    | U data = REG[024Ah] bits 15-8, original V data              |
| 10                    | Original U data, V data = REG[024Ah] bits 7-0               |
| 11                    | U data = REG[024Ah] bits 15-8, V data = REG[024Ah] bits 7-0 |

bits 11-10                      YRC Output Bpp Select bits [1:0]  
These bits specify the color depth in bits-per-pixel (bpp) for the YUV/RGB Converter output.

Table 10-47: YUV/RGB Converter Output Bpp Selection

| REG[0240h] bit 11-10 | YUV/RGB Converter Output Bpp |
|----------------------|------------------------------|
| 00                   | 16 bpp                       |
| 01 (default)         |                              |
| 10                   | Reserved                     |
| 11                   | 32 bpp                       |

bit 8

## YRC Output Data Format Select

This bit selects the output data format of the YUV/RGB Converter (YRC) when it is disabled (REG[0240h] bit 15 = 1). This bit has no effect when the YRC is enabled (REG[0240h] bit 15 = 0).

When this bit = 0, VYUY format is selected. See Table 10-48: “VYUY Output Data Format (REG[0240h] bit 8 = 0),” on page 213.

When this bit = 1, YUYV format is selected. See Table 10-49: “YUYV Output Data Format Select (REG[0240h] bit 8 = 1),” on page 214.

Table 10-48: VYUY Output Data Format (REG[0240h] bit 8 = 0)

| Cycle Count | 1       | 2       | 3       | 4       | ... | 2n+1         | 2n+2       |
|-------------|---------|---------|---------|---------|-----|--------------|------------|
| D15         | $V_0^7$ | $U_0^7$ | $V_2^7$ | $U_2^7$ | ... | $V_{2n}^7$   | $U_{2n}^7$ |
| D14         | $V_0^6$ | $U_0^6$ | $V_2^6$ | $U_2^6$ | ... | $V_{2n}^6$   | $U_{2n}^6$ |
| D13         | $V_0^5$ | $U_0^5$ | $V_2^5$ | $U_2^5$ | ... | $V_{2n}^5$   | $U_{2n}^5$ |
| D12         | $V_0^4$ | $U_0^4$ | $V_2^4$ | $U_2^4$ | ... | $V_{2n}^4$   | $U_{2n}^4$ |
| D11         | $V_0^3$ | $U_0^3$ | $V_2^3$ | $U_2^3$ | ... | $V_{2n}^3$   | $U_{2n}^3$ |
| D10         | $V_0^2$ | $U_0^2$ | $V_2^2$ | $U_2^2$ | ... | $V_{2n}^2$   | $U_{2n}^2$ |
| D9          | $V_0^1$ | $U_0^1$ | $V_2^1$ | $U_2^1$ | ... | $V_{2n}^1$   | $U_{2n}^1$ |
| D8          | $V_0^0$ | $U_0^0$ | $V_2^0$ | $U_2^0$ | ... | $V_{2n}^0$   | $U_{2n}^0$ |
| D7          | $Y_1^7$ | $Y_0^7$ | $Y_3^7$ | $Y_2^7$ | ... | $Y_{2n+1}^7$ | $Y_{2n}^7$ |
| D6          | $Y_1^6$ | $Y_0^6$ | $Y_3^6$ | $Y_2^6$ | ... | $Y_{2n+1}^6$ | $Y_{2n}^6$ |
| D5          | $Y_1^5$ | $Y_0^5$ | $Y_3^5$ | $Y_2^5$ | ... | $Y_{2n+1}^5$ | $Y_{2n}^5$ |
| D4          | $Y_1^4$ | $Y_0^4$ | $Y_3^4$ | $Y_2^4$ | ... | $Y_{2n+1}^4$ | $Y_{2n}^4$ |
| D3          | $Y_1^3$ | $Y_0^3$ | $Y_3^3$ | $Y_2^3$ | ... | $Y_{2n+1}^3$ | $Y_{2n}^3$ |
| D2          | $Y_1^2$ | $Y_0^2$ | $Y_3^2$ | $Y_2^2$ | ... | $Y_{2n+1}^2$ | $Y_{2n}^2$ |
| D1          | $Y_1^1$ | $Y_0^1$ | $Y_3^1$ | $Y_2^1$ | ... | $Y_{2n+1}^1$ | $Y_{2n}^1$ |
| D0          | $Y_1^0$ | $Y_0^0$ | $Y_3^0$ | $Y_2^0$ | ... | $Y_{2n+1}^0$ | $Y_{2n}^0$ |

Table 10-49: YUYV Output Data Format Select (REG[0240h] bit 8 = 1)

| Cycle Count | 1       | 2       | 3       | 4       | ... | 2n+1       | 2n+2         |
|-------------|---------|---------|---------|---------|-----|------------|--------------|
| D15         | $Y_0^7$ | $Y_1^7$ | $Y_2^7$ | $Y_3^7$ | ... | $Y_{2n}^7$ | $Y_{2n+1}^7$ |
| D14         | $Y_0^6$ | $Y_1^6$ | $Y_2^6$ | $Y_3^6$ | ... | $Y_{2n}^6$ | $Y_{2n+1}^6$ |
| D13         | $Y_0^5$ | $Y_1^5$ | $Y_2^5$ | $Y_3^5$ | ... | $Y_{2n}^5$ | $Y_{2n+1}^5$ |
| D12         | $Y_0^4$ | $Y_1^4$ | $Y_2^4$ | $Y_3^4$ | ... | $Y_{2n}^4$ | $Y_{2n+1}^4$ |
| D11         | $Y_0^3$ | $Y_1^3$ | $Y_2^3$ | $Y_3^3$ | ... | $Y_{2n}^3$ | $Y_{2n+1}^3$ |
| D10         | $Y_0^2$ | $Y_1^2$ | $Y_2^2$ | $Y_3^2$ | ... | $Y_{2n}^2$ | $Y_{2n+1}^2$ |
| D9          | $Y_0^1$ | $Y_1^1$ | $Y_2^1$ | $Y_3^1$ | ... | $Y_{2n}^1$ | $Y_{2n+1}^1$ |
| D8          | $Y_0^0$ | $Y_1^0$ | $Y_2^0$ | $Y_3^0$ | ... | $Y_{2n}^0$ | $Y_{2n+1}^0$ |
| D7          | $U_0^7$ | $V_0^7$ | $U_2^7$ | $V_2^7$ | ... | $U_{2n}^7$ | $V_{2n+1}^7$ |
| D6          | $U_0^6$ | $V_0^6$ | $U_2^6$ | $V_2^6$ | ... | $U_{2n}^6$ | $V_{2n+1}^6$ |
| D5          | $U_0^5$ | $V_0^5$ | $U_2^5$ | $V_2^5$ | ... | $U_{2n}^5$ | $V_{2n+1}^5$ |
| D4          | $U_0^4$ | $V_0^4$ | $U_2^4$ | $V_2^4$ | ... | $U_{2n}^4$ | $V_{2n+1}^4$ |
| D3          | $U_0^3$ | $V_0^3$ | $U_2^3$ | $V_2^3$ | ... | $U_{2n}^3$ | $V_{2n+1}^3$ |
| D2          | $U_0^2$ | $V_0^2$ | $U_2^2$ | $V_2^2$ | ... | $U_{2n}^2$ | $V_{2n+1}^2$ |
| D1          | $U_0^1$ | $V_0^1$ | $U_2^1$ | $V_2^1$ | ... | $U_{2n}^1$ | $V_{2n+1}^1$ |
| D0          | $U_0^0$ | $V_0^0$ | $U_2^0$ | $V_2^0$ | ... | $U_{2n}^0$ | $V_{2n+1}^0$ |

bit 7

Reserved

The default value for this bit is 0.

bit 6

YUV/RGB Rectangular Write Mode Enable

When this bit = 0, continuous write mode is selected. In continuous write mode, data is written to the frame buffer continuously based on the YUV/RGB Converter Frame Buffer Write Start Address registers (REG[0242h]-[0244h]).

When this bit = 1, rectangular write mode is selected. In rectangular write mode, data is written based on the X Pixel Size register (REG[024Ch]) and the Frame Buffer Line Address Offset register (REG[024Eh]).

## Note

YUV/RGB Rectangular Write Mode may only be enabled when Single Buffer Writing Mode is selected (REG[0240h] bit 5 = 0).

bit 5

Frame Buffer Writing Mode Select

This bit determines the write mode used by the YRC when writing YUV data to the frame buffer.

When this bit = 0, single buffer write mode is selected. In single buffer write mode, frames of data are written only to the memory section defined by REG[0244h] - REG[0242h].

When this bit = 1, double buffer write mode is selected. In double buffer write mode, frames of data are written alternately between the memory section defined by REG[0244h] - REG[0242h] and the the memory section defined by REG[0248h] - REG[0246h]. This mode can be used with double buffer mode (REG[0200h] bit 12 = 1) to prevent “tearing” of the camera image for fast moving images.

bit 4 YRC Input Data Type Select  
This bit specifies the data type of the YUV input to the YUV to RGB Converter (YRC).

Table 10-50: YUV Data Type Selection

| REG[0240h] bit 4 | YRC Input Data Type | YRC Input Data Range                                                     |
|------------------|---------------------|--------------------------------------------------------------------------|
| 0                | YUV Offset          | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$  |
| 1                | YCbCr Offset        | $16 \leq Y \leq 235$<br>$-113 \leq U \leq 112$<br>$-113 \leq V \leq 112$ |

bits 2-0 YUV/RGB Transfer Mode bits [2:0]  
These bits specify the YUV/RGB Transfer mode. Recommended settings are provided for various specifications..

Table 10-51: YUV/RGB Transfer Mode Selection

| REG[0240h] bits 2-0 | YUV/RGB Specification                                                          |
|---------------------|--------------------------------------------------------------------------------|
| 000                 | Reserved                                                                       |
| 001                 | Recommended for ITU-R BT.709                                                   |
| 010                 | Reserved                                                                       |
| 011                 | Reserved                                                                       |
| 100                 | Recommended for ITU-R BT.470-6 System M                                        |
| 101 (Default)       | Recommended for ITU-R BT.470-6 System B, G<br>(Recommended for ITU-R BT.601-5) |
| 110                 | SMPTE 170M                                                                     |
| 111                 | SMPTE 240M(1987)                                                               |

| REG[0242h] YUV/RGB Converter Write Start Address 0 Register 0 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                               |    |    |    |    |    |   |   |            |
| YUV/RGB Converter Write Start Address 0 bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| YUV/RGB Converter Write Start Address 0 bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[0244h] YUV/RGB Converter Write Start Address 0 Register 1 |    |    |    |    |                                                  |   |   | Read/Write |
|---------------------------------------------------------------|----|----|----|----|--------------------------------------------------|---|---|------------|
| Default = 0000h                                               |    |    |    |    |                                                  |   |   |            |
| n/a                                                           |    |    |    |    |                                                  |   |   |            |
| 15                                                            | 14 | 13 | 12 | 11 | 10                                               | 9 | 8 |            |
| n/a                                                           |    |    |    |    | YUV/RGB Converter Write Start Address bits 18-16 |   |   |            |
| 7                                                             | 6  | 5  | 4  | 3  | 2                                                | 1 | 0 |            |

REG[0244h] bits 2-0  
REG[0242h] bits 15-0 YUV/RGB Converter Write Start Address 0 bits [18:0]  
These bits determine the start address where the YUV/RGB Converter writes data. The YUV/RGB Converter writes data to the display buffer in 32-bit blocks, therefore bits 1-0 of this register must be set to 00.

## Registers

| REG[0246h] YUV/RGB Converter Write Start Address 1 Register 0 |    |    |    |    |    |   |   |
|---------------------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                               |    |    |    |    |    |   |   |
| YUV/RGB Converter Write Start Address 1 bits 15-8             |    |    |    |    |    |   |   |
| 15                                                            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| YUV/RGB Converter Write Start Address 1 bits 7-0              |    |    |    |    |    |   |   |
| 7                                                             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

| REG[0248h] YUV/RGB Converter Write Start Address 1 Register 1 |    |    |    |    |                                                    |   |   |
|---------------------------------------------------------------|----|----|----|----|----------------------------------------------------|---|---|
| Default = 0000h                                               |    |    |    |    |                                                    |   |   |
| n/a                                                           |    |    |    |    |                                                    |   |   |
| 15                                                            | 14 | 13 | 12 | 11 | 10                                                 | 9 | 8 |
| n/a                                                           |    |    |    |    | YUV/RGB Converter Write Start Address 1 bits 18-16 |   |   |
| 7                                                             | 6  | 5  | 4  | 3  | 2                                                  | 1 | 0 |

REG[0248h] bits 2-0

REG[0246h] bits 15-0 YUV/RGB Converter Write Start Address 1 bits [18:0]

These bits determine the start address for data input from the camera interface and for JPEG decoded images. This register value is valid when Frame Buffer Writing Mode Select bit (REG[0240h] bit 5) is set for double buffer writing mode.

| REG[024Ah] UV Data Fix Register |    |    |    |    |    |   |   |
|---------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                 |    |    |    |    |    |   |   |
| U Data Fix bits 7-0             |    |    |    |    |    |   |   |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| V Data Fix bits 7-0             |    |    |    |    |    |   |   |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-8

U Data Fix bits [7:0]

**These bits only have an effect when the UV Fix Select bits are set to 01 or 11 (REG[0240h] bits 13-12 = 01 or 11).** The U Data Input of the YUV/RGB Converter data is fixed to the value of these bits.

bits 7-0

V Data Fix bits [7:0]

**These bits only have an effect when the UV Fix Select bits are set to 10 or 11 (REG[0240h] bits 13-12 = 10 or 11).** The V Data Input of YUV/RGB Converter data is fixed to the value of these bits.

| REG[024Ch] YRC Rectangle Pixel Width Register |                                       |    |    |    |    |   |   |
|-----------------------------------------------|---------------------------------------|----|----|----|----|---|---|
| Default = 0000h                               |                                       |    |    |    |    |   |   |
| n/a                                           | YRC Rectangular Pixel Width bits 10-8 |    |    |    |    |   |   |
| 15                                            | 14                                    | 13 | 12 | 11 | 10 | 9 | 8 |
| YRC Rectangular Pixel Width bits 7-0          |                                       |    |    |    |    |   |   |
| 7                                             | 6                                     | 5  | 4  | 3  | 2  | 1 | 0 |

bits 10-0

YRC Rectangular Pixel Width Bits [10:0]

These bits specify the horizontal pixel size of the data being written when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 6 = 1). For a color depth of 16 bpp, it specifies an even number of pixels (only bits 9-1 are used). For a color depth of 32 bpp, it specifies every pixel (all bits 9-0 are used).

| REG[024Eh] YRC Rectangular Line Address Offset Register |    |    |    |                                               |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|-----------------------------------------------|----|---|---|------------|
| Default = 0000h                                         |    |    |    |                                               |    |   |   |            |
| n/a                                                     |    |    |    | YRC Rectangular Line Address Offset bits 11-8 |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11                                            | 10 | 9 | 8 |            |
| YRC Rectangular Line Address Offset bits 7-0            |    |    |    |                                               |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3                                             | 2  | 1 | 0 |            |

bits 11-0

**YRC Rectangular Line Address Offset Bits [11:0]**

These bits specify the number of pixels from the beginning of the current display line to the beginning of the next line when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 6 = 1).

For a color depth of 16 bpp, it specifies an even number of pixels (only bits 11-1 are used).

For a color depth of 32 bpp, it specifies every pixel (all bits 11-0 are used).

When the YUV/RGB Converter is disabled, it specifies every pixel (all bits 11-0 are used).

| REG[0260h] RGB/YUV Converter Configuration Register |     |          |                             |     |                                |   |   | Read/Write |
|-----------------------------------------------------|-----|----------|-----------------------------|-----|--------------------------------|---|---|------------|
| Default = 0005h                                     |     |          |                             |     |                                |   |   |            |
| RYC Disable                                         | n/a | Reserved |                             | n/a |                                |   |   |            |
| 15                                                  | 14  | 13       | 12                          | 11  | 10                             | 9 | 8 |            |
| n/a                                                 |     |          | RYC Output Data Type Select | n/a | RGB/YUV Transfer Mode bits 2-0 |   |   |            |
| 7                                                   | 6   | 5        | 4                           | 3   | 2                              | 1 | 0 |            |

bit 15

**RGB/YUV Converter (RYC) Disable**

This bit controls the RGB/YUV Converter. The RGB/YUV Converter is used for Memory Image JPEG Encode mode to convert RGB data in the display buffer into YUV data that can be encoded by the JPEG codec.

When this bit = 0, the RGB/YUV Converter is enabled.

When this bit = 1, the RGB/YUV Converter is disabled (bypass mode).

bits 13-12

Reserved

The default value for these bits is 0.

bit 4

**RYC Output Data Type Select**

This bit selects the output YUV data range of the RYC when performing a Memory Image JPEG Encode. It is recommended that this bit always be set to 0.

When this bit = 0, the data type is YUV.

When this bit = 1, the data type is YCbCr

bits 2-0

RGB/YUV Transfer Mode bits [2:0]

These bits specify the RGB/YUV transfer mode. Recommended settings are provided for various specifications..

*Table 10-52: RGB/YUV Transfer Mode Selection*

| <b>REG[0260h] bits 2-0</b> | <b>RGB/YUV Specification</b>                                                   |
|----------------------------|--------------------------------------------------------------------------------|
| 000                        | Reserved                                                                       |
| 001                        | Recommended for ITU-R BT.709                                                   |
| 010                        | Reserved                                                                       |
| 011                        | Reserved                                                                       |
| 100                        | Recommended for ITU-R BT.470-6 System M                                        |
| 101 (Default)              | Recommended for ITU-R BT.470-6 System B, G<br>(Recommended for ITU-R BT.601-5) |
| 110                        | SMPTE 170M                                                                     |
| 111                        | SMPTE 240M(1987)                                                               |

### **REG[0262h] is Reserved**

This register is Reserved and should not be written.

| REG[0264h] Memory Image JPEG Encode Horizontal Display Period Register |    |    |    |    |    |   | Read/Write                                               |
|------------------------------------------------------------------------|----|----|----|----|----|---|----------------------------------------------------------|
| Default = 0000h                                                        |    |    |    |    |    |   |                                                          |
| n/a                                                                    |    |    |    |    |    |   | Memory Image JPEG Encode Horizontal Display Period bit 8 |
| 15                                                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8                                                        |
| Memory Image JPEG Encode Horizontal Display Period bits 7-0            |    |    |    |    |    |   |                                                          |
| 7                                                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0                                                        |

bits 8-0

Memory Image JPEG Encode Horizontal Display Period bits [8:0]

These bits specify the Horizontal Display Period for the Memory Image JPEG Encode (MIJE) function, in 2 pixel resolution.

REG[0264h] bits 8-0 = (MIJE HDP in pixels ÷ 2) - 1

| REG[0266h] Memory Image JPEG Encode Vertical Display Period Register |    |    |    |    |    |   | Read/Write                                                |
|----------------------------------------------------------------------|----|----|----|----|----|---|-----------------------------------------------------------|
| Default = 0000h                                                      |    |    |    |    |    |   |                                                           |
| n/a                                                                  |    |    |    |    |    |   | Memory Image JPEG Encode Vertical Display Period bits 9-8 |
| 15                                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8                                                         |
| Memory Image JPEG Encode Vertical Display Period bits 7-0            |    |    |    |    |    |   |                                                           |
| 7                                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0                                                         |

bits 9-0

Memory Image JPEG Encode Vertical Display Period bits [9:0]

These bits specify the Vertical Display Period for the Memory Image JPEG Encode (MIJE) function, in 1 line resolution.

REG[0266h] bits 9-0 = MIJE VDP in number of lines - 1

### REG[0268h] is Reserved

This register is Reserved and should not be written.

| REG[0270h] Host Image JPEG Encode Control Register |                                            |     |    |                               |                             |     | Read/Write                         |
|----------------------------------------------------|--------------------------------------------|-----|----|-------------------------------|-----------------------------|-----|------------------------------------|
| Default = 0000h                                    |                                            |     |    |                               |                             |     |                                    |
| n/a                                                | Host RGB Encode Write Data Format bits 2-0 |     |    | Host RGB Encode Data End (RO) | Host RGB Encode Status (RO) | n/a |                                    |
| 15                                                 | 14                                         | 13  | 12 | 11                            | 10                          | 9   | 8                                  |
| n/a                                                | Host RGB Encode Mode Enable                | n/a |    |                               |                             |     | Host Image JPEG Encode Mode Select |
| 7                                                  | 6                                          | 5   | 4  | 3                             | 2                           | 1   | 0                                  |

bits 14-12

Host RGB Encode Write Data Format bits [2:0]

These bits select the host image JPEG encode write data format.

- When REG[0270h] bits [14:12] = 000b through 000b or 011b, the data is written to REG[0278h] only.
- When REG[0270h] bits [14:12] = 100b, 101b, 110b or 111b, the data is first written to REG[0278h], then REG[0276h], alternately.

Table 10-53: Host RGB Encode Write Data Format Selection

| REG[0270h] bits 14-12 | Host RGB Encode Write Data Format              |
|-----------------------|------------------------------------------------|
| 000                   | RGB 5:6:5                                      |
| 001                   | Reserved                                       |
| 010                   | RGB 4:4:4                                      |
| 011                   | RGB 3:3:2                                      |
| 100                   | RGB 8:8:8 (32 bit un-packed 1 pixel / 2 cycle) |
| 101                   | RGB 8:8:8 (24 bit packed 2 pixel / 3 cycle)    |
| 110                   | RGB 6:6:6 (32 bit un-packed 1 pixel / 2 cycle) |
| 111                   | RGB 6:6:6 (24 bit packed 2 pixel / 3 cycle)    |

bit 11

Host RGB Encode Data End (Read Only)

This bit indicates when the host image JPEG encode mode for host memory write is not finished.

When this bit = 0, host image JPEG encode mode for host memory write is finished.

When this bit = 1, host image JPEG encode mode for host memory write is not finished.

bit 10

Host RGB Encode Status (RO)

This bit indicates when the host image JPEG encode mode for host memory is active.

When this bit = 0, host image JPEG encode mode for host memory is inactive.

When this bit = 1, host image JPEG encode mode for host memory is active.

bit 6

Host RGB Encode Enable

This bit controls the host image JPEG encode mode for host memory.

When this bit = 0, host image JPEG encode mode for host memory is disabled.

When this bit = 1, host image JPEG encode mode for host memory is enabled.

bit 0                      Host Image JPEG Encode Mode Select  
 This bit selects the Host Image JPEG Encode source between encoding a host image from the S1D13715 memory or encoding a memory image from the host interface.  
 When this bit = 0, encode a host image from the S1D13715 memory.  
 When this bit = 1, encode from the host interface.

| REG[0272h] Host Image JPEG Encode Horizontal Pixel Count Register |    |    |    |                                                         |    |   |   |
|-------------------------------------------------------------------|----|----|----|---------------------------------------------------------|----|---|---|
| Default = 0000h                                                   |    |    |    |                                                         |    |   |   |
| Read/Write                                                        |    |    |    |                                                         |    |   |   |
| n/a                                                               |    |    |    | Host Image JPEG Encode Horizontal Pixel Count bits 10-8 |    |   |   |
| 15                                                                | 14 | 13 | 12 | 11                                                      | 10 | 9 | 8 |
| Host Image JPEG Encode Horizontal Pixel Count bits 7-0            |    |    |    |                                                         |    |   |   |
| 7                                                                 | 6  | 5  | 4  | 3                                                       | 2  | 1 | 0 |

bits 10-0                      Host Image JPEG Encode Horizontal Pixel Count bits [10:0]  
 These bits represent the number of horizontal pixels for the host image JPEG encode.  
 $\text{Horizontal Size} = (\text{Value of this Register}) + 1$   
 The maximum horizontal size that can be encoded is 2048 pixels.

| REG[0274h] Host Image JPEG Encode Vertical Line Count Register |    |    |    |                                                      |    |   |   |
|----------------------------------------------------------------|----|----|----|------------------------------------------------------|----|---|---|
| Default = 0000h                                                |    |    |    |                                                      |    |   |   |
| Read/Write                                                     |    |    |    |                                                      |    |   |   |
| n/a                                                            |    |    |    | Host Image JPEG Encode Vertical Line Count bits 10-8 |    |   |   |
| 15                                                             | 14 | 13 | 12 | 11                                                   | 10 | 9 | 8 |
| Host Image JPEG Encode Vertical Line Count bits 7-0            |    |    |    |                                                      |    |   |   |
| 7                                                              | 6  | 5  | 4  | 3                                                    | 2  | 1 | 0 |

bits 10-0                      Host Image JPEG Encode Vertical Line Count bits [10:0]  
 These bits represent the number of vertical pixels for the host image JPEG encode.  
 $\text{Vertical Size} = (\text{Value of this Register}) + 1$   
 The maximum vertical size that can be encoded is 2048 lines.

## Registers

| REG[0276h] Host Image JPEG Encode RGB Data Register 0 |    |    |    |    |    |   |   | Read/Write |
|-------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                       |    |    |    |    |    |   |   |            |
| Host Image JPEG Encode RGB Data bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Host Image JPEG Encode RGB Data bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[0278h] Host Image JPEG Encode RGB Data Register 1 |    |    |    |    |    |   |   | Read/Write |
|-------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                       |    |    |    |    |    |   |   |            |
| Host Image JPEG Encode RGB Data bits 31-24            |    |    |    |    |    |   |   |            |
| 15                                                    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Host Image JPEG Encode RGB Data bits 23-16            |    |    |    |    |    |   |   |            |
| 7                                                     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[0278h] bits 15-0

REG[0276h] bits 15-0 Host Image JPEG Encode RGB Data bits [31:0]

These bits are the RGB write data for the host image JPEG encode.

Table 10-54: Host Image JPEG Encode Write Data Format

| Host Image JPEG Encode Write Data Format          | Data Register     | Data Register Bits |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |
|---------------------------------------------------|-------------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|
|                                                   |                   | 15                 | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1  | 0  |
| RGB 5:6:5                                         | REG[0276h] Data 1 | Not Used           |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |
|                                                   | REG[0278h] Data 2 | R4                 | R3  | R2  | R1  | R0  | G5  | G4  | G3  | G2  | G1  | G0  | B4  | B3  | B2  | B1 | B0 |
| RGB 4:4:4                                         | REG[0276h] Data 1 | Not Used           |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |
|                                                   | REG[0278h] Data 2 | n/a                | n/a | n/a | n/a | R3  | R2  | R1  | R0  | G3  | G2  | G1  | G0  | B3  | B2  | B1 | B0 |
| RGB 3:3:2                                         | REG[0276h] Data 1 | Not Used           |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |
|                                                   | REG[0278h] Data 2 | R12                | R11 | R10 | G12 | G11 | G10 | B11 | B10 | R2  | R1  | R0  | G2  | G1  | G0  | B1 | B0 |
| RGB 8:8:8<br>(32 bit un-packed 1 pixel / 2 cycle) | REG[0276h] Data 2 | G7                 | G6  | G5  | G4  | G3  | G2  | G1  | G0  | B7  | B6  | B5  | B4  | B3  | B2  | B1 | B0 |
|                                                   | REG[0278h] Data 1 | n/a                | n/a | n/a | n/a | n/a | n/a | n/a | n/a | R7  | R6  | R5  | R4  | R3  | R2  | R1 | R0 |
| RGB 8:8:8<br>(24 bit packed 2 pixel / 3 cycle)    | REG[0276h] Data 1 | G7                 | G6  | G5  | G4  | G3  | G2  | G1  | G0  | B7  | B6  | B5  | B4  | B3  | B2  | B1 | B0 |
|                                                   | REG[0278h] Data 2 | B15                | B14 | B13 | B12 | B11 | B10 | B9  | B8  | R7  | R6  | R5  | R4  | R3  | R2  | R1 | R0 |
|                                                   | REG[0276h] Data 3 | R15                | R14 | R13 | R12 | R11 | R10 | R9  | R8  | G15 | G14 | G13 | G12 | G11 | G10 | G9 | G8 |
| RGB 6:6:6<br>(32 bit un-packed 1 pixel / 2 cycle) | REG[0276h] Data 1 | n/a                | n/a | G5  | G4  | G3  | G2  | G1  | G0  | n/a | n/a | B5  | B4  | B3  | B2  | B1 | B0 |
|                                                   | REG[0278h] Data 2 | n/a                | n/a | n/a | n/a | n/a | n/a | n/a | n/a | n/a | n/a | R5  | R4  | R3  | R2  | R1 | R0 |
| RGB 6:6:6<br>(24 bit packed 2 pixel / 3 cycle)    | REG[0276h] Data 1 | n/a                | n/a | G5  | G4  | G3  | G2  | G1  | G0  | n/a | n/a | B5  | B4  | B3  | B2  | B1 | B0 |
|                                                   | REG[0278h] Data 2 | n/a                | n/a | B13 | B12 | B11 | B10 | B9  | B8  | n/a | n/a | R5  | R4  | R3  | R2  | R1 | R0 |
|                                                   | REG[0276h] Data 3 | n/a                | n/a | R13 | R12 | R11 | R10 | R9  | R8  | n/a | n/a | G13 | G12 | G11 | G10 | G9 | G8 |

### REG[0280h] is Reserved

This register is Reserved and should not be written.

## 10.4.10 GPIO Registers

| REG[0300h] GPIO Status and Control Register 0 |               |               |               |               |               |              |              |
|-----------------------------------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Default = 0000h                               |               |               |               |               |               |              | Read/Write   |
| GPIO15 Config                                 | GPIO14 Config | GPIO13 Config | GPIO12 Config | GPIO11 Config | GPIO10 Config | GPIO9 Config | GPIO8 Config |
| 15                                            | 14            | 13            | 12            | 11            | 10            | 9            | 8            |
| GPIO7 Config                                  | GPIO6 Config  | GPIO5 Config  | GPIO4 Config  | GPIO3 Config  | GPIO2 Config  | GPIO1 Config | GPIO0 Config |
| 7                                             | 6             | 5             | 4             | 3             | 2             | 1            | 0            |

| REG[0302h] GPIO Status and Control Register 1 |    |               |               |               |               |               |               |
|-----------------------------------------------|----|---------------|---------------|---------------|---------------|---------------|---------------|
| Default = 0000h                               |    |               |               |               |               |               | Read/Write    |
| n/a                                           |    |               |               |               |               |               |               |
| 15                                            | 14 | 13            | 12            | 11            | 10            | 9             | 8             |
| n/a                                           |    | GPIO21 Config | GPIO20 Config | GPIO19 Config | GPIO18 Config | GPIO17 Config | GPIO16 Config |
| 7                                             | 6  | 5             | 4             | 3             | 2             | 1             | 0             |

REG[0302h] bits 5-0

REG[0300h] bits 15-0 GPIO[21:0] Pin IO Configuration

When the GPIO pins (GPIO[21:0]) are configured as inputs at RESET# (CNF1 = 1), these bits can be used to change individual GPIO pins between inputs/outputs. When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), these bits are ignored and the GPIO pins are always outputs.

When this bit = 0 (default), the corresponding GPIO pin is configured as an input pin.

When this bit = 1, the corresponding GPIO pin is configured as an output pin.

| REG[0304h] GPIO Status and Control Register 2 |                     |                     |                     |                     |                     |                    |                    |
|-----------------------------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|
| Default = 0000h                               |                     |                     |                     |                     |                     |                    | Read/Write         |
| GPIO15 Input Enable                           | GPIO14 Input Enable | GPIO13 Input Enable | GPIO12 Input Enable | GPIO11 Input Enable | GPIO10 Input Enable | GPIO9 Input Enable | GPIO8 Input Enable |
| 15                                            | 14                  | 13                  | 12                  | 11                  | 10                  | 9                  | 8                  |
| GPIO7 Input Enable                            | GPIO6 Input Enable  | GPIO5 Input Enable  | GPIO4 Input Enable  | GPIO3 Input Enable  | GPIO2 Input Enable  | GPIO1 Input Enable | GPIO0 Input Enable |
| 7                                             | 6                   | 5                   | 4                   | 3                   | 2                   | 1                  | 0                  |

| REG[0306h] GPIO Status and Control Register 3 |    |                     |                     |                     |                     |                     |                     |
|-----------------------------------------------|----|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Default = 0000h                               |    |                     |                     |                     |                     |                     | Read/Write          |
| n/a                                           |    |                     |                     |                     |                     |                     |                     |
| 15                                            | 14 | 13                  | 12                  | 11                  | 10                  | 9                   | 8                   |
| n/a                                           |    | GPIO21 Input Enable | GPIO20 Input Enable | GPIO19 Input Enable | GPIO18 Input Enable | GPIO17 Input Enable | GPIO16 Input Enable |
| 7                                             | 6  | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |

REG[0306h] bits 5-0

REG[0304h] bits 15-0 GPIO[21:0] Pin Input Enable

These bits are used to enable the input function of each GPIO pin. They must be changed to a 1 after power-on reset to enable the input function of the corresponding GPIO pin.

When this bit = 0 (default), the input function for the corresponding GPIO pin is disabled.

When this bit = 1, the input function for the corresponding GPIO pin is enabled.

### Note

When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), the GPIO pins are always outputs and these bits have no effect.

| REG[0308h] GPIO Pull Down Control Register 0 |                          |                          |                          |                          |                          |                         |                         |
|----------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------------|
| Default = FFFFh                              |                          |                          |                          |                          |                          |                         | Read/Write              |
| GPIO15 Pull-down Control                     | GPIO14 Pull-down Control | GPIO13 Pull-down Control | GPIO12 Pull-down Control | GPIO11 Pull-down Control | GPIO10 Pull-down Control | GPIO9 Pull-down Control | GPIO8 Pull-down Control |
| 15                                           | 14                       | 13                       | 12                       | 11                       | 10                       | 9                       | 8                       |
| GPIO7 Pull-down Control                      | GPIO6 Pull-down Control  | GPIO5 Pull-down Control  | GPIO4 Pull-down Control  | GPIO3 Pull-down Control  | GPIO2 Pull-down Control  | GPIO1 Pull-down Control | GPIO0 Pull-down Control |
| 7                                            | 6                        | 5                        | 4                        | 3                        | 2                        | 1                       | 0                       |

| REG[030Ah] GPIO Pull Down Control Register 1 |    |                          |                          |                          |                          |                          |                          |
|----------------------------------------------|----|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Default = 003Fh                              |    |                          |                          |                          |                          |                          | Read/Write               |
| n/a                                          |    |                          |                          |                          |                          |                          |                          |
| 15                                           | 14 | 13                       | 12                       | 11                       | 10                       | 9                        | 8                        |
| n/a                                          |    | GPIO21 Pull-down Control | GPIO20 Pull-down Control | GPIO19 Pull-down Control | GPIO18 Pull-down Control | GPIO17 Pull-down Control | GPIO16 Pull-down Control |
| 7                                            | 6  | 5                        | 4                        | 3                        | 2                        | 1                        | 0                        |

REG[030Ah] bits 5-0

REG[0308h] bits 15-0 GPIO[21:0] Pull-down Control

All GPIO pins have internal pull-down resistors. These bits individually control the state of the pull-down resistors.

When the bit = 1, the pull-down resistor for the associated GPIO pin is active.

When the bit = 0, the pull-down resistor for the associated GPIO pin is inactive.

| REG[030Ch] GPIO Status and Control Register 4 |               |               |               |               |               |              |              |
|-----------------------------------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Default = 0000h                               |               |               |               |               |               |              | Read/Write   |
| GPIO15 Status                                 | GPIO14 Status | GPIO13 Status | GPIO12 Status | GPIO11 Status | GPIO10 Status | GPIO9 Status | GPIO8 Status |
| 15                                            | 14            | 13            | 12            | 11            | 10            | 9            | 8            |
| GPIO7 Status                                  | GPIO6 Status  | GPIO5 Status  | GPIO4 Status  | GPIO3 Status  | GPIO2 Status  | GPIO1 Status | GPIO0 Status |
| 7                                             | 6             | 5             | 4             | 3             | 2             | 1            | 0            |

| REG[030Eh] GPIO Status and Control Register 5 |    |               |               |               |               |               |               |
|-----------------------------------------------|----|---------------|---------------|---------------|---------------|---------------|---------------|
| Default = 0000h                               |    |               |               |               |               |               | Read/Write    |
| n/a                                           |    |               |               |               |               |               |               |
| 15                                            | 14 | 13            | 12            | 11            | 10            | 9             | 8             |
| n/a                                           |    | GPIO21 Status | GPIO20 Status | GPIO19 Status | GPIO18 Status | GPIO17 Status | GPIO16 Status |
| 7                                             | 6  | 5             | 4             | 3             | 2             | 1             | 0             |

REG[030Eh] bits 5-0

REG[030Ch] bits 15-0 GPIO[21:0] Pin IO Status

When GPIOx is configured as an output (see REG[0300h]-REG[0302h]), writing a 1 to this bit drives GPIOx high and writing a 0 to this bit drives GPIOx low.

When GPIOx is configured as an input (see REG[0300h]-REG[0302h]), a read from this bit returns the status of GPIOx.

## Note

To read the status of a GPIO pin configured as an input, the GPIO pin must first have its input function enabled using REG[0304h]-REG[0306h].

### 10.4.11 Overlay Registers

| REG[0310h] Average Overlay Key Color Red Data Register |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                        |    |    |    |    |    |   |   |            |
| n/a                                                    |    |    |    |    |    |   |   |            |
| 15                                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Average Overlay Key Color Red Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0      Average Overlay Key Color Red Data bits [7:0]  
 These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the red color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**  
 If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**  
 If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0312h] Average Overlay Key Color Green Data Register |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                          |    |    |    |    |    |   |   |            |
| n/a                                                      |    |    |    |    |    |   |   |            |
| 15                                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Average Overlay Key Color Green Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

Average Overlay Key Color Green Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the green color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0314h] Average Overlay Key Color Blue Data Register |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                         |    |    |    |    |    |   |   |            |
| n/a                                                     |    |    |    |    |    |   |   |            |
| 15                                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Average Overlay Key Color Blue Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

Average Overlay Key Color Blue Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the blue color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0316h] AND Overlay Key Color Red Data Register |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                    |    |    |    |    |    |   |   |            |
| n/a                                                |    |    |    |    |    |   |   |            |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| AND Overlay Key Color Red Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

AND Overlay Key Color Red Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the red color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0318h] AND Overlay Key Color Green Data Register |    |    |    |    |    |   |   | Read/Write |
|------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                      |    |    |    |    |    |   |   |            |
| n/a                                                  |    |    |    |    |    |   |   |            |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| AND Overlay Key Color Green Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

AND Overlay Key Color Green Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the green color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[031Ah] AND Overlay Key Color Blue Data Register |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                     |    |    |    |    |    |   |   |
| Read/Write                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AND Overlay Key Color Blue Data bits 7-0            |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 7-0

AND Overlay Key Color Blue Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the blue color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[031Ch] OR Overlay Key Color Red Data Register |    |    |    |    |    |   |   |
|---------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                   |    |    |    |    |    |   |   |
| Read/Write                                        |    |    |    |    |    |   |   |
| n/a                                               |    |    |    |    |    |   |   |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OR Overlay Key Color Red Data bits 7-0            |    |    |    |    |    |   |   |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bit 7-0

OR Overlay Key Color Red Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the red color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[031Eh] OR Overlay Key Color Green Data Register |    |    |    |    |    |   |   | Read/Write |
|-----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                     |    |    |    |    |    |   |   |            |
| n/a                                                 |    |    |    |    |    |   |   |            |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| OR Overlay Key Color Green Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

OR Overlay Key Color Green Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the green color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0320h] OR Overlay Key Color Blue Data Register |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                    |    |    |    |    |    |   |   |            |
| n/a                                                |    |    |    |    |    |   |   |            |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| OR Overlay Key Color Blue Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

OR Overlay Key Color Blue Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the blue color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0322h] INV Overlay Key Color Red Data Register |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                    |    |    |    |    |    |   |   |            |
| n/a                                                |    |    |    |    |    |   |   |            |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| INV Overlay Key Color Red Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

INV Overlay Key Color Red Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the red color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0324h] INV Overlay Key Color Green Data Register |    |    |    |    |    |   |   | Read/Write |
|------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                      |    |    |    |    |    |   |   |            |
| n/a                                                  |    |    |    |    |    |   |   |            |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| INV Overlay Key Color Green Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

INV Overlay Key Color Green Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the green color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

## Note

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

## Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0326h] INV Overlay Key Color Blue Data Register |    |    |    |    |    |   |   | Read/Write |
|-----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                     |    |    |    |    |    |   |   |            |
| n/a                                                 |    |    |    |    |    |   |   |            |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| INV Overlay Key Color Blue Data bits 7-0            |    |    |    |    |    |   |   |            |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

bit 7-0

INV Overlay Key Color Blue Data bits [7:0]

These bits only have an effect when PIP<sup>+</sup> with Overlay is enabled (REG[0200h] bits 9-8 = 11). These bits set the blue color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 340.

**Note**

If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319.

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

| REG[0328h] Overlay Miscellaneous Register |     |                               |                              |                             |                              |                                  |                                      | Read/Write |
|-------------------------------------------|-----|-------------------------------|------------------------------|-----------------------------|------------------------------|----------------------------------|--------------------------------------|------------|
| Default = 0000h                           |     |                               |                              |                             |                              |                                  |                                      |            |
| Overlay PIP+ Window Bit Shift             | n/a | Overlay Main Window Bit Shift | n/a                          |                             |                              |                                  |                                      |            |
| 15                                        | 14  | 13                            | 12                           | 11                          | 10                           | 9                                | 8                                    |            |
| n/a                                       |     |                               | INV Overlay Key Color Enable | OR Overlay Key Color Enable | AND Overlay Key Color Enable | Average Overlay Key Color Enable | Transparent Overlay Key Color Enable |            |
| 7                                         | 6   | 5                             | 4                            | 3                           | 2                            | 1                                | 0                                    |            |

bit 15

Overlay PIP<sup>+</sup> Window Bit Shift

This bit only has an effect if the Display Mode Select bits are set for PIP<sup>+</sup> with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.

When this bit = 0, the PIP<sup>+</sup> window pixel data is normal.

When this bit = 1, the PIP<sup>+</sup> window is pixel data is bit shifted to the right by 1 bit.

bits 13

Overlay Main Window Bit Shift

This bit only has an effect if the Display Mode Select bits are set for PIP<sup>+</sup> with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.

When this bit = 0, the main window pixel data is normal.

When this bit = 1, the main window pixel data is bit shifted to the right by 1 bit.

bit 4

### INV Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.

When this bit = 1, the INV overlay key color function is enabled.

When this bit = 0, the INV overlay key color function is disabled.

#### Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 3

### OR Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.

When this bit = 1, the OR overlay key color function is enabled.

When this bit = 0, the OR overlay key color function is disabled.

#### Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 2

### AND Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.

When this bit = 1, the AND overlay key color function is enabled.

When this bit = 0, the AND overlay key color function is disabled.

#### Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn't apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

- 
- bit 1      Average Overlay Key Color Enable  
This bit only has an effect if the Display Mode Select bits are set for PIP<sup>+</sup> with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.  
When this bit = 1, the average overlay key color function is enabled.  
When this bit = 0, the average overlay key color function is disabled.
- Note**  
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.
- bit 0      Transparent Overlay Key Color Enable  
This bit only has an effect if the Display Mode Select bits are set for PIP<sup>+</sup> with Overlay (REG[0200h] bits 9-8 = 11). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 340.  
When this bit = 1, the transparent overlay key color function is enabled.  
When this bit = 0, the transparent overlay key color function is disabled.
- Note**  
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

10.4.12 LUT1 (Main Window)

|       | High Byte | Low Byte |
|-------|-----------|----------|
| 0400h | Green 0   | Red 0    |
| 0402h | n/a       | Blue 0   |
| 0404h | Green 1   | Red 1    |
|       | ⋮         | ⋮        |
| 07FEh | n/a       | Blue 255 |

Figure 10-2: LUT1 Mapping

| REG[0400 - 07FCh] LUT1 Data Register 0 |    |    |    |    |    |   |   |
|----------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable               |    |    |    |    |    |   |   |
| Read/Write                             |    |    |    |    |    |   |   |
| LUT1 Green Data bits 7-0               |    |    |    |    |    |   |   |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LUT1 Red Data bits 7-0                 |    |    |    |    |    |   |   |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

- bits 15-8

LUT1 (Main Window) Green Data bits [7:0]  
These bits are used to set the LUT1 Green Data. There are 256 entries in LUT1 from 0400h to 07FCh. LUT1 is used for the Main Window.
- bits 7-0

LUT1 (Main Window) Red Data bits [7:0]  
These bits are used to set the LUT1 Red Data. There are 256 entries in LUT1 from 0400h to 07FCh. LUT1 is used for the Main Window.

| REG[0402 - 07FEh] LUT1 Data Register 1 |    |    |    |    |    |   |   |
|----------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable               |    |    |    |    |    |   |   |
| Read/Write                             |    |    |    |    |    |   |   |
| n/a                                    |    |    |    |    |    |   |   |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LUT1 Blue Data bits 7-0                |    |    |    |    |    |   |   |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

- bits 7-0

LUT1 (Main Window) Blue Data bits [7:0]  
These bits are used to set the LUT1 Blue Data. There are 256 entries in LUT1 from 0402h to 07FEh. LUT1 is used for the Main Window.

### 10.4.13 LUT2 (PIP<sup>+</sup> Window)

|       | High Byte | Low Byte |
|-------|-----------|----------|
| 0800h | Green 0   | Red 0    |
| 0802h | n/a       | Blue 0   |
| 0804h | Green 1   | Red 1    |
|       | ⋮         | ⋮        |
| 08FEh | n/a       | Blue 63  |

Figure 10-3: LUT2 mapping

| REG[0800 - 08FCh] LUT2 Data Register 0 |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------|----|----|----|----|----|---|---|------------|
| Default = not applicable               |    |    |    |    |    |   |   |            |
| LUT2 Green Data bits 7-0               |    |    |    |    |    |   |   |            |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| LUT2 Red Data bits 7-0                 |    |    |    |    |    |   |   |            |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

- bits 15-8      LUT2 (PIP<sup>+</sup> Window) Green Data bits [7:0]  
 These bits are used to set the LUT2 Green Data. There are 64 entries in LUT2 from 0800h to 08FCh. LUT2 is used for the PIP<sup>+</sup> Window.
- bits 7-0      LUT2 (PIP<sup>+</sup> Window) Red Data bits [7:0]  
 These bits are used to set the LUT2 Red Data. There are 64 entries in LUT2 from 0800h to 08FCh. LUT2 is used for the PIP<sup>+</sup> Window.

| REG[0802 - 08FEh] LUT2 Data Register 1 |    |    |    |    |    |   |   | Read/Write |
|----------------------------------------|----|----|----|----|----|---|---|------------|
| Default = not applicable               |    |    |    |    |    |   |   |            |
| n/a                                    |    |    |    |    |    |   |   |            |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| LUT2 Blue Data bits 7-0                |    |    |    |    |    |   |   |            |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

- bits 7-0      LUT2 (PIP<sup>+</sup> Window) Blue Data bits [7:0]  
 These bits are used to set the LUT2 Blue Data. There are 64 entries in LUT2 from 0802h to 08FEh. LUT2 is used for the PIP<sup>+</sup> Window.

10.4.14 Resizer Operation Registers

**Note**  
The resizer registers must not be changed while receiving data from the camera interface, JPEG decoder, or host interface.

| REG[0930h] Global Resizer Control Register |    |    |                                 |                      |                         |                                 |          | Read/Write |  |
|--------------------------------------------|----|----|---------------------------------|----------------------|-------------------------|---------------------------------|----------|------------|--|
| Default = 0000h                            |    |    |                                 |                      |                         |                                 |          |            |  |
| n/a                                        |    |    |                                 |                      | Resizer Frame Reduction | Reserved                        | Reserved |            |  |
| 15                                         | 14 | 13 | 12                              | 11                   | 10                      | 9                               | 8        |            |  |
| n/a                                        |    |    | Captured Data Input Select (WO) | Output Source Select | n/a                     | Camera Display Control bits 1-0 |          |            |  |
| 7                                          | 6  | 5  | 4                               | 3                    | 2                       | 1                               | 0        |            |  |

- bit 10

Resizer Frame Reduction  
This bit controls frame reduction in the resizer block.  
When this bit = 1, the resizer performs frame reduction by using only every second frame.  
When this bit = 0, the resizer performs no reduction.
- bit 9

Reserved  
The default value for this bit is 0.
- bit 8

Reserved  
The default value for this bit is 0.
- bit 4

Captured Data Input Select (Write Only)  
This bit selects the data input for the capture resizer.  
When this bit = 1, input from the RGB/YUV Converter (RYC) is selected.  
When this bit = 0, input from the camera interface is selected.

bit 3

**Output Source Select**

This bit selects which resizer outputs data to the YUV/RGB Converter (YRC). Typically, the view resizer is selected when data comes from the camera interface since JPEG encode dimensions may differ from display dimensions. For JPEG decode and host to S1D13715 YUV mode, the view resizer must be selected.

When this bit = 0, the view resizer outputs data to the YRC.

When this bit = 1, the capture resizer outputs data to the YRC and the view resizer logic is powered down.

**Note**

During JPEG encoding, this bit must be set to an active resizer, or the YRC must be disabled (REG[0240h] bit 14 = 1).

*Table 10-55: Output Source Select*

| Output Source Select<br>REG[0930h] bit 3 | View Resizer Enable<br>REG[0940h] bit 0 | Capture Resizer Enable<br>REG[0960h] bit 0 | to YUV/RGB<br>Converter | to JPEG Line Buffer |
|------------------------------------------|-----------------------------------------|--------------------------------------------|-------------------------|---------------------|
| 0                                        | 0                                       | 0                                          | —                       | —                   |
| 0                                        | 0                                       | 1                                          | —                       | —                   |
| 0                                        | 1                                       | 0                                          | Available               | —                   |
| 0                                        | 1                                       | 1                                          | Available               | Available           |
| 1                                        | 0                                       | 0                                          | —                       | —                   |
| 1                                        | 0                                       | 1                                          | Available               | Available           |
| 1                                        | 1                                       | 0                                          | —                       | —                   |
| 1                                        | 1                                       | 1                                          | Available               | Available           |

0: View Resizer Selected

1: Capture Resizer Selected

bits 1-0

Camera Display Control bits [1:0]

These bits control how camera data is displayed when a JPEG encode operation is performed (REG[0980h] bits 3-1 = 000) and when YUV to Host mode (JPEG Bypass) is enabled (REG[0980h] bits 3-1 = 011 or 111).

*Table 10-56: Camera Display Control Selection*

| REG[0930h] bits 1-0 | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00                  | <p><b>JPEG Encode:</b><br/>YUV data from the camera interface is continuously written to the display buffer until a JPEG encode operation is performed. When a JPEG encode operation is started (REG[098Ah] bit 0 = 1), camera data is no longer written to the display buffer once the next frame is written. After REG[098Ah] bit 0 is set to 0, camera data is again written to the display buffer from the next frame.</p> <p><b>JPEG Bypass:</b><br/>YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.</p>                                                        |
| 01                  | <p><b>JPEG Encode:</b><br/>When a JPEG encode operation is started (REG[098Ah] bit 0 = 1), only the next frame of camera data is written to the display buffer. When a JPEG encode operation is not enabled (REG[098Ah] bit 0 = 0), camera data is not written to the display buffer.</p> <p><b>JPEG Bypass:</b><br/>YUV data from the camera interface is continuously written to the JPEG FIFO. When the shutter is enabled (REG[098Ah] bit 0 = 1), YUV data from the camera interface is converted by the YUV/RGB Converter to RGB data and is stored in the display buffer. When the shutter is disabled (REG[098Ah] bit 0 = 0), camera data is not written to the display buffer.</p> |
| 10                  | <p><b>JPEG Encode:</b><br/>Data from the camera interface is always written to the display buffer.</p> <p><b>JPEG Bypass:</b><br/>YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.</p>                                                                                                                                                                                                                                                                                                                                                                                |
| 11                  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

### REG[0932h] through REG[093Eh] are Reserved

These registers are Reserved and should not be written.

## View (Display) Resizer Registers

| REG[0940h] View Resizer Control Register |     |    |    |    |                                                             |                                           |                     |
|------------------------------------------|-----|----|----|----|-------------------------------------------------------------|-------------------------------------------|---------------------|
| Default = 0000h                          |     |    |    |    |                                                             |                                           |                     |
| Read/Write                               |     |    |    |    |                                                             |                                           |                     |
| n/a                                      |     |    |    |    |                                                             |                                           |                     |
| 15                                       | 14  | 13 | 12 | 11 | 10                                                          | 9                                         | 8                   |
| View Resizer Software Reset (WO)         | n/a |    |    |    | View Resizer Independent Horizontal/Vertical Scaling Enable | View Resizer Register Update VSYNC Enable | View Resizer Enable |
| 7                                        | 6   | 5  | 4  | 3  | 2                                                           | 1                                         | 0                   |

- bit 7 View Resizer Software Reset (Write Only)  
When the resizers are activated by writing a 1 to REG[0940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the view resizer logic is reset.  
When a 0 is written to this bit, there is no hardware effect.
- bit 2 View Resizer Independent Horizontal/Vertical Scaling Enable  
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[094Ch] bits 5-0 and vertical scaling rate is controlled by REG[094Eh] bits 13-8.  
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[094Ch] bits 5-0.
- bit 1 View Resizer Register Update VSYNC Enable  
When this bit = 1, the View Resizer uses the previous register value until the next camera VSYNC occurs.  
When this bit = 0, the View Resizer use the new register value immediately.
- bit 0 View Resizer Enable  
This bit controls the view resizer logic.  
When this bit = 1, the view resizer logic is enabled.  
When this bit = 0, the view resizer logic is disabled.

**Note**

When this bit and the Capture Resizer Enable bit (REG[0960h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

| REG[0944h] View Resizer Start X Position Register |    |    |    |    |    |   |   |
|---------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                   |    |    |    |    |    |   |   |
| Read/Write                                        |    |    |    |    |    |   |   |
| n/a                                               |    |    |    |    |    |   |   |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| View Resizer Start X Position bits 10-8           |    |    |    |    |    |   |   |
| View Resizer Start X Position bits 7-0            |    |    |    |    |    |   |   |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

- bits 10-0 View Resizer Start X Position bits [10:0]  
These bits determine the X start position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[0946h] View Resizer Start Y Position Register |    |    |    |    |                                         |   |   |
|---------------------------------------------------|----|----|----|----|-----------------------------------------|---|---|
| Default = 0000h                                   |    |    |    |    |                                         |   |   |
| Read/Write                                        |    |    |    |    |                                         |   |   |
| n/a                                               |    |    |    |    | View Resizer Start Y Position bits 10-8 |   |   |
| 15                                                | 14 | 13 | 12 | 11 | 10                                      | 9 | 8 |
| View Resizer Start Y Position bits 7-0            |    |    |    |    |                                         |   |   |
| 7                                                 | 6  | 5  | 4  | 3  | 2                                       | 1 | 0 |

bits 10-0

View Resizer Start Y Position bits [10:0]

These bits determine the Y start position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[0948h] View Resizer End X Position Register |    |    |    |    |                                       |   |   |
|-------------------------------------------------|----|----|----|----|---------------------------------------|---|---|
| Default = 027Fh                                 |    |    |    |    |                                       |   |   |
| Read/Write                                      |    |    |    |    |                                       |   |   |
| n/a                                             |    |    |    |    | View Resizer End X Position bits 10-8 |   |   |
| 15                                              | 14 | 13 | 12 | 11 | 10                                    | 9 | 8 |
| View Resizer End X Position bits 7-0            |    |    |    |    |                                       |   |   |
| 7                                               | 6  | 5  | 4  | 3  | 2                                     | 1 | 0 |

bits 10-0

View Resizer End X Position bits [10:0]

These bits determine the X End position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[094Ah] View Resizer End Y Position Register |    |    |    |    |                                       |   |   |
|-------------------------------------------------|----|----|----|----|---------------------------------------|---|---|
| Default = 01DFh                                 |    |    |    |    |                                       |   |   |
| Read/Write                                      |    |    |    |    |                                       |   |   |
| n/a                                             |    |    |    |    | View Resizer End Y Position bits 10-8 |   |   |
| 15                                              | 14 | 13 | 12 | 11 | 10                                    | 9 | 8 |
| View Resizer End Y Position bits 7-0            |    |    |    |    |                                       |   |   |
| 7                                               | 6  | 5  | 4  | 3  | 2                                     | 1 | 0 |

bits 10-0

View Resizer End Y Position bits [10:0]

These bits determine the Y end position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[094Ch] View Resizer Operation Setting Register 0 |    |                                               |    |    |    |   |   |
|------------------------------------------------------|----|-----------------------------------------------|----|----|----|---|---|
| Default = 0101h                                      |    |                                               |    |    |    |   |   |
| Read/Write                                           |    |                                               |    |    |    |   |   |
| n/a                                                  |    | View Resizer Vertical Scaling Rate bits 5-0   |    |    |    |   |   |
| 15                                                   | 14 | 13                                            | 12 | 11 | 10 | 9 | 8 |
| n/a                                                  |    | View Resizer Horizontal Scaling Rate bits 5-0 |    |    |    |   |   |
| 7                                                    | 6  | 5                                             | 4  | 3  | 2  | 1 | 0 |

bits 13-8

View Resizer Vertical Scaling Rate bits [5:0]

These bits determine the view resizer vertical scaling rate when independent horizontal/vertical scaling is enabled (REG[0940h] bit 2 = 1). Not all scaling rates are available for all scaling modes (see REG[094Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-57: “View Resizer Vertical Scaling Rate Selection,” on page 241.

Table 10-57: View Resizer Vertical Scaling Rate Selection

| REG[094Ch] bits 13-8 | View Resizer Vertical Scaling Rate |                             |                             |                             |
|----------------------|------------------------------------|-----------------------------|-----------------------------|-----------------------------|
|                      | REG[094Eh]<br>bits 1-0 = 00        | REG[094Eh]<br>bits 1-0 = 01 | REG[094Eh]<br>bits 1-0 = 10 | REG[094Eh]<br>bits 1-0 = 11 |
| 00 0000              | Reserved                           | Reserved                    | Reserved                    | Reserved                    |
| 00 0001              | n/a                                | 1/1                         | 1/1                         | Reserved                    |
| 00 0010              | n/a                                | 1/2                         | 1/2                         | Reserved                    |
| 00 0011              | n/a                                | 1/3                         | 1/3                         | Reserved                    |
| 00 0100              | n/a                                | 1/4                         | 1/4                         | Reserved                    |
| 00 0101              | n/a                                | 1/5                         | 1/5                         | Reserved                    |
| 00 0110              | n/a                                | 1/6                         | 1/6                         | Reserved                    |
| 00 0111              | n/a                                | 1/7                         | 1/7                         | Reserved                    |
| 00 1000              | n/a                                | 1/8                         | 1/8                         | Reserved                    |
| 00 1001              | n/a                                | 1/9                         | 1/9                         | Reserved                    |
| 00 1010              | n/a                                | 1/10                        | 1/10                        | Reserved                    |
| 00 1011              | n/a                                | 1/11                        | 1/11                        | Reserved                    |
| 00 1100              | n/a                                | 1/12                        | 1/12                        | Reserved                    |
| 00 1101              | n/a                                | 1/13                        | 1/13                        | Reserved                    |
| 00 1110              | n/a                                | 1/14                        | 1/14                        | Reserved                    |
| 00 1111              | n/a                                | 1/15                        | 1/15                        | Reserved                    |
| 01 0000              | n/a                                | 1/16                        | 1/16                        | Reserved                    |
| 01 0001              | n/a                                | 1/17                        | 1/17                        | Reserved                    |
| 01 0010              | n/a                                | 1/18                        | 1/18                        | Reserved                    |
| 01 0011              | n/a                                | 1/19                        | 1/19                        | Reserved                    |
| 01 0100              | n/a                                | 1/20                        | 1/20                        | Reserved                    |
| 01 0101              | n/a                                | 1/21                        | 1/21                        | Reserved                    |
| 01 0110              | n/a                                | 1/22                        | 1/22                        | Reserved                    |
| 01 0111              | n/a                                | 1/23                        | 1/23                        | Reserved                    |
| 01 1000              | n/a                                | 1/24                        | 1/24                        | Reserved                    |
| 01 1001              | n/a                                | 1/25                        | 1/25                        | Reserved                    |
| 01 1010              | n/a                                | 1/26                        | 1/26                        | Reserved                    |
| 01 1011              | n/a                                | 1/27                        | 1/27                        | Reserved                    |
| 01 1100              | n/a                                | 1/28                        | 1/28                        | Reserved                    |
| 01 1101              | n/a                                | 1/29                        | 1/29                        | Reserved                    |
| 01 1110              | n/a                                | 1/30                        | 1/30                        | Reserved                    |
| 01 1111              | n/a                                | 1/31                        | 1/31                        | Reserved                    |
| 10 0000              | n/a                                | 1/32                        | 1/32                        | Reserved                    |
| 10 0001 - 11 1111    | Reserved                           | Reserved                    | Reserved                    | Reserved                    |

bits 5-0

View Resizer Horizontal Scaling Rate bits [5:0]

When independent horizontal/vertical scaling is disabled (REG[0940h] bit 2 = 0), these bits determine the vertical and horizontal scaling rate. When independent horizontal/vertical scaling is enabled (REG[0940h] bit 2 = 1), these bits only determine the horizontal scaling rate. Not all scaling rates are available for all scaling modes (see REG[094Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-58: “View Resizer Horizontal Scaling Rate Selection,” on page 242.

Table 10-58: View Resizer Horizontal Scaling Rate Selection

| REG[094Ch] bits 5-0 | View Resizer Horizontal Scaling Rate |                             |                             |                             |
|---------------------|--------------------------------------|-----------------------------|-----------------------------|-----------------------------|
|                     | REG[094Eh]<br>bits 1-0 = 00          | REG[094Eh]<br>bits 1-0 = 01 | REG[094Eh]<br>bits 1-0 = 10 | REG[094Eh]<br>bits 1-0 = 11 |
| 00 0000             | Reserved                             | Reserved                    | Reserved                    | Reserved                    |
| 00 0001             | n/a                                  | 1/1                         | 1/1                         | Reserved                    |
| 00 0010             | n/a                                  | 1/2                         | 1/2                         | Reserved                    |
| 00 0011             | n/a                                  | 1/3                         | Reserved                    | Reserved                    |
| 00 0100             | n/a                                  | 1/4                         | 1/4                         | Reserved                    |
| 00 0101             | n/a                                  | 1/5                         | Reserved                    | Reserved                    |
| 00 0110             | n/a                                  | 1/6                         | Reserved                    | Reserved                    |
| 00 0111             | n/a                                  | 1/7                         | Reserved                    | Reserved                    |
| 00 1000             | n/a                                  | 1/8                         | 1/8                         | Reserved                    |
| 00 1001             | n/a                                  | 1/9                         | Reserved                    | Reserved                    |
| 00 1010             | n/a                                  | 1/10                        | Reserved                    | Reserved                    |
| 00 1011             | n/a                                  | 1/11                        | Reserved                    | Reserved                    |
| 00 1100             | n/a                                  | 1/12                        | Reserved                    | Reserved                    |
| 00 1101             | n/a                                  | 1/13                        | Reserved                    | Reserved                    |
| 00 1110             | n/a                                  | 1/14                        | Reserved                    | Reserved                    |
| 00 1111             | n/a                                  | 1/15                        | Reserved                    | Reserved                    |
| 01 0000             | n/a                                  | 1/16                        | 1/16                        | Reserved                    |
| 01 0001             | n/a                                  | 1/17                        | Reserved                    | Reserved                    |
| 01 0010             | n/a                                  | 1/18                        | Reserved                    | Reserved                    |
| 01 0011             | n/a                                  | 1/19                        | Reserved                    | Reserved                    |
| 01 0100             | n/a                                  | 1/20                        | Reserved                    | Reserved                    |
| 01 0101             | n/a                                  | 1/21                        | Reserved                    | Reserved                    |
| 01 0110             | n/a                                  | 1/22                        | Reserved                    | Reserved                    |
| 01 0111             | n/a                                  | 1/23                        | Reserved                    | Reserved                    |
| 01 1000             | n/a                                  | 1/24                        | Reserved                    | Reserved                    |
| 01 1001             | n/a                                  | 1/25                        | Reserved                    | Reserved                    |
| 01 1010             | n/a                                  | 1/26                        | Reserved                    | Reserved                    |
| 01 1011             | n/a                                  | 1/27                        | Reserved                    | Reserved                    |
| 01 1100             | n/a                                  | 1/28                        | Reserved                    | Reserved                    |
| 01 1101             | n/a                                  | 1/29                        | Reserved                    | Reserved                    |
| 01 1110             | n/a                                  | 1/30                        | Reserved                    | Reserved                    |
| 01 1111             | n/a                                  | 1/31                        | Reserved                    | Reserved                    |
| 10 0000             | n/a                                  | 1/32                        | 1/32                        | Reserved                    |
| 10 0001 - 11 1111   | Reserved                             | Reserved                    | Reserved                    | Reserved                    |

| REG[094Eh] View Resizer Operation Setting Register 1 |    |    |    |          |    |                                    |   |
|------------------------------------------------------|----|----|----|----------|----|------------------------------------|---|
| Default = 0000h                                      |    |    |    |          |    |                                    |   |
| Read/Write                                           |    |    |    |          |    |                                    |   |
| n/a                                                  |    |    |    |          |    |                                    |   |
| 15                                                   | 14 | 13 | 12 | 11       | 10 | 9                                  | 8 |
| n/a                                                  |    |    |    | Reserved |    | View Resizer Scaling Mode bits 1-0 |   |
| 7                                                    | 6  | 5  | 4  | 3        | 2  | 1                                  | 0 |

bits 3-2                      Reserved  
The default value for these bits is 0.

bits 1-0                      View Resizer Scaling Mode bits[1:0]  
These bits determine the view resizer scaling mode. Not all scaling modes are available for all scaling rates. Before selecting a scaling mode, set the View Resizer Vertical Scaling Rate bits (REG[094Eh] bits 13-8) and/or the View Resizer Horizontal Scaling Rate bits (REG[094Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the view resizer.

*Table 10-59: View Resizer Scaling Mode Selection*

| REG[094Eh] bits 1-0 | View Resizer Scaling Mode |
|---------------------|---------------------------|
| 00                  | no resizer scaling        |
| 01                  | V/H Reduction             |
| 10                  | V: Reduction, H: Average  |
| 11                  | Reserved                  |

Capture (Encode) Resizer Registers

| REG[0960h] Capture Resizer Control Register |     |    |    |    |                                                                |                                              |                        |
|---------------------------------------------|-----|----|----|----|----------------------------------------------------------------|----------------------------------------------|------------------------|
| Default = 0000h                             |     |    |    |    |                                                                |                                              | Read/Write             |
| n/a                                         |     |    |    |    |                                                                |                                              |                        |
| 15                                          | 14  | 13 | 12 | 11 | 10                                                             | 9                                            | 8                      |
| Capture Resizer Software Reset (WO)         | n/a |    |    |    | Capture Resizer Independent Horizontal/Vertical Scaling Enable | Capture Resizer Register Update VSYNC Enable | Capture Resizer Enable |
| 7                                           | 6   | 5  | 4  | 3  | 2                                                              | 1                                            | 0                      |

- bit 7

Capture Resizer Software Reset (Write Only)  
When the resizers are activated by writing a 1 to REG[940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the capture resizer logic is reset.  
When a 0 is written to this bit, there is no hardware effect.
- bit 2

Capture Resizer Independent Horizontal/Vertical Scaling Enable  
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[096Ch] bits 4-0 and vertical scaling rate is controlled by REG[096Ch] bits 12-8.  
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[096Ch] bits 4-0.
- bit 1

Capture Resizer Register Update VSYNC Enable  
When this bit = 1, the Capture Resizer uses the previous register value until the next camera VSYNC occurs.  
When this bit = 0, the Capture Resizer use the new register value immediately.
- bit 0

Capture Resizer Enable  
This bit controls the capture resizer logic.  
When this bit = 1, the capture resizer logic is enabled.  
When this bit = 0, the capture resizer logic is disabled.

**Note**  
When this bit and the View Resizer Enable bit (REG[0940h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

| REG[0964h] Capture Resizer Start X Position Register |    |    |    |    |                                            |   | Read/Write |  |
|------------------------------------------------------|----|----|----|----|--------------------------------------------|---|------------|--|
| Default = 0000h                                      |    |    |    |    |                                            |   |            |  |
| n/a                                                  |    |    |    |    | Capture Resizer Start X Position bits 10-0 |   |            |  |
| 15                                                   | 14 | 13 | 12 | 11 | 10                                         | 9 | 8          |  |
| Capture Resizer Start X Position bits 7-0            |    |    |    |    |                                            |   |            |  |
| 7                                                    | 6  | 5  | 4  | 3  | 2                                          | 1 | 0          |  |

bits 10-0

Capture Resizer Start X Position bits [10:0]

These bits determine the X start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

The following image size limitations must be observed when the JPEG functions (or JPEG Bypass) are used.

Table 10-60: Capture Resizer Limitations

| YUV Format | Minimum Horizontal Resolution | Minimum Vertical Resolution | Minimum Size       |
|------------|-------------------------------|-----------------------------|--------------------|
| YUV 4:4:4  | multiples of 1 pixel          | multiples of 1 line         | 8 pixels/8 lines   |
| YUV 4:2:2  | multiples of 2 pixels         | multiples of 1 line         | 16 pixels/8 lines  |
| YUV 4:2:0  | multiples of 2 pixels         | multiples of 2 lines        | 16 pixels/16 lines |
| YUV 4:1:1  | multiples of 4 pixels         | multiples of 1 line         | 32 pixels/8 lines  |

| REG[0966h] Capture Resizer Start Y Position Register |    |    |    |    |                                            |   | Read/Write |  |
|------------------------------------------------------|----|----|----|----|--------------------------------------------|---|------------|--|
| Default = 0000h                                      |    |    |    |    |                                            |   |            |  |
| n/a                                                  |    |    |    |    | Capture Resizer Start Y Position bits 10-0 |   |            |  |
| 15                                                   | 14 | 13 | 12 | 11 | 10                                         | 9 | 8          |  |
| Capture Resizer Start Y Position bits 7-0            |    |    |    |    |                                            |   |            |  |
| 7                                                    | 6  | 5  | 4  | 3  | 2                                          | 1 | 0          |  |

bits 10-0

Capture Resizer Start Y Position bits [10:0]

These bits determine the Y start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[0968h] Capture Resizer End X Position Register |    |    |    |    |                                          |   | Read/Write |  |
|----------------------------------------------------|----|----|----|----|------------------------------------------|---|------------|--|
| Default = 027Fh                                    |    |    |    |    |                                          |   |            |  |
| n/a                                                |    |    |    |    | Capture Resizer End X Position bits 10-0 |   |            |  |
| 15                                                 | 14 | 13 | 12 | 11 | 10                                       | 9 | 8          |  |
| Capture Resizer End X Position bits 7-0            |    |    |    |    |                                          |   |            |  |
| 7                                                  | 6  | 5  | 4  | 3  | 2                                        | 1 | 0          |  |

bits 10-0

Capture Resizer End X Position bits [10:0]

These bits determine the X End position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[096Ah] Capture Resizer End Y Position Register |    |    |    |    |                                          |   |   |
|----------------------------------------------------|----|----|----|----|------------------------------------------|---|---|
| Default = 01DFh                                    |    |    |    |    |                                          |   |   |
| Read/Write                                         |    |    |    |    |                                          |   |   |
| n/a                                                |    |    |    |    | Capture Resizer End Y Position bits 10-8 |   |   |
| 15                                                 | 14 | 13 | 12 | 11 | 10                                       | 9 | 8 |
| Capture Resizer End Y Position bits 7-0            |    |    |    |    |                                          |   |   |
| 7                                                  | 6  | 5  | 4  | 3  | 2                                        | 1 | 0 |

bits 10-0

Capture Resizer End Y Position bits [10:0]

These bits determine the Y end position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 358.

| REG[096Ch] Capture Resizer Operation Setting Register 0 |    |                                                  |    |    |    |   |   |
|---------------------------------------------------------|----|--------------------------------------------------|----|----|----|---|---|
| Default = 0101h                                         |    |                                                  |    |    |    |   |   |
| Read/Write                                              |    |                                                  |    |    |    |   |   |
| n/a                                                     |    | Capture Resizer Vertical Scaling Rate bits 5-0   |    |    |    |   |   |
| 15                                                      | 14 | 13                                               | 12 | 11 | 10 | 9 | 8 |
| n/a                                                     |    | Capture Resizer Horizontal Scaling Rate bits 5-0 |    |    |    |   |   |
| 7                                                       | 6  | 5                                                | 4  | 3  | 2  | 1 | 0 |

bits 13-8

Capture Resizer Vertical Scaling Rate bits [5:0]

These bits determine the capture resizer vertical scaling rate when independent horizontal/vertical scaling is enabled (REG[0960h] bit 2 = 1). Not all scaling rates are available for all scaling modes (see REG[096Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-61: “Capture Resizer Vertical Scaling Rate Selection,” on page 246.

Table 10-61: Capture Resizer Vertical Scaling Rate Selection

| REG[096Ch] bits 13-8 | Capture Resizer Vertical Scaling Rate |                             |                             |                             |
|----------------------|---------------------------------------|-----------------------------|-----------------------------|-----------------------------|
|                      | REG[096Eh]<br>bits 1-0 = 00           | REG[096Eh]<br>bits 1-0 = 01 | REG[096Eh]<br>bits 1-0 = 10 | REG[096Eh]<br>bits 1-0 = 11 |
| 00 0000              | Reserved                              | Reserved                    | Reserved                    | Reserved                    |
| 00 0001              | n/a                                   | 1/1                         | 1/1                         | Reserved                    |
| 00 0010              | n/a                                   | 1/2                         | 1/2                         | Reserved                    |
| 00 0011              | n/a                                   | 1/3                         | 1/3                         | Reserved                    |
| 00 0100              | n/a                                   | 1/4                         | 1/4                         | Reserved                    |
| 00 0101              | n/a                                   | 1/5                         | 1/5                         | Reserved                    |
| 00 0110              | n/a                                   | 1/6                         | 1/6                         | Reserved                    |
| 00 0111              | n/a                                   | 1/7                         | 1/7                         | Reserved                    |
| 00 1000              | n/a                                   | 1/8                         | 1/8                         | Reserved                    |
| 00 1001              | n/a                                   | 1/9                         | 1/9                         | Reserved                    |
| 00 1010              | n/a                                   | 1/10                        | 1/10                        | Reserved                    |
| 00 1011              | n/a                                   | 1/11                        | 1/11                        | Reserved                    |
| 00 1100              | n/a                                   | 1/12                        | 1/12                        | Reserved                    |
| 00 1101              | n/a                                   | 1/13                        | 1/13                        | Reserved                    |
| 00 1110              | n/a                                   | 1/14                        | 1/14                        | Reserved                    |
| 00 1111              | n/a                                   | 1/15                        | 1/15                        | Reserved                    |
| 01 0000              | n/a                                   | 1/16                        | 1/16                        | Reserved                    |
| 01 0001              | n/a                                   | 1/17                        | 1/17                        | Reserved                    |

Table 10-61: Capture Resizer Vertical Scaling Rate Selection (Continued)

|                   |          |          |          |          |
|-------------------|----------|----------|----------|----------|
| 01 0010           | n/a      | 1/18     | 1/18     | Reserved |
| 01 0011           | n/a      | 1/19     | 1/19     | Reserved |
| 01 0100           | n/a      | 1/20     | 1/20     | Reserved |
| 01 0101           | n/a      | 1/21     | 1/21     | Reserved |
| 01 0110           | n/a      | 1/22     | 1/22     | Reserved |
| 01 0111           | n/a      | 1/23     | 1/23     | Reserved |
| 01 1000           | n/a      | 1/24     | 1/24     | Reserved |
| 01 1001           | n/a      | 1/25     | 1/25     | Reserved |
| 01 1010           | n/a      | 1/26     | 1/26     | Reserved |
| 01 1011           | n/a      | 1/27     | 1/27     | Reserved |
| 01 1100           | n/a      | 1/28     | 1/28     | Reserved |
| 01 1101           | n/a      | 1/29     | 1/29     | Reserved |
| 01 1110           | n/a      | 1/30     | 1/30     | Reserved |
| 01 1111           | n/a      | 1/31     | 1/31     | Reserved |
| 10 0000           | n/a      | 1/32     | 1/32     | Reserved |
| 10 0001 - 11 1111 | Reserved | Reserved | Reserved | Reserved |

bits 5-0

Capture Resizer Horizontal Scaling Rate bits [5:0]

When independent horizontal/vertical scaling is disabled (REG[0960h] bit 2 = 0), these bits determine the vertical and horizontal scaling rate. When independent horizontal/vertical scaling is enabled (REG[0960h] bit 2 = 1), these bits only determine the horizontal scaling rate. Not all scaling rates are available for all scaling modes (see REG[096Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-62: “Capture Resizer Horizontal Scaling Rate Selection,” on page 247.

Table 10-62: Capture Resizer Horizontal Scaling Rate Selection

| REG[096Ch] bits 5-0 | Capture Resizer Horizontal Scaling Rate |                             |                             |                             |
|---------------------|-----------------------------------------|-----------------------------|-----------------------------|-----------------------------|
|                     | REG[096Eh]<br>bits 1-0 = 00             | REG[096Eh]<br>bits 1-0 = 01 | REG[096Eh]<br>bits 1-0 = 10 | REG[096Eh]<br>bits 1-0 = 11 |
| 00 0000             | Reserved                                | Reserved                    | Reserved                    | Reserved                    |
| 00 0001             | n/a                                     | 1/1                         | 1/1                         | Reserved                    |
| 00 0010             | n/a                                     | 1/2                         | 1/2                         | Reserved                    |
| 00 0011             | n/a                                     | 1/3                         | Reserved                    | Reserved                    |
| 00 0100             | n/a                                     | 1/4                         | 1/4                         | Reserved                    |
| 00 0101             | n/a                                     | 1/5                         | Reserved                    | Reserved                    |
| 00 0110             | n/a                                     | 1/6                         | Reserved                    | Reserved                    |
| 00 0111             | n/a                                     | 1/7                         | Reserved                    | Reserved                    |
| 00 1000             | n/a                                     | 1/8                         | 1/8                         | Reserved                    |
| 00 1001             | n/a                                     | 1/9                         | Reserved                    | Reserved                    |
| 00 1010             | n/a                                     | 1/10                        | Reserved                    | Reserved                    |
| 00 1011             | n/a                                     | 1/11                        | Reserved                    | Reserved                    |
| 00 1100             | n/a                                     | 1/12                        | Reserved                    | Reserved                    |
| 00 1101             | n/a                                     | 1/13                        | Reserved                    | Reserved                    |
| 00 1110             | n/a                                     | 1/14                        | Reserved                    | Reserved                    |
| 00 1111             | n/a                                     | 1/15                        | Reserved                    | Reserved                    |
| 01 0000             | n/a                                     | 1/16                        | 1/16                        | Reserved                    |
| 01 0001             | n/a                                     | 1/17                        | Reserved                    | Reserved                    |

*Table 10-62: Capture Resizer Horizontal Scaling Rate Selection (Continued)*

|                   |          |          |          |          |
|-------------------|----------|----------|----------|----------|
| 01 0010           | n/a      | 1/18     | Reserved | Reserved |
| 01 0011           | n/a      | 1/19     | Reserved | Reserved |
| 01 0100           | n/a      | 1/20     | Reserved | Reserved |
| 01 0101           | n/a      | 1/21     | Reserved | Reserved |
| 01 0110           | n/a      | 1/22     | Reserved | Reserved |
| 01 0111           | n/a      | 1/23     | Reserved | Reserved |
| 01 1000           | n/a      | 1/24     | Reserved | Reserved |
| 01 1001           | n/a      | 1/25     | Reserved | Reserved |
| 01 1010           | n/a      | 1/26     | Reserved | Reserved |
| 01 1011           | n/a      | 1/27     | Reserved | Reserved |
| 01 1100           | n/a      | 1/28     | Reserved | Reserved |
| 01 1101           | n/a      | 1/29     | Reserved | Reserved |
| 01 1110           | n/a      | 1/30     | Reserved | Reserved |
| 01 1111           | n/a      | 1/31     | Reserved | Reserved |
| 10 0000           | n/a      | 1/32     | 1/32     | Reserved |
| 10 0001 - 11 1111 | Reserved | Reserved | Reserved | Reserved |

## REG[096Eh] Capture Resizer Operation Setting Register 1

Default = 0000h

Read/Write

|     |    |    |    |          |    |                                       |   |
|-----|----|----|----|----------|----|---------------------------------------|---|
| n/a |    |    |    |          |    |                                       |   |
| 15  | 14 | 13 | 12 | 11       | 10 | 9                                     | 8 |
| n/a |    |    |    | Reserved |    | Capture Resizer Scaling Mode bits 1-0 |   |
| 7   | 6  | 5  | 4  | 3        | 2  | 1                                     | 0 |

bits 3-2

Reserved

The default value for these bits is 0.

bit 1-0

Capture Resizer Scaling Mode bits[1:0]

These bits determine the capture resizer scaling mode. Not all scaling rates are available for all scaling modes. Before selecting a scaling mode, set the Capture Resizer Vertical Scaling Rate bits (REG[096Eh] bits 13-8) and/or the Capture Resizer Horizontal Scaling Rate bits (REG[096Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the capture resizer.

*Table 10-63: Capture Resizer Scaling Mode Selection*

| REG[096Eh] bits 1-0 | Capture Resizer Scaling Mode |
|---------------------|------------------------------|
| 00                  | no resizer scaling           |
| 01                  | V/H Reduction                |
| 10                  | V: Reduction, H: Average     |
| 11                  | Reserved                     |

## 10.4.15 JPEG Module Registers

| REG[0980h] JPEG Control Register |          |    |                              |                            |    |   | Read/Write                   |
|----------------------------------|----------|----|------------------------------|----------------------------|----|---|------------------------------|
| Default = 0000h                  |          |    |                              |                            |    |   |                              |
| Reserved<br>n/a                  |          |    |                              |                            |    |   | JPEG 180°<br>Rotation Enable |
| 15                               | 14       | 13 | 12                           | 11                         | 10 | 9 | 8                            |
| JPEG Module SW<br>Reset (WO)     | Reserved |    | YUV Data No<br>Offset Select | JPEG Data Control bits 2-0 |    |   | JPEG Module<br>Enable        |
| 7                                | 6        | 5  | 4                            | 3                          | 2  | 1 | 0                            |

bits 15-12

Reserved

The default value for these bits is 0.

bit 8

JPEG 180° Rotation Enable

This bit is only for camera data encode. This bit selects the rotation mode for JPEG encoded data. For an overview diagram, see Section 18.4, “JPEG 180° Rotate Encode Diagram” on page 365.

When this bit = 1, the JPEG encoded data is rotated 180°.

When this bit = 0, the JPEG encoded data is normal.

### Note

The dimensions of the image must be in MCU size multiples.

bit 7

JPEG Module Software Reset (Write Only)

This bit initiates a software reset of the internal JPEG module circuit. The JPEG module should be reset using this bit before each JPEG encode operation.

This bit resets only the internal JPEG module circuit and has no effect on the JPEG codec registers (REG[1000h]-[17A2h], the JPEG codec or the JPEG module registers (REG[0980h]-[09E0h]), except as follows.

REG[0984] is reset except for bits 14, 5, and 1.

REG[09B4] is reset

REG[09B6] is reset

REG[09AC] is reset

REG[09AA] is reset

REG[09A8] is reset

REG[09A2] is reset

To reset the JPEG codec, set the JPEG Codec Software Reset bit (REG[1002h] bit 7) to 1.

When a 1 is written to this bit, the JPEG module is reset.

When a 0 is written to this bit, there is no hardware effect.

bit 6

Reserved

The default value for this bit is 0.

bit 5

Reserved

The default value for this bit is 0.

bit 4

## YUV Data No Offset Select

This bit specifies whether an offset is applied to the U and V data when in YUV Capture, YUV Display, Host Encode, and Host Decode modes, REG[0980h] bits [3:1] = 001, 011, 100, 101, or 111. This bit is used in conjunction with REG[0110h] bit 8 to select the desired YUV output capture range for YUV Capture mode.

When this bit = 0, an offset is applied to the U and V data (MSB is inverted).

When this bit = 1, no offset is applied to the U and V data is not modified.

The YUV data range depends on the interface data range and the YUV Data No Offset Select bit. For Host Decode mode, this bit must be set to 1.

Table 10-64: YUV Output Range Selection (REG[0980h] bits 3-1 = 011, 100 or 111)

| Camera Interface Input<br>YUV Data | REG[0110h] bit 8 | REG[0980h] bit 4 | YUV Output Data Range                                                                                                                                       |
|------------------------------------|------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Straight Data                      | 0                | 0                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |
|                                    |                  | 1                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |
|                                    | 1                | 0                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |
|                                    |                  | 1                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |

Table 10-64: YUV Output Range Selection (REG[0980h] bits 3-1 = 011, 100 or 111) (Continued)

| Camera Interface Input<br>YUV Data | REG[0110h] bit 8 | REG[0980h] bit 4 | YUV Output Data Range                                                                                                                                       |
|------------------------------------|------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Offset Data                        | 0                | 0                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |
|                                    |                  | 1                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |
|                                    | 1                | 0                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |
|                                    |                  | 1                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |

Table 10-65: YUV Input Range Selection (REG[0980h] bits 3-1 = 001, 100 or 101)

| Host Interface Input YUV Data | REG[0980h] bit 4 | YUV Input Data Range                                                                                                                                        |
|-------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Straight Data                 | 0                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |
|                               | 1                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |
| Offset Data                   | 0                | $0 \leq Y \leq 255$<br>$0 \leq U \leq 255$<br>$0 \leq V \leq 255$<br>or<br>$16 \leq Y \leq 235$<br>$16 \leq Cb \leq 240$<br>$16 \leq Cr \leq 240$           |
|                               | 1                | $0 \leq Y \leq 255$<br>$-128 \leq U \leq 127$<br>$-128 \leq V \leq 127$<br>or<br>$16 \leq Y \leq 235$<br>$-112 \leq Cb \leq 112$<br>$-112 \leq Cr \leq 112$ |

bits 3-1

JPEG Data Control bits [2:0]

Table 10-66: JPEG Data Mode Selection

| REG[0980h] bits 3-1 | JPEG Data Mode                                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------|---------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000                 | JPEG Encode/Decode                                            | <p>In this mode the encode data paths are:</p> <ul style="list-style-type: none"> <li>• <b>Camera Interface</b> =&gt; Capture Resizer =&gt; JPEG Line Buffer =&gt; Codec Core =&gt; JPEG FIFO =&gt; Host Interface</li> <li>• <b>Display Buffer</b> =&gt; RGB/YUV Converter =&gt; Capture Resizer =&gt; JPEG Line Buffer =&gt; Codec Core =&gt; JPEG FIFO =&gt; Host Interface</li> <li>• <b>Host Interface</b> =&gt; RGB/YUV Converter =&gt; Capture Resizer =&gt; JPEG Line Buffer =&gt; Codec Core =&gt; JPEG FIFO =&gt; Host Interface</li> </ul> <p>In this mode the decode data path is:</p> <ul style="list-style-type: none"> <li>• <b>Host Interface</b> =&gt; JPEG FIFO =&gt; Codec Core =&gt; JPEG Line Buffer =&gt; View Resizer =&gt; RGB/YUV Converter =&gt; Display Buffer</li> </ul> |
| 001                 | YUV Data Input from Host (YUV 4:2:2)                          | The data by-passes the JPEG Module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 010                 |                                                               | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 011                 | YUV Data Output to Host (YUV 4:2:2)                           | The data by-passes the JPEG Module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 100                 | Host Input/Output JPEG Encode/Decode (YUV 4:2:0 or YUV 4:2:2) | <p>In this mode the encode data path is:</p> <ul style="list-style-type: none"> <li>• <b>Host Interface</b> =&gt; JPEG Line Buffer =&gt; Capture Resizer =&gt; Codec Core =&gt; JPEG FIFO =&gt; Host Interface</li> </ul> <p>In this mode the decode data path is:</p> <ul style="list-style-type: none"> <li>• <b>Host Interface</b> =&gt; JPEG FIFO =&gt; Codec Core =&gt; JPEG Line Buffer =&gt; View Resizer =&gt; Host Interface</li> </ul>                                                                                                                                                                                                                                                                                                                                                     |
| 101                 | YUV Data Input from Host (YUV 4:2:0)                          | The data by-passes the JPEG Module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 110                 |                                                               | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 111                 | YUV Data Output to Host (YUV 4:2:0)                           | The data by-passes the JPEG Module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

bit 0

JPEG Module Enable

This bit enables/disables the JPEG module and its associated registers. **If the JPEG module is disabled, REG[1000h] - REG[17A2h] must not be accessed.**

When this bit = 1, the JPEG module is enabled and a clock source is supplied.

When this bit = 0, the JPEG module is disabled and the clock source is disabled.

**Note**

The JPEG module must be disabled before the View Resizer Enable bit (REG[0940h] bit 0) or the Capture Resizer Enable bit (REG[0960h] bit 0) are disabled.

| REG[0982h] JPEG Status Flag Register |                                 |                                          |                         |                                  |                                     |                                | Read/Write                           |
|--------------------------------------|---------------------------------|------------------------------------------|-------------------------|----------------------------------|-------------------------------------|--------------------------------|--------------------------------------|
| Default = 8080h                      |                                 |                                          |                         |                                  |                                     |                                |                                      |
| Reserved                             | JPEG Codec File Out Status (RO) | JPEG FIFO Threshold Status bits 1-0 (RO) |                         | Encode Size Limit Violation Flag | JPEG FIFO Threshold Trigger Flag    | JPEG FIFO Full Flag            | JPEG FIFO Empty Flag                 |
| 15                                   | 14                              | 13                                       | 12                      | 11                               | 10                                  | 9                              | 8                                    |
| Reserved                             |                                 | JPEG Decode Complete Flag                | Decode Marker Read Flag | Reserved                         | JPEG Line Buffer Overflow Flag (RO) | JPEG Codec Interrupt Flag (RO) | JPEG Line Buffer Interrupt Flag (RO) |
| 7                                    | 6                               | 5                                        | 4                       | 3                                | 2                                   | 1                              | 0                                    |

- bit 15                      Reserved  
The default value for this bit is 1.
- bit 14                      JPEG Codec File Out Status (Read Only)  
This bit indicates the status of the JPEG Codec output.  
When this bit = 1, the JPEG Codec is encoding or outputting encoded data.  
When this bit = 0, the JPEG Codec is not outputting encoded data.
- bits 13-12                JPEG FIFO Threshold Status bits [1:0] (Read Only)  
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size register (REG[09A4h]) for information on setting the JPEG FIFO size.

Table 10-67: JPEG FIFO Threshold Status

| REG[0982h] bits 13-12 | JPEG FIFO Threshold Status                       |
|-----------------------|--------------------------------------------------|
| 00                    | no data (same as empty)                          |
| 01                    | more than 4 bytes of data exist                  |
| 10                    | more than 1/4 of specified FIFO size data exists |
| 11                    | more than 1/2 of specified FIFO size data exists |

- bit 11                      Encode Size Limit Violation Flag  
This flag is asserted when the JPEG compressed data size is over the encode size limit as specified in the Encode Size Limit registers (REG[09B0h], REG[09B2h]). This flag is masked by the JPEG Encode Size Limit Violation Interrupt Enable bit and is only available when REG[0986h] bit 11 = 1.
- For Reads:  
When this bit = 1, an encode size limit violation has occurred.  
When this bit = 0, no violation has occurred.
- For Writes:  
When a 1 is written to this bit, the Encode Size Limit Violation Flag is cleared.  
When a 0 is written to this bit, there is no hardware effect.

**Note**  
The Encode Size Limit Violation Flag can only be cleared when an Encode Size Limit Violation no longer exists. This can be done by setting the Encode Size Limit to a value greater than the Encode Size Result (REG[09B0h] - REG[09B2h] > REG[09B4h] - REG[09B6h]), or by resetting the JPEG Module (REG[0980h] bit 7 = 1).

**Note**

For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.

bit 10

**JPEG FIFO Threshold Trigger Flag**

This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is masked by the JPEG FIFO Threshold Trigger Interrupt Enable bit and is only available when REG[0986h] bit 10 = 1.

**For Reads:**

When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.

When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.

**For Writes:**

When a 1 is written to this bit, the FIFO Threshold Trigger Flag is cleared.

When a 0 is written to this bit, there is no hardware effect.

**Note**

The JPEG FIFO Threshold Trigger Flag can only be cleared when a JPEG FIFO Threshold Trigger Flag condition no longer exists. This can be done by increasing the JPEG FIFO Threshold (REG[09A0h] bits 5-4), emptying the JPEG FIFO until it drops below the specified threshold, or by resetting the JPEG Module (REG[0980h] bit 7 = 1).

**Note**

For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.

bit 9

**JPEG FIFO Full Flag**

This flag is asserted when the JPEG FIFO is full. This flag is masked by the JPEG FIFO Full Interrupt Enable bit and is only available when REG[0986h] bit 9 = 1.

**For Reads:**

When this bit = 1, the JPEG FIFO is full.

When this bit = 0, the JPEG FIFO is not full.

**For Writes:**

When a 1 is written to this bit, the JPEG FIFO Full Flag is cleared.

When a 0 is written to this bit, there is no hardware effect.

**Note**

The JPEG FIFO Full Flag can only be cleared when the JPEG FIFO is no longer full, or after a JPEG Module Software Reset (REG[0980h] bit 7 = 1).

**Note**

For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 8 | <p>JPEG FIFO Empty Flag</p> <p>This flag is asserted when the JPEG FIFO is empty. This flag is masked by the JPEG FIFO Empty Interrupt Enable bit and is only available when REG[0986h] bit 8 = 1.</p> <p>For Reads:</p> <p>When this bit = 1, the JPEG FIFO is empty.</p> <p>When this bit = 0, the JPEG FIFO is not empty.</p> <p>For Writes:</p> <p>When a 1 is written to this bit, the JPEG FIFO Empty Flag is cleared.</p> <p>When a 0 is written to this bit, there is no hardware effect.</p> <p><b>Note</b></p> <p>The JPEG FIFO Empty Flag can only be cleared when the JPEG FIFO is no longer empty, or after a JPEG Module Software Reset (REG[0980h] bit 7 = 1).</p> <p><b>Note</b></p> <p>For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.</p>                                                                        |
| bit 7 | <p>Reserved</p> <p>The default value for this bit is 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| bit 6 | <p>Reserved</p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| bit 5 | <p>JPEG Decode Complete Flag</p> <p>This flag is asserted when the JPEG decode operation is finished. This flag is masked by the JPEG Decode Complete Interrupt Enable bit and is only available when REG[0986h] bit 5 = 1.</p> <p>For Reads:</p> <p>When this bit = 1, the JPEG decode operation is finished.</p> <p>When this bit = 0, the JPEG decode operation is not finished yet.</p> <p>For Writes:</p> <p>When a 1 is written to this bit, this bit is cleared.</p> <p>When a 0 is written to this bit, there is no hardware effect.</p> <p><b>Note</b></p> <p>When error detection is enabled (REG[101Ch] bits 1-0 = 01) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.</p> <p><b>Note</b></p> <p>For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.</p> |

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|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 4 | <p><b>Decode Marker Read Flag</b></p> <p>This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file. This flag is masked by the JPEG Decode Marker Read Interrupt Enable bit and is only available when REG[0986h] bit 4 = 1.</p> <p>When this bit = 1, a JPEG decode marker has been read.</p> <p>When this bit = 0, a JPEG decode marker has not been read.</p> <p>To clear this flag, disable the Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).</p> <p><b>Note</b></p> <p>For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.</p> |
| bit 3 | <p><b>Reserved</b></p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| bit 2 | <p><b>JPEG Line Buffer Overflow Flag (Read Only)</b></p> <p>This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is masked by the JPEG Line Buffer Overflow Interrupt Enable bit and is only available when REG[0986h] bit 2 = 1.</p> <p>When this bit = 1, a JPEG Line Buffer overflow has occurred.</p> <p>When this bit = 0, a JPEG Line Buffer overflow has not occurred.</p> <p>To clear this flag, perform a JPEG Software Reset (REG[0980h] bit 7 = 1).</p> <p><b>Note</b></p> <p>For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.</p>                                          |
| bit 1 | <p><b>JPEG Codec Interrupt Flag (Read Only)</b></p> <p>This flag is asserted when the JPEG codec generates an interrupt. This flag is masked by the JPEG Codec Interrupt Enable bit and is only available when REG[0986h] bit 1 = 1).</p> <p>When this bit = 1, the JPEG codec has generated an interrupt.</p> <p>When this bit = 0, the JPEG codec has not generated an interrupt.</p> <p>To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).</p> <p><b>Note</b></p> <p>For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 368.</p>                                                       |

## Registers

bit 0

JPEG Line Buffer Interrupt Flag (Read Only)

This bit is valid only when YUV Capture/Display or Host Decode/Encode mode is selected (REG[0980h] bits 3-1  $\neq$  000). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is used for YUV data transfers or Host Decode/Encode operations with interrupt handling. This flag is masked by the JPEG Line Buffer Interrupt Enable bit and is only available when REG[0986h] bit 0 = 1). This bit is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h].

When this bit = 1, the JPEG Line Buffer has generated an interrupt.

When this bit = 0, the JPEG Line Buffer has not generated an interrupt.

| REG[0984h] JPEG Raw Status Flag Register |                            |                                     |                                  |                                      |                                      |                               | Read Only                           |
|------------------------------------------|----------------------------|-------------------------------------|----------------------------------|--------------------------------------|--------------------------------------|-------------------------------|-------------------------------------|
| Default = 8180h                          |                            |                                     |                                  |                                      |                                      |                               |                                     |
| Reserved                                 | JPEG Codec File Out Status | JPEG FIFO Threshold Status bits 1-0 |                                  | Raw Encode Size Limit Violation Flag | Raw JPEG FIFO Threshold Trigger Flag | Raw JPEG FIFO Full Flag       | Raw JPEG FIFO Empty Flag            |
| 15                                       | 14                         | 13                                  | 12                               | 11                                   | 10                                   | 9                             | 8                                   |
| Reserved                                 |                            | Raw JPEG Decode Complete Flag       | Raw JPEG Decode Marker Read Flag | Reserved                             | Raw JPEG Line Buffer Overflow Flag   | Raw JPEG Codec Interrupt Flag | Raw JPEG Line Buffer Interrupt Flag |
| 7                                        | 6                          | 5                                   | 4                                | 3                                    | 2                                    | 1                             | 0                                   |

bit 15

Reserved

The default value for this bit is 1.

bit 14

JPEG Codec File Out Status (Read Only)

This bit provides the status of the JPEG Codec output.

When this bit = 1, the JPEG Codec is encoding or outputting encoded data.

When this bit = 0, the JPEG Codec is not outputting encoded data.

### Note

This bit has the same functionality as REG[0982h] bit 14.

bits 13-12

JPEG FIFO Threshold Status bits [1:0] (Read Only)

These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size Register (REG[09A4h]) for information on setting the JPEG FIFO Size.

Table 10-68: JPEG FIFO Threshold Status

| REG[0984h] bits 13-12 | JPEG FIFO Threshold Status                       |
|-----------------------|--------------------------------------------------|
| 00                    | no data (same as empty)                          |
| 01                    | more than 4 bytes of data exist                  |
| 10                    | more than 1/4 of specified FIFO size data exists |
| 11                    | more than 1/2 of specified FIFO size data exists |

### Note

These bits have the same functionality as REG[0982h] bits 13-12.

|                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 11                                                                                            | <p>Raw Encode Size Limit Violation Flag (Read Only)</p> <p>This flag is asserted when the JPEG encoded data size is over the size limit as specified in the Encode Size Limit registers (REG[09B02h] - REG[09B2h]). This flag is not affected by the JPEG Encode Size Limit Violation Interrupt Enable bit (REG[0986h] bit 11).</p> <p>When this bit = 1, an encode size limit violation has occurred.</p> <p>When this bit = 0, no violation has occurred.</p> <p>To clear this flag, write a 1 to the Encode Size Limit Violation Flag, REG[0982h] bit 11, when an Encode Size Limit Violation condition no longer exists. (i.e. Set the Encode Size Limit, REG[09B0h] and REG[09B2h] &gt; Encode Size Result, REG[09B4h] and REG[09B6h], or reset the JPEG Module, REG[0980h] bit 7 = 1.)</p>                                                                                                                 |
| bit 10                                                                                            | <p>Raw JPEG FIFO Threshold Trigger Flag (Read Only)</p> <p>This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0] bits 5-4). This flag is not affected by the JPEG FIFO Threshold Trigger Interrupt Enable bit (REG[0986h] bit 10).</p> <p>When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.</p> <p>When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.</p> <p>To clear this flag, write a 1 to the JPEG FIFO Threshold Trigger Flag, REG[0982] bit 10, when a JPEG FIFO Threshold Trigger condition no longer exists. (i.e. Set the JPEG FIFO Threshold in REG[09A0] bits [5:4] greater, empty the JPEG FIFO until it's level is below the specified threshold, or reset the JPEG Module, REG[0980] bit 7 = 1.)</p> |
| bit 9                                                                                             | <p>Raw JPEG FIFO Full Flag (Read Only)</p> <p>This flag is asserted when the JPEG FIFO is full. This flag is not affected by the JPEG FIFO Full Interrupt Enable bit (REG[0986h] bit 9).</p> <p>When this bit = 1, the JPEG FIFO is full.</p> <p>When this bit = 0, the JPEG FIFO is not full.</p> <p>To clear this flag, write a 1 to the JPEG FIFO Full Flag, REG[0982h] bit 9, when the JPEG FIFO is no longer full or after a JPEG Module reset, REG[0980h] bit 7 = 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| bit 8                                                                                             | <p>Raw JPEG FIFO Empty Flag (Read Only)</p> <p>This flag is asserted when the JPEG FIFO is empty. This flag is not affected by the JPEG FIFO Empty Interrupt Enable bit (REG[0986h] bit 8).</p> <p>When this bit = 1, the JPEG FIFO is empty.</p> <p>When this bit = 0, the JPEG FIFO is not empty.</p> <p>To clear this flag, write a 1 to the JPEG FIFO Empty Flag, REG[0982h] bit 8, when the JPEG FIFO is no longer empty or after a JPEG Module reset, REG[0980h] bit 7 = 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <p><b>Note</b></p> <p>This bit is not affected by the JPEG FIFO Clear bit (REG[09A0h] bit 2).</p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| bit 7                                                                                             | <p>Reserved</p> <p>The default value for this bit is 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| bit 6                                                                                             | <p>Reserved</p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 5 | <p>Raw JPEG Decode Complete Flag (Read Only)</p> <p>This flag is asserted when the JPEG decode operation is finished. This flag is not affected by the JPEG Decode Complete Interrupt Enable bit (REG[0986h] bit 5).</p> <p>When this bit = 1, the JPEG decode operation is finished.</p> <p>When this bit = 0, the JPEG decode operation is not finished yet.</p> <p>To clear this flag, write a 1 to the JPEG Decode Complete Flag (REG[0982h] bit 5 = 1).</p> <p><b>Note</b></p> <p>When error detection is enabled (REG[101Ch] bits 1-0 = 01) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.</p> |
| bit 4 | <p>Raw JPEG Decode Marker Read Flag (Read Only)</p> <p>This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file and when REG[0986h] bit 4 = 1.</p> <p>When this bit = 1, a JPEG decode marker has been read.</p> <p>When this bit = 0, a JPEG decode marker has not been read.</p> <p>To clear this flag, disable the JPEG Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).</p>                                                                                                                                                                                                                  |
| bit 3 | <p>Reserved</p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| bit 2 | <p>Raw JPEG Line Buffer Overflow Flag (Read Only)</p> <p>This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is not affected by the JPEG Line Buffer Overflow Interrupt Enable (REG[0986h] bit 2).</p> <p>When this bit = 1, a JPEG Line Buffer overflow has occurred.</p> <p>When this bit = 0, a JPEG Line Buffer overflow has not occurred.</p> <p>To clear this flag, perform a JPEG module software reset (REG[0980h] bit 7 = 1).</p>                                                                                                                                                                                                          |
| bit 1 | <p>Raw JPEG Codec Interrupt Flag (Read Only)</p> <p>This flag is asserted when an interrupt is generated by the JPEG codec. This flag is not affected by the JPEG Codec Interrupt Enable bit (REG[0986h] bit 1).</p> <p>When this bit = 1, the JPEG codec has generated an interrupt.</p> <p>When this bit = 0, no interrupt has been generated.</p> <p>To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).</p>                                                                                                                                                                                                                                   |
| bit 0 | <p>Raw JPEG Line Buffer Interrupt Flag</p> <p>This bit is valid only when YUV Capture/Display mode is selected (REG[0980h] bits 3-1 ≠ 000). This flag is not affected by the JPEG Line Buffer Interrupt Enable bit (REG[0986h] bit 0). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h].</p> <p>When this bit = 1, the JPEG Line Buffer has generated an interrupt.</p> <p>When this bit = 0, the JPEG Line Buffer has not generated an interrupt.</p>                                                                                                       |

| REG[0986h] JPEG Interrupt Control Register |    |                                       |                                     |                                              |                                              |                                 |                                   |
|--------------------------------------------|----|---------------------------------------|-------------------------------------|----------------------------------------------|----------------------------------------------|---------------------------------|-----------------------------------|
| Default = 0000h                            |    |                                       |                                     |                                              |                                              |                                 |                                   |
| Reserved                                   |    |                                       |                                     | Encode Size Limit Violation Interrupt Enable | JPEG FIFO Threshold Trigger Interrupt Enable | JPEG FIFO Full Interrupt Enable | JPEG FIFO Empty Interrupt Enable  |
| 15                                         | 14 | 13                                    | 12                                  | 11                                           | 10                                           | 9                               | 8                                 |
| Reserved                                   |    | JPEG Decode Complete Interrupt Enable | Decode Marker Read Interrupt Enable | Reserved                                     | JPEG Line Buffer Overflow Interrupt Enable   | JPEG Codec Interrupt Enable     | JPEG Line Buffer Interrupt Enable |
| 7                                          | 6  | 5                                     | 4                                   | 3                                            | 2                                            | 1                               | 0                                 |

- bits 15-12      Reserved  
The default value for these bits is 0.
- bit 11      Encode Size Limit Violation Interrupt Enable  
This bit controls the encode size limit violation interrupt. The status of this interrupt can be determined using the Encode Size Limit Violation Flag bit (REG[0982h] bit 11).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.
- bit 10      JPEG FIFO Threshold Trigger Interrupt Enable  
This bit controls the JPEG FIFO threshold trigger interrupt. The status of this interrupt can be determined using the JPEG FIFO Threshold Trigger Flag bit (REG[0982h] bit 10).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.
- bit 9      JPEG FIFO Full Interrupt Enable  
This bit controls the JPEG FIFO full interrupt. The status of this interrupt can be determined using the JPEG FIFO Full Flag bit (REG[0982h] bit 9).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.
- bit 8      JPEG FIFO Empty Interrupt Enable  
This bit controls the JPEG FIFO empty interrupt. The status of this interrupt can be determined using the JPEG FIFO Empty Flag bit (REG[0982h] bit 8).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.
- bit 7      Reserved  
The default value for this bit is 0.
- bit 6      Reserved  
The default value for this bit is 0.
- bit 5      JPEG Decode Complete Interrupt Enable  
This bit controls the JPEG decode complete interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag bit (REG[0982h] bit 5).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.

## Registers

---

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 4 | <p>JPEG Decode Marker Read Interrupt Enable</p> <p>This bit controls the JPEG decode marker read interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag (REG[0982h] bit 4).</p> <p>When this bit = 1, the interrupt is enabled.</p> <p>When this bit = 0, the interrupt is disabled.</p>                                                                                                                            |
| bit 3 | <p>Reserved</p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                |
| bit 2 | <p>JPEG Line Buffer Overflow Interrupt Enable</p> <p>This bit controls the JPEG line buffer overflow interrupt. The status of this interrupt can be determined using the Line Buffer Overflow Flag (REG[0982h] bit 2).</p> <p>When this bit = 1, the interrupt is enabled.</p> <p>When this bit = 0, the interrupt is disabled.</p>                                                                                                                        |
| bit 1 | <p>JPEG Codec Interrupt Enable</p> <p>This bit controls the JPEG codec interrupt. The status of this interrupt can be determined using the JPEG Codec Interrupt Flag (REG[0982h] bit 1).</p> <p>When this bit = 1, the interrupt is enabled.</p> <p>When this bit = 0, the interrupt is disabled.</p>                                                                                                                                                      |
| bit 0 | <p>JPEG Line Buffer Interrupt Enable</p> <p>This bit controls the JPEG Line Buffer Interrupt. The status of this interrupt can be determined using the JPEG Line Buffer Interrupt Flag (REG[0982h] bit 0).</p> <p>When this bit = 1, the interrupt is enabled.</p> <p>When this bit = 0, the interrupt is disabled.</p> <p>This bit should be disabled if YUV Data is not being input from host and then displayed (REG[0980h] bits 3-1 = 001 or 101).</p> |

### REG[0988h] is Reserved

This register is Reserved and should not be written.

| REG[098Ah] JPEG Code Start/Stop Control Register |    |    |    |     |    |    |   | Write Only              |
|--------------------------------------------------|----|----|----|-----|----|----|---|-------------------------|
| Default = 0000h                                  |    |    |    |     |    |    |   |                         |
| 15                                               | 14 | 13 | 12 | n/a | 11 | 10 | 9 | 8                       |
| n/a                                              |    |    |    |     |    |    |   | JPEG Start/Stop Control |
| 7                                                | 6  | 5  | 4  | 3   | 2  | 1  | 0 |                         |

bit 0                      JPEG Start/Stop Control (Write Only)  
 This bit controls the JPEG codec for both JPEG encode mode and YUV data capture (JPEG bypass) mode. This bit is not used for JPEG decoding.

For JPEG Encode:  
 When this bit is set to 1, the JPEG codec starts capturing the next frame and then stops.  
 When this bit is set to 0, the JPEG codec will be ready to capture from the next frame.

For YUV Data Capture (JPEG Bypass):  
 When this bit is set to 1, YUV data capturing starts from the next frame.  
 When this bit is set to 0, YUV data capturing stops at the end of the current frame.

**REG[098Ch] through REG[098Eh] are Reserved**

These registers are Reserved and should not be written.

10.4.16 JPEG FIFO Setting Register

| REG[09A0h] JPEG FIFO Control Register |    |                                      |    |          |                      |                          | Read/Write |
|---------------------------------------|----|--------------------------------------|----|----------|----------------------|--------------------------|------------|
| Default = 0000h                       |    |                                      |    |          |                      |                          |            |
| Reserved                              |    |                                      |    |          |                      |                          |            |
| 15                                    | 14 | 13                                   | 12 | 11       | 10                   | 9                        | 8          |
| Reserved                              |    | JPEG FIFO Trigger Threshold bits 1-0 |    | Reserved | JPEG FIFO Clear (WO) | JPEG FIFO Direction (RO) | n/a        |
| 7                                     | 6  | 5                                    | 4  | 3        | 2                    | 1                        | 0          |

- bits 15-6

Reserved  
The default value for these bits is 0.
- bits 5-4

JPEG FIFO Trigger Threshold bits[1:0]  
These bits set the JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10) when the specified conditions are met.

Table 10-69: JPEG FIFO Trigger Threshold Selection

| REG[09A0h] bits 5-4 | JPEG FIFO Trigger Threshold                                                                             |
|---------------------|---------------------------------------------------------------------------------------------------------|
| 00                  | Never trigger                                                                                           |
| 01                  | Trigger when the JPEG FIFO contains 4 bytes of data or more                                             |
| 10                  | Trigger when the JPEG FIFO contains more than 1/4 of the specified JPEG FIFO size (REG[09A4h] bits 3-0) |
| 11                  | Trigger when the JPEG FIFO contains more than 1/2 of the specified JPEG FIFO size (REG[09A4h] bits 3-0) |

- bit 3

Reserved  
The default value for this bit is 0.

bit 2                      JPEG FIFO Clear (Write Only)

This bit clears the JPEG FIFO. It is recommended that the JPEG module should also be reset (REG[0980h] bit 7 = 1) when the JPEG FIFO is cleared.

When this bit = 1, the JPEG FIFO, the JPEG FIFO Read/Write Pointer registers (REG[09AAh]-[09ACh]), and the JPEG FIFO Valid Data Size registers (REG[09A8h] are cleared.

When this bit = 0, there is no hardware effect.

The following sequence is used clear the JPEG FIFO.

- 1. Clear the JPEG FIFO, REG[09A0h] bit 2 = 1.
- 2. Perform 2 dummy reads from REG[09A6h] to ensure that the JPEG FIFO is empty.
- 3. Reset the JPEG module, REG[0980h] bit 7 = 1.

**Note**

Clearing the JPEG FIFO using this bit has no effect on the Raw JPEG FIFO Empty Flag (REG[0984h] bit 8).

**Note**

This bit only clears the JPEG FIFO and does not clear the JPEG Line Buffer. For details on using the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 367.

bit 1                      JPEG FIFO Direction Bit (Read Only)

This bit indicates the configuration of the JPEG FIFO.

When this bit = 1, the JPEG FIFO is configured to transmit (decode process).

When this bit = 0, the JPEG FIFO is configured to receive (encode process).

| REG[09A2h] JPEG FIFO Status Register |    |    |    |                                     |    |                       |                        |
|--------------------------------------|----|----|----|-------------------------------------|----|-----------------------|------------------------|
| Default = 8001h                      |    |    |    |                                     |    |                       | Read Only              |
| Reserved<br>15                       | 14 | 13 | 12 | n/a<br>11                           | 10 | 9                     | 8                      |
| Reserved                             |    |    |    | JPEG FIFO Threshold Status bits 1-0 |    | JPEG FIFO Full Status | JPEG FIFO Empty Status |
| 7                                    | 6  | 5  | 4  | 3                                   | 2  | 1                     | 0                      |

bit 15                      Reserved

The default value for this bit is 0.

bits 3-2                      JPEG FIFO Threshold Status bits [1:0] (Read Only)  
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size register (REG[09A4h]) for information on setting the JPEG FIFO size.

Table 10-70: JPEG FIFO Threshold Status

| REG[09A2h] bits 3-2 | JPEG FIFO Threshold Status                       |
|---------------------|--------------------------------------------------|
| 00                  | no data (same as empty)                          |
| 01                  | more than 4 bytes of data exist                  |
| 10                  | more than 1/4 of specified FIFO size data exists |
| 11                  | more than 1/2 of specified FIFO size data exists |

**Note**  
These bits have the same functionality as REG[0982h] bits 13-12.

bit 1                      JPEG FIFO Full Status (Read Only)  
This bit indicates whether the JPEG FIFO is full.  
When this bit = 1, the JPEG FIFO is full.  
When this bit = 0, the JPEG FIFO is not full.

bit 0                      JPEG FIFO Empty Status (Read Only)  
This bit indicates that the JPEG FIFO is empty.  
When this bit = 1, the JPEG FIFO is empty.  
When this bit = 0, the JPEG FIFO is not empty.

| REG[09A4h] JPEG FIFO Size Register |    |    |                         |    |    |   |   | Read/Write |
|------------------------------------|----|----|-------------------------|----|----|---|---|------------|
| Default = 0000h                    |    |    |                         |    |    |   |   |            |
| Reserved                           |    |    |                         |    |    |   |   |            |
| 15                                 | 14 | 13 | 12                      | 11 | 10 | 9 | 8 |            |
| Reserved                           |    |    | JPEG FIFO Size bits 4-0 |    |    |   |   |            |
| 7                                  | 6  | 5  | 4                       | 3  | 2  | 1 | 0 |            |

bits 15-5                      Reserved  
The default value for these bits is 0.

bits 4-0                      JPEG FIFO Size bits [4:0]  
These bits determine the JPEG FIFO size in 4K byte units. The maximum size of the JPEG FIFO is 128K bytes. These bits also specify the amount of memory reserved for the JPEG FIFO.

JPEG FIFO size = (REG[09A4h] bits 4-0 + 1) x 4K bytes

**Note**  
For further information on S1D13715 memory mapping, see Section 8, “Memory Allocation” on page 118.

| <b>REG[09A6h] JPEG FIFO Read/Write Port Register</b> |    |    |    |    |    |   |   |
|------------------------------------------------------|----|----|----|----|----|---|---|
| Default = Not Applicable                             |    |    |    |    |    |   |   |
| Read/Write                                           |    |    |    |    |    |   |   |
| JPEG FIFO Read/Write Port bits 15-8                  |    |    |    |    |    |   |   |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| JPEG FIFO Read/Write Port bits 7-0                   |    |    |    |    |    |   |   |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

JPEG FIFO Read/Write Port bits[15:0]

These bits are the access port for the JPEG FIFO. The current address pointed to by the port can be determined using the JPEG FIFO Read Pointer register (REG[09AAh]) and the JPEG FIFO Write Pointer register (REG[09ACh]).

When JPEG encoding is selected, these bits are used as the JPEG FIFO read data port. When JPEG decoding is selected, these bits are used as the JPEG FIFO write data port. When YUV data is output to the Host interface (REG[0980] bits 3-1 = 011 or 111), these bits are used as the JPEG FIFO read data port.

**Note**

Since the JPEG FIFO is 32 bits wide and the Host CPU interface is 16 bits wide, this register must be accessed an even number of times.

| <b>REG[09A8h] JPEG FIFO Valid Data Size Register</b> |    |    |    |    |    |   |   |
|------------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                      |    |    |    |    |    |   |   |
| Read Only                                            |    |    |    |    |    |   |   |
| JPEG FIFO Valid Data Size bits 15-8                  |    |    |    |    |    |   |   |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| JPEG FIFO Valid Data Size bits 7-0                   |    |    |    |    |    |   |   |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

JPEG FIFO Valid Data Size bits[15:0] (Read Only)

These bits indicate the valid data size in 32-bit units which can be read from the JPEG FIFO. If the JPEG file size is not aligned on 32-bit boundaries, the JPEG FIFO may contain more data (1 to 3 bytes) than the indicated size. See the Encode Size Result registers (REG[09B4h]-[09B6h]) to determine the correct data size.

| <b>REG[09AAh] JPEG FIFO Read Pointer Register</b> |    |    |    |    |    |   |   |
|---------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                                   |    |    |    |    |    |   |   |
| Read Only                                         |    |    |    |    |    |   |   |
| JPEG FIFO Read Pointer bits 15-8                  |    |    |    |    |    |   |   |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| JPEG FIFO Read Pointer bits 7-0                   |    |    |    |    |    |   |   |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

JPEG FIFO Read Pointer bits[15:0] (Read Only)

These bits are used during evaluation and are for reference only. These bits indicate the 32-bit read pointer into the JPEG FIFO. The read pointer is automatically incremented when either a read or write to/from the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 367.

| REG[09ACh] JPEG FIFO Write Pointer Register |    |    |    |    |    |   |   |
|---------------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                             |    |    |    |    |    |   |   |
| Read Only                                   |    |    |    |    |    |   |   |
| JPEG FIFO Write Pointer bits 15-8           |    |    |    |    |    |   |   |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| JPEG FIFO Write Pointer bits 7-0            |    |    |    |    |    |   |   |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-0

JPEG FIFO Write Pointer bits[15:0] (Read Only)  
These bits are used during evaluation and are for reference only. These bits indicate the 32-bit write pointer into the JPEG FIFO. The write pointer is automatically incremented when a write to the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 367.

| REG[09B0h] Encode Size Limit Register 0 |    |    |    |    |    |   |   |
|-----------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                         |    |    |    |    |    |   |   |
| Read/Write                              |    |    |    |    |    |   |   |
| Encode Size Limit bits 15-8             |    |    |    |    |    |   |   |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Encode Size Limit bits 7-0              |    |    |    |    |    |   |   |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

| REG[09B2h] Encode Size Limit Register 1 |    |    |    |    |    |   |   |
|-----------------------------------------|----|----|----|----|----|---|---|
| Default = 0000h                         |    |    |    |    |    |   |   |
| Read/Write                              |    |    |    |    |    |   |   |
| n/a                                     |    |    |    |    |    |   |   |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Encode Size Limit bits 23-16            |    |    |    |    |    |   |   |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[09B2h] bits 7-0

REG[09B0h] bits 15-0 Encode Size Limit bits[23:0]  
**These bits are required for the JPEG encode process only.** These bits specify the data size limit, in bytes, for the encoded JPEG file.

Note

Setting these registers to 0 will disable the Encode Size Limit Violation function and REG[0984h] bit 11 will not be set.

| REG[09B4h] Encode Size Result Register 0 |    |    |    |    |    |   |   | Read Only |
|------------------------------------------|----|----|----|----|----|---|---|-----------|
| Default = 0000h                          |    |    |    |    |    |   |   |           |
| Encode Size Result bits 15-8             |    |    |    |    |    |   |   |           |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |           |
| Encode Size Result bits 7-0              |    |    |    |    |    |   |   |           |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |           |

| REG[09B6h] Encode Size Result Register 1 |    |    |    |    |    |   |   | Read Only |
|------------------------------------------|----|----|----|----|----|---|---|-----------|
| Default = 0000h                          |    |    |    |    |    |   |   |           |
| n/a                                      |    |    |    |    |    |   |   |           |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |           |
| Encode Size Result bits 23-16            |    |    |    |    |    |   |   |           |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |           |

REG[09B6h] bits 7-0

REG[09B4h] bits 15-0 Encode Size Result bits[23:0] (Read Only)

**These bits are required for the JPEG encode process only.** These bits indicate the data size result, in bytes, for the encoded JPEG file.

| REG[09B8h] JPEG File Size Register 0 |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                      |    |    |    |    |    |   |   |            |
| JPEG File Size bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| JPEG File Size bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[09BAh] JPEG File Size Register 1 |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                      |    |    |    |    |    |   |   |            |
| n/a                                  |    |    |    |    |    |   |   |            |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| JPEG File Size bits 23-16            |    |    |    |    |    |   |   |            |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[09BAh] bits 7-0

REG[09B8h] bits 15-0 JPEG File Size bits[23:0]

**These bits are required for the JPEG decode process only.** These bits specify the JPEG file size in bytes and must be set before the Host begins writing decoded data to the JPEG FIFO.

## REG[09BCh] is Reserved

This register is Reserved and should not be written.

## 10.4.17 JPEG Line Buffer Setting Register

| REG[09C0h] JPEG Line Buffer Status Flag Register |    |    |    |    |                            |                            |                             | Read/Write |
|--------------------------------------------------|----|----|----|----|----------------------------|----------------------------|-----------------------------|------------|
| Default = 0000h                                  |    |    |    |    |                            |                            |                             |            |
| 15                                               | 14 | 13 | 12 | 11 | 10                         | 9                          | 8                           |            |
| n/a                                              |    |    |    |    | JPEG Line Buffer Full Flag | JPEG Line Buffer Half Flag | JPEG Line Buffer Empty Flag |            |
| 7                                                | 6  | 5  | 4  | 3  | 2                          | 1                          | 0                           |            |

bit 2

### JPEG Line Buffer Full Flag

This flag is asserted when the JPEG Line Buffer becomes full. This flag is masked by the JPEG Line Buffer Full Interrupt Enable bit and is only available when REG[09C6h] bit 2 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000).

When this bit = 1, the JPEG Line Buffer is full.

When this bit = 0, the JPEG Line Buffer is not full.

To clear this flag, when the JPEG Line Buffer is not full, write a 1 to this bit.

bit 1

### JPEG Line Buffer Half Full Flag

This flag is asserted when the JPEG Line Buffer has become half full. This flag is masked by the JPEG Line Buffer Half Full Interrupt Enable bit and is only available when REG[09C6h] bit 1 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000).

When this bit = 1, the JPEG Line Buffer is half full.

When this bit = 0, the JPEG Line Buffer is not half full.

To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to this bit.

bit 0

### JPEG Line Buffer Empty Flag

This flag is asserted when the JPEG Line Buffer contains less than or equal to 16 bytes of YUV 4:2:2 data or 8 bytes of YUV 4:2:0 data. This flag is masked by the JPEG Line Buffer Empty Interrupt Enable bit and is only available when REG[09C6h] bit 0 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000).

When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.

When this bit = 0, the JPEG Line Buffer is not empty.

To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to this bit.

| REG[09C2h] JPEG Line Buffer Raw Status Flag Register |    |    |    |    |                                |                                |                                 |  |  |
|------------------------------------------------------|----|----|----|----|--------------------------------|--------------------------------|---------------------------------|--|--|
| Default = 0000h                                      |    |    |    |    |                                |                                |                                 |  |  |
| Read Only                                            |    |    |    |    |                                |                                |                                 |  |  |
| n/a                                                  |    |    |    |    |                                |                                |                                 |  |  |
| 15                                                   | 14 | 13 | 12 | 11 | 10                             | 9                              | 8                               |  |  |
| n/a                                                  |    |    |    |    | Raw JPEG Line Buffer Full Flag | Raw JPEG Line Buffer Half Flag | Raw JPEG Line Buffer Empty Flag |  |  |
| 7                                                    | 6  | 5  | 4  | 3  | 2                              | 1                              | 0                               |  |  |

- bit 2      Raw JPEG Line Buffer Full Flag (Read Only)  
 This flag is asserted when the JPEG Line Buffer becomes full. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2). This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1  $\neq$  000).  
 When this bit = 0, the JPEG Line Buffer is not half full.  
 When this bit = 1, the JPEG Line Buffer is full.  
 When this bit = 0, the JPEG Line Buffer is not full.
- To clear this flag, when the JPEG Line Buffer is not full, write a 1 to REG[09C0h] bit 2.
- bit 1      Raw JPEG Line Buffer Half Full Flag (Read Only)  
 This flag is asserted when the JPEG Line Buffer becomes half full. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1). This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1  $\neq$  000).  
 When this bit = 0, the JPEG Line Buffer is not half full.  
 When this bit = 1, the JPEG Line Buffer is half full.  
 When this bit = 0, the JPEG Line Buffer is not half full.
- To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to REG[09C0h] bit 1.
- bit 0      Raw JPEG Line Buffer Empty Flag (Read Only)  
 This flag is asserted when the JPEG Line Buffer contains less than or equal to 16 bytes of YUV 4:2:2 data or 8 bytes of YUV 4:2:0 data. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0). This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1  $\neq$  000).  
 When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.  
 When this bit = 0, the JPEG Line Buffer is not empty
- To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to REG[09C0h] bit 0.

| REG[09C4h] JPEG Line Buffer Raw Current Status Register |                |                |                |                |                                               |                                                    |                                                |
|---------------------------------------------------------|----------------|----------------|----------------|----------------|-----------------------------------------------|----------------------------------------------------|------------------------------------------------|
| Default = F001h                                         |                |                |                |                |                                               |                                                    | Read Only                                      |
| Reserved<br>15                                          | Reserved<br>14 | Reserved<br>13 | Reserved<br>12 | Reserved<br>11 | Reserved<br>10                                | Reserved<br>9                                      | Reserved<br>8                                  |
| Reserved<br>7                                           | n/a            |                |                |                | Raw JPEG Line Buffer Full Current Status<br>2 | Raw JPEG Line Buffer Half Full Current Status<br>1 | Raw JPEG Line Buffer Empty Current Status<br>0 |

- bits 15-7      Reserved  
The default value for bits 15 - 12 is 1 and the default value for bits 11 - 8 is 0.
- bit 2      Raw JPEG Line Buffer Full Current Status (Read Only)  
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2).  
When this bit = 1, the JPEG Line Buffer is full.  
When this bit = 0, the JPEG Line Buffer is not full.
- bit 1      Raw JPEG Line Buffer Half Full Current Status (Read Only)  
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1).  
When this bit = 1, the JPEG Line Buffer is half full.  
When this bit = 0, the JPEG Line Buffer is not half full.
- bit 0      Raw Line Buffer Empty Current Status (Read Only)  
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0).  
When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.  
When this bit = 0, the JPEG Line Buffer is not empty.

| REG[09C6h] JPEG Line Buffer Interrupt Control Register |    |    |    |    |                                             |                                                  |                                              |
|--------------------------------------------------------|----|----|----|----|---------------------------------------------|--------------------------------------------------|----------------------------------------------|
| Default = 0000h                                        |    |    |    |    |                                             |                                                  | Read/Write                                   |
| n/a                                                    |    |    |    |    |                                             |                                                  |                                              |
| 15                                                     | 14 | 13 | 12 | 11 | 10                                          | 9                                                | 8                                            |
| n/a                                                    |    |    |    |    | JPEG Line Buffer Full Interrupt Enable<br>2 | JPEG Line Buffer Half Full Interrupt Enable<br>1 | JPEG Line Buffer Empty Interrupt Enable<br>0 |
| 7                                                      | 6  | 5  | 4  | 3  |                                             |                                                  |                                              |

- bit 2      JPEG Line Buffer Full Interrupt Enable  
This bit controls the JPEG Line Buffer Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Full Flag (REG[09C0h] bit 2).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.
- bit 1      JPEG Line Buffer Half Full Interrupt Enable  
This bit controls the JPEG Line Buffer Half Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Half Full Flag (REG[09C0h] bit 1).  
When this bit = 1, the interrupt is enabled.  
When this bit = 0, the interrupt is disabled.

- bit 0                      JPEG Line Buffer Empty Interrupt Enable  
 This bit controls the JPEG Line Buffer Empty Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0).  
 When this bit = 1, the interrupt is enabled.  
 When this bit = 0, the interrupt is disabled.

### REG[09C8h] through REG[09CEh] are Reserved

These registers are Reserved and should not be written.

| REG[09D0h] JPEG Line Buffer Configuration Register        |    |    |    |          |                                                 |   |   |
|-----------------------------------------------------------|----|----|----|----------|-------------------------------------------------|---|---|
| Default = 2800h                                           |    |    |    |          |                                                 |   |   |
| Read/Write                                                |    |    |    |          |                                                 |   |   |
| JPEG Line Buffer Raw Horizontal Pixel Size bits 10-4 (RO) |    |    |    |          |                                                 |   |   |
| Reserved                                                  | 14 | 13 | 12 | 11       | 10                                              | 9 | 8 |
| 15                                                        |    |    |    |          |                                                 |   |   |
| JPEG Line Buffer Raw Horizontal Pixel Size bits 3-0 (RO)  |    |    |    | Reserved | JPEG Line Buffer Horizontal Pixel Size bits 2-0 |   |   |
| 7                                                         | 6  | 5  | 4  | 3        | 2                                               | 1 | 0 |

- bit 15                      Reserved  
 The default value for this bit is 0.
- bits 14-4                  JPEG Line Buffer Raw Horizontal Pixel Size bits [10:0] (Read Only)  
 These bits provide actual number of the horizontal pixel size supported by the JPEG Line Buffer as set in REG[09D0h] bits 2-0.
- bit 3                        Reserved  
 The default value for this bit is 0.
- bits 2-0                    JPEG Line Buffer Horizontal Pixel Size bits [2:0]  
 1600These bits indicate the horizontal pixel size supported by the JPEG Line Buffer.

Table 10-71: Supported Horizontal Pixel Size

| REG[09D0h] bits 2-0 | Supported Horizontal Pixel Size | Line Buffer Size |
|---------------------|---------------------------------|------------------|
| 000                 | VGA (640)                       | 30k Bytes        |
| 001                 | SVGA (800)                      | 38k Bytes        |
| 010                 | XGA (1024)                      | 48k Bytes        |
| 011                 | SXGA (1280)                     | 60k Bytes        |
| 100                 | UXGA (1600)                     | 75k Bytes        |
| 101 - 111           | Reserved                        |                  |

| REG[09D2h] JPEG Line Buffer Address Offset Register |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = 0060h                                     |    |    |    |    |    |   |   |
| Read/Write                                          |    |    |    |    |    |   |   |
| Reserved                                            |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| JPEG Line Buffer Address Offset bits 6-0            |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

bits 15-7

Reserved

The default value for these bits is 0.

bits 6-0

JPEG Line Buffer Address Offset bits [6:0]

These bits provide the address offset of the JPEG Line Buffer, and therefore the size (default is 256 bytes), as follows.

$\text{REG}[09D2h] \text{ bits } 6-0 = [(128 \times 1024) - (\text{XSize} \times 2 \times 24 \times F)] \gg 10$

$\text{Offset Value}(h) = (\text{REG}[09C2h] \text{ bits } 6-0) \ll 10 + 30000h$

Where:

XSize = Horizontal Size = 640 | 800 | 1024 | 1280 | 1600

F (YUV format) = 1 (4:2:0 & 4:4:4) | 0.75 (4:2:2) | 0.5 (4:1:1)

$\gg 10$  represents a 10 bit, shift right operator

$\ll 10$  represents a 10 bit, shift left operator

### Note

YUV 4:4:4 format is possible for JPEG decoding only.

Table 10-72: Line Buffer Address Offset Examples

| Horizontal Size (XSIZE) | K Bytes | REG[09D2h] Value | Offset Value | Area            |
|-------------------------|---------|------------------|--------------|-----------------|
| 1600                    | 75      | 35h              | 3D400h       | 3D400h - 4FFFFh |
| 1280                    | 60      | 44h              | 41000h       | 41000h - 4FFFFh |
| 1024                    | 48      | 50h              | 44000h       | 44000h - 4FFFFh |
| 800                     | 38      | 5Ah              | 46800h       | 46800h - 4FFFFh |
| 640                     | 30      | 62h              | 48800h       | 48800h - 4FFFFh |

### REG[09D4h] through REG[09DEh] are Reserved

These registers are Reserved and should not be written.

| REG[09E0h] JPEG Line Buffer Read/Write Port Register |    |    |    |    |    |   |            |
|------------------------------------------------------|----|----|----|----|----|---|------------|
| Default = 0000h                                      |    |    |    |    |    |   |            |
|                                                      |    |    |    |    |    |   | Read/Write |
| JPEG Line Buffer Read/Write Port bits 15-8           |    |    |    |    |    |   |            |
| 15                                                   | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| JPEG Line Buffer Read/Write Port bits 7-0            |    |    |    |    |    |   |            |
| 7                                                    | 6  | 5  | 4  | 3  | 2  | 1 | 0          |

bits 15-0

JPEG Line Buffer Read/Write Port bits [15:0]

If YUV data is being input from the Host, these bits are used as the JPEG Line Buffer read/write port. For all other modes, these bits have no hardware effect.

When YUV data is input from Host I/F (REG[0980] bits 3-1 = 001b or 101b), this port becomes the JPEG Line Buffer write port.

When encoded YUV data is input from Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer write port.

When decoded YUV data is output to Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer read port.

## 10.4.18 Interrupt Control Registers

| REG[0A00h] Interrupt Status Register |    |    |                       |                         |                       |                         |                        |
|--------------------------------------|----|----|-----------------------|-------------------------|-----------------------|-------------------------|------------------------|
| Default = 0000h                      |    |    |                       |                         |                       |                         |                        |
| Read Only                            |    |    |                       |                         |                       |                         |                        |
| n/a                                  |    |    |                       |                         |                       |                         |                        |
| 15                                   | 14 | 13 | 12                    | 11                      | 10                    | 9                       | 8                      |
| n/a                                  |    |    | Host Interrupt Status | Camera Interrupt Status | JPEG Interrupt Status | BitBLT Interrupt Status | Debug Interrupt Status |
| 7                                    | 6  | 5  | 4                     | 3                       | 2                     | 1                       | 0                      |

- bit 4      Host Interrupt Status (Read Only)  
This bit indicates the status of the Host interrupt.  
When this bit = 0, no Host interrupt has occurred.  
When this bit = 1, a Host interrupt has occurred. Status flags must be read in REG[0A0Ah] to determine the exact nature of the interrupt.
- bit 3      Camera Interrupt Status (Read Only)  
This bit indicates the status of the Camera Interrupt.  
When this bit = 0, no Camera interrupt has occurred.  
When this bit = 1, a Camera interrupt has occurred. Status flags must be read in REG[0116h] to determine the exact nature of the interrupt.
- bit 2      JPEG Interrupt Status (Read Only)  
This bit indicates the status of the JPEG Interrupt.  
When this bit = 0, no JPEG interrupt has occurred.  
When this bit = 1, a JPEG interrupt has occurred. Status flags must be read in REG[0982h] to determine the exact nature of the interrupt.
- bit 1      BitBLT Interrupt Status (Read Only)  
This bit indicates the status of the BitBLT Interrupt.  
When this bit = 0, no BitBLT interrupt has occurred.  
When this bit = 1, a BitBLT interrupt has occurred. Status flags must be read in REG[8030h] to determine the exact nature of the interrupt.
- bit 0      Debug Interrupt Status (Read Only)  
This bit indicates the status of the Debug Interrupt.  
When this bit = 0, no Debug interrupt has occurred.  
When this bit = 1, a Debug interrupt has occurred. Status flags must be read in REG[0A06h] to determine the exact nature of the interrupt.

| REG[0A02h] Interrupt Control Register 0 |    |    |                       |                         |                       |                         |                        |
|-----------------------------------------|----|----|-----------------------|-------------------------|-----------------------|-------------------------|------------------------|
| Default = 0000h                         |    |    |                       |                         |                       |                         |                        |
| Read/Write                              |    |    |                       |                         |                       |                         |                        |
| n/a                                     |    |    |                       |                         |                       |                         |                        |
| 15                                      | 14 | 13 | 12                    | 11                      | 10                    | 9                       | 8                      |
| n/a                                     |    |    | Host Interrupt Enable | Camera Interrupt Enable | JPEG Interrupt Enable | BitBLT Interrupt Enable | Debug Interrupt Enable |
| 7                                       | 6  | 5  | 4                     | 3                       | 2                     | 1                       | 0                      |

- bit 4      Host Interrupt Enable  
This bit controls the Host interface interrupt.  
When this bit = 0, the interrupt is disabled.  
When this bit = 1, the interrupt is enabled.

- bit 3      Camera Interrupt Enable  
This bit controls the Camera interface interrupt.  
When this bit = 0, the interrupt is disabled.  
When this bit = 1, the interrupt is enabled.
- bit 2      JPEG Interrupt Enable  
This bit controls the JPEG codec interrupt.  
When this bit = 0, the interrupt is disabled.  
When this bit = 1, the interrupt is enabled.
- bit 1      BitBLT Interrupt Enable  
This bit controls the BitBLT interrupt.  
When this bit = 0, the interrupt is disabled.  
When this bit = 1, the interrupt is enabled.
- bit 0      Debug Interrupt Enable  
This bit controls the debug interrupt.  
When this bit = 0, the interrupt is disabled.  
When this bit = 1, the interrupt is enabled.

| REG[0A04h] Interrupt Control Register 1 |    |    |                       |                         |                       |                         |                        | Read/Write |
|-----------------------------------------|----|----|-----------------------|-------------------------|-----------------------|-------------------------|------------------------|------------|
| Default = 0000h                         |    |    |                       |                         |                       |                         |                        |            |
| n/a                                     |    |    |                       |                         |                       |                         |                        |            |
| 15                                      | 14 | 13 | 12                    | 11                      | 10                    | 9                       | 8                      |            |
| n/a                                     |    |    | Host Manual Interrupt | Camera Manual Interrupt | JPEG Manual Interrupt | BitBLT Manual Interrupt | Debug Manual Interrupt |            |
| 7                                       | 6  | 5  | 4                     | 3                       | 2                     | 1                       | 0                      |            |

- bit 4      Host Manual Interrupt  
This bit manually sets a Host interface interrupt.  
When this bit = 0, the interrupt is cleared.  
When this bit = 1, the interrupt is asserted.
- bit 3      Camera Manual Interrupt  
This bit manually sets a Camera interface interrupt.  
When this bit = 0, the interrupt is cleared.  
When this bit = 1, the interrupt is asserted.
- bit 2      JPEG Manual Interrupt  
This bit manually sets a JPEG codec interrupt.  
When this bit = 0, the interrupt is cleared.  
When this bit = 1, the interrupt is asserted.
- bit 1      BitBLT Manual Interrupt  
This bit manually sets a BitBLT interrupt.  
When this bit = 0, the interrupt is cleared.  
When this bit = 1, the interrupt is asserted.
- bit 0      Debug Manual Interrupt  
This bit manually sets a debug interrupt.  
When this bit = 0, the interrupt is cleared.  
When this bit = 1, the interrupt is asserted.

| REG[0A06h] Debug Status Register |    |    |    |    |    |                         |                                    |
|----------------------------------|----|----|----|----|----|-------------------------|------------------------------------|
| Default = 0000h                  |    |    |    |    |    |                         |                                    |
| Read/Write                       |    |    |    |    |    |                         |                                    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9                       | 8                                  |
| n/a                              |    |    |    |    |    | Display FIFO Empty Flag | YUV/RGB Write Buffer Overflow Flag |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1                       | 0                                  |

bit 1

## Display FIFO Empty Flag

This flag is not masked and indicates whether the panel interface has attempted to read data from the display FIFO while it is empty. This flag can be used to generate an interrupt (INT signal) to the Host by setting both the Display FIFO Empty Interrupt Enable (REG[0A08h] bit 1 = 1) and the Debug Interrupt Enable (REG[0A02h] bit 0 = 1).

For Reads:

When this bit = 1, the panel interface has attempted to read data from the display FIFO while it is empty.

When this bit = 0, the panel interface has not attempted to read data from the display FIFO while it is empty.

For Writes:

When this bit is written as 1, the Display FIFO Empty Flag is cleared.

When this bit is written as 0, there is no hardware effect.

bit 0

## YUV/RGB Write Buffer Overflow Flag

For Reads:

When this bit = 1, a write buffer overflow has occurred in the path from the YUV/RGB converter to the display buffer.

When this bit = 0, no write buffer overflow has occurred.

For Writes:

When this bit is written as 1, the YUV/RGB write buffer overflow flag is cleared.

When this bit is written as 0, there is no hardware effect.

| REG[0A08h] Interrupt Control for Debug Register |    |    |    |    |    |                                     |                                                |
|-------------------------------------------------|----|----|----|----|----|-------------------------------------|------------------------------------------------|
| Default = 0000h                                 |    |    |    |    |    |                                     |                                                |
| Read/Write                                      |    |    |    |    |    |                                     |                                                |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9                                   | 8                                              |
| n/a                                             |    |    |    |    |    | Display FIFO Empty Interrupt Enable | YUV/RGB Write Buffer Overflow Interrupt Enable |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1                                   | 0                                              |

bit 1

## Display FIFO Empty Interrupt Enable

This bit controls the display FIFO empty interrupt.

When this bit = 1, the display FIFO empty interrupt is enabled

When this bit = 0, the display FIFO empty interrupt is disabled.

bit 0 YUV/RGB Write Buffer Overflow Interrupt Enable  
 This bit controls the YUV/RGB write buffer overflow flag interrupt output.  
 When this bit = 0, the YUV/RGB write buffer overflow interrupt is disabled.  
 When this bit = 1, the YUV/RGB write buffer overflow interrupt is enabled

| REG[0A0Ah] Host Cycle Interrupt Status Register |     |                                                                 |                                                                |                                                                      |                                                                     |                                                               |          |
|-------------------------------------------------|-----|-----------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------|----------|
| Default = 0000h                                 |     |                                                                 |                                                                |                                                                      |                                                                     |                                                               |          |
| Read/Write                                      |     |                                                                 |                                                                |                                                                      |                                                                     |                                                               |          |
| Cycle Time Out<br>Interrupt Raw Status          | n/a |                                                                 |                                                                |                                                                      |                                                                     |                                                               |          |
| 15                                              | 14  | 13                                                              | 12                                                             | 11                                                                   | 10                                                                  | 9                                                             | 8        |
| n/a                                             |     | BitBLT FIFO<br>Terminate Write<br>Cycle Interrupt<br>Raw Status | BitBLT FIFO<br>Terminate Read<br>Cycle Interrupt<br>Raw Status | JPEG Line Buffer<br>Terminate Write<br>Cycle Interrupt<br>Raw Status | JPEG Line Buffer<br>Terminate Read<br>Cycle Interrupt<br>Raw Status | JPEG FIFO<br>Terminate Write<br>Cycle Interrupt<br>Raw Status | Reserved |
| 7                                               | 6   | 5                                                               | 4                                                              | 3                                                                    | 2                                                                   | 1                                                             | 0        |

bit 15 Cycle Time Out Interrupt Raw Status  
 This bit indicates the raw status of the Cycle Time Out Interrupt which happens when an access cycle to/from the JPEG FIFO, JPEG Line Buffer, or BitBLT FIFO lasts longer than the specified Time Out Value (REG[0A0Eh] bits 4-0). If a Cycle Time Out Interrupt occurs and the Cycle Time Out Interrupt is enabled (REG[0A0Ch] bit 15 = 1) and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.  
 When this bit = 1, a Cycle Time Out Interrupt has occurred.  
 When this bit = 0, a interrupt has not occurred.

To clear this bit, write a 1 to this bit.

bit 5 BitBLT FIFO Terminate Write Cycle Interrupt Raw Status  
 This bit indicates the status of the BitBLT FIFO Terminate Write Cycle Interrupt.  
 When this bit = 1, a BitBLT FIFO Terminate Write Cycle Interrupt has occurred.  
 When this bit = 0, no interrupt has occurred.

To clear this bit, write this bit as 1.

bit 4 BitBLT FIFO Terminate Read Cycle Interrupt Raw Status  
 This bit indicates the status of the BitBLT FIFO Terminate Read Cycle Interrupt.  
 When this bit = 1, a BitBLT FIFO Terminate Read Cycle Interrupt has occurred.  
 When this bit = 0, no interrupt has occurred.

To clear this bit, write this bit as 1.

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 3 | <p>JPEG Line Buffer Terminate Write Cycle Interrupt Raw Status</p> <p>This bit indicates the status of the JPEG Line Buffer Terminate Write Cycle Interrupt which happens when a write cycle attempts to write to the JPEG line buffer when it is full. When this happens, the cycle is terminated and no data is written to the JPEG line buffer. This interrupt is used to determine whether another write must be performed. If a JPEG Line Buffer Terminate Write Cycle Interrupt occurs and the JPEG Line Buffer Terminate Write Cycle Interrupt is enabled (REG[0A0Ch] bit 3 = 1), and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.</p> <p>When this bit = 1, a JPEG Line Buffer Terminate Write Cycle Interrupt has occurred.</p> <p>When this bit = 0, an interrupt has not occurred.</p> <p>To clear this bit, write a 1 to this bit.</p> |
| bit 2 | <p>JPEG Line Buffer Terminate Read Cycle Interrupt Raw Status</p> <p>This bit indicates the status of the JPEG Line Buffer Terminate Read Cycle Interrupt which happens when a read cycle attempts to read from the JPEG line buffer when it is empty. When this happens, the cycle is terminated and no data is read from the JPEG line buffer. This interrupt is used to determine whether another read must be performed. If a JPEG Line Buffer Terminate Read Cycle Interrupt occurs and the JPEG Line Buffer Terminate Read Cycle Interrupt is enabled (REG[0A0Ch] bit 2 = 1), and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.</p> <p>When this bit = 1, a JPEG Line Buffer Terminate Read Cycle Interrupt has occurred.</p> <p>When this bit = 0, an interrupt has not occurred.</p> <p>To clear this bit, write a 1 to this bit.</p>       |
| bit 1 | <p>JPEG FIFO Terminate Write Cycle Interrupt Raw Status</p> <p>This bit indicates the status of the JPEG FIFO Terminate Write Cycle Interrupt which happens when a write cycle attempts to write to the JPEG FIFO when it is full. When this happens, the cycle is terminated and no data is written to the JPEG FIFO. This interrupt is used to determine whether another write must be performed. If a JPEG FIFO Terminate Write Cycle Interrupt occurs and the JPEG FIFO Terminate Write Cycle Interrupt is enabled (REG[0A0Ch] bit 1 = 1), and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.</p> <p>When this bit = 1, a JPEG FIFO Terminate Write Cycle Interrupt has occurred.</p> <p>When this bit = 0, an interrupt has not occurred.</p> <p>To clear this bit, write a 1 to this bit.</p>                                                  |
| bit 0 | <p>Reserved</p> <p>The default value for this bit is 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| REG[0A0Ch] Host Cycle Interrupt Control Register |     |                                                             |                                                            |                                                                  |                                                                 |                                                           |          |
|--------------------------------------------------|-----|-------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------|----------|
| Default = 0000h                                  |     |                                                             |                                                            |                                                                  |                                                                 |                                                           |          |
| Read/Write                                       |     |                                                             |                                                            |                                                                  |                                                                 |                                                           |          |
| Cycle Time Out<br>Interrupt Enable               | n/a |                                                             |                                                            |                                                                  |                                                                 |                                                           |          |
| 15                                               | 14  | 13                                                          | 12                                                         | 11                                                               | 10                                                              | 9                                                         | 8        |
| n/a                                              |     | BitBLT FIFO<br>Terminate Write<br>Cycle Interrupt<br>Enable | BitBLT FIFO<br>Terminate Read<br>Cycle Interrupt<br>Enable | JPEG Line Buffer<br>Terminate Write<br>Cycle Interrupt<br>Enable | JPEG Line Buffer<br>Terminate Read<br>Cycle Interrupt<br>Enable | JPEG FIFO<br>Terminate Write<br>Cycle Interrupt<br>Enable | Reserved |
| 7                                                | 6   | 5                                                           | 4                                                          | 3                                                                | 2                                                               | 1                                                         | 0        |

- bit 15      Cycle Time Out Interrupt Enable  
When this bit is 1, the Host Interrupt Request bit is set.  
When this bit is 0, the Host Interrupt Request bit is not set.
- bit 5      BitBLT FIFO Terminate Write Cycle Interrupt Enable  
When this bit is 1, the interrupt is enabled.  
When this bit is 0, the interrupt is disabled.
- bit 4      BitBLT FIFO Terminate Read Cycle Interrupt Enable  
When this bit is 1, interrupt is enabled.  
When this bit is 0, interrupt is disabled.
- bit 3      JPEG Line Buffer Terminate Write Cycle Interrupt Enable  
When this bit is 1, the Host Interrupt Request bit is set.  
When this bit is 0, the Host Interrupt Request bit is not set.
- bit 2      JPEG Line Buffer Terminate Read Cycle Interrupt Enable  
When this bit is 1, the Host Interrupt Request bit is set.  
When this bit is 0, the Host Interrupt Request bit is not set.
- bit 1      JPEG FIFO Terminate Write Cycle Interrupt Enable  
When this bit is 1, the Host Interrupt Request bit is set.  
When this bit is 0, the Host Interrupt Request bit is not set.
- bit 0      Reserved  
The default value for this bit is 0.

| REG[0A0Eh] Cycle Time Out Control Register |    |     |                         |    |    |   | Read/Write |
|--------------------------------------------|----|-----|-------------------------|----|----|---|------------|
| Default = 0000h                            |    |     |                         |    |    |   |            |
| 15                                         | 14 | 13  | 12                      | 11 | 10 | 9 | 8          |
| Immediate Terminate Cycle Enable           |    | n/a | Time Out Value bits 4-0 |    |    |   |            |
| 7                                          | 6  | 5   | 4                       | 3  | 2  | 1 | 0          |

bit 7 Immediate Terminate Cycle Enable  
Terminate cycles are used to terminate (or end) read/write cycles to the JPEG FIFO (write only), JPEG Line Buffer and BitBLT FIFO. This bit in conjunction with the Time Out Value bits (REG[0A0Eh] bits 4-0) determines when a terminate cycle is generated. The following tables summarizes the conditions that cause a terminate cycle to be generated.

**Note**  
When the Immediate Terminate Cycle function is enabled (REG[0A0Eh] bit 7 = 1), the Time Out Value bits (REG[0A0Eh] bits 4-0) must be set to 1Fh.

Table 10-73: Terminate Cycle Generation Summary

| REG[0A0Eh] bit 7 | REG[0A0Eh] bits 4-0 | Terminate Cycle Generation                                                                                                                                                                                                                                                                                                                                                                           |
|------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                | = 11111             | If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated once the Time Out Value of 1Fh is exceeded.                                                                                                                                                                                                 |
|                  | ≠ 11111             | If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated once the Time Out Value is exceeded.                                                                                                                                                                                                        |
| 1                | = 11111             | If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated immediately.<br><br>If a write access to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read access from a JPEG Line Buffer/BitBLT FIFO exceeds the Time Out Value (REG[0A0Eh] bits 4-0) of 1Fh, a terminate cycle is generated immediately. |

bits 4-0 Time Out Value bits[4:0]  
These bits control the length of time (time out value) allowed for an access cycle to the JPEG FIFO, JPEG Line Buffer, or BitBLT FIFO to take place before a terminate cycle is generated. The time out value is specified as follows and should be configured to a default value of 1Fh at initialization.  
REG[0A0Eh] bits 4-0 = Time Out Value in CLKs  
Time Out Value = Internal System Clock ÷ 2

REG[0A10h] is Reserved

This register is Reserved and should not be written.

| REG[0A40h] Interrupt Request Status Register |    |    |                                               |                                    |                                  |                                    |                                   |
|----------------------------------------------|----|----|-----------------------------------------------|------------------------------------|----------------------------------|------------------------------------|-----------------------------------|
| Default = 0000h                              |    |    |                                               |                                    |                                  |                                    |                                   |
| Read Only                                    |    |    |                                               |                                    |                                  |                                    |                                   |
| n/a                                          |    |    |                                               |                                    |                                  |                                    |                                   |
| 15                                           | 14 | 13 | 12                                            | 11                                 | 10                               | 9                                  | 8                                 |
| n/a                                          |    |    | Host Interface<br>Interrupt Request<br>Status | Camera Interrupt<br>Request Status | JPEG Interrupt<br>Request Status | BitBLT Interrupt<br>Request Status | Debug Interrupt<br>Request Status |
| 7                                            | 6  | 5  | 4                                             | 3                                  | 2                                | 1                                  | 0                                 |

- bit 4                      Host Interface Interrupt Request Status (Read Only)  
 When this bit = 1, a host interface interrupt request has occurred.  
 When this bit = 0, a host interface interrupt has not occurred.
- bit 3                      Camera Interrupt Request Status (Read Only)  
 When this bit = 1, a camera interrupt request has occurred.  
 When this bit = 0, a camera interrupt request has not occurred.
- bit 2                      JPEG Interrupt Request Status (Read Only)  
 When this bit = 1, a JPEG interrupt request has occurred.  
 When this bit = 0, a JPEG interrupt request has not occurred.
- bit 1                      BitBLT Interrupt Request Status (Read Only)  
 When this bit = 1, a BitBLT interrupt request has occurred.  
 When this bit = 0, a BitBLT interrupt request has not occurred.
- bit 0                      Debug Interrupt Request Status (Read Only)  
 When this bit = 1, a debug interrupt request has occurred.  
 When this bit = 0, a debug interrupt request has not occurred.

#### 10.4.19 JPEG Encode Performance Register

| REG[0F00h] JPEG Encode Performance Register |    |    |    |    |    |   |                                |
|---------------------------------------------|----|----|----|----|----|---|--------------------------------|
| Default = 0001h                             |    |    |    |    |    |   |                                |
| Read/Write                                  |    |    |    |    |    |   |                                |
| n/a                                         |    |    |    |    |    |   |                                |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8                              |
| n/a                                         |    |    |    |    |    |   | JPEG Encode<br>High Speed Mode |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0                              |

- bit 0                      JPEG Encode High Speed Mode  
 When this bit = 1, the JPEG Encoding process runs in “Normal Mode” (default).  
 When this bit = 0, the JPEG Encoding process runs in “High Speed Mode”. When High Speed Mode is enabled, the Huffman Tables must be programmed according to the tables specified in the ISO/IEC IS 10918-1 ANNEX K in the ITU-T recommendation T.81 book K. For recommended values see the bit descriptions for the Huffman Tables (REG[1400h] - [17A2h]).

10.4.20 JPEG Codec Registers

| REG[1000h] Operation Mode Setting Register |     |    |          |                      |                       |                            |   |
|--------------------------------------------|-----|----|----------|----------------------|-----------------------|----------------------------|---|
| Default = 0000h                            |     |    |          |                      |                       | Read/Write                 |   |
| n/a                                        |     |    |          |                      |                       |                            |   |
| 15                                         | 14  | 13 | 12       | 11                   | 10                    | 9                          | 8 |
| Reserved                                   | n/a |    | Reserved | Marker Insert Enable | JPEG Operation Select | YUV Format Select bits 1-0 |   |
| 7                                          | 6   | 5  | 4        | 3                    | 2                     | 1                          | 0 |

- bit 7

Reserved  
The default value for this bit is 0.
- bit 4

Reserved  
The default value for this bit is 0.
- bit 3

Marker Insert Enable  
This bit determines if the marker (see REG[1020h] - [1066h]) is inserted during JPEG encoding. During JPEG decoding this bit is ignored.  
When this bit = 1, the entire marker is inserted into the JPEG file.  
When this bit = 0, the marker is not inserted.
- Note**  
When the marker is inserted, the entire 36 byte marker (REG[1020h] - [1066h]) is inserted into the JPEG file regardless of what value the marker length bits (REG[1024h] - [1026h]) specify.
- bit 2

JPEG Operation Select  
This bit selects the JPEG operation and the input source for the resizer block. This bit should be set to 0 when resizing data from the camera. This bit must be cleared before the JPEG module is disabled (REG[0980h] bit 0 = 0).

Table 10-74: JPEG Operation Selection

| REG[1000h] bit 2 | JPEG Operation | Resizer Source                              |
|------------------|----------------|---------------------------------------------|
| 0                | Encode         | Camera data / Memory image data / Host data |
| 1                | Decode         | JPEG decoded data                           |

bits 1-0

YUV Format Select bits[1:0]

These bits select the YUV format of the JPEG codec. For the JPEG encode process, these bits must be set to the desired YUV format. For the JPEG decode process, these bits are read only and indicate the YUV format of the data being decoded.

Table 10-75: YUV Format Selection

| REG[1000h] bits 1-0 | YUV Format            |
|---------------------|-----------------------|
| 00                  | 4:4:4 (decode only)   |
| 01                  | 4:2:2 (encode/decode) |
| 10                  | 4:2:0 (encode/decode) |
| 11                  | 4:1:1 (encode/decode) |

**Note**

Only YUV 4:2:0 and YUV 4:2:2 are supported for Host input JPEG decode/encode.

| REG[1002h] Command Setting Register |     |    |    |    |    |   |                      | Write Only |
|-------------------------------------|-----|----|----|----|----|---|----------------------|------------|
| Default = not applicable            |     |    |    |    |    |   |                      |            |
| 15                                  | 14  | 13 | 12 | 11 | 10 | 9 | 8                    |            |
| JPEG Codec SW Reset                 | n/a |    |    |    |    |   | JPEG Operation Start |            |
| 7                                   | 6   | 5  | 4  | 3  | 2  | 1 | 0                    |            |

**Note**

This register is write only. Reading this register may cause the JPEG Codec to behave unexpectedly.

**Note**

When the JPEG codec is working, this register must not be written to, except to perform a JPEG codec software reset.

bit 7

JPEG Codec Software Reset (Write Only)

This bit initiates a software reset of the JPEG Codec. The JPEG Codec registers (REG[1000h]-[17A2h]) are not affected.

When a 1 is written to this bit, the JPEG Codec is reset.

When a 0 is written to this bit, there is no hardware effect.

bit 0

JPEG Operation Start (Write Only)

This bit is used to begin a JPEG operation.

When a 1 is written to this bit, the JPEG operation is started.

When a 0 is written to this bit, there is no hardware effect.

## Registers

| REG[1004h] JPEG Operation Status Register |    |    |    |    |    |   |                            |
|-------------------------------------------|----|----|----|----|----|---|----------------------------|
| Default = 0000h                           |    |    |    |    |    |   |                            |
| Read Only                                 |    |    |    |    |    |   |                            |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9 | 8                          |
| n/a                                       |    |    |    |    |    |   |                            |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1 | 0                          |
| n/a                                       |    |    |    |    |    |   | JPEG Operation Status (RO) |
|                                           |    |    |    |    |    |   | 0                          |

bit 0      JPEG Operation Status (Read Only)  
 This bit indicates the state of the JPEG codec and clears the JPEG codec interrupt (REG[0982h] bit 1) when read.  
 When this bit = 1, the JPEG codec is busy (a decode or encode operation is in progress).  
 When this bit = 0, the JPEG codec is idle.

| REG[1006h] Quantization Table Number Register |    |    |    |    |                      |                      |                      |
|-----------------------------------------------|----|----|----|----|----------------------|----------------------|----------------------|
| Default = 0000h                               |    |    |    |    |                      |                      |                      |
| Read/Write                                    |    |    |    |    |                      |                      |                      |
| 15                                            | 14 | 13 | 12 | 11 | 10                   | 9                    | 8                    |
| n/a                                           |    |    |    |    |                      |                      |                      |
| 7                                             | 6  | 5  | 4  | 3  | Color 3 Table Select | Color 2 Table Select | Color 1 Table Select |
| n/a                                           |    |    |    |    | 2                    | 1                    | 0                    |

bit 2      Color 3 Table Select  
 When this bit = 1, the Color 3 Table uses Quantization Table No. 1 (REG[1280-12FEh].  
 When this bit = 0, the Color 3 Table uses Quantization Table No. 0 (REG[1200-127Eh].

bit 1      Color 2 Table Select  
 When this bit = 1, the Color 2 Table uses Quantization Table No. 1 (REG[1280-12FEh].  
 When this bit = 0, the Color 2 Table uses Quantization Table No. 0 (REG[1200-127Eh].

bit 0      Color 1 Table Select  
 When this bit = 1, the Color 1 Table uses Quantization Table No. 1 (REG[1280-12FEh].  
 When this bit = 0, the Color 1 Table uses Quantization Table No. 0 (REG[1200-127Eh].

| REG[1008h] Huffman Table Number Register |    |                         |                         |                         |                         |                         |                         |
|------------------------------------------|----|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Default = 0000h                          |    |                         |                         |                         |                         |                         |                         |
| Read/Write                               |    |                         |                         |                         |                         |                         |                         |
| 15                                       | 14 | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| n/a                                      |    |                         |                         |                         |                         |                         |                         |
| 7                                        | 6  | AC Color 3 Table Select | DC Color 3 Table Select | AC Color 2 Table Select | DC Color 2 Table Select | AC Color 1 Table Select | DC Color 1 Table Select |
| n/a                                      |    | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |

bit 5      AC Color 3 Table Select  
 When this bit = 1, the AC Color 3 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).  
 When this bit = 0, the AC Color 3 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).

---

|       |                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 4 | <p>DC Color 3 Table Select</p> <p>When this bit = 1, the DC Color 3 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).</p> <p>When this bit = 0, the DC Color 3 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).</p> |
| bit 3 | <p>AC Color 2 Table Select</p> <p>When this bit = 1, the AC Color 2 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).</p> <p>When this bit = 0, the AC Color 2 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).</p> |
| bit 2 | <p>DC Color 2 Table Select</p> <p>When this bit = 1, the DC Color 2 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).</p> <p>When this bit = 0, the DC Color 2 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).</p> |
| bit 1 | <p>AC Color 1 Table Select</p> <p>When this bit = 1, the AC Color 1 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).</p> <p>When this bit = 0, the AC Color 1 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).</p> |
| bit 0 | <p>DC Color 1 Table Select</p> <p>When this bit = 1, the DC Color 1 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).</p> <p>When this bit = 0, the DC Color 1 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).</p> |

| REG[100Ah] DRI Setting Register 0 |    |    |    |    |    |   |   | Read/Write |
|-----------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                   |    |    |    |    |    |   |   |            |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| DRI Value bits 15-8               |    |    |    |    |    |   |   |            |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[100Ch] DRI Setting Register 1 |    |    |    |    |    |   |   | Read/Write |
|-----------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                   |    |    |    |    |    |   |   |            |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| DRI Value bits 7-0                |    |    |    |    |    |   |   |            |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[100Ah] bits 7-0

REG[100Ch] bits 7-0     DRI Value bits [15:0]

These bits determine the MCU number for RST marker insertion during encoding. During decoding, these bits are ignored. The DRI value bits must be set when JPEG 180° Rotation Encode is enabled (REG[0980h] bit 8 = 1). The DRI (Designated Restart Interval) value must be set as follows.

$$\text{DRI} = \text{Image Width} / \text{Horizontal MCU Size}$$

Where:

MCU Size depends on the YUV format (REG[1000h] bits 1-0) as follows

Table 10-76: MCU Size

| REG[1000h] bits 1-0 | YUV Format | MCU Size (Horizontal x Vertical) |
|---------------------|------------|----------------------------------|
| 00                  | Reserved   | Reserved                         |
| 01                  | 4:2:2      | 16 x 8                           |
| 10                  | 4:2:0      | 16 x 16                          |
| 11                  | 4:1:1      | 32 x 8                           |

| REG[100Eh] Vertical Pixel Size Register 0 |    |    |    |    |    |   |   | Read/Write |
|-------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                           |    |    |    |    |    |   |   |            |
| n/a                                       |    |    |    |    |    |   |   |            |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Y Pixel Size bits 15-8                    |    |    |    |    |    |   |   |            |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[1010h] Vertical Pixel Size Register 1 |    |    |    |    |    |   |   | Read/Write |
|-------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                           |    |    |    |    |    |   |   |            |
| n/a                                       |    |    |    |    |    |   |   |            |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Y Pixel Size bits 7-0                     |    |    |    |    |    |   |   |            |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[100Eh] bits 7-0

REG[1010h] bits 7-0 Y Pixel Size bits[15:0]

For the JPEG encode process, these bits specify the vertical image size before encoding takes place.

For the JPEG decode process, these bits are read-only and indicate the vertical image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

*Table 10-77: Vertical Pixel Size Minimum Resolution Restrictions*

| YUV Format            | Minimum Resolution |
|-----------------------|--------------------|
| 4:4:4 (decode only)   | 1x1                |
| 4:2:2 (encode/decode) | 2x1                |
| 4:2:0 (encode/decode) | 2x2                |
| 4:1:1 (encode/decode) | 4x1                |

#### Note

For all processes (JPEG encode/decode and YUV capture/display) the following formula must be valid.

$$\text{Vertical Pixel Size} > 1$$

| REG[1012h] Horizontal Pixel Size Register 0 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                             |    |    |    |    |    |   |   |            |
| n/a                                         |    |    |    |    |    |   |   |            |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| X Pixel Size bits 15-8                      |    |    |    |    |    |   |   |            |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[1014h] Horizontal Pixel Size Register 1 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                             |    |    |    |    |    |   |   |            |
| n/a                                         |    |    |    |    |    |   |   |            |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| X Pixel Size bits 7-0                       |    |    |    |    |    |   |   |            |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[1012h] bits 7-0

REG[1014h] bits 7-0      X Pixel Size bits[15:0]

For the JPEG encode process, these bits specify the horizontal image size before encoding takes place.

For the JPEG decode process, these bits are read-only and indicate the horizontal image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

Table 10-78: Horizontal Pixel Size Minimum Resolution Restrictions

| YUV Format | Minimum Resolution | Minimum Horizontal Pixel Size |
|------------|--------------------|-------------------------------|
| 4:2:2      | 2x1                | 2                             |
| 4:2:0      | 2x2                | 16                            |
| 4:1:1      | 4x1                | 4                             |

REG[1016h] through REG[101Ah] are Reserved

These registers are Reserved and should not be written.

| REG[101Ch] RST Marker Operation Setting Register |    |    |    |    |    |                                      |   |
|--------------------------------------------------|----|----|----|----|----|--------------------------------------|---|
| Default = 0000h                                  |    |    |    |    |    |                                      |   |
| Read/Write                                       |    |    |    |    |    |                                      |   |
| n/a                                              |    |    |    |    |    |                                      |   |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9                                    | 8 |
| n/a                                              |    |    |    |    |    | RST Marker Operation Select bits 1-0 |   |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1                                    | 0 |

bits 1-0

RST Marker Operation Select bits[1:0]

For the JPEG decode process, these bits select the RST Marker Operation.

For the JPEG encode process, these bits are not used.

Table 10-79: RST Marker Selection

| REG[101Ch] bits 1-0 | RST Marker Operation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00                  | <b>Error detection and data revise function is turned off</b><br>This option should only be used when it is certain that the JPEG file to be decoded is correct and has no errors. If there is an error in the file, no error detection will take place and the decode process will not finish correctly.                                                                                                                                                                                                                                                                            |
| 01                  | <b>Error detection on</b><br>When an error is detected during the decode process, the decode process finishes and the JPEG interrupt is asserted (REG[0A00h] bit 2 = 1). To determine the exact nature of the operational error see REG[0982h]. To determine the JPEG decode error (file error), check the JPEG Error Status bits (REG[101Eh] bits 6-3). Because the decode process finished before normal completion, all data can not be displayed. If the JPEG file is to be decoded again with the Data Revise function on, a software reset is required (see REG[1002h] bit 7). |
| 10                  | <b>Data revise function on</b><br>When an error is detected during the decode process, data is skipped/added automatically and the decode process continues normally to the end of file. After the decode process finishes, a data revise interrupt is asserted. Because the decode process is finished completely, the next JPEG file can be decoded immediately.                                                                                                                                                                                                                   |
| 11                  | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| REG[101Eh] RST Marker Operation Status Register |                            |    |    |    |     |   |           |
|-------------------------------------------------|----------------------------|----|----|----|-----|---|-----------|
| Default = 0000h                                 |                            |    |    |    |     |   | Read Only |
| n/a                                             |                            |    |    |    |     |   |           |
| 15                                              | 14                         | 13 | 12 | 11 | 10  | 9 | 8         |
| Revise Code                                     | JPEG Error Status bits 3-0 |    |    |    | n/a |   |           |
| 7                                               | 6                          | 5  | 4  | 3  | 2   | 1 | 0         |

bit 7

Revise Code (Read Only)  
**This bit is valid only when the data revise function is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 10]).**  
For the JPEG decode process, this bit indicates whether a revise operation has been done.  
For the JPEG encode process, this bit is not used.  
When this bit = 1, a revise operation was done.  
When this bit = 0, a revise operation was not done.

bits 6-3

JPEG Error Status[3:0] (Read Only)  
**These bits are valid only when error detection is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 01]).**  
For the JPEG decode process, these bits indicate the type of JPEG error. If these bits return 0000, no error has occurred.  
For the JPEG encode process, these bits are not used.

Table 10-80: JPEG Error Status

| REG[101Eh] bits 6-3 | JPEG Error Status      |
|---------------------|------------------------|
| 0000                | No error               |
| 0001 - 1010         | Reserved               |
| 1011                | Restart interval error |
| 1100                | Image size error       |
| 1101 - 1111         | Reserved               |

| REG[1020 - 1066h] Insertion Marker Data Register |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 00FFh                                  |    |    |    |    |    |   |   |            |
| n/a                                              |    |    |    |    |    |   |   |            |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Insert marker Data bits 7-0                      |    |    |    |    |    |   |   |            |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[1020h-1066h] These registers (36 bytes) store the Insertion Marker Data which gets inserted into the JPEG file. Only the even bytes are used. All unused registers (up to REG[1200h]) should be filled with FFh. The registers are defined as follows.

Table 10-81: Insertion Marker Data Register Usage

| Register           | Description                                                                                                                |
|--------------------|----------------------------------------------------------------------------------------------------------------------------|
| REG[1020h]-[1022h] | These registers set the insertion marker code type.                                                                        |
| REG[1024h]-[1026h] | These registers set the marker length (0002h - 0022h).                                                                     |
| REG[1028h]-[1066h] | These registers set the marker data (up to a maximum of 32 bytes). Note that all unused registers must be filled with FFh. |

| REG[1200 - 127Eh] Quantization Table No. 0 Register |    |    |    |    |    |   |   | Read/Write |
|-----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = not applicable                            |    |    |    |    |    |   |   |            |
| n/a                                                 |    |    |    |    |    |   |   |            |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Quantization Table No. 0 bits 7-0                   |    |    |    |    |    |   |   |            |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[1200-127Eh] Quantization Table No. 0  
These registers are used for the JPEG encode process only.

| REG[1280 - 12FEh] Quantization Table No. 1 Register |    |    |    |    |    |   |   | Write Only |
|-----------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = not applicable                            |    |    |    |    |    |   |   |            |
| n/a                                                 |    |    |    |    |    |   |   |            |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| Quantization Table No. 1 bits 7-0                   |    |    |    |    |    |   |   |            |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

REG[1280-12FEh] Quantization Table No. 1  
These registers are used for the JPEG encode process only.

| REG[1400 - 141Eh] DC Huffman Table No. 0 Register 0 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DC Huffman Table No. 0 Register 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1400-141Eh] DC Huffman Table No. 0 (Write Only)  
 These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-82: DC Huffman Table No. 0 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1400h] | 00h   | REG[1408h] | 01h   | REG[1410h] | 01h   | REG[1418h] | 00h   |
| REG[1402h] | 01h   | REG[140Ah] | 01h   | REG[1412h] | 00h   | REG[141Ah] | 00h   |
| REG[1404h] | 05h   | REG[140Ch] | 01h   | REG[1414h] | 00h   | REG[141Ch] | 00h   |
| REG[1406h] | 01h   | REG[140Eh] | 01h   | REG[1416h] | 00h   | REG[141Eh] | 00h   |

| REG[1420 - 1436h] DC Huffman Table No. 0 Register 1 |    |    |    |                                            |    |   |   |
|-----------------------------------------------------|----|----|----|--------------------------------------------|----|---|---|
| Default = not applicable                            |    |    |    |                                            |    |   |   |
| Write Only                                          |    |    |    |                                            |    |   |   |
| n/a                                                 |    |    |    |                                            |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11                                         | 10 | 9 | 8 |
| Reserved (must be all 0)                            |    |    |    | DC Huffman Table No. 0 Register 1 bits 3-0 |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3                                          | 2  | 1 | 0 |

REG[1420-1436h] DC Huffman Table No. 0 (Write Only)  
 These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-83: DC Huffman Table No. 1 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1420h] | 00h   | REG[1426h] | 03h   | REG[142Ch] | 06h   | REG[1432h] | 09h   |
| REG[1422h] | 01h   | REG[1428h] | 04h   | REG[142Eh] | 07h   | REG[1434h] | 0Ah   |
| REG[1424h] | 02h   | REG[142Ah] | 05h   | REG[1430h] | 08h   | REG[1436h] | 0Bh   |

| REG[1440 - 145Eh] AC Huffman Table No. 0 Register 0 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AC Huffman Table No. 0 Register 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1440-145Eh] AC Huffman Table No. 0 (Write Only)  
 These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-84: AC Huffman Table No. 0 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1440h] | 00h   | REG[1448h] | 03h   | REG[1450h] | 05h   | REG[1458h] | 00h   |
| REG[1442h] | 02h   | REG[144Ah] | 02h   | REG[1452h] | 05h   | REG[145Ah] | 00h   |
| REG[1444h] | 01h   | REG[144Ch] | 04h   | REG[1454h] | 04h   | REG[145Ch] | 01h   |
| REG[1446h] | 03h   | REG[144Eh] | 03h   | REG[1456h] | 04h   | REG[145Eh] | 7Dh   |

| REG[1460 - 15A2h] AC Huffman Table No. 0 Register 1 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AC Huffman Table No. 0 Register 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1460-15A2h] AC Huffman Table No. 0 (Write Only)  
 These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-85: AC Huffman Table No. 0 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1460h] | 01h   | REG[14B0h] | 17h   | REG[1500h] | 6Ah   | REG[1550h] | B7h   |
| REG[1462h] | 02h   | REG[14B2h] | 18h   | REG[1502h] | 73h   | REG[1552h] | B8h   |
| REG[1464h] | 03h   | REG[14B4h] | 19h   | REG[1504h] | 74h   | REG[1554h] | B9h   |
| REG[1466h] | 00h   | REG[14B6h] | 1Ah   | REG[1506h] | 75h   | REG[1556h] | BAh   |
| REG[1468h] | 04h   | REG[14B8h] | 25h   | REG[1508h] | 76h   | REG[1558h] | C2h   |
| REG[146Ah] | 11h   | REG[14BAh] | 26h   | REG[150Ah] | 77h   | REG[155Ah] | C3h   |
| REG[146Ch] | 05h   | REG[14BCh] | 27h   | REG[150Ch] | 78h   | REG[155Ch] | C4h   |
| REG[146Eh] | 12h   | REG[14BEh] | 28h   | REG[150Eh] | 79h   | REG[155Eh] | C5h   |
| REG[1470h] | 21h   | REG[14C0h] | 29h   | REG[1510h] | 7Ah   | REG[1560h] | C6h   |
| REG[1472h] | 31h   | REG[14C2h] | 2Ah   | REG[1512h] | 83h   | REG[1562h] | C7h   |
| REG[1474h] | 41h   | REG[14C4h] | 34h   | REG[1514h] | 84h   | REG[1564h] | C8h   |
| REG[1476h] | 06h   | REG[14C6h] | 35h   | REG[1516h] | 85h   | REG[1566h] | C9h   |
| REG[1478h] | 13h   | REG[14C8h] | 36h   | REG[1518h] | 86h   | REG[1568h] | CAh   |
| REG[147Ah] | 51h   | REG[14CAh] | 37h   | REG[151Ah] | 87h   | REG[156Ah] | D2h   |
| REG[147Ch] | 61h   | REG[14CCh] | 38h   | REG[151Ch] | 88h   | REG[156Ch] | D3h   |
| REG[147Eh] | 07h   | REG[14CEh] | 39h   | REG[151Eh] | 89h   | REG[156Eh] | D4h   |
| REG[1480h] | 22h   | REG[14D0h] | 3Ah   | REG[1520h] | 8Ah   | REG[1570h] | D5h   |
| REG[1482h] | 71h   | REG[14D2h] | 43h   | REG[1522h] | 92h   | REG[1572h] | D6h   |
| REG[1484h] | 14h   | REG[14D4h] | 44h   | REG[1524h] | 93h   | REG[1574h] | D7h   |
| REG[1486h] | 32h   | REG[14D6h] | 45h   | REG[1526h] | 94h   | REG[1576h] | D8h   |
| REG[1488h] | 81h   | REG[14D8h] | 46h   | REG[1528h] | 95h   | REG[1578h] | D9h   |
| REG[148Ah] | 91h   | REG[14DAh] | 47h   | REG[152Ah] | 96h   | REG[157Ah] | DAh   |
| REG[148Ch] | A1h   | REG[14DCh] | 48h   | REG[152Ch] | 97h   | REG[157Ch] | E1h   |
| REG[148Eh] | 08h   | REG[14DEh] | 49h   | REG[152Eh] | 98h   | REG[157Eh] | E2h   |
| REG[1490h] | 23h   | REG[14E0h] | 4Ah   | REG[1530h] | 99h   | REG[1580h] | E3h   |
| REG[1492h] | 42h   | REG[14E2h] | 53h   | REG[1532h] | 9Ah   | REG[1582h] | E4h   |
| REG[1494h] | B1h   | REG[14E4h] | 54h   | REG[1534h] | A2h   | REG[1584h] | E5h   |
| REG[1496h] | C1h   | REG[14E6h] | 55h   | REG[1536h] | A3h   | REG[1586h] | E6h   |
| REG[1498h] | 15h   | REG[14E8h] | 56h   | REG[1538h] | A4h   | REG[1588h] | E7h   |
| REG[149Ah] | 52h   | REG[14EAh] | 57h   | REG[153Ah] | A5h   | REG[158Sh] | E8h   |
| REG[149Ch] | D1h   | REG[14ECh] | 58h   | REG[153Ch] | A6h   | REG[158Ch] | E9h   |
| REG[149Eh] | F0h   | REG[14EEh] | 59h   | REG[153Eh] | A7h   | REG[158Eh] | EAh   |
| REG[14A0h] | 24h   | REG[14F0h] | 5Ah   | REG[1540h] | A8h   | REG[1590h] | F1h   |
| REG[14A2h] | 33h   | REG[14F2h] | 63h   | REG[1542h] | A9h   | REG[1592h] | F2h   |
| REG[14A4h] | 62h   | REG[14F4h] | 64h   | REG[1544h] | AAh   | REG[1594h] | F3h   |
| REG[14A6h] | 72h   | REG[14F6h] | 65h   | REG[1546h] | B2h   | REG[1596h] | F4h   |
| REG[14A8h] | 82h   | REG[14F8h] | 66h   | REG[1548h] | B3h   | REG[1598h] | F5h   |
| REG[14AAh] | 09h   | REG[14FAh] | 67h   | REG[154Ah] | B4h   | REG[159Ah] | F6h   |
| REG[14ACh] | 0Ah   | REG[14FCh] | 68h   | REG[154Ch] | B5h   | REG[159Ch] | F7h   |
| REG[14AEh] | 16h   | REG[14FEh] | 69h   | REG[154Eh] | B6h   | REG[159Eh] | F8h   |
|            |       |            |       |            |       | REG[15A0h] | F9h   |
|            |       |            |       |            |       | REG[15A2h] | FAh   |

| REG[1600 - 161Eh] DC Huffman Table No. 1 Register 0 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DC Huffman Table 1 Register No. 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1600-161Eh] DC Huffman Table No. 1 (Write Only)  
 These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-86: DC Huffman Table No. 1 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1600h] | 00h   | REG[1608h] | 01h   | REG[1610h] | 01h   | REG[1618h] | 00h   |
| REG[1602h] | 03h   | REG[160Ah] | 01h   | REG[1612h] | 01h   | REG[161Ah] | 00h   |
| REG[1604h] | 01h   | REG[160Ch] | 01h   | REG[1614h] | 01h   | REG[161Ch] | 00h   |
| REG[1606h] | 01h   | REG[160Eh] | 01h   | REG[1616h] | 00h   | REG[161Eh] | 00h   |

| REG[1620 - 1636h] DC Huffman Table No. 1 Register 1 |    |    |    |                                            |    |   |   |
|-----------------------------------------------------|----|----|----|--------------------------------------------|----|---|---|
| Default = not applicable                            |    |    |    |                                            |    |   |   |
| Write Only                                          |    |    |    |                                            |    |   |   |
| n/a                                                 |    |    |    |                                            |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11                                         | 10 | 9 | 8 |
| Reserved (must be all 0)                            |    |    |    | DC Huffman Table No. 1 Register 1 bits 3-0 |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3                                          | 2  | 1 | 0 |

REG[1620-1636h] DC Huffman Table No. 1 (Write Only)  
 These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-87: DC Huffman Table No. 1 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1620h] | 00h   | REG[1626h] | 03h   | REG[162Ch] | 06h   | REG[1632h] | 09h   |
| REG[1622h] | 01h   | REG[1628h] | 04h   | REG[162Eh] | 07h   | REG[1634h] | 0Ah   |
| REG[1624h] | 02h   | REG[162Ah] | 05h   | REG[1630h] | 08h   | REG[1636h] | 0Bh   |

| REG[1640 - 165Eh] AC Huffman Table No. 1 Register 0 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AC Huffman Table No. 1 Register 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1640-165Eh] AC Huffman Table No. 1 (Write Only)  
 These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-88: AC Huffman Table No. 1 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1640h] | 00h   | REG[1648h] | 04h   | REG[1650h] | 07h   | REG[1658h] | 00h   |
| REG[1642h] | 02h   | REG[164Ah] | 04h   | REG[1652h] | 05h   | REG[165Ah] | 01h   |
| REG[1644h] | 01h   | REG[164Ch] | 03h   | REG[1654h] | 04h   | REG[165Ch] | 02h   |
| REG[1646h] | 02h   | REG[164Eh] | 04h   | REG[1656h] | 04h   | REG[165Eh] | 77h   |

| REG[1660 - 17A2h] AC Huffman Table No. 1 Register 1 |    |    |    |    |    |   |   |
|-----------------------------------------------------|----|----|----|----|----|---|---|
| Default = not applicable                            |    |    |    |    |    |   |   |
| Write Only                                          |    |    |    |    |    |   |   |
| n/a                                                 |    |    |    |    |    |   |   |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AC Huffman Table No. 1 Register 0 bits 7-0          |    |    |    |    |    |   |   |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |

REG[1660-17A2h] AC Huffman Table No. 1 (Write Only)  
 These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode “High Speed Mode” is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-89: AC Huffman Table No. 1 Values for High Speed Mode

| Register   | Value | Register   | Value | Register   | Value | Register   | Value |
|------------|-------|------------|-------|------------|-------|------------|-------|
| REG[1660h] | 00h   | REG[16B0h] | E1h   | REG[1500h] | 69h   | REG[1550h] | B5h   |
| REG[1662h] | 01h   | REG[16B2h] | 25h   | REG[1502h] | 6Ah   | REG[1552h] | B6h   |
| REG[1664h] | 02h   | REG[16B4h] | F1h   | REG[1504h] | 73h   | REG[1554h] | B7h   |
| REG[1666h] | 03h   | REG[16B6h] | 17h   | REG[1506h] | 74h   | REG[1556h] | B8h   |
| REG[1668h] | 11h   | REG[16B8h] | 18h   | REG[1508h] | 75h   | REG[1558h] | B9h   |
| REG[166Ah] | 04h   | REG[16BAh] | 19h   | REG[150Ah] | 76h   | REG[155Ah] | BAh   |
| REG[166Ch] | 05h   | REG[16BCh] | 1Ah   | REG[150Ch] | 77h   | REG[155Ch] | C2h   |
| REG[166Eh] | 21h   | REG[16BEh] | 26h   | REG[150Eh] | 78h   | REG[155Eh] | C3h   |
| REG[1670h] | 31h   | REG[16C0h] | 27h   | REG[1510h] | 79h   | REG[1560h] | C4h   |
| REG[1672h] | 06h   | REG[16C2h] | 28h   | REG[1512h] | 7Ah   | REG[1562h] | C5h   |
| REG[1674h] | 12h   | REG[16C4h] | 29h   | REG[1514h] | 82h   | REG[1564h] | C6h   |
| REG[1676h] | 41h   | REG[16C6h] | 2Ah   | REG[1516h] | 83h   | REG[1566h] | C7h   |
| REG[1678h] | 51h   | REG[16C8h] | 35h   | REG[1518h] | 84h   | REG[1568h] | C8h   |
| REG[167Ah] | 07h   | REG[16CAh] | 36h   | REG[151Ah] | 85h   | REG[156Ah] | C9h   |
| REG[167Ch] | 61h   | REG[16CCh] | 37h   | REG[151Ch] | 86h   | REG[156Ch] | CAh   |
| REG[167Eh] | 71h   | REG[16CEh] | 38h   | REG[151Eh] | 87h   | REG[156Eh] | D2h   |
| REG[1680h] | 13h   | REG[16D0h] | 39h   | REG[1520h] | 88h   | REG[1570h] | D3h   |
| REG[1682h] | 22h   | REG[16D2h] | 3Ah   | REG[1522h] | 89h   | REG[1572h] | D4h   |
| REG[1684h] | 32h   | REG[16D4h] | 43h   | REG[1524h] | 8Ah   | REG[1574h] | D5h   |
| REG[1686h] | 81h   | REG[16D6h] | 44h   | REG[1526h] | 92h   | REG[1576h] | D6h   |
| REG[1688h] | 08h   | REG[16D8h] | 45h   | REG[1528h] | 93h   | REG[1578h] | D7h   |
| REG[168Ah] | 14h   | REG[16DAh] | 46h   | REG[152Ah] | 94h   | REG[157Ah] | D8h   |
| REG[168Ch] | 42h   | REG[16DCh] | 47h   | REG[152Ch] | 95h   | REG[157Ch] | D9h   |
| REG[168Eh] | 91h   | REG[16DEh] | 48h   | REG[152Eh] | 96h   | REG[157Eh] | DAh   |
| REG[1690h] | A1h   | REG[16E0h] | 49h   | REG[1530h] | 97h   | REG[1580h] | E2h   |
| REG[1692h] | B1h   | REG[16E2h] | 4Ah   | REG[1532h] | 98h   | REG[1582h] | E3h   |
| REG[1694h] | C1h   | REG[16E4h] | 53h   | REG[1534h] | 99h   | REG[1584h] | E4h   |
| REG[1696h] | 09h   | REG[16E6h] | 54h   | REG[1536h] | 9Ah   | REG[1586h] | E5h   |
| REG[1698h] | 23h   | REG[16E8h] | 55h   | REG[1538h] | A2h   | REG[1588h] | E6h   |
| REG[169Ah] | 33h   | REG[16EAh] | 56h   | REG[153Ah] | A3h   | REG[158Sh] | E7h   |
| REG[169Ch] | 52h   | REG[16ECh] | 57h   | REG[153Ch] | A4h   | REG[158Ch] | E8h   |
| REG[169Eh] | F0h   | REG[16EEh] | 58h   | REG[153Eh] | A5h   | REG[158Eh] | E9h   |
| REG[16A0h] | 15h   | REG[16F0h] | 59h   | REG[1540h] | A6h   | REG[1590h] | EAh   |
| REG[16A2h] | 62h   | REG[16F2h] | 5Ah   | REG[1542h] | A7h   | REG[1592h] | F2h   |
| REG[16A4h] | 72h   | REG[16F4h] | 63h   | REG[1544h] | A8h   | REG[1594h] | F3h   |
| REG[16A6h] | D1h   | REG[16F6h] | 64h   | REG[1546h] | A9h   | REG[1596h] | F4h   |
| REG[16A8h] | 0Ah   | REG[16F8h] | 65h   | REG[1548h] | AAh   | REG[1598h] | F5h   |
| REG[16AAh] | 16h   | REG[16FAh] | 66h   | REG[154Ah] | B2h   | REG[159Ah] | F6h   |
| REG[16ACh] | 24h   | REG[16FCh] | 67h   | REG[154Ch] | B3h   | REG[159Ch] | F7h   |
| REG[16AEh] | 34h   | REG[16FEh] | 68h   | REG[154Eh] | B4h   | REG[159Eh] | F8h   |
|            |       |            |       |            |       | REG[15A0h] | F9h   |
|            |       |            |       |            |       | REG[15A2h] | FAh   |

## 10.4.21 2D BitBLT Registers

### Note

The S1D13715 BitBLT engine does not support 32 bpp .

| REG[8000h] BitBLT Control Register 0 |    |    |    |     |    |   |               |
|--------------------------------------|----|----|----|-----|----|---|---------------|
| Default = 0000h                      |    |    |    |     |    |   |               |
| Write Only                           |    |    |    |     |    |   |               |
| 15                                   | 14 | 13 | 12 | 11  | 10 | 9 | 8             |
| n/a                                  |    |    |    | n/a |    |   |               |
| BitBLT Reset                         |    |    |    |     |    |   | BitBLT Enable |
| 7                                    | 6  | 5  | 4  | 3   | 2  | 1 | 0             |

- bit 7 BitBLT Reset (Write Only)  
When a 1 is written to this bit, the 2D BitBLT engine is reset.  
When a 0 is written to this bit, there is no hardware effect.
- bit 0 BitBLT Enable (Write Only)  
When a 1 is written to this bit, the 2D BitBLT operation is started.  
When a 0 is written to this bit, the 2D BitBLT operation is terminated.

| REG[8002h] BitBLT Control Register 1 |    |    |    |    |                     |                    |                      |
|--------------------------------------|----|----|----|----|---------------------|--------------------|----------------------|
| Default = 0000h                      |    |    |    |    |                     |                    |                      |
| Read/Write                           |    |    |    |    |                     |                    |                      |
| Reserved                             |    |    |    |    |                     |                    |                      |
| 15                                   | 14 | 13 | 12 | 11 | 10                  | 9                  | 8                    |
| n/a                                  |    |    |    |    | Color Format Select | Dest Linear Select | Source Linear Select |
| 7                                    | 6  | 5  | 4  | 3  | 2                   | 1                  | 0                    |

- bits 15-8 Reserved  
The default value for these bits is 0.
- bit 2 BitBLT Color Format Select  
This bit selects the color format that the 2D operation is applied to.  
When this bit = 0, 8 bpp (256 color) format is selected.  
When this bit = 1, 16 bpp (64K color) format is selected.
- Note**  
The BitBLT engine does not support color depths of 32 bpp.
- bit 1 BitBLT Destination Linear Select  
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.  
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory.  
The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.
- bit 0 BitBLT Source Linear Select  
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.  
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory.  
The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.

| REG[8004h] BitBLT Status Register 0 |                |                |                  |     |    |   |                    |
|-------------------------------------|----------------|----------------|------------------|-----|----|---|--------------------|
| Default = 0000h                     |                |                |                  |     |    |   |                    |
| Read Only                           |                |                |                  |     |    |   |                    |
| 15                                  | 14             | 13             | 12               | 11  | 10 | 9 | 8                  |
| n/a                                 | FIFO Not Empty | FIFO Half Full | FIFO Full Status | n/a |    |   | BitBLT Busy Status |
| 7                                   | 6              | 5              | 4                | 3   | 2  | 1 | 0                  |

bit 6 BitBLT FIFO Not-Empty Status (Read Only)  
 This bit indicates if the BitBLT FIFO is empty or not.  
 When this bit = 0, the BitBLT FIFO is empty.  
 When this bit = 1, the BitBLT FIFO has at least one entry.  
 To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of words available in the BitBLT FIFO under different status conditions.

Table 10-90: Possible BitBLT FIFO Writes

| BitBLT Status Register (REG[8004h]) |                       |                  | Word Writes Available |
|-------------------------------------|-----------------------|------------------|-----------------------|
| FIFO Not Empty Status               | FIFO Half Full Status | FIFO Full Status |                       |
| 0                                   | 0                     | 0                | 16                    |
| 1                                   | 0                     | 0                | 8                     |
| 1                                   | 1                     | 0                | up to 8               |
| 1                                   | 1                     | 1                | 0 (do not write)      |

bit 5 BitBLT FIFO Half Full Status (Read Only)  
 This bit indicates whether the BitBLT FIFO is more or less than half full.  
 When this bit = 1, the BitBLT FIFO is half full or greater than half full.  
 When this bit = 0, the BitBLT FIFO is less than half full.

bit 4 BitBLT FIFO Full Status (Read Only)  
 This bit indicates whether the BitBLT FIFO is full or not. **This bit must be confirmed as not full (0) before writing to the BitBLT FIFO.**  
 When this bit = 1, the BitBLT FIFO is full.  
 When this bit = 0, the BitBLT FIFO is not full.

bit 0 BitBLT Busy Status (Read Only)  
 This bit indicates the state of the current BitBLT operation.  
 When this bit = 1, the BitBLT operation is in progress.  
 When this bit = 0, the BitBLT operation is complete.

| REG[8006h] BitBLT Status Register 1 |    |    |    |                                            |    |   |   |
|-------------------------------------|----|----|----|--------------------------------------------|----|---|---|
| Default = 0010h                     |    |    |    |                                            |    |   |   |
| Read Only                           |    |    |    |                                            |    |   |   |
| n/a                                 |    |    |    | Number of Used FIFO Entries                |    |   |   |
| 15                                  | 14 | 13 | 12 | 11                                         | 10 | 9 | 8 |
| n/a                                 |    |    |    | Number of Free FIFO Entries (0 means full) |    |   |   |
| 7                                   | 6  | 5  | 4  | 3                                          | 2  | 1 | 0 |

bits 12-8      Number of Used FIFO Entries bits [4:0] (Read Only)  
 These bits indicate the number of FIFO entries currently in use.

bits 4-0      Number of Free FIFO Entries bits [4:0] (Read Only)  
 These bits indicate the number of empty FIFO entries available. If these bits return a 0, the FIFO is full.

| REG[8008h] BitBLT Command Register 0 |    |    |    |                           |    |   |   |
|--------------------------------------|----|----|----|---------------------------|----|---|---|
| Default = 0000h                      |    |    |    |                           |    |   |   |
| Read/Write                           |    |    |    |                           |    |   |   |
| n/a                                  |    |    |    |                           |    |   |   |
| 15                                   | 14 | 13 | 12 | 11                        | 10 | 9 | 8 |
| n/a                                  |    |    |    | BitBLT Operation bits 3-0 |    |   |   |
| 7                                    | 6  | 5  | 4  | 3                         | 2  | 1 | 0 |

bits 3-0      BitBLT Operation bits [3:0]  
 These bits specify the 2D Operation to be performed.

Table 10-91: BitBLT Operation Selection

| BitBLT Operation bits [3:0] | BitBLT Operation                                  |
|-----------------------------|---------------------------------------------------|
| 0000                        | Reserved                                          |
| 0001                        | Read BitBLT                                       |
| 0010                        | Move BitBLT in positive direction with ROP        |
| 0011                        | Move BitBLT in negative direction with ROP        |
| 0100                        | Reserved                                          |
| 0101                        | Transparent Move BitBLT in positive direction     |
| 0110                        | Pattern Fill with ROP                             |
| 0111                        | Pattern Fill with transparency                    |
| 1000                        | Reserved                                          |
| 1001                        | Reserved                                          |
| 1010                        | Move BitBLT with Color Expansion                  |
| 1011                        | Move BitBLT with Color Expansion and transparency |
| 1100                        | Solid Fill                                        |
| Other combinations          | Reserved                                          |

| REG[800Ah] BitBLT Command Register 1 |    |    |    |                            |    |   |   |
|--------------------------------------|----|----|----|----------------------------|----|---|---|
| Default = 0000h                      |    |    |    |                            |    |   |   |
| Read/Write                           |    |    |    |                            |    |   |   |
| n/a                                  |    |    |    |                            |    |   |   |
| 15                                   | 14 | 13 | 12 | 11                         | 10 | 9 | 8 |
| n/a                                  |    |    |    | BitBLT ROP Code bits [3:0] |    |   |   |
| 7                                    | 6  | 5  | 4  | 3                          | 2  | 1 | 0 |

bits 3-0

BitBLT Raster Operation Code/Color Expansion bits [3:0]

These bits determine the ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

Table 10-92: BitBLT ROP Code/Color Expansion Function Selection

| BitBLT ROP Code bits [3:0] | Boolean Function for Write BitBLT and Move BitBLT | Boolean Function for Pattern Fill      | Start Bit Position for Color Expansion |
|----------------------------|---------------------------------------------------|----------------------------------------|----------------------------------------|
| 0000                       | 0 (Blackness)                                     | 0 (Blackness)                          | bit 0                                  |
| 0001                       | $\sim S \cdot \sim D$ or $\sim(S + D)$            | $\sim P \cdot \sim D$ or $\sim(P + D)$ | bit 1                                  |
| 0010                       | $\sim S \cdot D$                                  | $\sim P \cdot D$                       | bit 2                                  |
| 0011                       | $\sim S$                                          | $\sim P$                               | bit 3                                  |
| 0100                       | $S \cdot \sim D$                                  | $P \cdot \sim D$                       | bit 4                                  |
| 0101                       | $\sim D$                                          | $\sim D$                               | bit 5                                  |
| 0110                       | $S \wedge D$                                      | $P \wedge D$                           | bit 6                                  |
| 0111                       | $\sim S + \sim D$ or $\sim(S \cdot D)$            | $\sim P + \sim D$ or $\sim(P \cdot D)$ | bit 7                                  |
| 1000                       | $S \cdot D$                                       | $P \cdot D$                            | bit 0                                  |
| 1001                       | $\sim(S \wedge D)$                                | $\sim(P \wedge D)$                     | bit 1                                  |
| 1010                       | $D$                                               | $D$                                    | bit 2                                  |
| 1011                       | $\sim S + D$                                      | $\sim P + D$                           | bit 3                                  |
| 1100                       | $S$                                               | $P$                                    | bit 4                                  |
| 1101                       | $S + \sim D$                                      | $P + \sim D$                           | bit 5                                  |
| 1110                       | $S + D$                                           | $P + D$                                | bit 6                                  |
| 1111                       | 1 (Whiteness)                                     | 1 (Whiteness)                          | bit 7                                  |

**Note**

S = Source, D = Destination, P = Pattern.

| REG[800Ch] BitBLT Source Start Address Register 0 |    |    |    |    |    |   |   | Read/Write |
|---------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                   |    |    |    |    |    |   |   |            |
| BitBLT Source Start Address bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| BitBLT Source Start Address bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[800Eh] BitBLT Source Start Address Register 1 |    |    |    |                                        |    |   |   | Read/Write |
|---------------------------------------------------|----|----|----|----------------------------------------|----|---|---|------------|
| Default = 0000h                                   |    |    |    |                                        |    |   |   |            |
| n/a                                               |    |    |    |                                        |    |   |   |            |
| 15                                                | 14 | 13 | 12 | 11                                     | 10 | 9 | 8 |            |
|                                                   |    |    |    | BitBLT Source Start Address bits 20-16 |    |   |   |            |
| 7                                                 | 6  | 5  | 4  | 3                                      | 2  | 1 | 0 |            |

REG[800Eh] bits 4-0

REG[800Ch] bits 15-0 BitBLT Source Start Address bits [20:0]

These bits specify the source start address for the BitBLT operation.  
If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation.

Value programmed to the Source Start Address Register =  
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

Table 10-93: BitBLT Source Start Address Selection

| Color Format | Pattern Base Address[20:0]        | Pattern Line Offset[2:0]         | Pixel Offset[3:0]                |
|--------------|-----------------------------------|----------------------------------|----------------------------------|
| 8 bpp        | BitBLT Source Start Address[20:6] | BitBLT Source Start Address[5:3] | BitBLT Source Start Address[2:0] |
| 16 bpp       | BitBLT Source Start Address[20:7] | BitBLT Source Start Address[6:4] | BitBLT Source Start Address[3:0] |

| REG[8010h] BitBLT Destination Start Address Register 0 |    |    |    |    |    |   |   | Read/Write |
|--------------------------------------------------------|----|----|----|----|----|---|---|------------|
| Default = 0000h                                        |    |    |    |    |    |   |   |            |
| BitBLT Destination Start Address bits 15-8             |    |    |    |    |    |   |   |            |
| 15                                                     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |
| BitBLT Destination Start Address bits 7-0              |    |    |    |    |    |   |   |            |
| 7                                                      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |

| REG[8012h] BitBLT Destination Start Address Register 1 |    |    |                                             |    |    |   |   | Read/Write |
|--------------------------------------------------------|----|----|---------------------------------------------|----|----|---|---|------------|
| Default = 0000h                                        |    |    |                                             |    |    |   |   |            |
| n/a                                                    |    |    |                                             |    |    |   |   |            |
| 15                                                     | 14 | 13 | 12                                          | 11 | 10 | 9 | 8 |            |
| n/a                                                    |    |    | BitBLT Destination Start Address bits 20-16 |    |    |   |   |            |
| 7                                                      | 6  | 5  | 4                                           | 3  | 2  | 1 | 0 |            |

REG[8012h] bits 4-0

REG[8010h] bits 15-0 BitBLT Destination Start Address bits [20:0]

These bits specify the destination start address for the BitBLT operation.

| REG[8014h] BitBLT Memory Address Offset Register |    |    |    |                                        |    |   |   | Read/Write |
|--------------------------------------------------|----|----|----|----------------------------------------|----|---|---|------------|
| Default = 0000h                                  |    |    |    |                                        |    |   |   |            |
| n/a                                              |    |    |    | BitBLT Memory Address Offset bits 10-8 |    |   |   |            |
| 15                                               | 14 | 13 | 12 | 11                                     | 10 | 9 | 8 |            |
| BitBLT Memory Address Offset bits 7-0            |    |    |    |                                        |    |   |   |            |
| 7                                                | 6  | 5  | 4  | 3                                      | 2  | 1 | 0 |            |

bits 10-0

BitBLT Memory Address Offset bits [10:0]

These bits are the display's 11-bit address offset from the starting word of line  $n$  to the starting word of line  $n + 1$ . They are used only for address calculation when the BitBLT is configured as a rectangular region of memory. They are not used for the displays.

| REG[8018h] BitBLT Width Register |    |    |    |    |    |                       |   | Read/Write |
|----------------------------------|----|----|----|----|----|-----------------------|---|------------|
| Default = 0000h                  |    |    |    |    |    |                       |   |            |
| n/a                              |    |    |    |    |    | BitBLT Width bits 9-8 |   |            |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9                     | 8 |            |
| BitBLT Width bits 7-0            |    |    |    |    |    |                       |   |            |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1                     | 0 |            |

bits 9-0

BitBLT Width bits [9:0]

These bits determine the BitBLT width in pixels.

BitBLT width in pixels = (REG[8018h] bits 9-0) + 1

| REG[801Ch] BitBLT Height Register |    |    |    |    |    |   | Read/Write             |  |
|-----------------------------------|----|----|----|----|----|---|------------------------|--|
| Default = 0000h                   |    |    |    |    |    |   |                        |  |
| n/a                               |    |    |    |    |    |   | BitBLT Height bits 9-8 |  |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9 | 8                      |  |
| BitBLT Height bits 7-0            |    |    |    |    |    |   |                        |  |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1 | 0                      |  |

bits 9-0

BitBLT Height bits [9:0]

These bits determine the BitBLT height in lines.

BitBLT height in lines = (REG[801Ch] bits 9-0) + 1

| REG[8020h] BitBLT Background Color Register |    |    |    |    |    |   |   | Read/Write |  |
|---------------------------------------------|----|----|----|----|----|---|---|------------|--|
| Default = 0000h                             |    |    |    |    |    |   |   |            |  |
| BitBLT Background Color bits 15-8           |    |    |    |    |    |   |   |            |  |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |  |
| BitBLT Background Color bits 7-0            |    |    |    |    |    |   |   |            |  |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |  |

bits 15-0

BitBLT Background Color bits [15:0]

These bits specify the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

| REG[8024h] BitBLT Foreground Color Register |    |    |    |    |    |   |   | Read/Write |  |
|---------------------------------------------|----|----|----|----|----|---|---|------------|--|
| Default = 0000h                             |    |    |    |    |    |   |   |            |  |
| BitBLT Foreground Color bits 15-8           |    |    |    |    |    |   |   |            |  |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |            |  |
| BitBLT Foreground Color bits 7-0            |    |    |    |    |    |   |   |            |  |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |            |  |

bits 15-0

BitBLT Foreground Color bits [15:0]

These bits specify the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

| REG[8030h] BitBLT Interrupt Status Register |    |    |    |    |    |   |   | Read/Write                     |  |
|---------------------------------------------|----|----|----|----|----|---|---|--------------------------------|--|
| Default = 0000h                             |    |    |    |    |    |   |   |                                |  |
| n/a                                         |    |    |    |    |    |   |   |                                |  |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |                                |  |
| n/a                                         |    |    |    |    |    |   |   | BitBLT Operation Complete Flag |  |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |                                |  |

bit 0

BitBLT Operation Complete Flag

This bit is set when the BitBLT operation is finished. This bit is masked by REG[8032h] bit 0.

When a 1 is written to this bit, the flag is cleared.

When a 0 is written to this bit, there is no hardware effect.

| REG[8032h] BitBLT Interrupt Control Register |    |    |    |     |    |    |   | Read/Write                                 |
|----------------------------------------------|----|----|----|-----|----|----|---|--------------------------------------------|
| Default = 0000h                              |    |    |    |     |    |    |   |                                            |
| 15                                           | 14 | 13 | 12 | n/a | 11 | 10 | 9 | 8                                          |
| n/a                                          |    |    |    |     |    |    |   | BitBLT Operation Complete Interrupt Enable |
| 7                                            | 6  | 5  | 4  | 3   | 2  | 1  | 0 |                                            |

bit 0

**BitBLT Operation Complete Interrupt Enable**

This bit determines whether an interrupt is generated when the current BitBLT operation finishes.

When this bit = 0, the interrupt is disabled.

When this bit = 1, the interrupt is enabled.

| REG[10000h] 2D BitBLT Data Memory Mapped Region Register |    |    |    |    |    |   |   | Read/Write            |
|----------------------------------------------------------|----|----|----|----|----|---|---|-----------------------|
| Default = not applicable                                 |    |    |    |    |    |   |   |                       |
| 15                                                       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | BitBLT Data bits 15-8 |
| 7                                                        | 6  | 5  | 4  | 3  | 2  | 1 | 0 | BitBLT Data bits 7-0  |

bits 15-0

**BitBLT Data bits [15:0]**

This register specifies the BitBLT data when a Direct Interface is selected (CNF[4:2]).

When an Indirect Interface is selected, BitBLT data must be specified using the Indirect Interface 2D BitBLT Data Read/Write Port register (REG[002Ah]).

# 11 Power Save Modes

## 11.1 Power-On/Power-Off Sequence

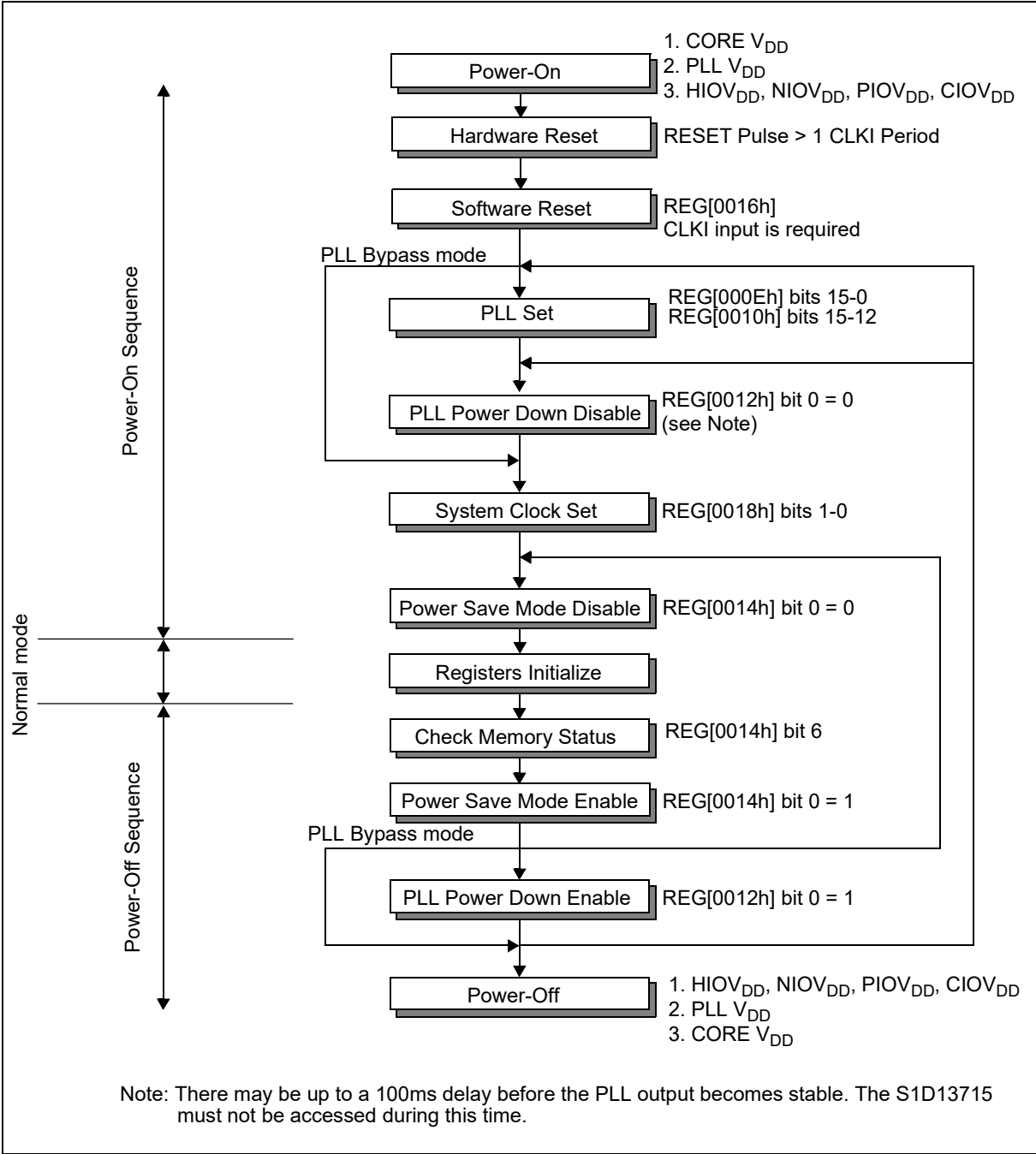
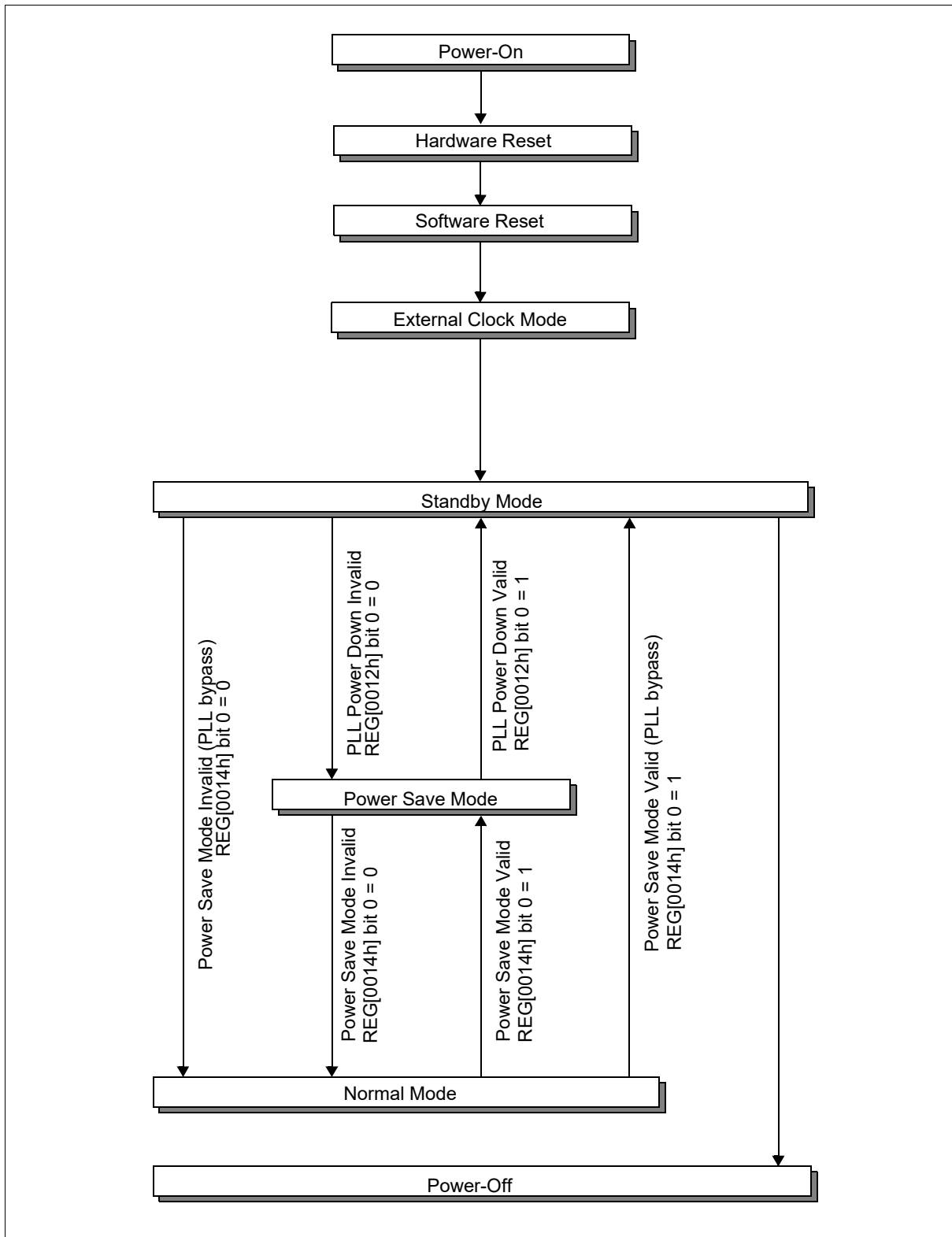


Figure 11-1: Power-On/Power-Off Sequence

*Figure 11-2: Power Save Modes*

### 11.1.1 Power-On

When powering-on the S1D13715, the following sequence must be used unless all power is active within 10 ms.

1. COREV<sub>DD</sub> On
2. PLLV<sub>DD</sub> On
3. HIOV<sub>DD</sub>, PIOV<sub>DD</sub>, CIOV<sub>DD</sub> On

### 11.1.2 Reset

After power-on, an active low hardware reset pulse, which is one external clock cycle (CLKI) in length, must be input to the S1D13715 RESET# pin. All registers, including the Clock Setting registers (REG[000Eh]-[0018h]) are reset by a hardware reset. After releasing the RESET# signal, the Clock Setting registers are immediately accessible.

A software reset is enabled by writing to REG[0016h]. All registers above REG[0018h] are reset to the default values by a software reset (REG[0000h] - [0018h] are not reset). The following conditions apply to software reset.

- After initialization, and before the software reset (REG[0016h]), Power Save Mode should be enabled (REG[0014h] bit 0 = 1).
- After the software reset, Power Save Mode can be disabled (REG[0016h] bit 0 = 0) after waiting 100ms. All registers, synchronous and asynchronous, may now be accessed.

### 11.1.3 Standby Mode

Standby Mode offers the lowest power consumption because all internal clock supplies are stopped and the PLL is disabled. This mode must be entered before turning off the power supplies or setting the PLL registers.

In order to switch to the Standby Mode, a PLL power down should be executed (REG[0012h] bit 0 = 1). After power down, the CLKI input should be continued for a minimum 100us to allow the PLL power down to complete.

### 11.1.4 Power Save Mode

Power Save Mode stops all internal clock supplies. This mode must be entered before setting the System Clock Setting register (REG[0018h]). Also, there may be up to a 100ms delay before the PLL output becomes stable after it is enabled. The S1D1715 should be in Power Save Mode during this time.

### 11.1.5 Normal Mode

All functions are available in Normal Mode. However, clocks to modules that are not in use are dynamically stopped. Before enabling Power Save Mode (REG[0014] bit 0 = 1) from Normal Mode, confirm that the memory controller is idle (REG[0014h] bit 6 = 1).

### 11.1.6 Power-Off

When powering-off the S1D13715, the following sequence must be used.

1. HIOV<sub>DD</sub>, PIOV<sub>DD</sub>, CIOV<sub>DD</sub> Off
2. PLLV<sub>DD</sub> Off
3. COREV<sub>DD</sub> Off

## 11.2 Power Save Mode Function

Table 11-1: Power Save Mode Function Selection

| Item                                                                    |                                                                        | Reset State | Power Save Mode | Normal Mode |
|-------------------------------------------------------------------------|------------------------------------------------------------------------|-------------|-----------------|-------------|
| IO (Register) Access Possible?                                          | REG[0000h-0018h],<br>REG[0300h-030Eh]                                  | Yes         | Yes             | Yes         |
|                                                                         | All other registers                                                    | No          | No              | Yes         |
| Memory Access Possible?                                                 |                                                                        | No          | No              | Yes         |
| Look-Up Table Registers Access Possible?                                |                                                                        | No          | No              | Yes         |
| Display Active?                                                         |                                                                        | No          | No              | Yes         |
| LCD1, LCD2 Interface Outputs and GPIO Pins configured for Panel Support | FPCS1#                                                                 | Inactive    | Inactive        | Active      |
|                                                                         | All other pins                                                         | Forced Low  | Forced Low      | Active      |
| GPIO Pins configured as GPIOs                                           | CNF2 = 1                                                               | Input       | GPIO State      | GPIO State  |
|                                                                         | CNF2 = 0                                                               | Forced Low  | GPO State       | GPO State   |
| Camera Interface Pins                                                   |                                                                        | Forced Low  | Forced Low      | Active      |
| System Clock                                                            |                                                                        | Forced Low  | Active          | Active      |
| Pixel Clock                                                             |                                                                        | Forced Low  | Forced Low      | Active      |
| Serial Clock                                                            | For the LCD2 Serial Panel I/F setting (REG[0032h] bits 1,0 = 00 or 10) | Inactive    | Active          | Active      |
|                                                                         | For all other settings                                                 | Forced Low  | Forced Low      | Active      |
| Camera1, Camera2 Clock                                                  |                                                                        | Forced Low  | Forced Low      | Active      |
| JPEG Module                                                             | REG[0980] bit 0 = 0                                                    | Inactive    | Inactive        | Inactive    |
|                                                                         | REG[0980] bit 0 = 1                                                    | Inactive    | Inactive        | Active      |
| BitBLT Module                                                           |                                                                        | Inactive    | Inactive        | Active      |

# 12 LUT Architecture

## 12.1 LUT1 (Main Window) for 8 bpp

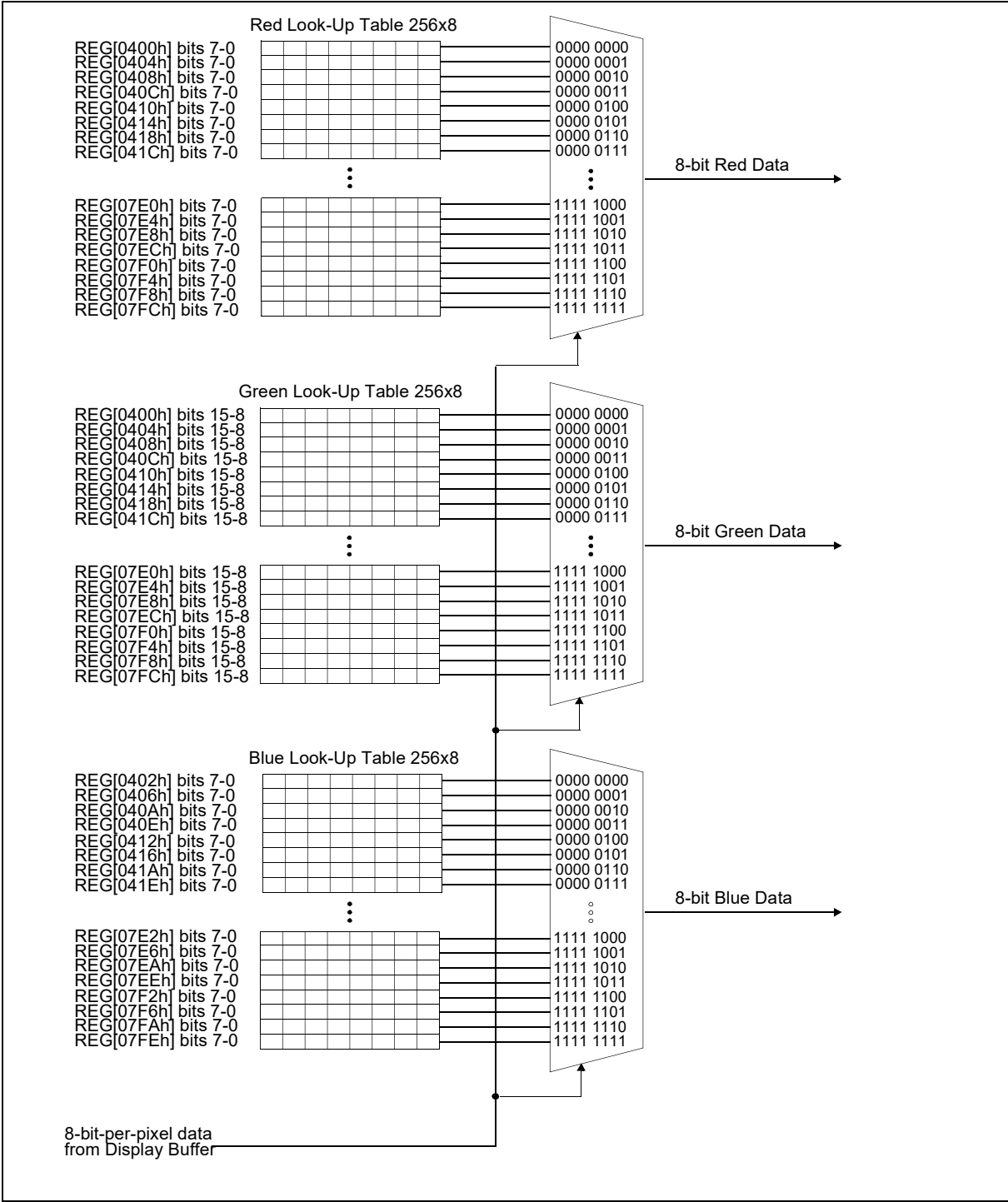


Figure 12-1: LUT1 (Main Window) for 8 Bpp Architecture

## 12.2 LUT2 (PIP<sup>+</sup> Window) for 8 Bpp Architecture

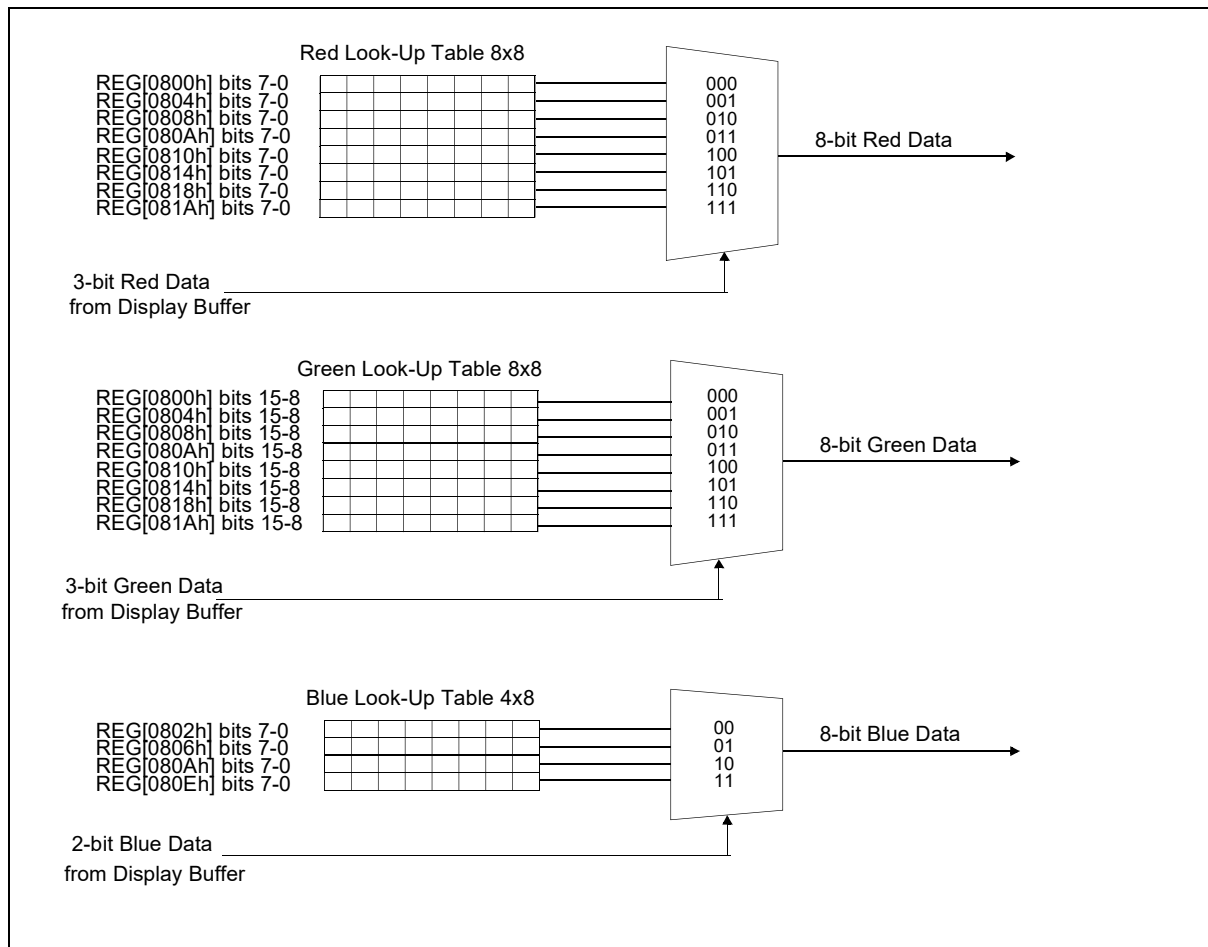


Figure 12-2: LUT2 (PIP<sup>+</sup> Window) for 8 Bpp Architecture

12.3 LUT1 (Main Window) for 16 Bpp Architecture

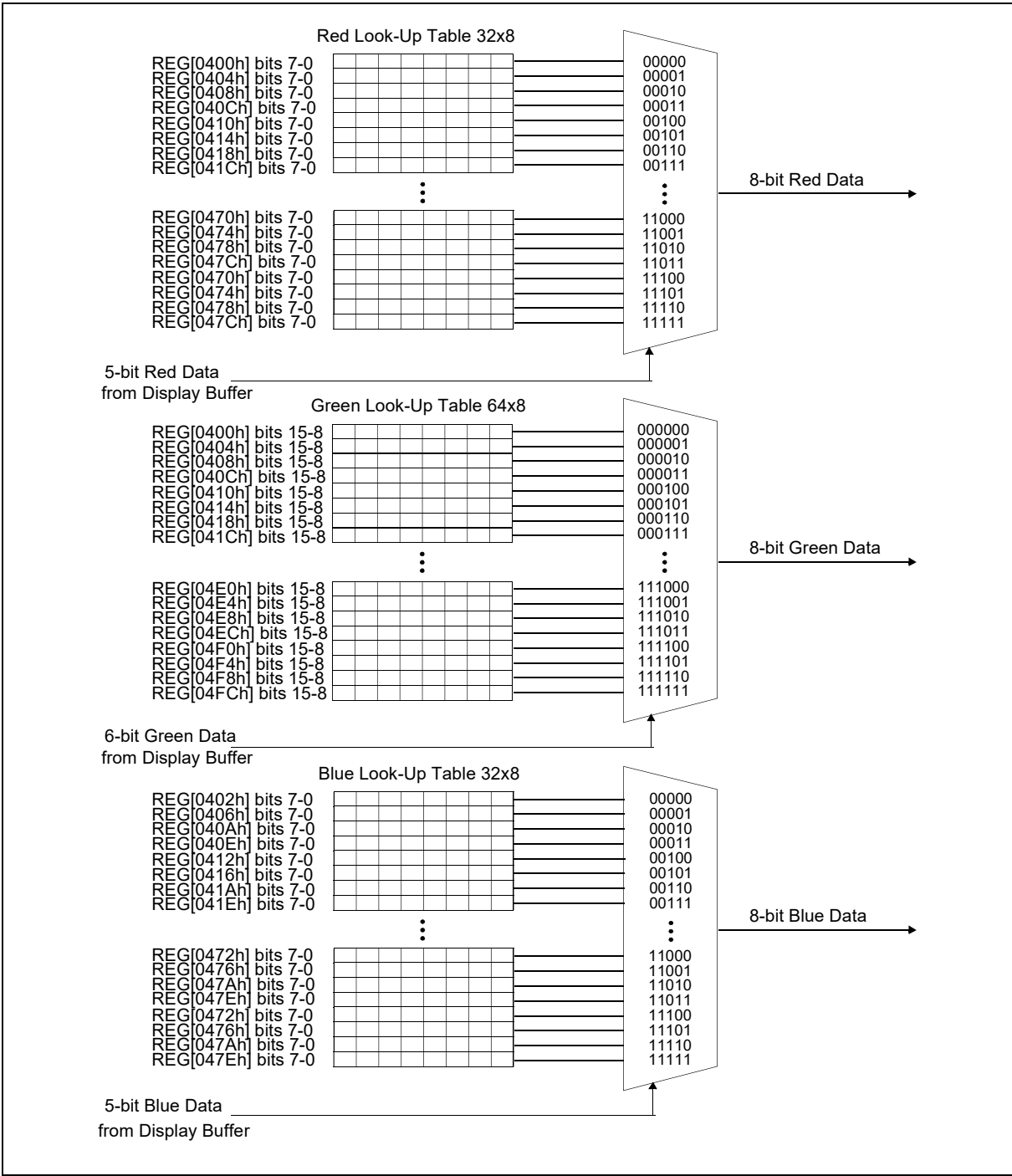


Figure 12-3: LUT1 (Main Window) for 16 Bpp Architecture

## 12.4 LUT2 (PIP<sup>+</sup> Window) for 16 Bpp Architecture

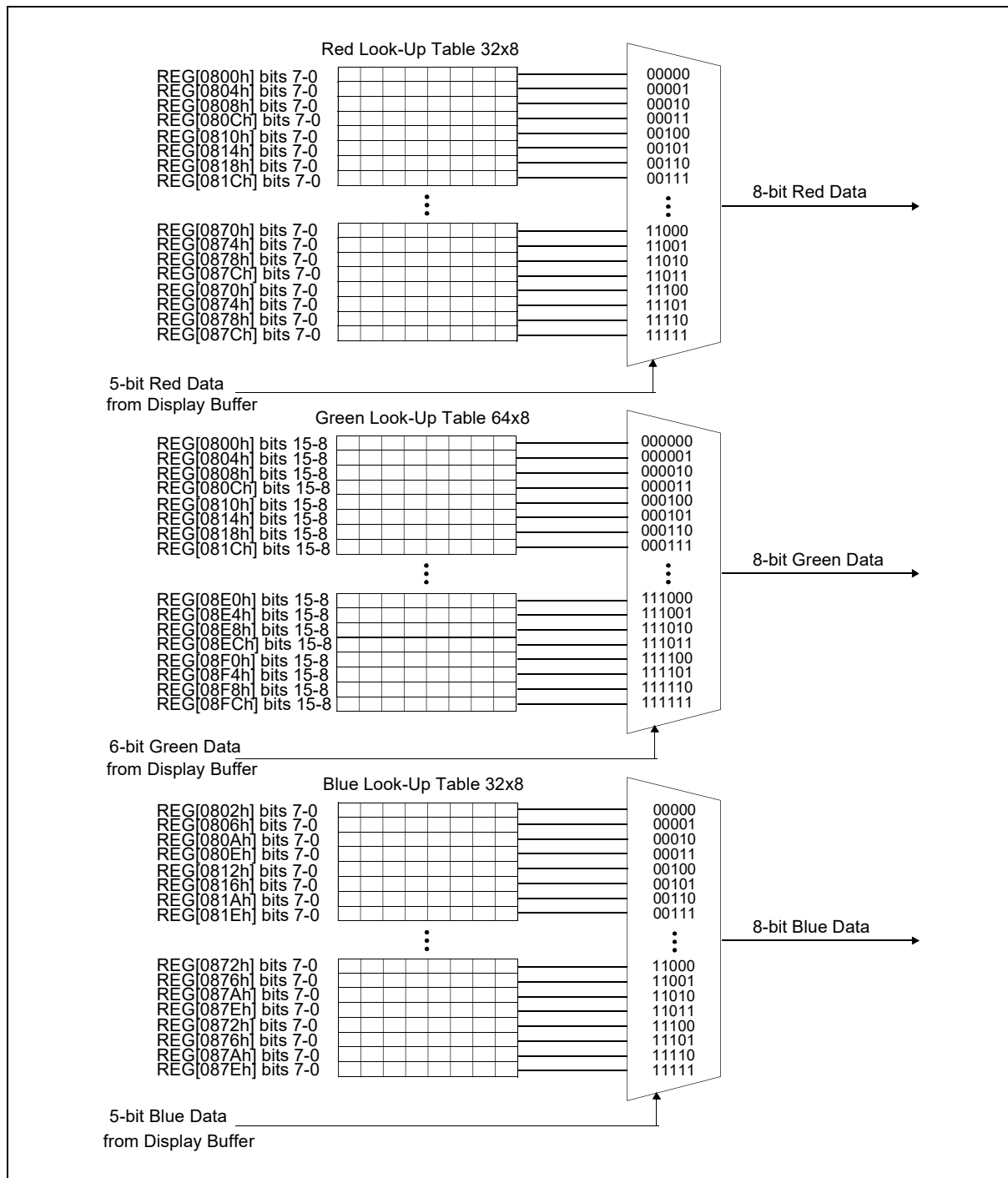


Figure 12-4: LUT2 (PIP<sup>+</sup> Window) for 16 Bpp Architecture

# 13 Display Data Formats

## 13.1 Display Data for LUT Mode

### 13.1.1 8 Bpp Mode

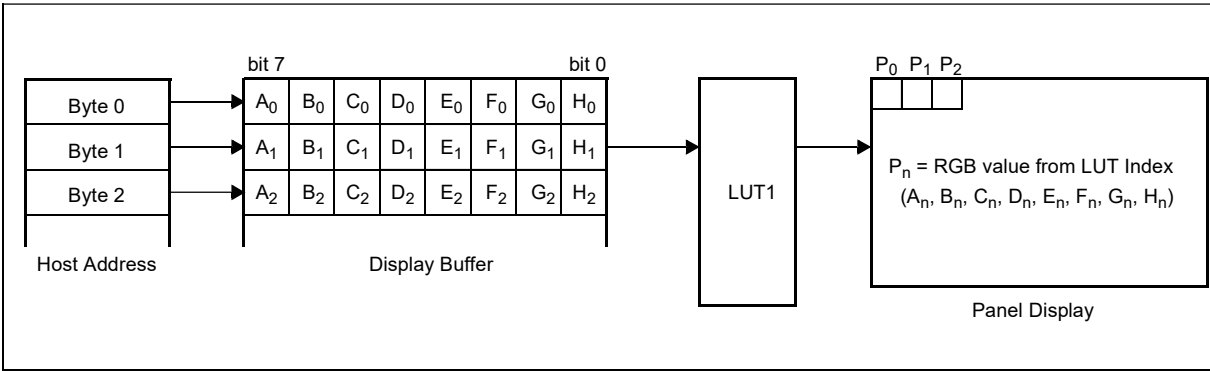


Figure 13-1: LUT1 for 8 Bpp Mode

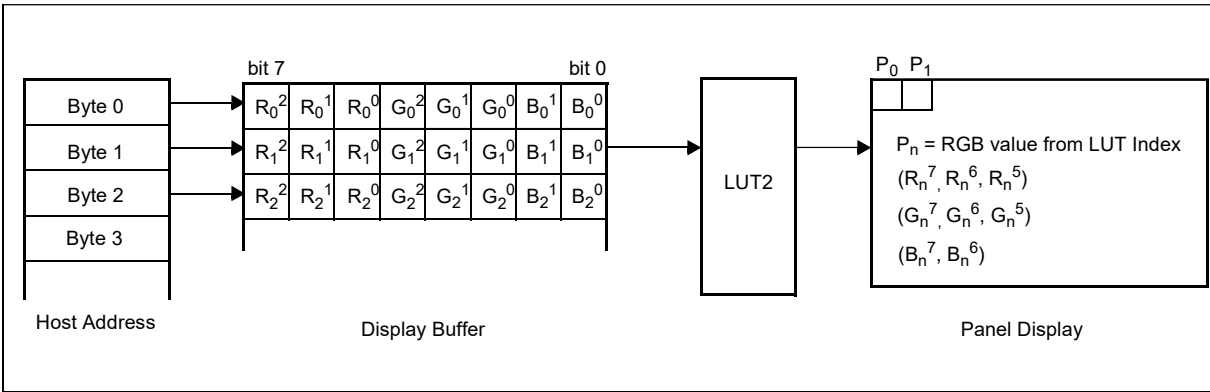


Figure 13-2: LUT2 for 8 Bpp Mode

### 13.1.2 16 Bpp Mode

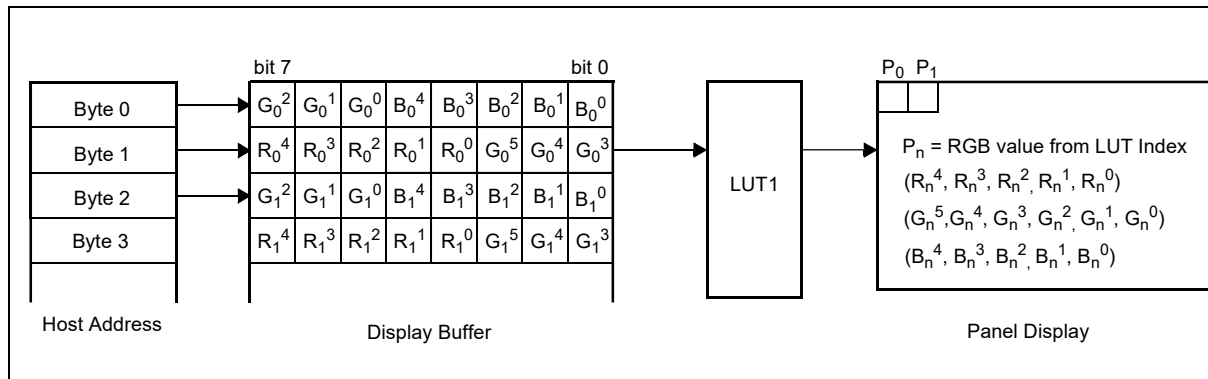


Figure 13-3: LUT1 for 16 Bpp Mode

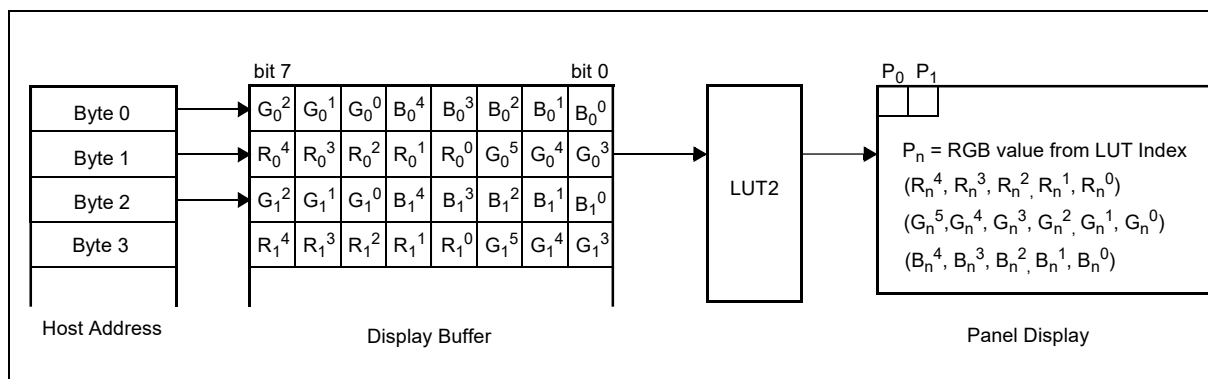


Figure 13-4: LUT2 for 16 Bpp Mode

### 13.1.3 32 bppMode

The LUT is always bypassed at a color depth of 32 bpp. See Section 13.2.3, “32 Bpp Mode” on page 318.

13.2 Display Data for LUT Bypass Mode

13.2.1 8 Bpp Mode

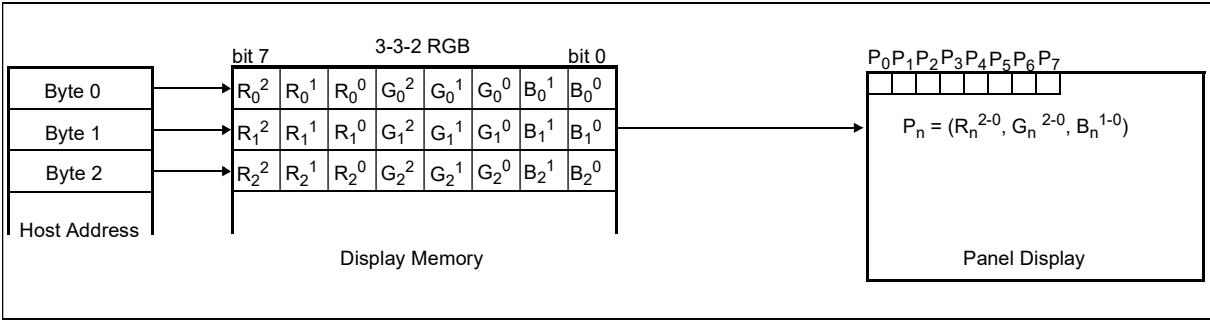


Figure 13-5: LUT Bypass for 8 Bpp mode

13.2.2 16 Bpp Mode

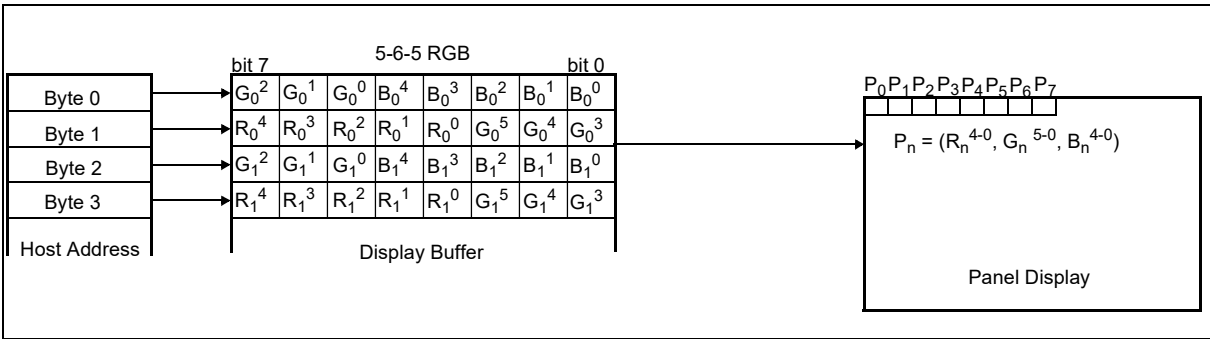


Figure 13-6: LUT Bypass for 16 Bpp mode

13.2.3 32 Bpp Mode

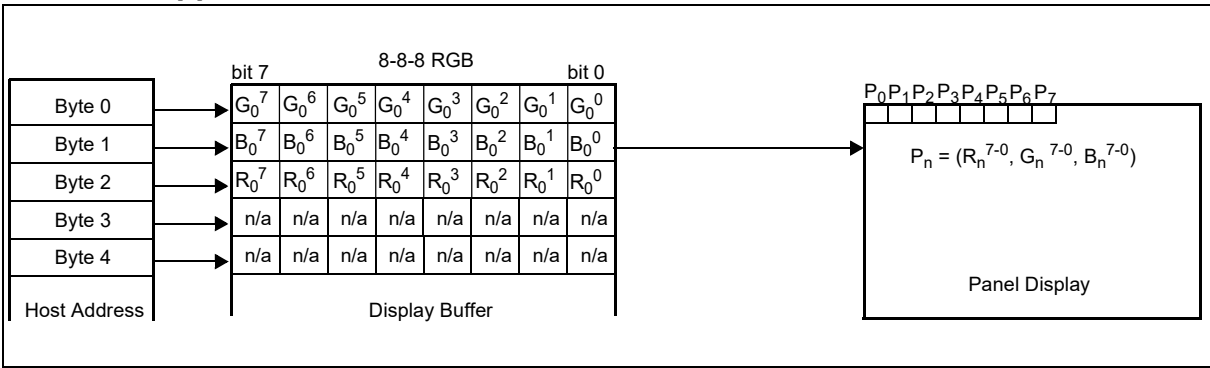


Figure 13-7: LUT Bypass for 32 bpp Mode

**Note**  
32 bpp always bypasses the LUT.

### 13.3 Display Data Flow

The 8 bpp or 16 bpp data in the display buffer is expanded to 24 bpp (RGB=8:8:8) either by the internal LUT or by bit cover (see Section 13.3.2, “Bit Cover When LUT Bypassed” on page 319). For 32 bpp data, the 24 bits of pixel data automatically bypass the LUT. Before being output, the LCD data is altered depending on the specified LCD panel data format. For more information, see Section 5.6, “LCD Interface Pin Mapping” on page 46, Section 13.4, “Parallel Data Format” on page 320 and Section 13.5, “Serial Data Format” on page 327.

#### 13.3.1 Display Buffer Data

Display data can be stored in the display buffer as either 8 bpp, 16 bpp or 32 bpp. Data from the camera interface or JPEG decoder must be stored as 16 bpp or 32 bpp only. The data format for each color depth differs based on whether the LUT is used or the LUT is bypassed. For 32bpp, the LUT is always bypassed.

#### 13.3.2 Bit Cover When LUT Bypassed

When the LUT is bypassed, 8 bpp and 16 bpp data are not indexed using the LUT. The data is expanded to 24 bpp (or bit covered) by copying the MSB to the LSBs as follows.

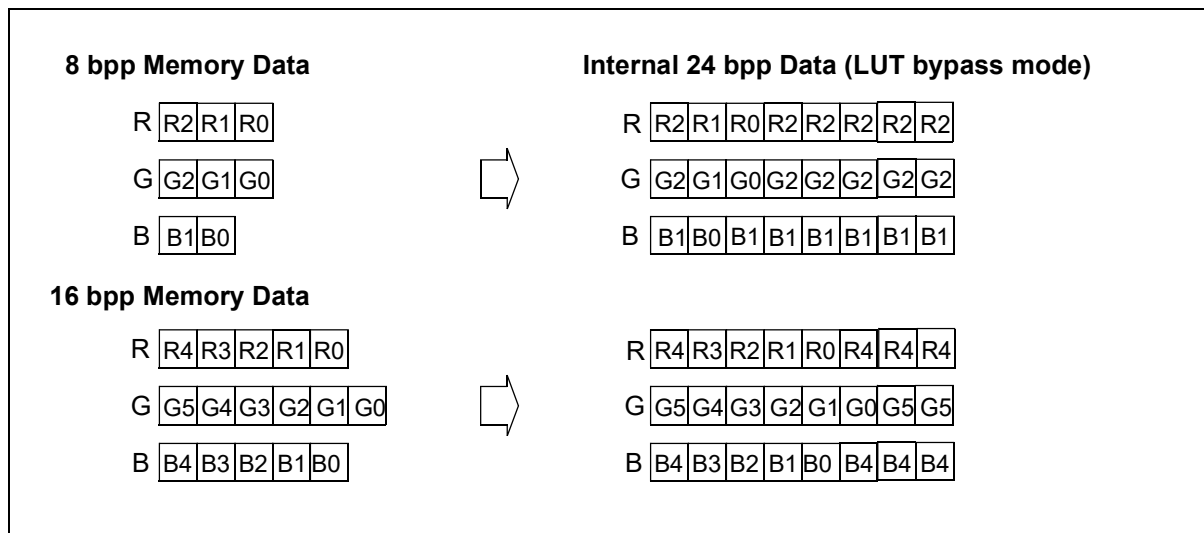


Figure 13-8: Data Bit Cover When the LUT is Bypassed

#### 13.3.3 Overlay

The overlay function compares 24-bit data after the LUT. If the 24-bit data is the same as the Overlay key color (see REG[0204h] - REG[0208h], REG[0304h] - REG[0326h]), the data that will be output is the PIP+ window data instead of the main window data. For more information on the overlay function, see Section 15.1, “Overlay Display” on page 340.

## 13.4 Parallel Data Format

When the Panel Interface bits are set for a parallel panel(s) (REG[0032h] bits 1-0 = 01 or 10 or 11), a parallel data format must be selected. REG[0056h] bits 2-0 select the data format for LCD1 and REG[005Eh] bits 2-0 select the data format for LCD2.

### Note

When REG[0032h] bits 1-0 = 10, Mode 2 is enabled and only LCD1 is configured as a parallel panel. When REG[0032h] bits 1-0 = 11, Mode 3 is enabled and both LCD1 and LCD2 are configured as parallel panels. When REG[0032h] bits 1-0 = 01, Mode 4 is enabled and only LCD2 is configured as a parallel panel. For more information on possible panel combinations, see REG[0032h] bits 1-0 in Section 10.4.4, “LCD Panel Interface Generic Setting Register” on page 149.

### 13.4.1 8-Bit Parallel, RGB=3:3:2

When REG[0056h] bits 2-0 = 000, the LCD1 data format is specified as this format.  
When REG[005Eh] bits 2-0 = 000, the LCD2 data format is specified as this format.

*Table 13-1: 8-Bit Parallel, RGB=3:2:2 Data Format Selection*

|    | Cycle Count |         |         |     |         |
|----|-------------|---------|---------|-----|---------|
|    | 1           | 2       | 3       | ... | n+1     |
| D7 | $R_0^5$     | $R_1^5$ | $R_2^5$ | ... | $R_n^5$ |
| D6 | $R_0^4$     | $R_1^4$ | $R_2^4$ | ... | $R_n^4$ |
| D5 | $R_0^3$     | $R_1^3$ | $R_2^3$ | ... | $R_n^3$ |
| D4 | $G_0^5$     | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D3 | $G_0^4$     | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D2 | $G_0^3$     | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D1 | $B_0^5$     | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D0 | $B_0^4$     | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |

### 13.4.2 8-Bit Parallel, RGB=4:4:4

When REG[0056h] bits 2-0 = 001, the LCD1 data format is specified as this format.

When REG[005Eh] bits 2-0 = 001, the LCD2 data format is specified as this format.

*Table 13-2: 8-Bit Parallel, RGB=4:4:4 Data Format Selection*

|    | Cycle Count |         |         |     |         |             |             |
|----|-------------|---------|---------|-----|---------|-------------|-------------|
|    | 1           | 2       | 3       | ... | 3n+1    | 3n+2        | 3n+3        |
| D7 | $R_0^5$     | $B_0^5$ | $G_1^5$ | ... | $R_n^5$ | $B_n^5$     | $G_{n+1}^5$ |
| D6 | $R_0^4$     | $B_0^4$ | $G_1^4$ | ... | $R_n^4$ | $B_n^4$     | $G_{n+1}^4$ |
| D5 | $R_0^3$     | $B_0^3$ | $G_1^3$ | ... | $R_n^3$ | $B_n^3$     | $G_{n+1}^3$ |
| D4 | $R_0^2$     | $B_0^2$ | $G_1^2$ | ... | $R_n^2$ | $B_n^2$     | $G_{n+1}^2$ |
| D3 | $G_0^5$     | $R_1^5$ | $B_1^5$ | ... | $G_n^5$ | $R_{n+1}^5$ | $B_{n+1}^5$ |
| D2 | $G_0^4$     | $R_1^4$ | $B_1^4$ | ... | $G_n^4$ | $R_{n+1}^4$ | $B_{n+1}^4$ |
| D1 | $G_0^3$     | $R_1^3$ | $B_1^3$ | ... | $G_n^3$ | $R_{n+1}^3$ | $B_{n+1}^3$ |
| D0 | $G_0^2$     | $R_1^2$ | $B_1^2$ | ... | $G_n^2$ | $R_{n+1}^2$ | $B_{n+1}^2$ |

### 13.4.3 8-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 011, the LCD1 data format is specified as this format.

When REG[005Eh] bits 2-0 = 011, the LCD2 data format is specified as this format.

*Table 13-3: 8-Bit Parallel, RGB=8:8:8 Data Format Selection*

|    | Cycle Count |         |         |     |         |         |         |
|----|-------------|---------|---------|-----|---------|---------|---------|
|    | 1           | 2       | 3       | ... | 3n+1    | 3n+2    | 3n+3    |
| D7 | $R_0^7$     | $G_0^7$ | $B_0^7$ | ... | $R_n^7$ | $G_n^7$ | $B_n^7$ |
| D6 | $R_0^6$     | $G_0^6$ | $B_0^6$ | ... | $R_n^6$ | $G_n^6$ | $B_n^6$ |
| D5 | $R_0^5$     | $G_0^5$ | $B_0^5$ | ... | $R_n^5$ | $G_n^5$ | $B_n^5$ |
| D4 | $R_0^4$     | $G_0^4$ | $B_0^4$ | ... | $R_n^4$ | $G_n^4$ | $B_n^4$ |
| D3 | $R_0^3$     | $G_0^3$ | $B_0^3$ | ... | $R_n^3$ | $G_n^3$ | $B_n^3$ |
| D2 | $R_0^2$     | $G_0^2$ | $B_0^2$ | ... | $R_n^2$ | $G_n^2$ | $B_n^2$ |
| D1 | $R_0^1$     | $G_0^1$ | $B_0^1$ | ... | $R_n^1$ | $G_n^1$ | $B_n^1$ |
| D0 | $R_0^0$     | $G_0^0$ | $B_0^0$ | ... | $R_n^0$ | $G_n^0$ | $B_n^0$ |

## 13.4.4 16-Bit Parallel, RGB=4:4:4

When REG[0056h] bits 2-0 = 101, the LCD1 data format is specified as this format.  
 When REG[005Eh] bits 2-0 = 101, the LCD2 data format is specified as this format.

*Table 13-4: 16-Bit Parallel, RGB=4:4:4 Data Format Selection*

|     | Cycle Count |         |         |     |         |
|-----|-------------|---------|---------|-----|---------|
|     | 1           | 2       | 3       | ... | n+1     |
| D15 | $R_0^5$     | $R_1^5$ | $R_2^5$ | ... | $R_n^5$ |
| D14 | $R_0^4$     | $R_1^4$ | $R_2^4$ | ... | $R_n^4$ |
| D13 | $R_0^3$     | $R_1^3$ | $R_2^3$ | ... | $R_n^3$ |
| D12 | $R_0^2$     | $R_1^2$ | $R_2^2$ | ... | $R_n^2$ |
| D11 | $G_0^5$     | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D10 | $G_0^4$     | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D9  | $G_0^3$     | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D8  | $G_0^2$     | $G_1^2$ | $G_2^2$ | ... | $G_n^2$ |
| D7  | $B_0^5$     | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D6  | $B_0^4$     | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |
| D5  | $B_0^3$     | $B_1^3$ | $B_2^3$ | ... | $B_n^3$ |
| D4  | $B_0^2$     | $B_1^2$ | $B_2^2$ | ... | $B_n^2$ |
| D3  |             |         |         | ... |         |
| D2  |             |         |         | ... |         |
| D1  |             |         |         | ... |         |
| D0  |             |         |         | ... |         |

### 13.4.5 16-Bit Parallel, RGB=5:6:5

When REG[0056h] bits 2-0 = 110, the LCD1 data format is specified as this format.

When REG[005Eh] bits 2-0 = 110, the LCD2 data format is specified as this format.

*Table 13-5: 16-Bit Parallel, RGB=5:6:5 Data Format Selection*

| Cycle Count | 1       | 2       | 3       | ... | n+1     |
|-------------|---------|---------|---------|-----|---------|
| D15         | $R_0^5$ | $R_1^5$ | $R_2^5$ | ... | $R_n^5$ |
| D14         | $R_0^4$ | $R_1^4$ | $R_2^4$ | ... | $R_n^4$ |
| D13         | $R_0^3$ | $R_1^3$ | $R_2^3$ | ... | $R_n^3$ |
| D12         | $R_0^2$ | $R_1^2$ | $R_2^2$ | ... | $R_n^2$ |
| D11         | $R_0^1$ | $R_1^1$ | $R_2^1$ | ... | $R_n^1$ |
| D10         | $G_0^5$ | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D9          | $G_0^4$ | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D8          | $G_0^3$ | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D7          | $G_0^2$ | $G_1^2$ | $G_2^2$ | ... | $G_n^2$ |
| D6          | $G_0^1$ | $G_1^1$ | $G_2^1$ | ... | $G_n^1$ |
| D5          | $G_0^0$ | $G_1^0$ | $G_2^0$ | ... | $G_n^0$ |
| D4          | $B_0^5$ | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D3          | $B_0^4$ | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |
| D2          | $B_0^3$ | $B_1^3$ | $B_2^3$ | ... | $B_n^3$ |
| D1          | $B_0^2$ | $B_1^2$ | $B_2^2$ | ... | $B_n^2$ |
| D0          | $B_0^1$ | $B_1^1$ | $B_2^1$ | ... | $B_n^1$ |

## 13.4.6 18-Bit Parallel, RGB=6:6:6

When REG[0056h] bits 2-0 = 111, the LCD1 data format is specified as this format.

When REG[005Eh] bits 2-0 = 111, the LCD2 data format is specified as this format.

*Table 13-6: 18-Bit Parallel, RGB=6:6:6 Data Format Selection*

| Cycle Count | 1       | 2       | 3       | ... | n+1     |
|-------------|---------|---------|---------|-----|---------|
| D17         | $R_0^5$ | $R_1^5$ | $R_2^5$ | ... | $R_n^5$ |
| D16         | $R_0^4$ | $R_1^4$ | $R_2^4$ | ... | $R_n^4$ |
| D15         | $R_0^3$ | $R_1^3$ | $R_2^3$ | ... | $R_n^3$ |
| D14         | $R_0^2$ | $R_1^2$ | $R_2^2$ | ... | $R_n^2$ |
| D13         | $R_0^1$ | $R_1^1$ | $R_2^1$ | ... | $R_n^1$ |
| D12         | $R_0^0$ | $R_1^0$ | $R_2^0$ | ... | $R_n^0$ |
| D11         | $G_0^5$ | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D10         | $G_0^4$ | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D9          | $G_0^3$ | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D8          | $G_0^2$ | $G_1^2$ | $G_2^2$ | ... | $G_n^2$ |
| D7          | $G_0^1$ | $G_1^1$ | $G_2^1$ | ... | $G_n^1$ |
| D6          | $G_0^0$ | $G_1^0$ | $G_2^0$ | ... | $G_n^0$ |
| D5          | $B_0^5$ | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D4          | $B_0^4$ | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |
| D3          | $B_0^3$ | $B_1^3$ | $B_2^3$ | ... | $B_n^3$ |
| D2          | $B_0^2$ | $B_1^2$ | $B_2^2$ | ... | $B_n^2$ |
| D1          | $B_0^1$ | $B_1^1$ | $B_2^1$ | ... | $B_n^1$ |
| D0          | $B_0^0$ | $B_1^0$ | $B_2^0$ | ... | $B_n^0$ |

### 13.4.7 16-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 010, the LCD1 data format is specified as this format.

When REG[005Eh] bits 2-0 = 010, the LCD2 data format is specified as this format.

*Table 13-7: 16-Bit Parallel, RGB=8:8:8 Data Format Selection*

|     | Cycle Count |         |         |     |         |
|-----|-------------|---------|---------|-----|---------|
|     | 1           | 2       | 3       | ... | n+1     |
| D15 | $R_0^7$     | $B_0^7$ | $G_1^7$ | ... | $R_n^7$ |
| D14 | $R_0^6$     | $B_0^6$ | $G_1^6$ | ... | $R_n^6$ |
| D13 | $R_0^5$     | $B_0^5$ | $G_1^5$ | ... | $R_n^5$ |
| D12 | $R_0^4$     | $B_0^4$ | $G_1^4$ | ... | $R_n^4$ |
| D11 | $R_0^3$     | $B_0^3$ | $G_1^3$ | ... | $R_n^3$ |
| D10 | $R_0^2$     | $B_0^2$ | $G_1^2$ | ... | $R_n^2$ |
| D9  | $R_0^1$     | $B_0^1$ | $G_1^1$ | ... | $R_n^1$ |
| D8  | $R_0^0$     | $B_0^0$ | $G_1^0$ | ... | $R_n^0$ |
| D7  | $G_0^7$     | $R_1^7$ | $B_1^7$ | ... | $G_n^7$ |
| D6  | $G_0^6$     | $R_1^6$ | $B_1^6$ | ... | $G_n^6$ |
| D5  | $G_0^5$     | $R_1^5$ | $B_1^5$ | ... | $G_n^5$ |
| D4  | $G_0^4$     | $R_1^4$ | $B_1^4$ | ... | $G_n^4$ |
| D3  | $G_0^3$     | $R_1^3$ | $B_1^3$ | ... | $G_n^3$ |
| D2  | $G_0^2$     | $R_1^2$ | $B_1^2$ | ... | $G_n^2$ |
| D1  | $G_0^1$     | $R_1^1$ | $B_1^1$ | ... | $G_n^1$ |
| D0  | $G_0^0$     | $R_1^0$ | $B_1^0$ | ... | $G_n^0$ |

## 13.4.8 24-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 100, the LCD1 data format is specified as this format.  
When REG[005Eh] bits 2-0 = 100, the LCD2 data format is specified as this format.

Table 13-8: 24-Bit Parallel, RGB=8:8:8 Data Format Selection

|     | Cycle Count |         |         |     |         |
|-----|-------------|---------|---------|-----|---------|
|     | 1           | 2       | 3       | ... | n+1     |
| D23 | $R_0^7$     | $R_1^7$ | $R_2^7$ |     | $R_n^7$ |
| D22 | $R_0^6$     | $R_1^6$ | $R_2^6$ |     | $R_n^6$ |
| D21 | $R_0^5$     | $R_1^5$ | $R_2^5$ |     | $R_n^5$ |
| D20 | $R_0^4$     | $R_1^4$ | $R_2^4$ |     | $R_n^4$ |
| D19 | $R_0^3$     | $R_1^3$ | $R_2^3$ |     | $R_n^3$ |
| D18 | $R_0^2$     | $R_1^2$ | $R_2^2$ |     | $R_n^2$ |
| D17 | $R_0^1$     | $R_1^1$ | $R_2^1$ |     | $R_n^1$ |
| D16 | $R_0^0$     | $R_1^0$ | $R_2^0$ |     | $R_n^0$ |
| D15 | $G_0^7$     | $G_1^7$ | $G_2^7$ | ... | $G_n^7$ |
| D14 | $G_0^6$     | $G_1^6$ | $G_2^6$ | ... | $G_n^6$ |
| D13 | $G_0^5$     | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D12 | $G_0^4$     | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D11 | $G_0^3$     | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D10 | $G_0^2$     | $G_1^2$ | $G_2^2$ | ... | $G_n^2$ |
| D9  | $G_0^1$     | $G_1^1$ | $G_2^1$ | ... | $G_n^1$ |
| D8  | $G_0^0$     | $G_1^0$ | $G_2^0$ | ... | $G_n^0$ |
| D7  | $B_0^7$     | $B_1^7$ | $B_2^7$ | ... | $B_n^7$ |
| D6  | $B_0^6$     | $B_1^6$ | $B_2^6$ | ... | $B_n^6$ |
| D5  | $B_0^5$     | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D4  | $B_0^4$     | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |
| D3  | $B_0^3$     | $B_1^3$ | $B_2^3$ | ... | $B_n^3$ |
| D2  | $B_0^2$     | $B_1^2$ | $B_2^2$ | ... | $B_n^2$ |
| D1  | $B_0^1$     | $B_1^1$ | $B_2^1$ | ... | $B_n^1$ |
| D0  | $B_0^0$     | $B_1^0$ | $B_2^0$ | ... | $B_n^0$ |

## 13.5 Serial Data Format

When the Panel Interface bits are set for a serial panel (REG[0032h] bits 1-0 = 00 or 10), a serial data format must be selected. REG[005Ch] bits 3-2 select the data format for LCD2. A data direction which sets either the MSB or the LSB first can also be specified using REG[005Ch] bit 4.

### Note

When REG[0032h] bits 1-0 = 00, Mode 1 is enabled and LCD2 is configured as a serial panel. When REG[0032h] bits 1-0 = 10, Mode 2 is enabled and LCD2 is configured as a serial panel. For more information on possible panel combinations, see REG[0032h] bits 1-0 in Section 10.4.4, “LCD Panel Interface Generic Setting Register” on page 149.

### 13.5.1 8-Bit Serial, RGB=3:3:2

When REG[005Ch] bits 1-0 = 00, the LCD2 data format is specified as this format.

Table 13-9: 8-Bit Serial, RGB=3:2:2 Data Format Selection

|    | Cycle Count |         |         |     |         |
|----|-------------|---------|---------|-----|---------|
|    | 1           | 2       | 3       | ... | n+1     |
| D7 | $R_0^5$     | $R_1^5$ | $R_2^5$ | ... | $R_n^5$ |
| D6 | $R_0^4$     | $R_1^4$ | $R_2^4$ | ... | $R_n^4$ |
| D5 | $R_0^3$     | $R_1^3$ | $R_2^3$ | ... | $R_n^3$ |
| D4 | $G_0^5$     | $G_1^5$ | $G_2^5$ | ... | $G_n^5$ |
| D3 | $G_0^4$     | $G_1^4$ | $G_2^4$ | ... | $G_n^4$ |
| D2 | $G_0^3$     | $G_1^3$ | $G_2^3$ | ... | $G_n^3$ |
| D1 | $B_0^5$     | $B_1^5$ | $B_2^5$ | ... | $B_n^5$ |
| D0 | $B_0^4$     | $B_1^4$ | $B_2^4$ | ... | $B_n^4$ |

### 13.5.2 8-Bit Serial, RGB=4:4:4

When REG[005Ch] bits 1-0 = 01, the LCD2 data format is specified as this format.

Table 13-10: 8-Bit Serial, RGB=4:4:4 Data Format Selection

|    | Cycle Count |         |         |     |         |             |             |
|----|-------------|---------|---------|-----|---------|-------------|-------------|
|    | 1           | 2       | 3       | ... | 3n+1    | 3n+2        | 3n+3        |
| D7 | $R_0^5$     | $B_0^5$ | $G_1^5$ | ... | $R_n^5$ | $B_n^5$     | $G_{n+1}^5$ |
| D6 | $R_0^4$     | $B_0^4$ | $G_1^4$ | ... | $R_n^4$ | $B_n^4$     | $G_{n+1}^4$ |
| D5 | $R_0^3$     | $B_0^3$ | $G_1^3$ | ... | $R_n^3$ | $B_n^3$     | $G_{n+1}^3$ |
| D4 | $R_0^2$     | $B_0^2$ | $G_1^2$ | ... | $R_n^2$ | $B_n^2$     | $G_{n+1}^2$ |
| D3 | $G_0^5$     | $R_1^5$ | $B_1^5$ | ... | $G_n^5$ | $R_{n+1}^5$ | $B_{n+1}^5$ |
| D2 | $G_0^4$     | $R_1^4$ | $B_1^4$ | ... | $G_n^4$ | $R_{n+1}^4$ | $B_{n+1}^4$ |
| D1 | $G_0^3$     | $R_1^3$ | $B_1^3$ | ... | $G_n^3$ | $R_{n+1}^3$ | $B_{n+1}^3$ |
| D0 | $G_0^2$     | $R_1^2$ | $B_1^2$ | ... | $G_n^2$ | $R_{n+1}^2$ | $B_{n+1}^2$ |

## 13.6 YUV Input / Output Data Format

### 13.6.1 YUV 4:2:2 Data Input / Output Format

YUV 4:2:2 output format is selected when REG[0980h] bits 3-1 = 011 and YUV 4:2:2 input format is selected when REG[0980h] bits 3-1 = 001.

Table 13-11: YUV 4:2:2 Data Format

|     | Cycle Count |         |         |         |     |            |              |
|-----|-------------|---------|---------|---------|-----|------------|--------------|
|     | 1           | 2       | 3       | 4       | ... | 2n+1       | 2n+2         |
| D15 | $Y_0^7$     | $Y_1^7$ | $Y_2^7$ | $Y_3^7$ | ... | $Y_{2n}^7$ | $Y_{2n+1}^7$ |
| D14 | $Y_0^6$     | $Y_1^6$ | $Y_2^6$ | $Y_3^6$ | ... | $Y_{2n}^6$ | $Y_{2n+1}^6$ |
| D13 | $Y_0^5$     | $Y_1^5$ | $Y_2^5$ | $Y_3^5$ | ... | $Y_{2n}^5$ | $Y_{2n+1}^5$ |
| D12 | $Y_0^4$     | $Y_1^4$ | $Y_2^4$ | $Y_3^4$ | ... | $Y_{2n}^4$ | $Y_{2n+1}^4$ |
| D11 | $Y_0^3$     | $Y_1^3$ | $Y_2^3$ | $Y_3^3$ | ... | $Y_{2n}^3$ | $Y_{2n+1}^3$ |
| D10 | $Y_0^2$     | $Y_1^2$ | $Y_2^2$ | $Y_3^2$ | ... | $Y_{2n}^2$ | $Y_{2n+1}^2$ |
| D9  | $Y_0^1$     | $Y_1^1$ | $Y_2^1$ | $Y_3^1$ | ... | $Y_{2n}^1$ | $Y_{2n+1}^1$ |
| D8  | $Y_0^0$     | $Y_1^0$ | $Y_2^0$ | $Y_3^0$ | ... | $Y_{2n}^0$ | $Y_{2n+1}^0$ |
| D7  | $U_0^7$     | $V_0^7$ | $U_2^7$ | $V_2^7$ | ... | $U_{2n}^7$ | $V_{2n+1}^7$ |
| D6  | $U_0^6$     | $V_0^6$ | $U_2^6$ | $V_2^6$ | ... | $U_{2n}^6$ | $V_{2n+1}^6$ |
| D5  | $U_0^5$     | $V_0^5$ | $U_2^5$ | $V_2^5$ | ... | $U_{2n}^5$ | $V_{2n+1}^5$ |
| D4  | $U_0^4$     | $V_0^4$ | $U_2^4$ | $V_2^4$ | ... | $U_{2n}^4$ | $V_{2n+1}^4$ |
| D3  | $U_0^3$     | $V_0^3$ | $U_2^3$ | $V_2^3$ | ... | $U_{2n}^3$ | $V_{2n+1}^3$ |
| D2  | $U_0^2$     | $V_0^2$ | $U_2^2$ | $V_2^2$ | ... | $U_{2n}^2$ | $V_{2n+1}^2$ |
| D1  | $U_0^1$     | $V_0^1$ | $U_2^1$ | $V_2^1$ | ... | $U_{2n}^1$ | $V_{2n+1}^1$ |
| D0  | $U_0^0$     | $V_0^0$ | $U_2^0$ | $V_2^0$ | ... | $U_{2n}^0$ | $V_{2n+1}^0$ |

### 13.6.2 YUV 4:2:0 Data Input / Output Format

YUV 4:2:0 format is selected when REG[0980h] bits 3-1 = 111 and YUV 4:2:2 input format is selected when REG[0980h] bits 3-1 = 101. This data format differs between even and odd lines. The line number count starts at 0.

Table 13-12: YUV 4:2:0 Data Format (Even Line)

|     | Cycle Count |         |         |         |     |            |              |
|-----|-------------|---------|---------|---------|-----|------------|--------------|
|     | 1           | 2       | 3       | 4       | ... | 2n         | 2n+1         |
| D15 | $Y_0^7$     | $Y_1^7$ | $Y_2^7$ | $Y_3^7$ | ... | $Y_{2n}^7$ | $Y_{2n+1}^7$ |
| D14 | $Y_0^6$     | $Y_1^6$ | $Y_2^6$ | $Y_3^6$ | ... | $Y_{2n}^6$ | $Y_{2n+1}^6$ |
| D13 | $Y_0^5$     | $Y_1^5$ | $Y_2^5$ | $Y_3^5$ | ... | $Y_{2n}^5$ | $Y_{2n+1}^5$ |
| D12 | $Y_0^4$     | $Y_1^4$ | $Y_2^4$ | $Y_3^4$ | ... | $Y_{2n}^4$ | $Y_{2n+1}^4$ |
| D11 | $Y_0^3$     | $Y_1^3$ | $Y_2^3$ | $Y_3^3$ | ... | $Y_{2n}^3$ | $Y_{2n+1}^3$ |
| D10 | $Y_0^2$     | $Y_1^2$ | $Y_2^2$ | $Y_3^2$ | ... | $Y_{2n}^2$ | $Y_{2n+1}^2$ |
| D9  | $Y_0^1$     | $Y_1^1$ | $Y_2^1$ | $Y_3^1$ | ... | $Y_{2n}^1$ | $Y_{2n+1}^1$ |
| D8  | $Y_0^0$     | $Y_1^0$ | $Y_2^0$ | $Y_3^0$ | ... | $Y_{2n}^0$ | $Y_{2n+1}^0$ |
| D7  | $U_0^7$     | $V_0^7$ | $U_2^7$ | $V_2^7$ | ... | $U_{2n}^7$ | $V_{2n+1}^7$ |
| D6  | $U_0^6$     | $V_0^6$ | $U_2^6$ | $V_2^6$ | ... | $U_{2n}^6$ | $V_{2n+1}^6$ |
| D5  | $U_0^5$     | $V_0^5$ | $U_2^5$ | $V_2^5$ | ... | $U_{2n}^5$ | $V_{2n+1}^5$ |
| D4  | $U_0^4$     | $V_0^4$ | $U_2^4$ | $V_2^4$ | ... | $U_{2n}^4$ | $V_{2n+1}^4$ |
| D3  | $U_0^3$     | $V_0^3$ | $U_2^3$ | $V_2^3$ | ... | $U_{2n}^3$ | $V_{2n+1}^3$ |
| D2  | $U_0^2$     | $V_0^2$ | $U_2^2$ | $V_2^2$ | ... | $U_{2n}^2$ | $V_{2n+1}^2$ |
| D1  | $U_0^1$     | $V_0^1$ | $U_2^1$ | $V_2^1$ | ... | $U_{2n}^1$ | $V_{2n+1}^1$ |
| D0  | $U_0^0$     | $V_0^0$ | $U_2^0$ | $V_2^0$ | ... | $U_{2n}^0$ | $V_{2n+1}^0$ |

Table 13-13: YUV 4:2:0 Data Format (Odd Line)

|     | Cycle Count |         |     |              |
|-----|-------------|---------|-----|--------------|
|     | 1           | 2       | ... | n+1          |
| D15 | $Y_1^7$     | $Y_3^7$ | ... | $Y_{2n+1}^7$ |
| D14 | $Y_1^6$     | $Y_3^6$ | ... | $Y_{2n+1}^6$ |
| D13 | $Y_1^5$     | $Y_3^5$ | ... | $Y_{2n+1}^5$ |
| D12 | $Y_1^4$     | $Y_3^4$ | ... | $Y_{2n+1}^4$ |
| D11 | $Y_1^3$     | $Y_3^3$ | ... | $Y_{2n+1}^3$ |
| D10 | $Y_1^2$     | $Y_3^2$ | ... | $Y_{2n+1}^2$ |
| D9  | $Y_1^1$     | $Y_3^1$ | ... | $Y_{2n+1}^1$ |
| D8  | $Y_1^0$     | $Y_3^0$ | ... | $Y_{2n+1}^0$ |
| D7  | $Y_0^7$     | $Y_2^7$ | ... | $Y_{2n}^7$   |
| D6  | $Y_0^6$     | $Y_2^6$ | ... | $Y_{2n}^6$   |
| D5  | $Y_0^5$     | $Y_2^5$ | ... | $Y_{2n}^5$   |
| D4  | $Y_0^4$     | $Y_2^4$ | ... | $Y_{2n}^4$   |
| D3  | $Y_0^3$     | $Y_2^3$ | ... | $Y_{2n}^3$   |
| D2  | $Y_0^2$     | $Y_2^2$ | ... | $Y_{2n}^2$   |
| D1  | $Y_0^1$     | $Y_2^1$ | ... | $Y_{2n}^1$   |
| D0  | $Y_0^0$     | $Y_2^0$ | ... | $Y_{2n}^0$   |

## 13.7 YUV/RGB Conversion

The YUV/RGB Converter (YRC) converts YUV image data from the Camera interface (YUV 4:2:2), from the JPEG decoder (YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV 4:1:1), or from the Host (YUV 4:2:2, 4:2:0) to RGB data (RGB 5:6:5, RGB 8:8:8). The YUV data range input can be selected using the YRC Input Data Type Select bit (REG[0240h] bit 4) and the transfer mode can be selected using the YUV/RGB Transfer mode bits (REG[0240h] bits 2-0).

The YUV/RGB Converter uses the following parameters and equations.

$$\begin{aligned} 0 &\leq Y \leq 255 \\ -128 &\leq U \leq 127 \\ -128 &\leq V \leq 127 \end{aligned}$$

Table 13-14: YUV/RGB Conversion Parameter Table

| Transfer Mode                                   | REG[0240h] bit 2-0 | Color          | E <sub>y</sub> | E <sub>pb</sub> | E <sub>pr</sub> |
|-------------------------------------------------|--------------------|----------------|----------------|-----------------|-----------------|
| Recommendation<br>ITU-R BT.709                  | 001                | E <sub>R</sub> | 1.000          | 0.000           | 1.575           |
|                                                 |                    | E <sub>G</sub> | 1.000          | -0.187          | -0.468          |
|                                                 |                    | E <sub>B</sub> | 1.002          | 1.855           | 0.000           |
| Recommendation<br>ITU-R BT.470-6<br>System M    | 100                | E <sub>R</sub> | 1.000          | 0.001           | 1.400           |
|                                                 |                    | E <sub>G</sub> | 1.000          | -0.333          | -0.712          |
|                                                 |                    | E <sub>B</sub> | 1.000          | 1.780           | 0.002           |
| Recommendation<br>ITU-R BT.470-6<br>System B, G | 101                | E <sub>R</sub> | 1.000          | 0.000           | 1.402           |
|                                                 |                    | E <sub>G</sub> | 1.000          | -0.344          | -0.714          |
|                                                 |                    | E <sub>B</sub> | 1.000          | 1.772           | 0.000           |
| SMPTE 170M                                      | 110                | E <sub>R</sub> | 1.000          | 0.000           | 1.402           |
|                                                 |                    | E <sub>G</sub> | 1.000          | -0.344          | -0.714          |
|                                                 |                    | E <sub>B</sub> | 1.000          | 1.772           | 0.000           |
| SMPTE 240M(1987)                                | 111                | E <sub>R</sub> | 1.000          | 0.000           | 1.576           |
|                                                 |                    | E <sub>G</sub> | 1.000          | -0.226          | -0.477          |
|                                                 |                    | E <sub>B</sub> | 1.000          | 1.826           | 0.000           |

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} E_R E_y & E_R E_{pb} & E_R E_{pr} \\ E_G E_y & E_G E_{pb} & E_G E_{pr} \\ E_B E_y & E_B E_{pb} & E_B E_{pr} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Figure 13-9: YUV/RGB Conversion Equation

## 13.8 RGB/YUV Conversion

The RGB/YUV Converter (RYC) converts RGB data to YUV or YCbCr data format (see REG[0260h] bit 4). This allows the contents of the display buffer (including PIP<sup>+</sup> window with rotated camera images) to be converted to YUV format and then encoded to JPEG data which the Host can transfer. To enable the RGB/YUV Converter, clear the RGB/YUV Converter Disable bit (REG[0260h] bit 15 = 0).

The RGB/YUV Converter uses the following parameters and equations.

Where the RGB input is:

$$0 \leq R \leq 255$$

$$0 \leq G \leq 255$$

$$0 \leq B \leq 255$$

and the YUV output is:

$$0 \leq Y \leq 255$$

$$0 \leq U \leq 255$$

$$0 \leq V \leq 255$$

the YCbCr output limit is:

$$16 \leq Y \leq 235$$

$$16 \leq Cb \leq 240$$

$$16 \leq Cr \leq 240$$

Table 13-15: RGB/YUV Conversion Parameter Table

| Transfer Mode                                   | REG[0260h] bit 2-0 | Color    | E'g     | E'b     | E'r     |
|-------------------------------------------------|--------------------|----------|---------|---------|---------|
| Recommendation<br>ITU-R BT.709                  | 001                | Y (E'y)  | 0.7152  | 0.0722  | 0.2126  |
|                                                 |                    | U (E'pb) | -0.3860 | 0.5000  | -0.1150 |
|                                                 |                    | V (E'pr) | -0.4540 | -0.0460 | 0.5000  |
| Recommendation<br>ITU-R BT.470-6<br>System M    | 100                | Y (E'y)  | 0.5900  | 0.1100  | 0.3000  |
|                                                 |                    | U (E'pb) | -0.3310 | 0.5000  | -0.1690 |
|                                                 |                    | V (E'pr) | -0.4210 | -0.0790 | 0.5000  |
| Recommendation<br>ITU-R BT.470-6<br>System B, G | 101                | Y (E'y)  | 0.5870  | 0.1140  | 0.2990  |
|                                                 |                    | U (E'pb) | -0.3310 | 0.5000  | -0.1690 |
|                                                 |                    | V (E'pr) | -0.4190 | -0.0810 | 0.5000  |
| SMPTE 170M                                      | 110                | Y (E'y)  | 0.5870  | 0.1140  | 0.2990  |
|                                                 |                    | U (E'pb) | -0.3310 | 0.5000  | -0.1690 |
|                                                 |                    | V (E'pr) | -0.4190 | -0.0810 | 0.5000  |
| SMPTE 240M(1987)                                | 111                | Y (E'y)  | 0.7010  | 0.0870  | 0.2120  |
|                                                 |                    | U (E'pb) | -0.3840 | 0.5000  | -0.1160 |
|                                                 |                    | V (E'pr) | -0.4450 | -0.0550 | 0.5000  |

For YUV conversion, the equation is summarized as:

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} E'g & E'b & E'r \\ E'g & E'b & E'r \\ E'g & E'b & E'r \end{bmatrix} \cdot \begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

*Figure 13-10: YUV Conversion Equation*

For YCbCr conversion, the equation is summarized as:

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} \frac{219}{255} & 0 & 0 \\ 0 & \frac{224}{255} & 0 \\ 0 & 0 & \frac{224}{255} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix}$$

*Figure 13-11: YUV Conversion Equation*

# 14 SwivelView™

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

The image is not actually rotated in the display buffer since there is no address translation during CPU read/write. The image is rotated during display refresh.

## 14.1 SwivelView Modes

### 14.1.1 90° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13715 in the following sense: A–B–C–D. The display is refreshed by the S1D13715 in the following sense: B–D–A–C.

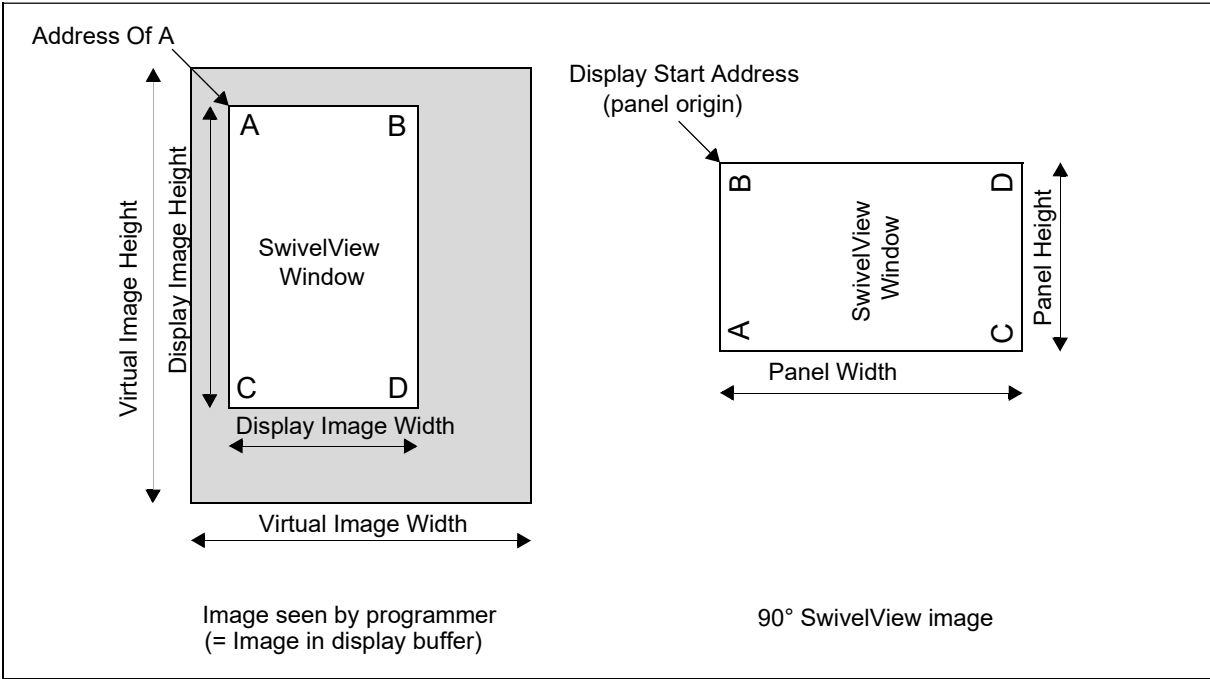


Figure 14-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView.

**Display Start Address**

The display refresh circuitry starts at pixel “B”, therefore the Display Start Address register must be programmed with the address of pixel “B”.

Display Start Address = Address of A + Line Address Offset - (bpp ÷ 8)

**Line Address Offset**

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

**Memory Address of a Given Pixel**

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x Virtual Image Width] x bpp ÷ 8

### 14.1.2 180° SwivelView

The following figure shows how the programmer sees a landscape image and how the image is being displayed. The application image is written to the S1D13715 in the following sense: A–B–C–D. The display is refreshed by the S1D13715 in the following sense: D–C–B–A.

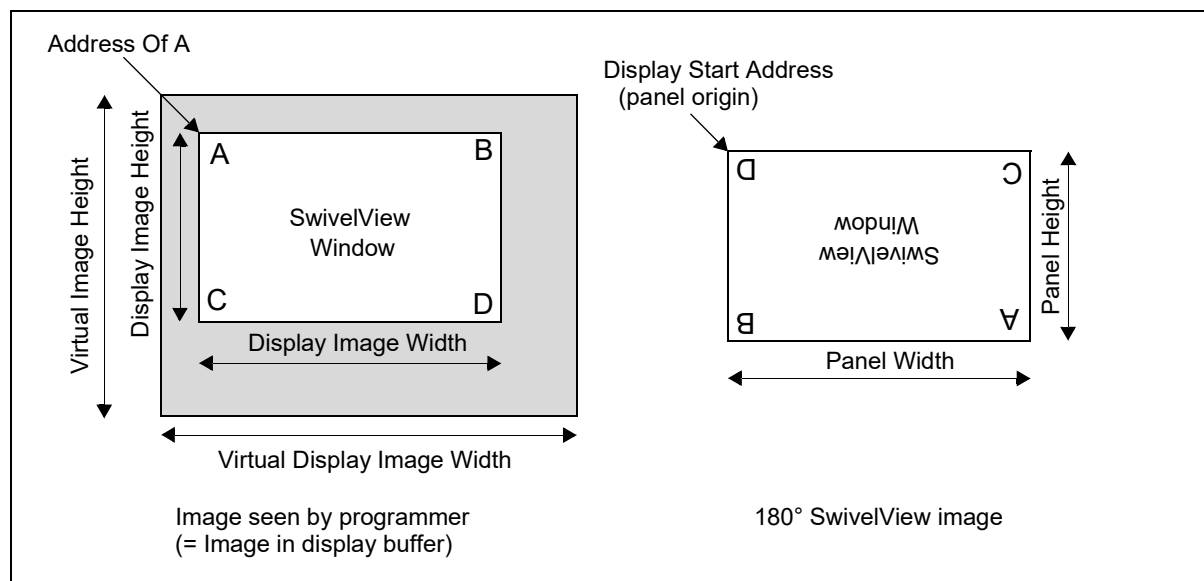


Figure 14-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView.

#### Display Start Address

The display refresh circuitry starts at pixel “D”, therefore the Display Start Address register must be programmed with the address of pixel “D”.

Display Start Address = Address of A + Line Address Offset x Display Image Height - (bpp ÷ 8)

#### Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

#### Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x Virtual Image Height] x bpp ÷ 8

### 14.1.3 270° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13715 in the following sense: A-B-C-D. The display is refreshed by the S1D13715 in the following sense: C-A-D-B.

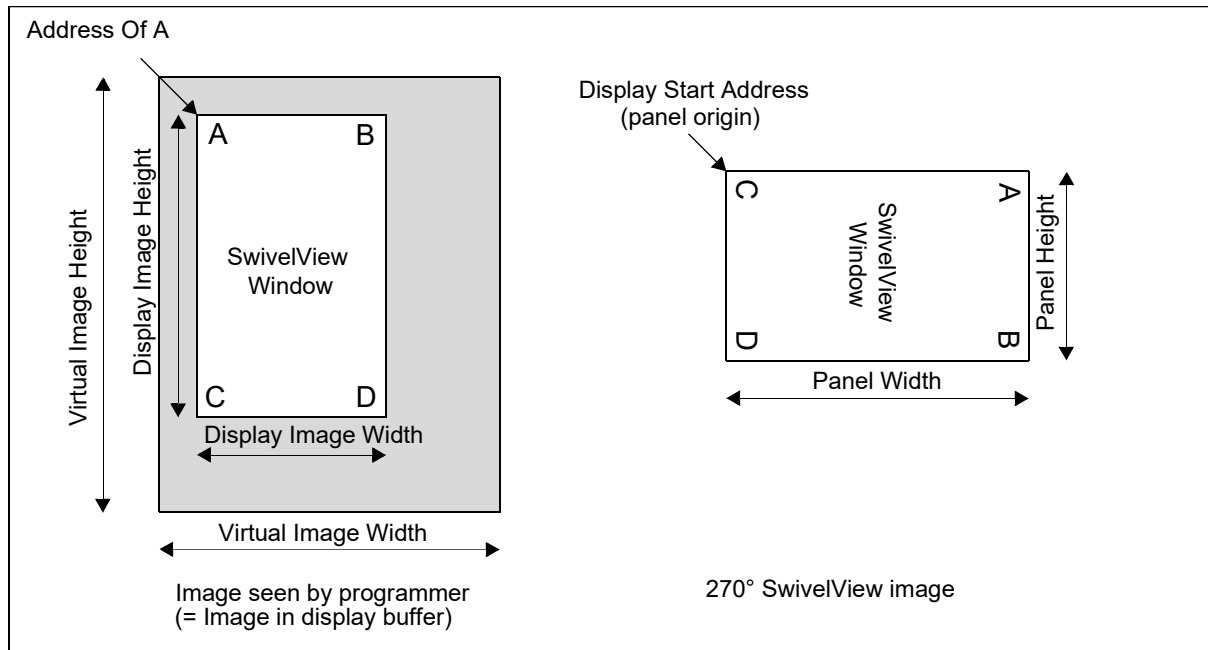


Figure 14-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView.

#### Display Start Address

The display refresh circuitry starts at pixel “C”, therefore the Display Start Address register must be programmed with the address of pixel “C”.

Display Start Address  
 = Address of A + Line Address Offset × (Display Image Width - 1)

#### Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width × bpp ÷ 8

#### Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) × Virtual Image Width] × bpp ÷ 8

# 15 Picture-in-Picture Plus (PIP+)

Picture-in-Picture Plus (PIP+) enables a secondary window (or PIP+ window) within the main display window. The PIP+ window may be positioned anywhere within the main window display and is controlled using the PIP+ Window control registers (REG[0218h]-[0228h]). The PIP+ window color depth (REG[0200h] bits 3-2) and SwivelView orientation (REG[0202h] bits 5-4) are independent from the Main window.

The following diagrams show examples of a PIP+ window within a main window and the registers used to position it.

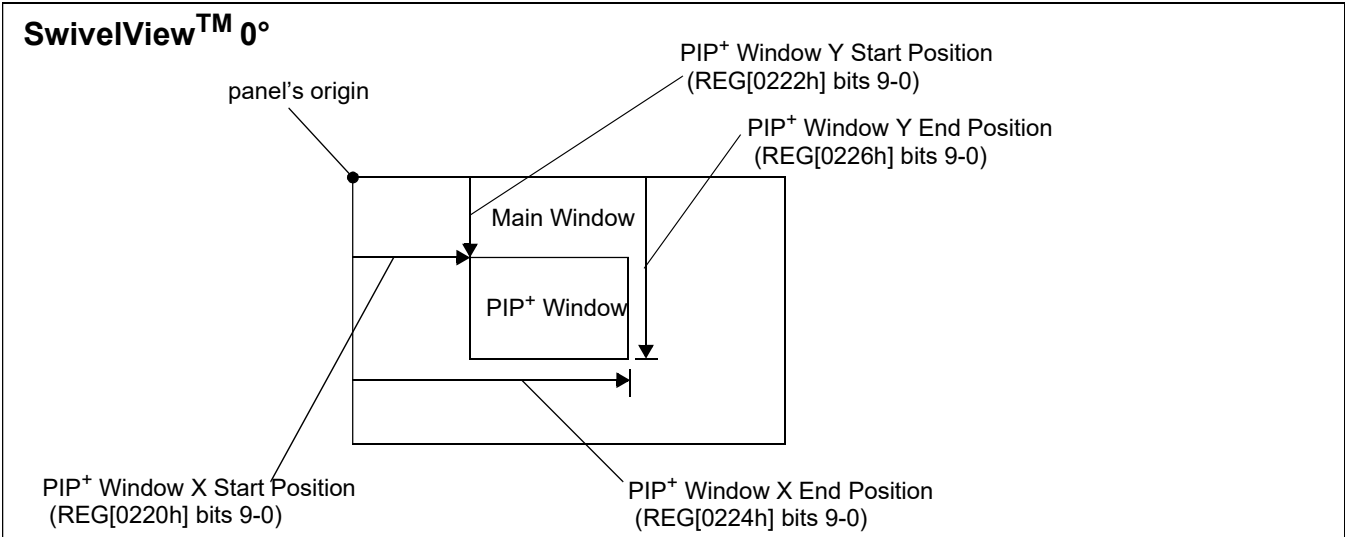


Figure 15-1: PIP+ with SwivelView Disabled (SwivelView 0°)

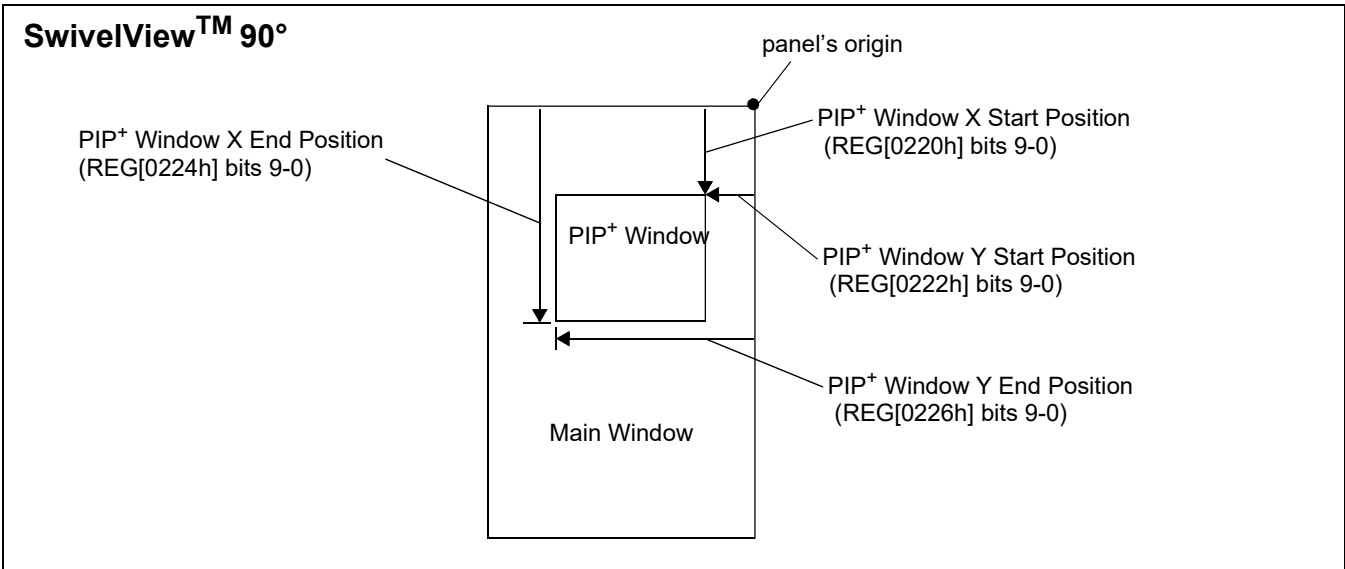


Figure 15-2: PIP+ with SwivelView 90° Enabled

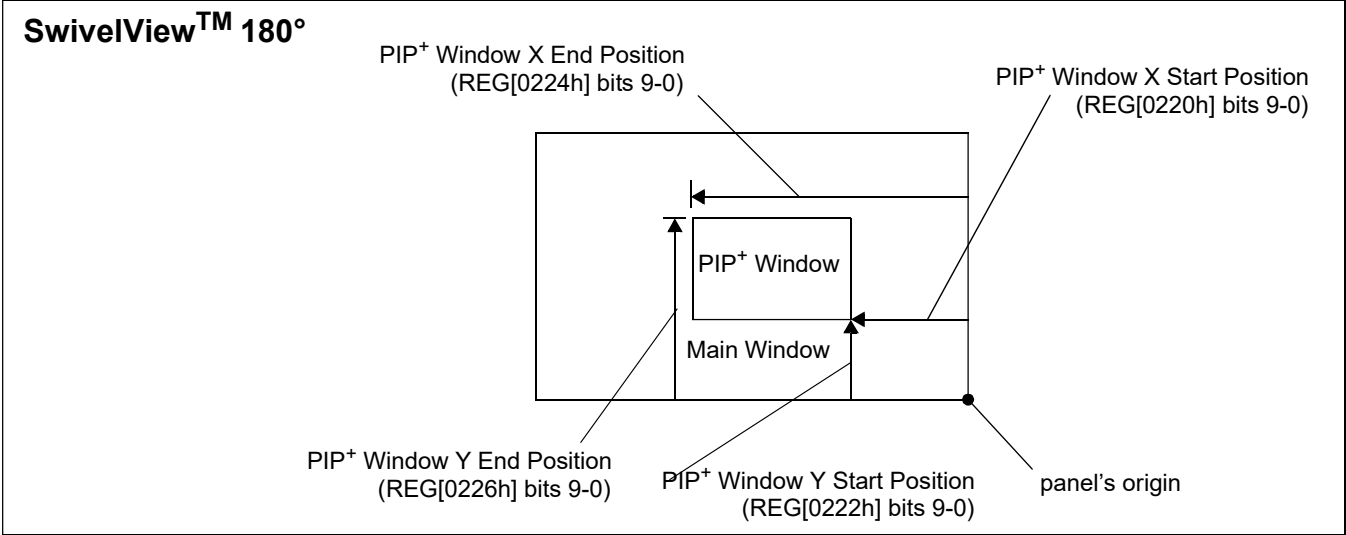


Figure 15-3: PIP+ with SwivelView 180° Enabled

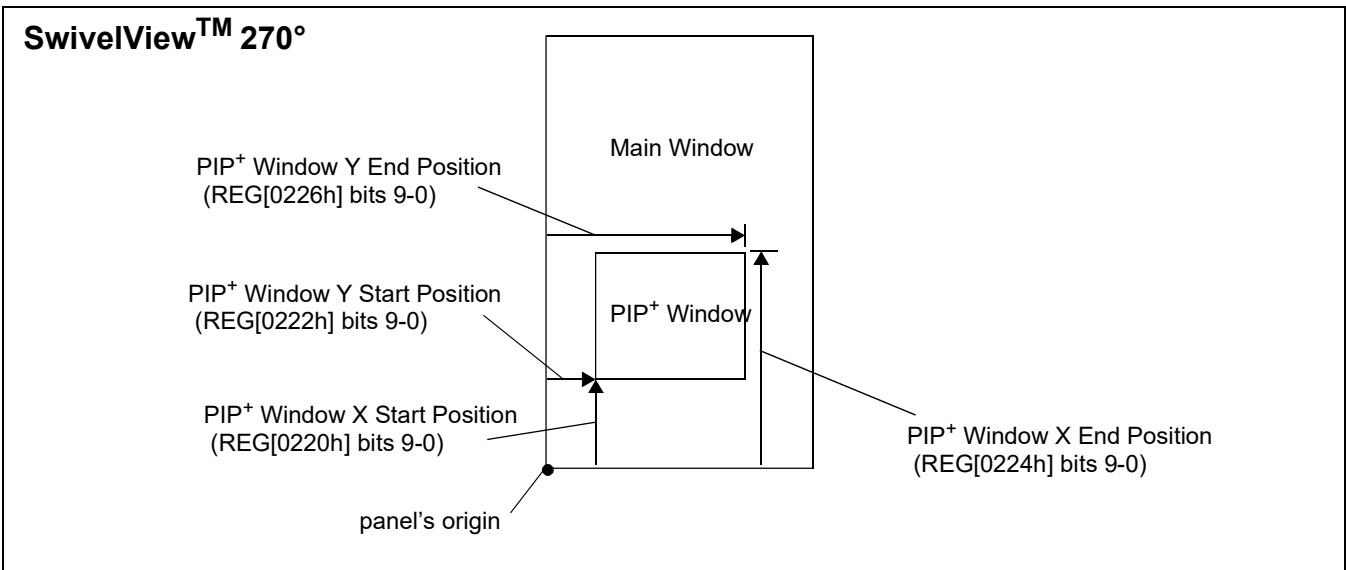


Figure 15-4: PIP+ with SwivelView 270° Enabled

## 15.1 Overlay Display

When Picture-in-Picture Plus (PIP<sup>+</sup>) is enabled, the S1D13715 supports an overlay with the following functions: Transparent, Average, AND, OR, and INV. Each RGB component of the overlay function key colors are set using REG[0204h]-[0208h] and REG[0304h]-[0326h].

The overlay settings are specified using the Overlay Key Color registers for each RGB color and individual Overlay Key Color Enable bits (see REG[0328h]) as follows.

Table 15-1: Overlay Mode Selection

| Register                                                                | Overlay PIP <sup>+</sup><br>Window Bit Shift<br>(REG[0328h] bit 15) | Overlay Main<br>Window Bit Shift<br>(REG[0328h] bit 13) | Display Image                                             |
|-------------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------------|
| Transparent Overlay Key Color<br>REG[0204h]<br>REG[0206h]<br>REG[0208h] | 0                                                                   | *                                                       | PIP <sup>+</sup> window data                              |
|                                                                         | 1                                                                   |                                                         | (PIP <sup>+</sup> window data)/2                          |
| Average Overlay Key Color<br>REG[0310h]<br>REG[0312h]<br>REG[0314h]     | 0                                                                   | 0                                                       | ((PIP <sup>+</sup> window data) + (Key Color data))/2     |
|                                                                         |                                                                     | 1                                                       | ((PIP <sup>+</sup> window data) + (Key Color data))/2/2   |
|                                                                         | 1                                                                   | 0                                                       | ((PIP <sup>+</sup> window data)/2 + (Key Color data))/2   |
|                                                                         |                                                                     | 1                                                       | ((PIP <sup>+</sup> window data)/2 + (Key Color data))/2/2 |
| AND Overlay Key Color<br>REG[0316h]<br>REG[0318h]<br>REG[031Ah]         | 0                                                                   | 0                                                       | (PIP <sup>+</sup> window data) AND (Key Color data)       |
|                                                                         |                                                                     | 1                                                       | (PIP <sup>+</sup> window data) AND (Key Color data)/2     |
|                                                                         | 1                                                                   | 0                                                       | (PIP <sup>+</sup> window data)/2 AND (Key Color data)     |
|                                                                         |                                                                     | 1                                                       | (PIP <sup>+</sup> window data)/2 AND (Key Color data)/2   |
| OR Overlay Key Color<br>REG[031Ch]<br>REG[031Eh]<br>REG[0320h]          | 0                                                                   | 0                                                       | (PIP <sup>+</sup> window data) OR (Key Color data)        |
|                                                                         |                                                                     | 1                                                       | (PIP <sup>+</sup> window data) OR (Key Color data)/2      |
|                                                                         | 1                                                                   | 0                                                       | (PIP <sup>+</sup> window data)/2 OR (Key Color data)      |
|                                                                         |                                                                     | 1                                                       | (PIP <sup>+</sup> window data)/2 OR (Key Color data)/2    |
| INV Overlay Key Color<br>REG[0322h]<br>REG[0324h]<br>REG[0326h]         | 0                                                                   | *                                                       | Negative image of (PIP <sup>+</sup> window data)          |
|                                                                         | 1                                                                   |                                                         | Negative image of (PIP <sup>+</sup> window data)/2        |

The following table shows the resulting PIP+ window color when overlay is combined with the PIP+ Window Bit Shift and the Main Window Bit Shift functions.

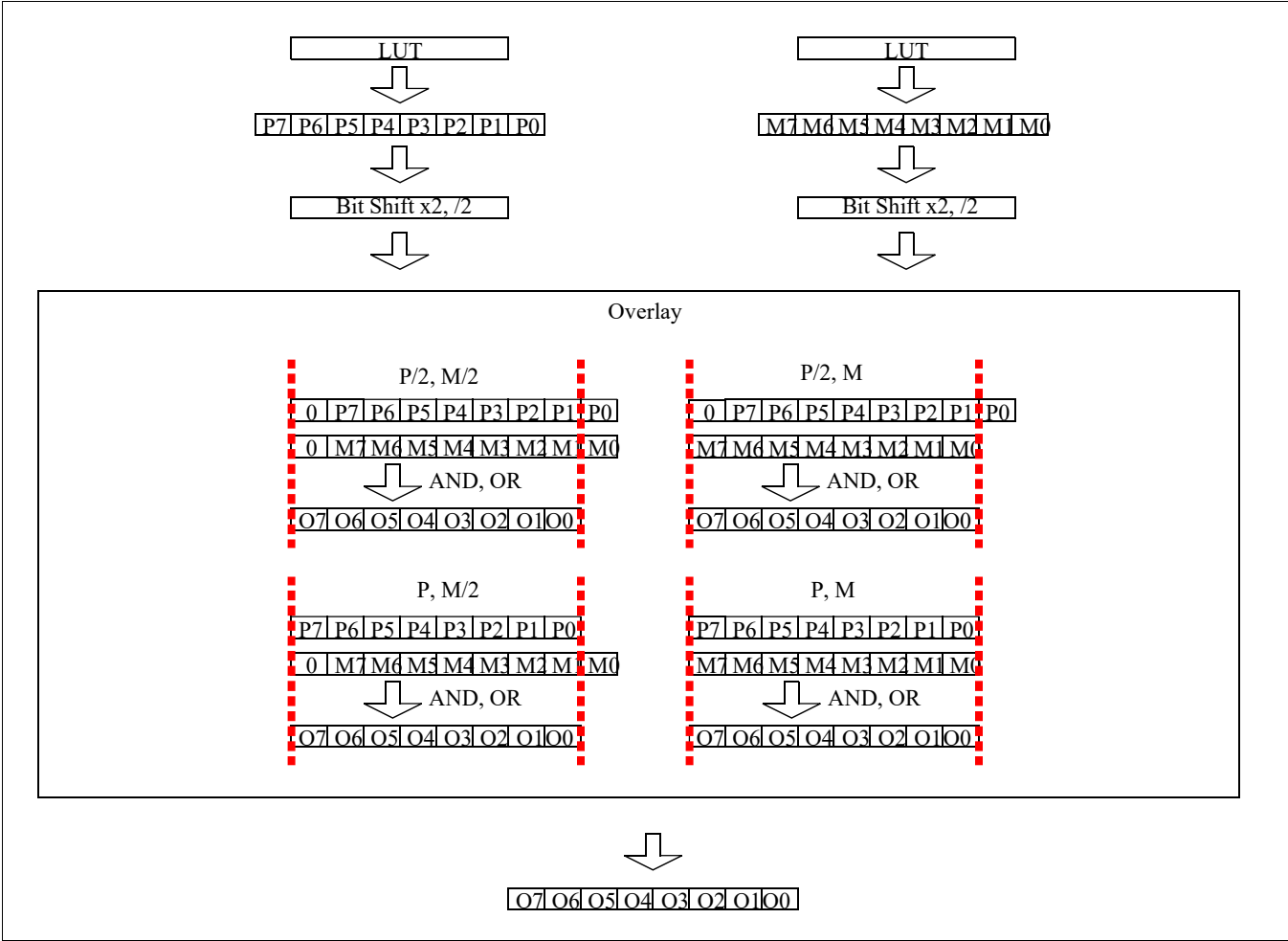


Figure 15-5: Data Flow for Bit Shift Function

15.1.1 Overlay Display Effects

- When PIP+ is disabled (REG[0200h] bits 9-8 = 00)
- Only the Main window is displayed and the PIP+ Window is ignored.
- When PIP+ is enabled (REG[0200h] bits 9-8 = 01)
- The PIP+ window area “overlays” the Main window area. The Overlay Key Color settings are ignored.
- When PIP+ with overlay is enabled (REG[0200h] bits 9-8 = 11)
- The PIP+ window area “overlays” the Main window area only on areas of the Main window where the color matches the overlay key color. For the Main window area, only the Main window is displayed.

- For the PIP+ Window area, if the Main window data is same as the Overlay Key color, then the PIP+ window data is mixed with the Main window data as specified for each overlay function (see Figure 15-6: “Overlay Display Effects 1,” on page 342). If the Main window data differs from the Overlay Key color, then the Main window data is displayed. If two or more Overlays are active, they have the following priority: Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. A lower priority overlay function is ignored and only the highest priority overlay function is displayed.



Figure 15-6: Overlay Display Effects 1



Figure 15-7: Overlay Display Effects 2

**Note**

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. In the case where Transparent and INV overlay are enabled, the INV function is ignored.

# 16 2D BitBLT Engine

## 16.1 Overview

The purpose of the BitBLT Engine is to off-load the work of the CPU for moving pixel data to and from the CPU and display memory and also for moving pixel data from one location to another in display memory.

There are 5 BitBLTs (Bit Block Transfer) which are used to move pixel data from one location to another.

- **Read BitBLT:** Move pixel data from Display Memory to CPU
- **Move BitBLT:** Move pixel data from one location in Display Memory to another
- **Pattern Fill BitBLT:** Move a Pixel Pattern in Display Memory and duplicate several times to produce a larger image
- **Solid Fill BitBLT:** Move a Single Color to a location in Memory

The BitBLT Engine can perform several Data Functions in combination with some of the BitBLT functions on the pixel data.

- **ROP:** Perform a Boolean function on the pixel data
- **Transparency:** Only write pixel data of which the color does not match the Transparent Color.

The BitBLT Engine supports pixel data color depths of 8 bpp and 16 bpp and CPU data transfers of 16-bits or 8-bits.

The destination and source BitBLTs can be set to be either contiguous linear blocks of memory (Linear) or as a rectangular region of memory (Rectangular).

### Note

The S1D13715 BitBLT engine does not support 32 bpp modes.

## 16.2 BitBLTs

### 16.2.1 Read BitBLT

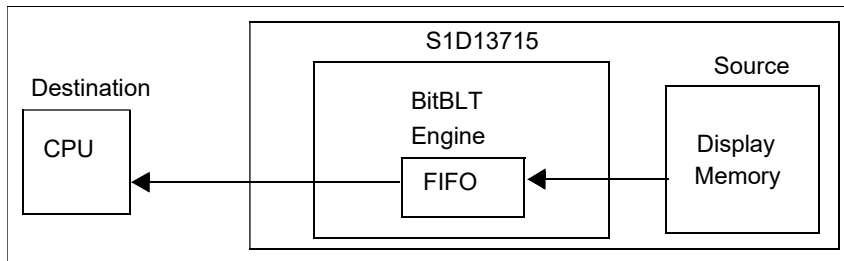


Figure 16-1: Read BitBLT Data Flow

Data can be read from memory by the Host CPU using the BitBLT Engine. The source of the data is the S1D13715 internal memory (stored as either Linear or Rectangular data format). The destination of the data to the Host CPU can also be configured to either Linear or Rectangular data format. No data functions like ROP, Transparency or Color Expansion are supported for Read BitBLTs. If these features are enabled, they are ignored. The Read Phase can also be set for either the first data read at the start of the BitBLT for Linear or at the start of each line for Rectangular. The Read Phase allows the user to set which byte in the data read is the first byte read from memory.

### 16.2.2 Move BitBLT

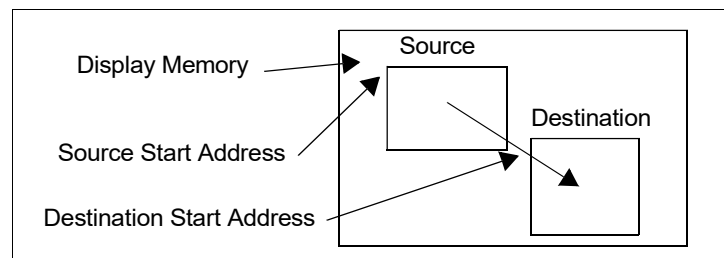


Figure 16-2: Move BitBLT data flow

The Move BitBLT copies data from the source area in memory to the destination area. The source data can also be ROP'ed with the destination data and then written back to the destination. The source data can also be Color Expanded using the Color Expansion data function and then stored to the destination. Transparency can also be applied to the source data. The source and the destination can be in either Linear or Rectangular data format. The top left hand corner of the BitBLT Window is always specified as the start address for the source and destination.

16.2.3 Pattern Fill BitBLT

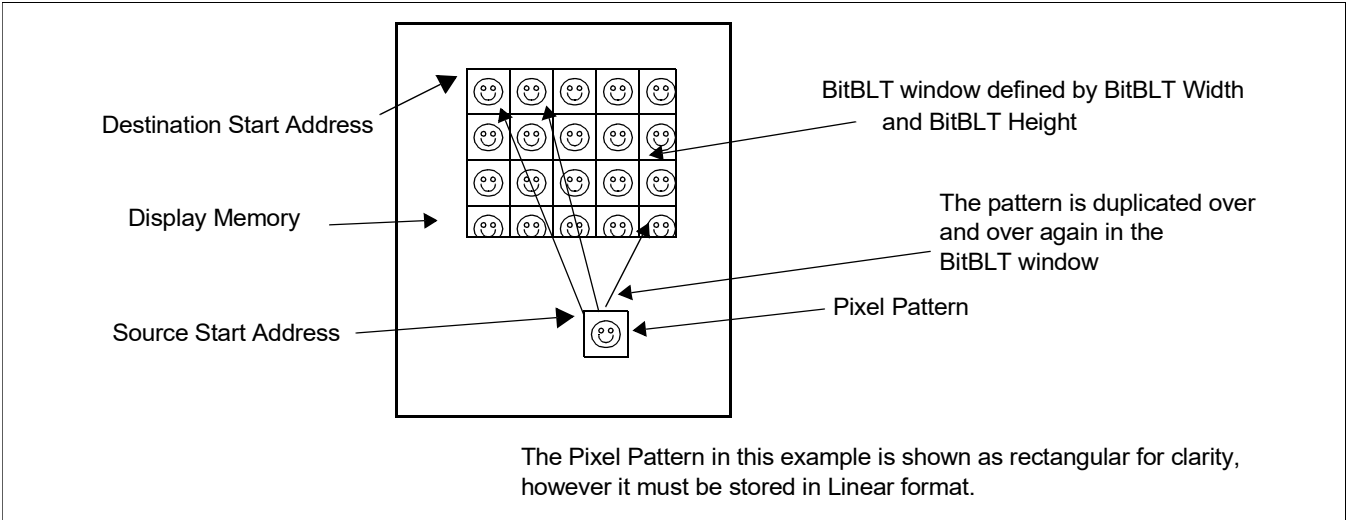


Figure 16-3: Pattern Fill Drawing

The Pattern Fill BitBLT allows an 8 x 8 pixel pattern to be duplicated multiple times to a larger area in memory as shown in the example above. The Pixel Pattern is stored at one location and it is read and drawn multiple times to the BitBLT window. For Pattern Fill BitBLTs, the Pixel Pattern, which is the source data, must be Linear and the destination, which is the BitBLT window, must be Rectangular. The source data can also be ROP'ed with the destination data and then written back to the destination.

The start of the Pixel Pattern must be aligned to a 16-bit address. The Pixel Pattern can be drawn to a BitBLT window area of 1 x 1 pixel to a max of the BitBLT Width x BitBLT Height.

16.2.4 Solid Fill BitBLT

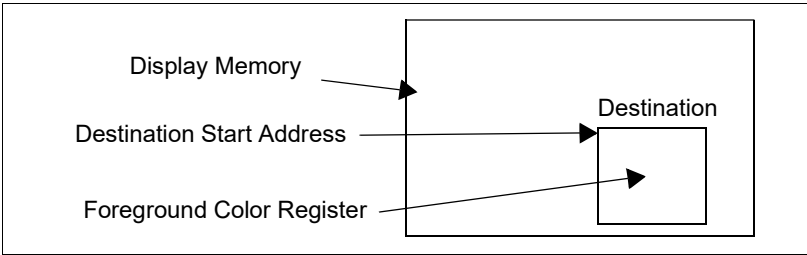


Figure 16-4: Solid Fill BitBLT Data Flow

For Solid Fill BitBLTs, the foreground color is written to the destination. The foreground color can be ROP'ed with the destination. The destination can also be Linear or Rectangular data format.

For 8 bpp, the foreground color is specified by REG[8024h] bits 7-0.  
 For 16 bpp, the foreground color is specified by REG[8024h] bits 15-0.

### 16.2.5 BitBLT Terms

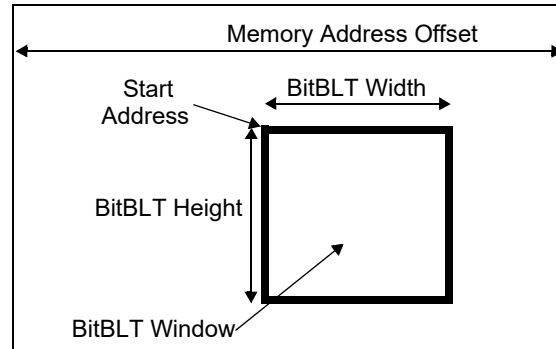
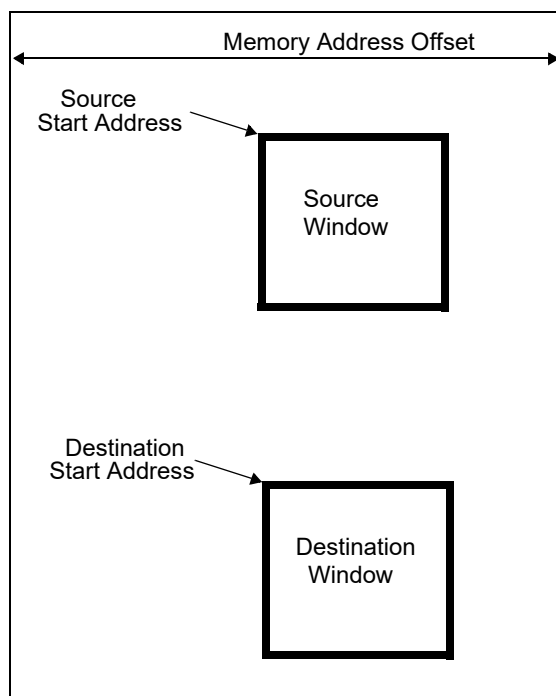


Figure 16-5: BitBLT Terms

|                       |                                                                                                                                                  |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Memory Address Offset | Width of the display (i.e. Main Window width or PIP+ Window width) in 16-bit words. The source and destination share the memory address offsets. |
| Start Address         | Top left corner of the BitBLT window specified in bytes.                                                                                         |
| BitBLT Width          | Width of the BitBLT in pixels.                                                                                                                   |
| BitBLT Height         | Height of the BitBLT in pixels.                                                                                                                  |
| BitBLT Window         | The area of the display memory to work with.                                                                                                     |

For each bitBLT there is a source of data and a destination for the result data. The source is the location where the data for the data function (i.e. color expansion, ROP, and transparency) is read from. The destination is where the data for the data function (i.e. ROP) is read from and also the location where the result is written to.

### 16.2.6 Source and Destination



*Figure 16-6: Source and Destination*

### 16.3 Data Functions

The following data functions are supported by the BitBLT Engine. For some BitBLTs these functions can be combined together for some BitBLTs.

- Color Expansion
- ROP
- Transparency

### 16.3.1 ROP

ROPs allow for a boolean function to be applied to the source and destination data. The boolean function is selected using the BitBLT ROP Code bits (REG[800Ah] bits 3-0). Functions such as AND, OR, XOR, NAND, NOR, and others can be selected. The following example shows the results for 3 different ROPs with the same source and destination input.

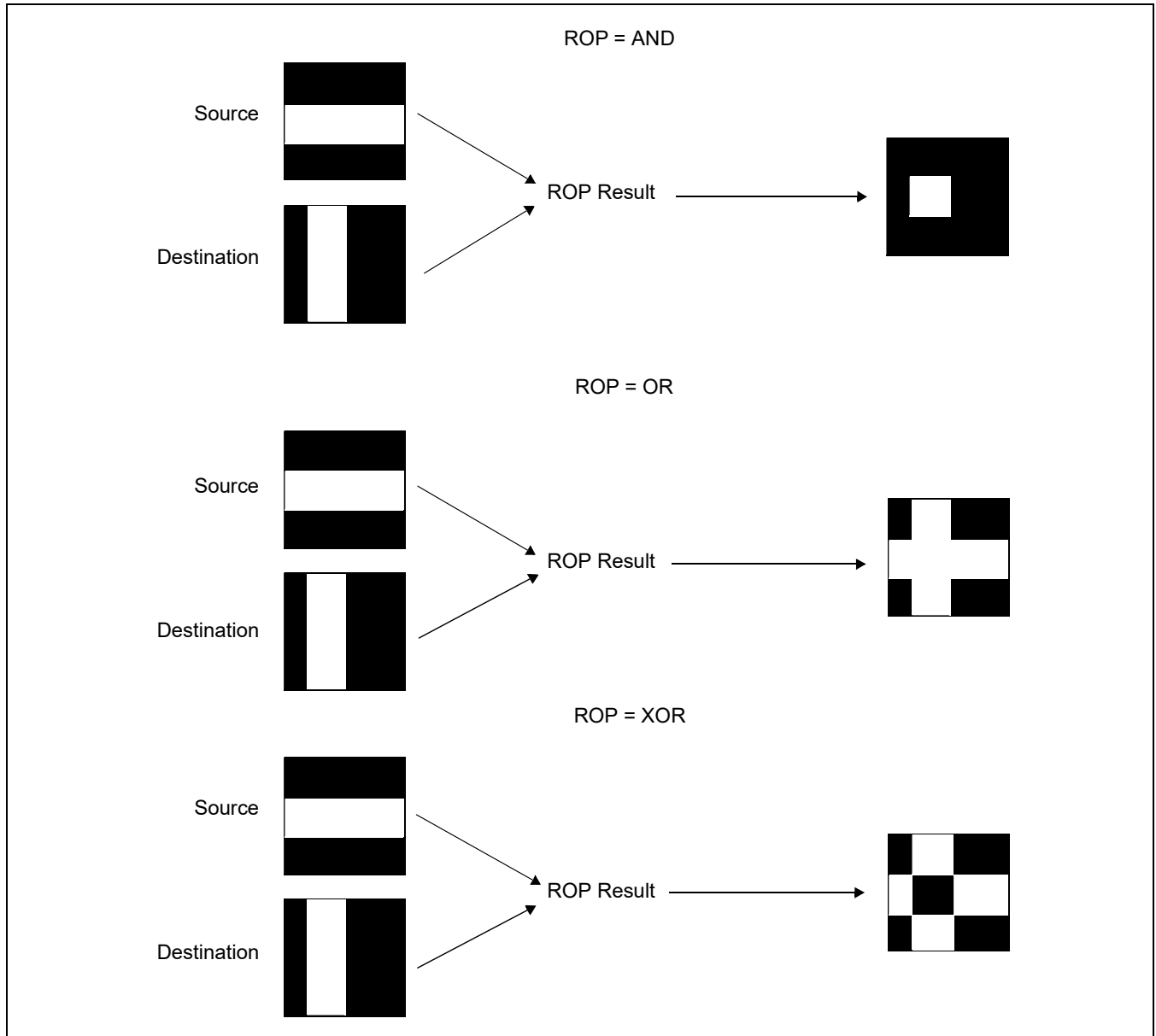
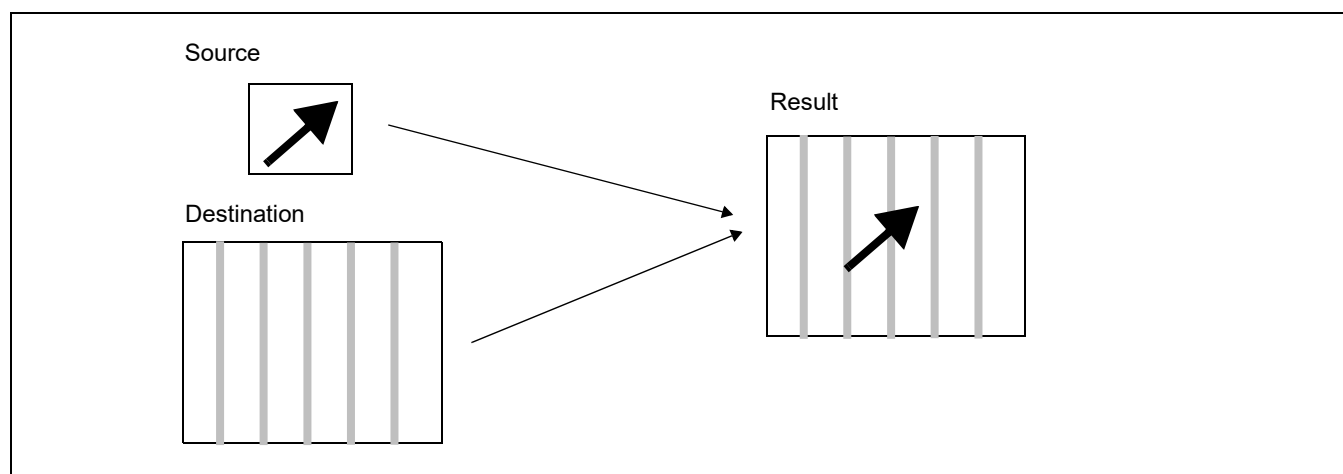


Figure 16-7: ROP Example

### 16.3.2 Transparency

Transparency allows for colors which do not match the background color to be written to the destination. This is useful when a non-square image contained in the BitBLT window is to be written over another image. For example, a mouse pointer is stored in memory as a block, but when the pointer is written to the display only the color of the pointer is written and the colors around it are not. The following example shows how the source image of a mouse pointer with its color set to black and color around it set to white would appear over the destination image using Transparency. The white color (which matches the background color) around the mouse pointer is not written over the destination image, yet the black mouse pointer is.



*Figure 16-8: Transparency Example*

## 16.4 Linear / Rectangular

Most BitBLTs support linear or rectangular data formats for the source and destination.

Linear means that the data in memory or to be written by the Host CPU is in a continuous format with no gaps between the EOL (End of Line) and SOL (Start of Line). The line offset is ignored for the linear data format. The following example shows how each line of linear data is stored in display memory for a BitBLT with a height of 5. Note that the SOL of Line 2 starts right after the EOL of Line 1. For 8 bpp, the next SOL starts in the byte after the previous lines EOL. For 16 bpp, it is the word after the previous line's EOL.

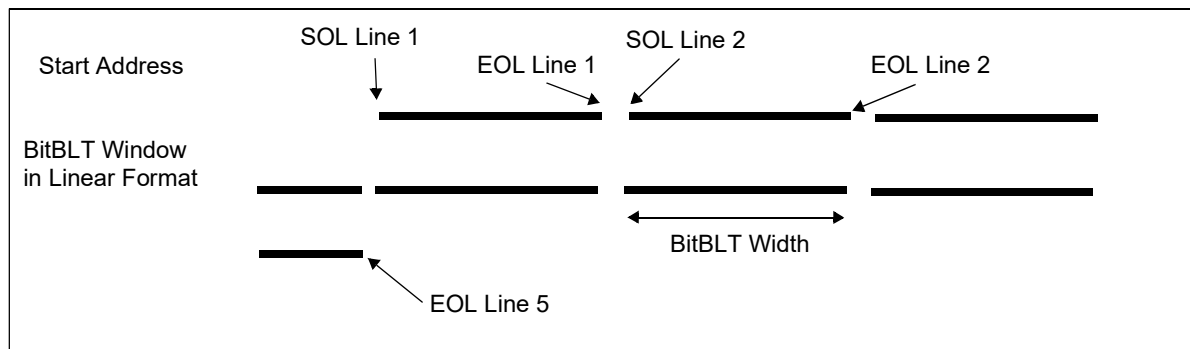


Figure 16-9: Memory Linear Example

The following example shows how linear Host CPU data is written for 16-bit writes. The SOL of the next line starts in the same 16-bit data as the EOL of the previous line.

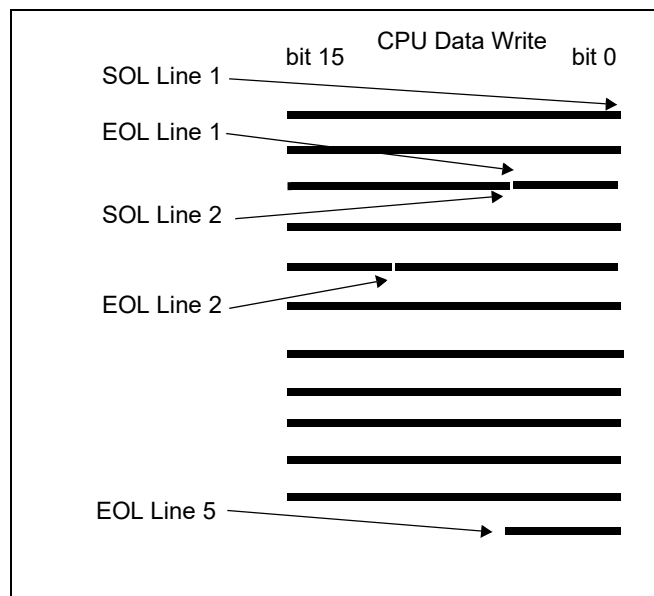


Figure 16-10: Memory Linear Example

Rectangular means that after each EOL, the SOL of the next line is the SOL of the current line plus the line offset for memory accesses. For Host CPU accesses, the SOL of the next line is always in the data written after the data with the EOL.

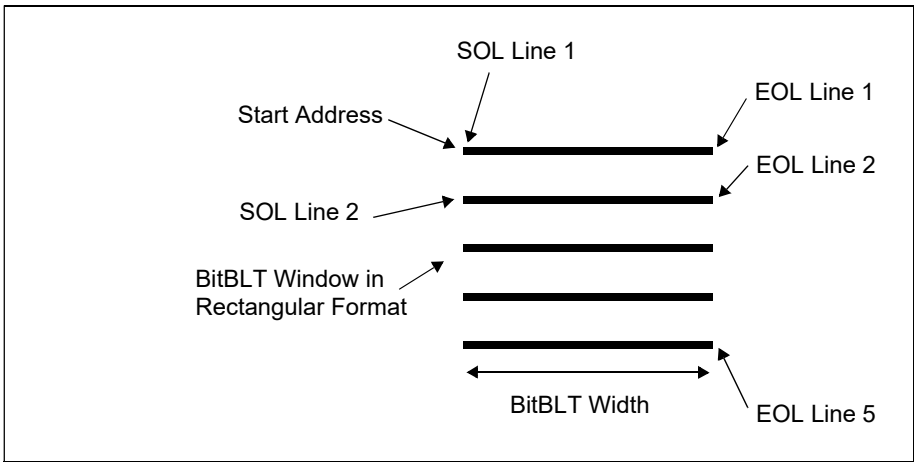


Figure 16-11: Memory Rectangular Example

The following example shows how rectangular Host CPU data is written for 16-bit writes. The SOL of the next line starts in the next 16-bit data after the EOL of the previous line.

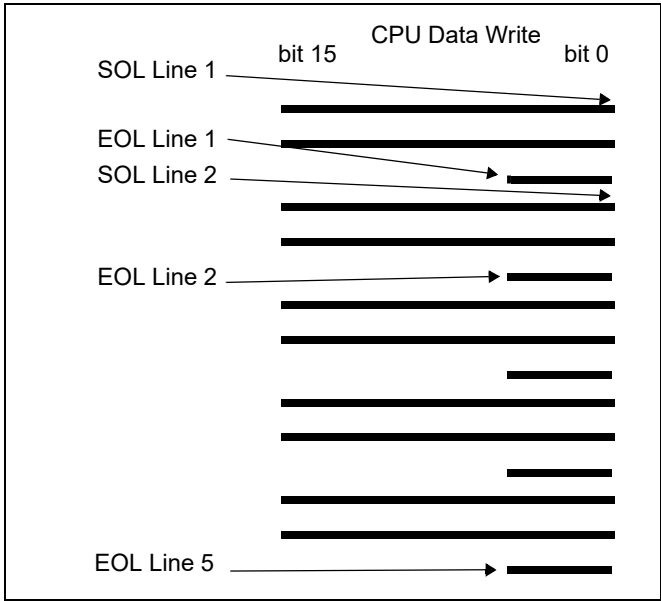


Figure 16-12: Memory Linear Example

## 17 Resizers

Resizers perform the trimming and scaling functions that can be used to “resize” image data from the camera interface and/or the JPEG decoder. There are two resizers, one for viewing image data and one for viewing/capturing image data.

Image data from the camera interface (always YUV 4:2:2 format) can use either the View resizer or the Capture resizer before being stored in the display memory. If image data from the camera interface is being sent to the JPEG Codec for JPEG encoding, it must use the Capture resizer. View and Capture resizer functions are configured independently.

Image data from the JPEG decoder (YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV 4:1:1 formats) or from the Host CPU can only use the View resizer before being stored in the display buffer.

The resize function is a two stage process - trimming then scaling.

### 17.1 Trimming Function

The trimming function is similar to cropping an image and “trims” the unwanted portion of the image. The trimming is controlled using the Resizer X/Y Start/End Position registers (REG[0944h]-[094Ah] or REG[0964h]-[096Ah]). The Start and End addresses programmed in these registers are limited by the size of the actual camera image or the actual size of the decoded JPEG image and must not be set to a value greater than these actual sizes. The Start and End Position registers are set in 1 pixel increments.

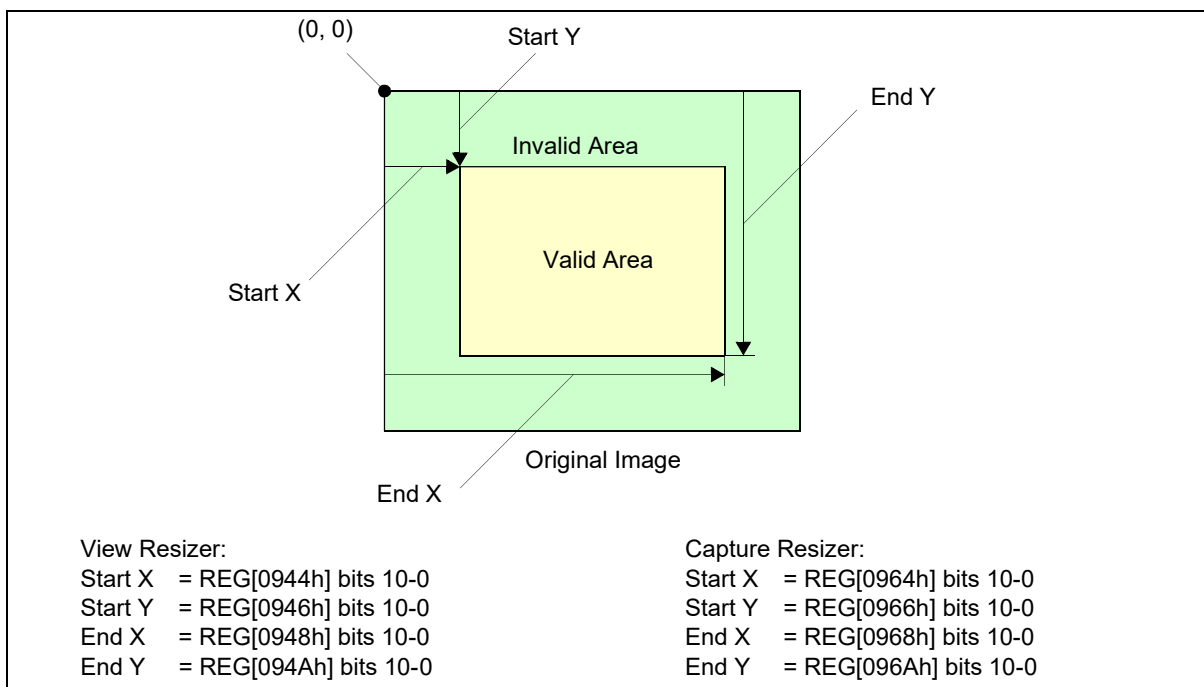


Figure 17-1: Trimming Function

17.2 Scaling Function

The scaling function takes place after the trimming stage and it specifies the desired compression ratio to be applied to the image. When image data is scaled by the capture resizer for JPEG Encoding, the JPEG Codec size registers must be set for the image size **after** scaling.

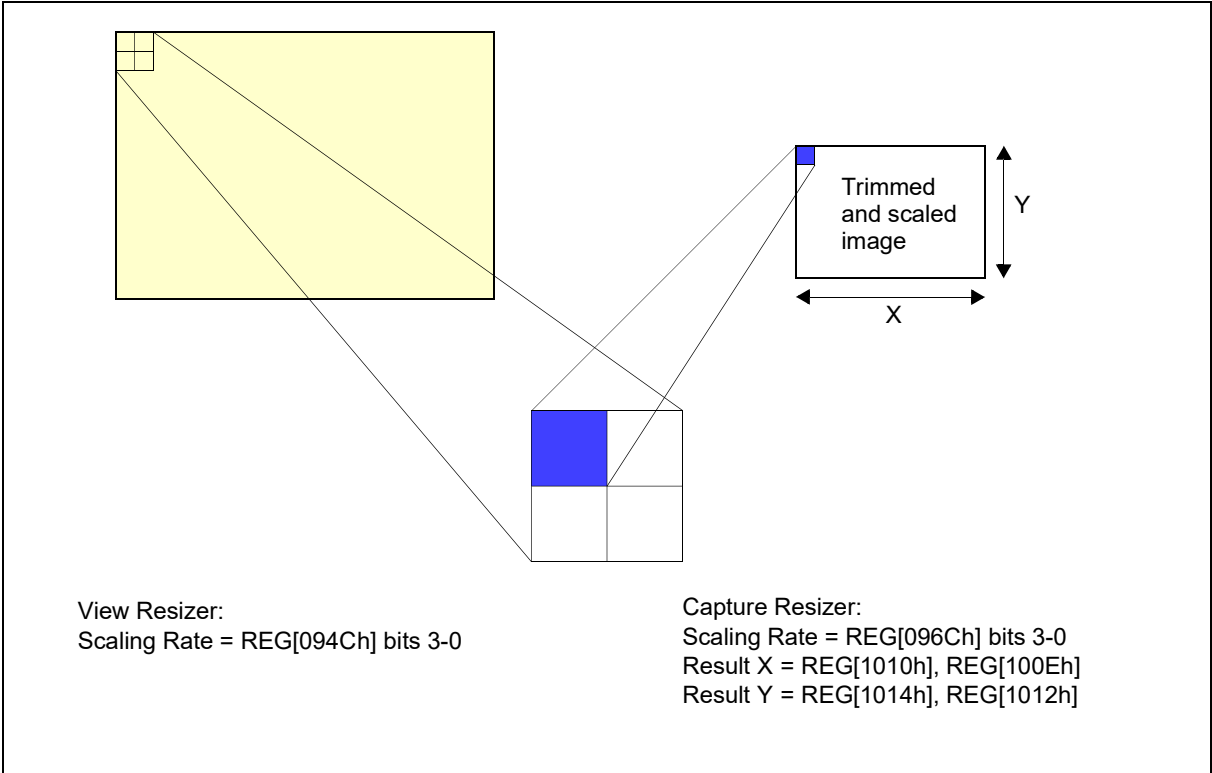


Figure 17-2: Scaling Example (1/2 Scaling)

17.2.1 1/2 Scaling

For 1/2 scaling, each 2x2 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

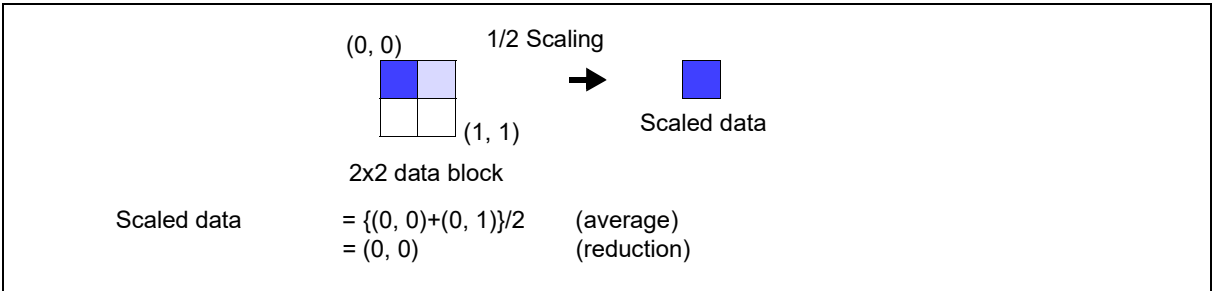


Figure 17-3: 1/2 Compression

17.2.2 1/3 Scaling

For 1/3 scaling, each 3x3 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

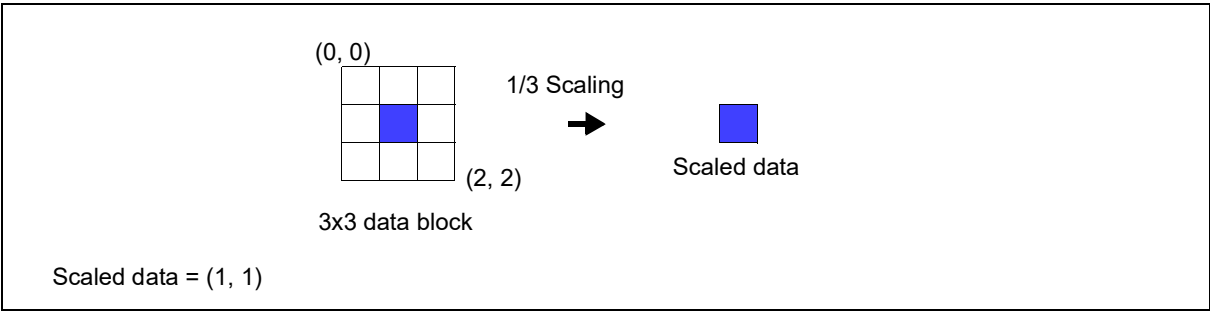


Figure 17-4: 1/3 Scaling

17.2.3 1/4 Scaling

For 1/4 scaling, each 4x4 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

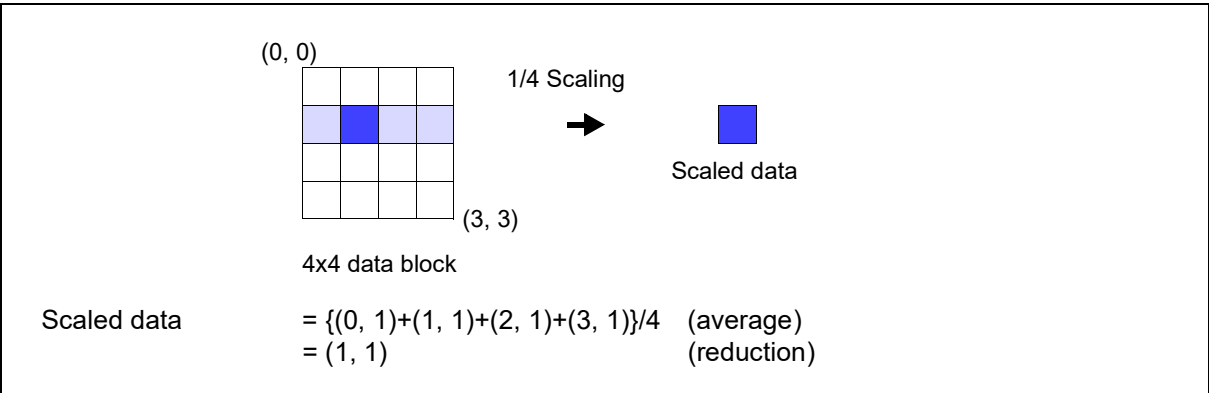


Figure 17-5: 1/4 Scaling

17.2.4 1/5 Scaling

For 1/5 Scaling, each 5x5 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

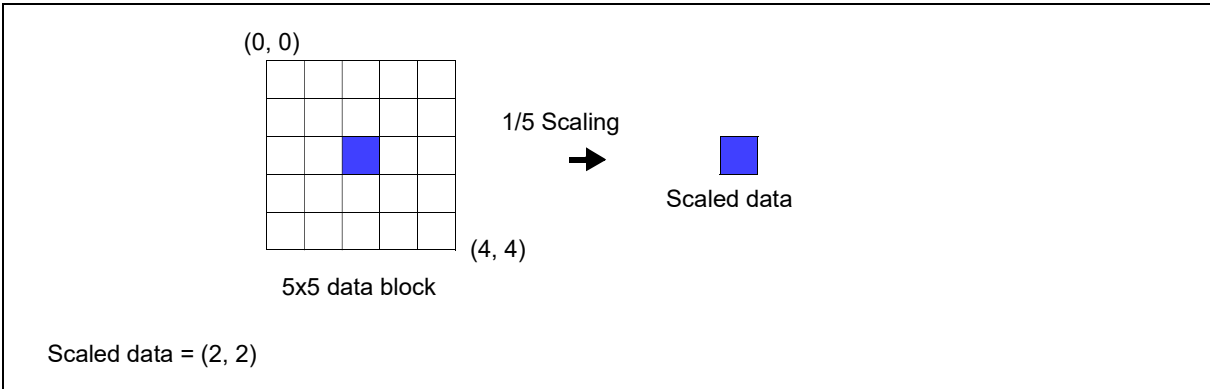


Figure 17-6: 1/5 Scaling

17.2.5 1/6 Scaling

For 1/6 scaling, each 6x6 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

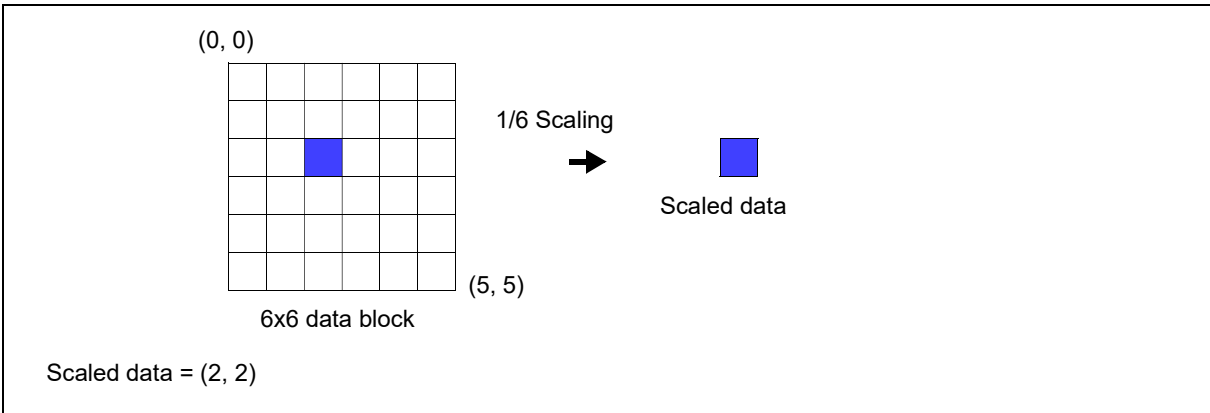


Figure 17-7: 1/6 Scaling

### 17.2.6 1/7 Scaling

For 1/7 scaling, each 7x7 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

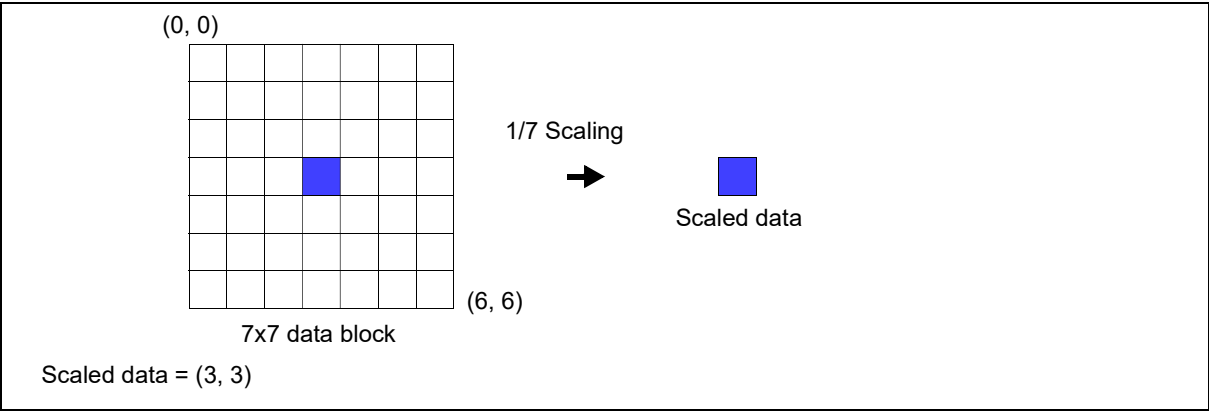


Figure 17-8: 1/7 Scaling

### 17.2.7 1/8 Scaling

For 1/8 scaling, each 8x8 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

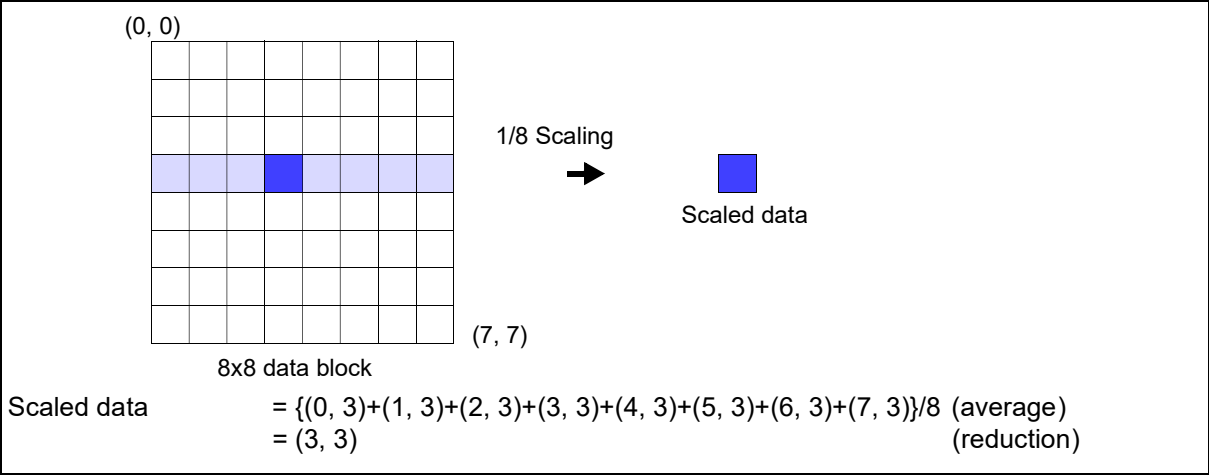


Figure 17-9: 1/8 Scaling

### 17.3 Resizer Restrictions

If any of the resizer registers must be changed while data is being received (from the camera interface, from the JPEG Decoder, or from the Host CPU), the View Resizer Register Update VSYNC Enable bit (REG[0940h] bit 1) or the Capture Resizer Update VSYNC Enable bit (REG[0960h] bit 1) must be set to 1 before changing any resizer register values.

The resizer X/Y Start/End Position registers must not be set larger than the incoming image size.

The dimensions specified by the View Resizer X/Y Start/End Position registers (REG[0944h] - REG[094Ah]) must be divisible by the View Resizer Scaling Rate (REG[094Ch] bits 5-0). The dimensions specified by the Capture Resizer X/Y Start/End Position registers (REG[0964h] - REG[096Ah]) must be divisible by the Capture Resizer Scaling Rate (REG[096Ch] bits 5-0).

Refer to the following table for a summary of the resizer horizontal restrictions.

*Table 17-1: Resizer Horizontal Restrictions Summary*

| YUV Format | Scaling Rate | Start Position | Resolution | YUV Format     | Scaling Rate | Start Position | Resolution | YUV Format   | Scaling Rate | Start Position | Resolution |
|------------|--------------|----------------|------------|----------------|--------------|----------------|------------|--------------|--------------|----------------|------------|
| 4:4:4      | 1/1          | 1 pixel        | 1 pixel    | 4:2:2<br>4:2:0 | 1/1          | 2 pixel        | 2 pixels   | YUV<br>4:1:1 | 1/1          | 4 pixel        | 4 pixels   |
|            | 1/2          |                | 2 pixels   |                | 1/2          |                | 2 pixels   |              | 1/2          |                | 4 pixels   |
|            | 1/3          |                | 3 pixels   |                | 1/3          |                | 6 pixels   |              | 1/3          |                | 12 pixels  |
|            | 1/4          |                | 4 pixels   |                | 1/4          |                | 4 pixels   |              | 1/4          |                | 4 pixels   |
|            | 1/5          |                | 5 pixels   |                | 1/5          |                | 10 pixels  |              | 1/5          |                | 20 pixels  |
|            | 1/6          |                | 6 pixels   |                | 1/6          |                | 6 pixels   |              | 1/6          |                | 12 pixels  |
|            | 1/7          |                | 7 pixels   |                | 1/7          |                | 14 pixels  |              | 1/7          |                | 28 pixels  |
|            | 1/8          |                | 8 pixels   |                | 1/8          |                | 8 pixels   |              | 1/8          |                | 8 pixels   |
|            | 1/9          |                | 9 pixels   |                | 1/9          |                | 18 pixels  |              | 1/9          |                | 36 pixels  |
|            | 1/10         |                | 10 pixels  |                | 1/10         |                | 10 pixels  |              | 1/10         |                | 20 pixels  |
|            | 1/11         |                | 11 pixels  |                | 1/11         |                | 22 pixels  |              | 1/11         |                | 44 pixels  |
|            | 1/12         |                | 12 pixels  |                | 1/12         |                | 12 pixels  |              | 1/12         |                | 12 pixels  |
|            | 1/13         |                | 13 pixels  |                | 1/13         |                | 26 pixels  |              | 1/13         |                | 52 pixels  |
|            | 1/14         |                | 14 pixels  |                | 1/14         |                | 14 pixels  |              | 1/14         |                | 28 pixels  |
|            | 1/15         |                | 15 pixels  |                | 1/15         |                | 30 pixels  |              | 1/15         |                | 60 pixels  |
|            | 1/16         |                | 16 pixels  |                | 1/16         |                | 16 pixels  |              | 1/16         |                | 16 pixels  |
|            | 1/17         |                | 17 pixels  |                | 1/17         |                | 34 pixels  |              | 1/17         |                | 68 pixels  |
|            | 1/18         |                | 18 pixels  |                | 1/18         |                | 18 pixels  |              | 1/18         |                | 36 pixels  |
|            | 1/19         |                | 19 pixels  |                | 1/19         |                | 38 pixels  |              | 1/19         |                | 76 pixels  |
|            | 1/20         |                | 20 pixels  |                | 1/20         |                | 20 pixels  |              | 1/20         |                | 20 pixels  |
|            | 1/21         |                | 21 pixels  |                | 1/21         |                | 42 pixels  |              | 1/21         |                | 84 pixels  |
|            | 1/22         |                | 22 pixels  |                | 1/22         |                | 22 pixels  |              | 1/22         |                | 44 pixels  |
|            | 1/23         |                | 23 pixels  |                | 1/23         |                | 46 pixels  |              | 1/23         |                | 92 pixels  |
|            | 1/24         |                | 24 pixels  |                | 1/24         |                | 24 pixels  |              | 1/24         |                | 24 pixels  |
|            | 1/25         |                | 25 pixels  |                | 1/25         |                | 50 pixels  |              | 1/25         |                | 100 pixels |
|            | 1/26         |                | 26 pixels  |                | 1/26         |                | 26 pixels  |              | 1/26         |                | 52 pixels  |
|            | 1/27         |                | 27 pixels  |                | 1/27         |                | 54 pixels  |              | 1/27         |                | 108 pixels |
|            | 1/28         |                | 28 pixels  |                | 1/28         |                | 28 pixels  |              | 1/28         |                | 28 pixels  |
|            | 1/29         |                | 29 pixels  |                | 1/29         |                | 58 pixels  |              | 1/29         |                | 116 pixels |
|            | 1/30         |                | 30 pixels  |                | 1/30         |                | 30 pixels  |              | 1/30         |                | 60 pixels  |
|            | 1/31         |                | 31 pixels  |                | 1/31         |                | 62 pixels  |              | 1/31         |                | 124 pixels |
|            | 1/32         |                | 32 pixels  |                | 1/32         |                | 32 pixels  |              | 1/32         |                | 32 pixels  |

Refer to the following table for a summary of the resizer vertical restrictions.

*Table 17-2: Resizer Vertical Restrictions Summary*

| YUV Format              | Scaling Rate | Start Position | Resolution | YUV Format | Scaling Rate | Start Position | Resolution |
|-------------------------|--------------|----------------|------------|------------|--------------|----------------|------------|
| 4:4:4<br>4:2:2<br>4:1:1 | 1/1          | 1 line         | 1 pixel    | 4:2:0      | 1/1          | 2 lines        | 2 pixels   |
|                         | 1/2          |                | 2 pixels   |            | 1/2          |                | 2 pixels   |
|                         | 1/3          |                | 3 pixels   |            | 1/3          |                | 6 pixels   |
|                         | 1/4          |                | 4 pixels   |            | 1/4          |                | 4 pixels   |
|                         | 1/5          |                | 5 pixels   |            | 1/5          |                | 10 pixels  |
|                         | 1/6          |                | 6 pixels   |            | 1/6          |                | 6 pixels   |
|                         | 1/7          |                | 7 pixels   |            | 1/7          |                | 14 pixels  |
|                         | 1/8          |                | 8 pixels   |            | 1/8          |                | 8 pixels   |
|                         | 1/9          |                | 9 pixels   |            | 1/9          |                | 18 pixels  |
|                         | 1/10         |                | 10 pixels  |            | 1/10         |                | 10 pixels  |
|                         | 1/11         |                | 11 pixels  |            | 1/11         |                | 22 pixels  |
|                         | 1/12         |                | 12 pixels  |            | 1/12         |                | 12 pixels  |
|                         | 1/13         |                | 13 pixels  |            | 1/13         |                | 26 pixels  |
|                         | 1/14         |                | 14 pixels  |            | 1/14         |                | 14 pixels  |
|                         | 1/15         |                | 15 pixels  |            | 1/15         |                | 30 pixels  |
|                         | 1/16         |                | 16 pixels  |            | 1/16         |                | 16 pixels  |
|                         | 1/17         |                | 17 pixels  |            | 1/17         |                | 34 pixels  |
|                         | 1/18         |                | 18 pixels  |            | 1/18         |                | 18 pixels  |
|                         | 1/19         |                | 19 pixels  |            | 1/19         |                | 38 pixels  |
|                         | 1/20         |                | 20 pixels  |            | 1/20         |                | 20 pixels  |
|                         | 1/21         |                | 21 pixels  |            | 1/21         |                | 42 pixels  |
|                         | 1/22         |                | 22 pixels  |            | 1/22         |                | 22 pixels  |
|                         | 1/23         |                | 23 pixels  |            | 1/23         |                | 46 pixels  |
|                         | 1/24         |                | 24 pixels  |            | 1/24         |                | 24 pixels  |
|                         | 1/25         |                | 25 pixels  |            | 1/25         |                | 50 pixels  |
|                         | 1/26         |                | 26 pixels  |            | 1/26         |                | 26 pixels  |
|                         | 1/27         |                | 27 pixels  |            | 1/27         |                | 54 pixels  |
|                         | 1/28         |                | 28 pixels  |            | 1/28         |                | 28 pixels  |
|                         | 1/29         |                | 29 pixels  |            | 1/29         |                | 58 pixels  |
|                         | 1/30         |                | 30 pixels  |            | 1/30         |                | 30 pixels  |
|                         | 1/31         |                | 31 pixels  |            | 1/31         |                | 62 pixels  |
|                         | 1/32         |                | 32 pixels  |            | 1/32         |                | 32 pixels  |

## 18 Digital Video Functions

The following is an overview block diagram of how the digital video functions interact.

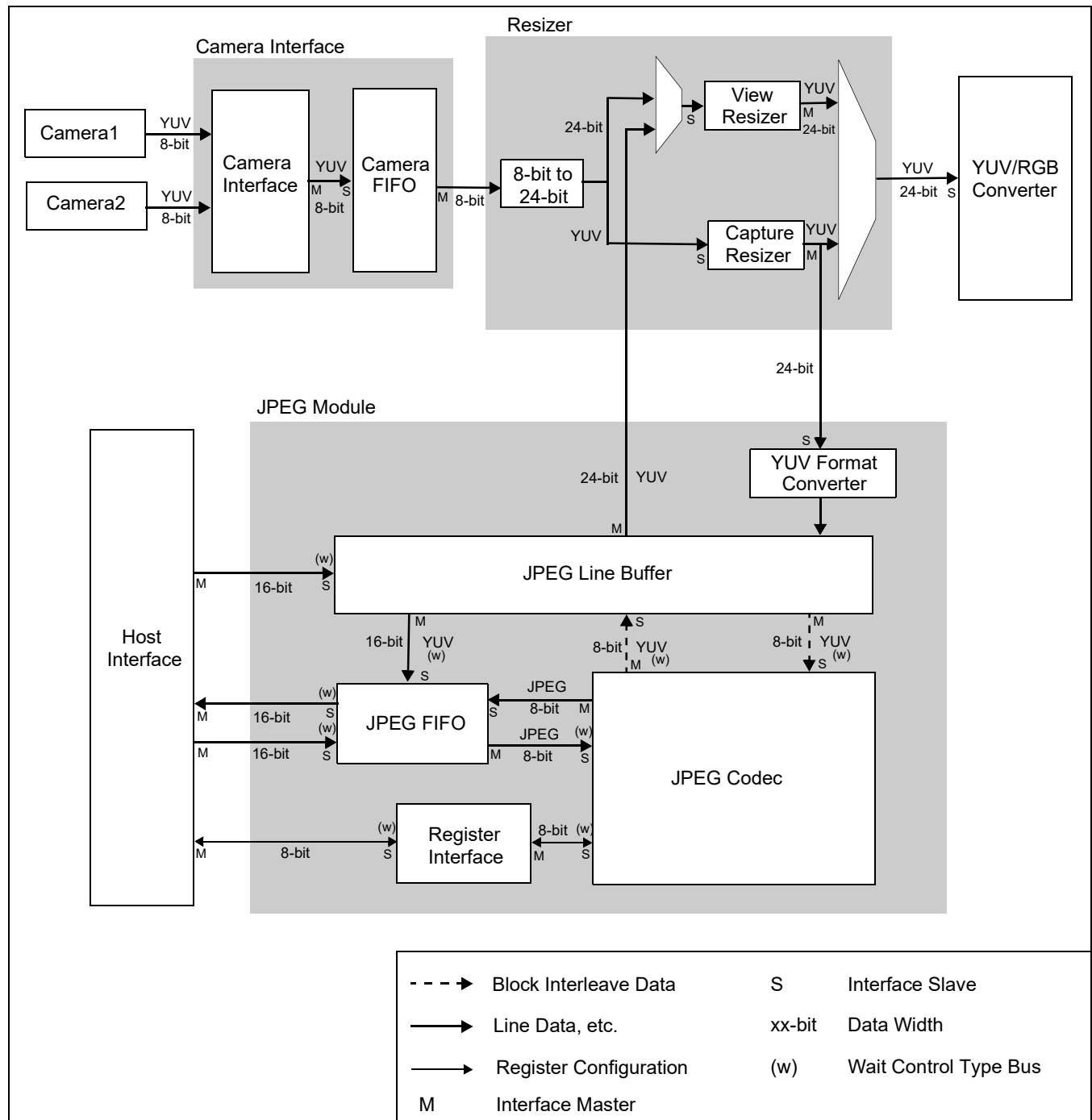


Figure 18-1: Digital Video Functions

18.1 Display Image Data from the Camera Interface

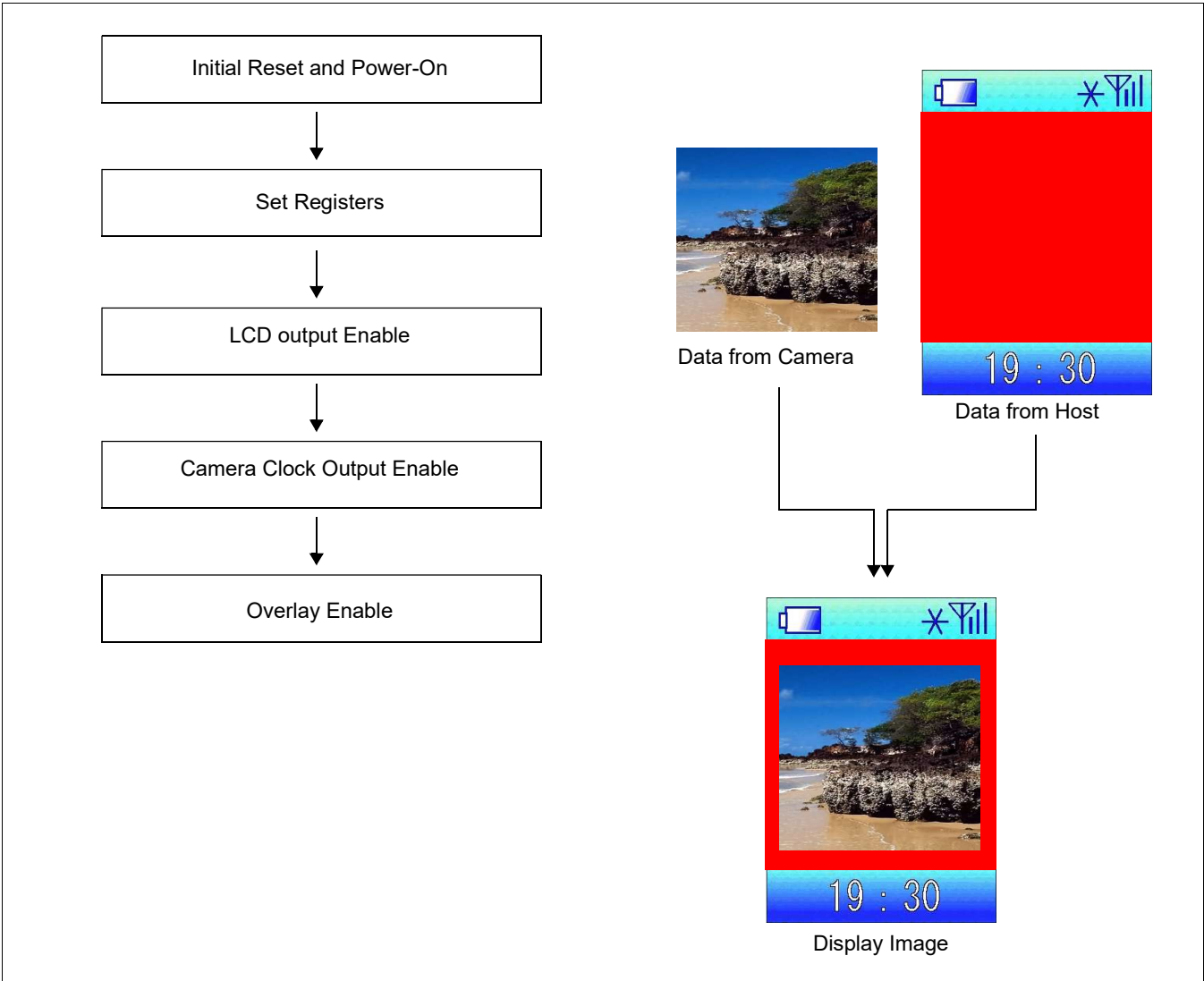


Figure 18-2: Display Image Data from the Camera Interface

## 18.2 JPEG Encode and Camera Data to the Host

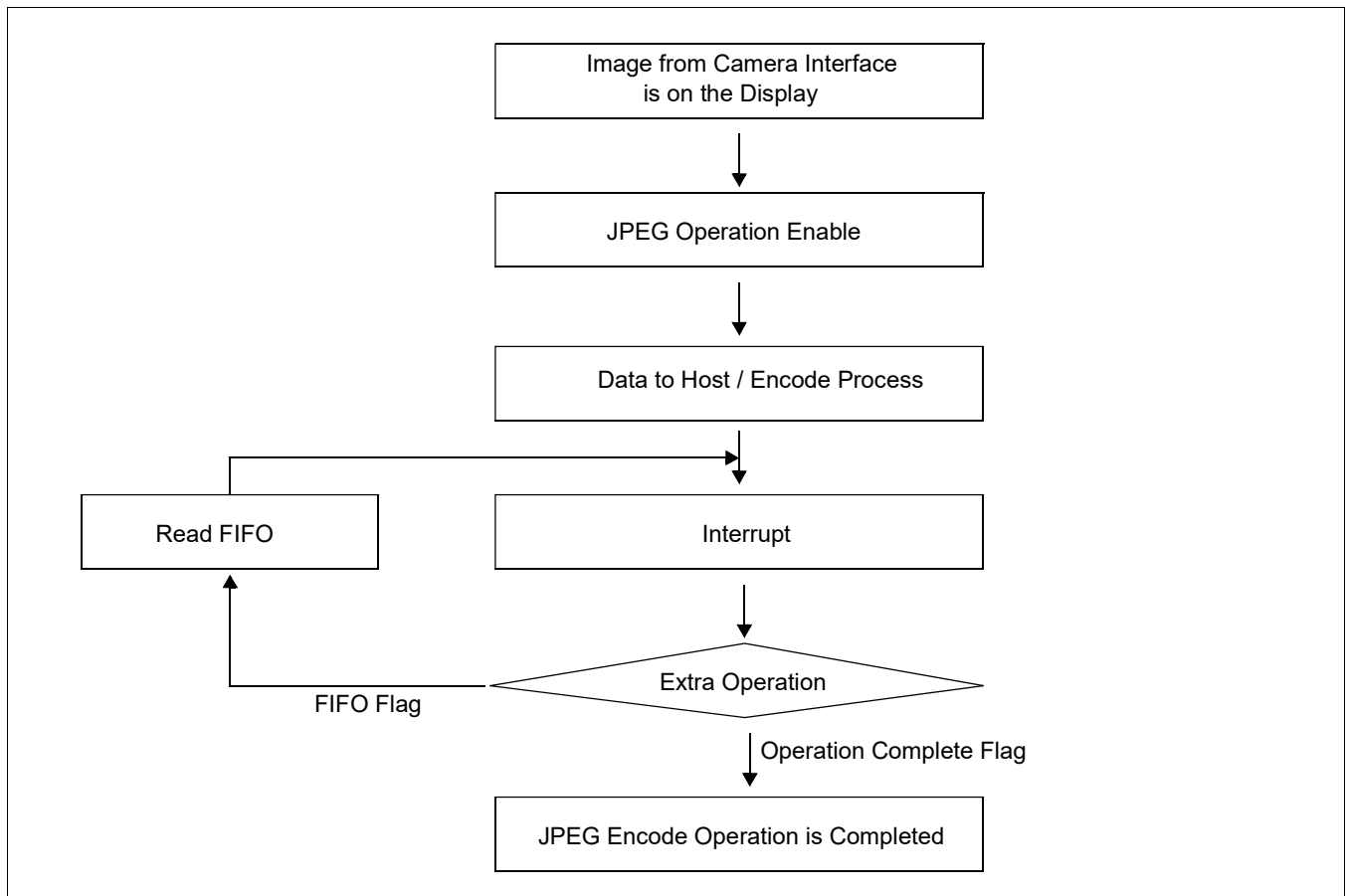


Figure 18-3: JPEG Encode Data from the Camera Interface

18.3 JPEG Decode and Display Data from the Host

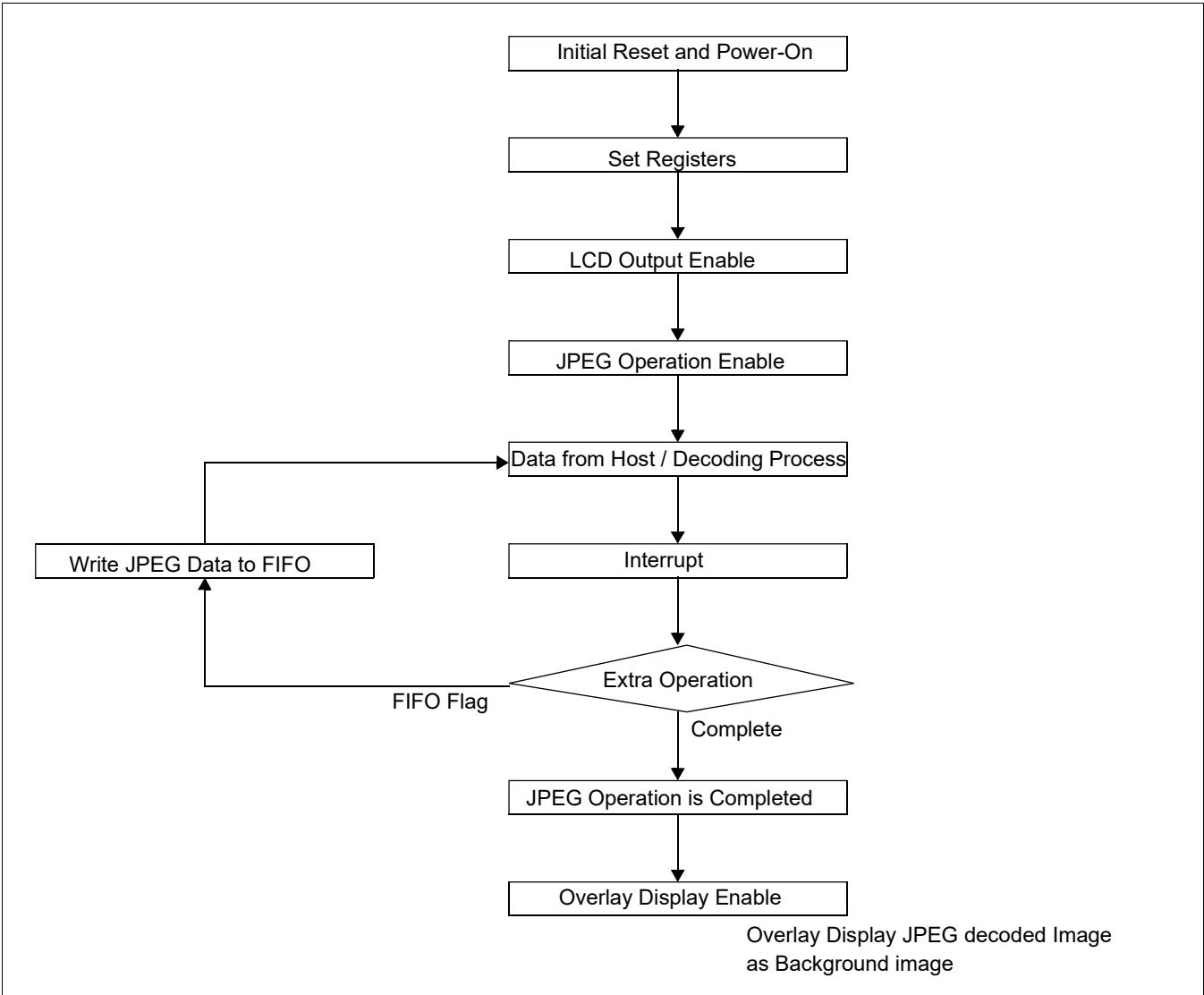


Figure 18-4: JPEG Decode and Display Data from the Host

## 18.4 JPEG 180° Rotate Encode Diagram

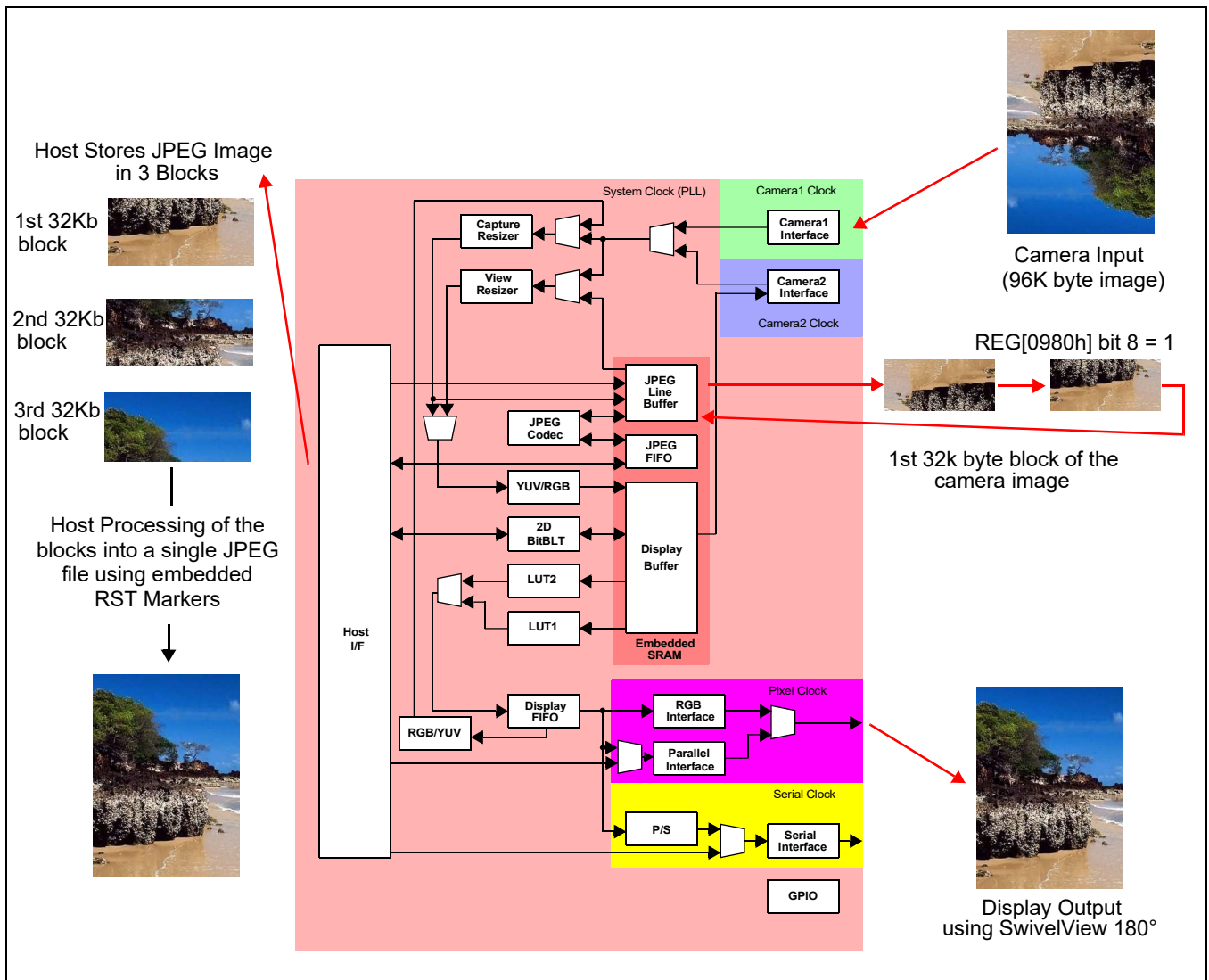


Figure 18-5: JPEG 180° Rotate Encode Diagram

## 19 JPEG Encode/Decode Operation

The S1D13715 JPEG Codec is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 1600 x 1200 and the image to be compressed/decompressed must be YUV format with a minimum resolution as shown in Table 19-1: “Minimum Resolution Restrictions”.

The following image restrictions must be observed for JPEG encode/decode, YUV data input from the Host (only YUV 4:2:2, 4:2:0), and YUV data to the Host (only YUV 4:2:2, 4:2:0). The image must be in YUV format and the minimum image resolution must be set based on the YUV format as follows.

*Table 19-1: Minimum Resolution Restrictions*

| YUV Format            | Minimum Resolution |
|-----------------------|--------------------|
| 4:4:4 (decode only)   | 1x1                |
| 4:2:2 (encode/decode) | 2x1                |
| 4:2:0 (encode/decode) | 2x2                |
| 4:1:1 (encode/decode) | 4x1                |

The quantization table accommodates two compression tables and four decompression tables. The Huffman table accommodates two tables for each AC and DC. It is possible to insert markers (up to a 36 byte maximum size) during the encoding process. Markers which can be processed and automatically translated during the decoding process are SOI, SOF0, SOS, DQT, DHT, DRI, RSTm and EOI. The decoding process supports YUV 4:4:4, YUV 4:2:2, YUV 4:1:1 and YUV 4:2:0, and the encoding process supports YUV 4:2:2, 4:1:1 and 4:2:0 format. RGB format is not supported. The image data processing ratio is almost less than 1/15 second at 640x480 resolution. However, the image data processing ratio is not guaranteed since it depends on the image data, the Huffman table and the quantization table.

## 19.1 JPEG Features

### 19.1.1 JPEG FIFO

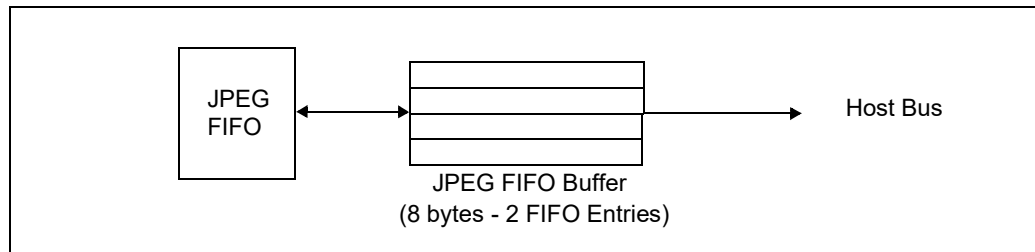


Figure 19-1: JPEG FIFO Overview

The JPEG FIFO is mapped at the beginning of the display buffer and is programmable to a maximum size of 128K bytes using REG[09A4h]. The JPEG file size and Host CPU performance should be considered when determining the JPEG FIFO size.

The status of the JPEG FIFO can be checked using the JPEG FIFO Status register (REG[09A2h]). It is also possible to indicate the JPEG FIFO status using interrupts via the JPEG Interrupt Control register (REG[0986h]).

The JPEG FIFO must be read by the Host CPU during the JPEG encode process. There are two methods.

1. High Performance - Before reading the JPEG FIFO, check how much data is available in the FIFO using the status bits in the JPEG FIFO Status register (REG[09A2h]). Next, read the FIFO through REG[09A6h] based on the available amount of data. Note that the FIFO must be read twice for each entry in the FIFO (32-bit FIFO but only 16-bit read/write port). Continue to check and read the FIFO until it is empty. This method offers the best performance because it is possible to transfer the block of data in the FIFO without a FIFO status check for each entry. If the JPEG FIFO is read while no data is in the FIFO, a terminate cycle will occur and no data will be read from the FIFO.
2. Low Performance - Before reading the JPEG FIFO, confirm that the FIFO is not empty using the JPEG FIFO Empty Status bit (REG[09A2h] bit 0) and JPEG FIFO Threshold Status bits (REG[09A2h] bits 3-2). After confirmation, read one entry from the FIFO. Note that the FIFO must be read twice for each entry in the FIFO (32-bit FIFO but only 16-bit read/write port).

The JPEG FIFO must be written by the Host CPU during the JPEG decode process. Much like the methods for reading the JPEG FIFO, writing to the JPEG FIFO can be done entry by entry or as a block of data once it has been determined how many entries are available in the JPEG FIFO. If the JPEG FIFO is full and data is written to it by the Host CPU, a terminate cycle will occur and no data will be read from the FIFO.

### 19.1.2 JPEG Codec Interrupts

The JPEG codec can generate the following interrupts to avoid continuously polling the JPEG status bits. Using interrupts decreases the CPU load for a JPEG process. For information on the JPEG Interrupt register bits, see the register descriptions in Section 10.4.15, “JPEG Module Registers” on page 249.

**1. JPEG Codec Interrupt Flag (REG[0982h] bit 1)**

This flag is asserted when all JPEG processes have finished without errors, or during the decode process when a RST marker process error is detected. This interrupt flag should be enabled when RST marker error detection is enabled.

However, if the RST marker is not required during the decode process, confirm that the operation has finished using the JPEG Decode Complete Flag (REG[0982h] bit 5). For the encoding process, confirm that the operation has finished using the JPEG FIFO Empty Flag (REG[0982h] bit 8) and the JPEG Operation Status bit (REG[1004h] bit 0).

**2. JPEG Line Buffer Overflow Flag (REG[0982h] bit 2)**

If the JPEG FIFO is read slower than the JPEG Line Buffer is written to during the encoding process, this flag is asserted when the JPEG Line Buffer overflows. This flag should be enabled for JPEG encoding.

**3. JPEG Decode Marker Read Flag (REG[0982h] bit 4)**

During JPEG decoding, this flag is asserted when marker information is read from the JPEG file. Marker information may include resize settings or LCD settings. JPEG decoding is stopping while this flag is asserted and does not restart until after this flag is cleared (REG[0986h] bit 4 = 0).

**4. JPEG Decode Complete Flag (REG[0982h] bit 5)**

This flag is asserted after the JPEG decode process is finished and the decompressed image data is stored in memory. This flag is useful as a trigger for enabling the overlay or display of the image.

**5. JPEG FIFO Empty Flag (REG[0982h] bit 8)**

This flag is asserted when the JPEG FIFO is empty. For the decode process, this flag is useful for timing JPEG data writes to the FIFO and to identify when the JPEG decode process is finished completely. For the encode process, this flag indicates that the entire JPEG file has been read by the host.

**6. JPEG FIFO Full Flag (REG[0982h] bit 9)**

This flag is asserted when the JPEG FIFO is full. For the encode process, this flag is used as a trigger for increasing the priority of host reads to the FIFO. For the decode process, this flag indicates if it is possible to write data to the FIFO.

**7. JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10)**

This flag is asserted when the amount of data in the JPEG FIFO meets the condition programmed into the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is useful for timing when the host will start to read JPEG compressed data in the FIFO.

8. **Encode Size Limit Violation Flag (REG[0982h] bit 11)**

This flag is asserted when the compressed JPEG data size is greater than the programmed size in the JPEG Encode Size Limit registers (see REG[09B0h] - REG[09B2h]).

19.1.3 **JPEG Bypass Modes**

The S1D13715 can bypass the JPEG Codec in order for the Host CPU to capture raw YUV data from the camera interface (YUV Data Capture Mode). The S1D13715 can also bypass the JPEG Codec in order for the Host CPU to send raw YUV data to be displayed (YUV Data Display Mode). For YUV Data Capture Mode, YUV data is still sent to the Host CPU through the JPEG FIFO which is accessed through REG[09A6h]. For YUV Data Display Mode, the JPEG FIFO is bypassed and the Host CPU writes YUV data directly to the JPEG Line Buffer using the JPEG Line Buffer Write Port (REG[09E0h]).

The raw YUV data can be in either of the two YUV format as follows (YUV 4:2:2 = 2x1, YUV 4:2:0 = 2x2).

|            | YUV 4:2:2 | YUV 4:2:0 |
|------------|-----------|-----------|
| Nth line   | UYVYUYVY  | UYVYUYVY  |
| N+1th line | UYVYUYVY  | YYYYYYYY  |

19.2 Example Sequences

19.2.1 JPEG Encoding Process

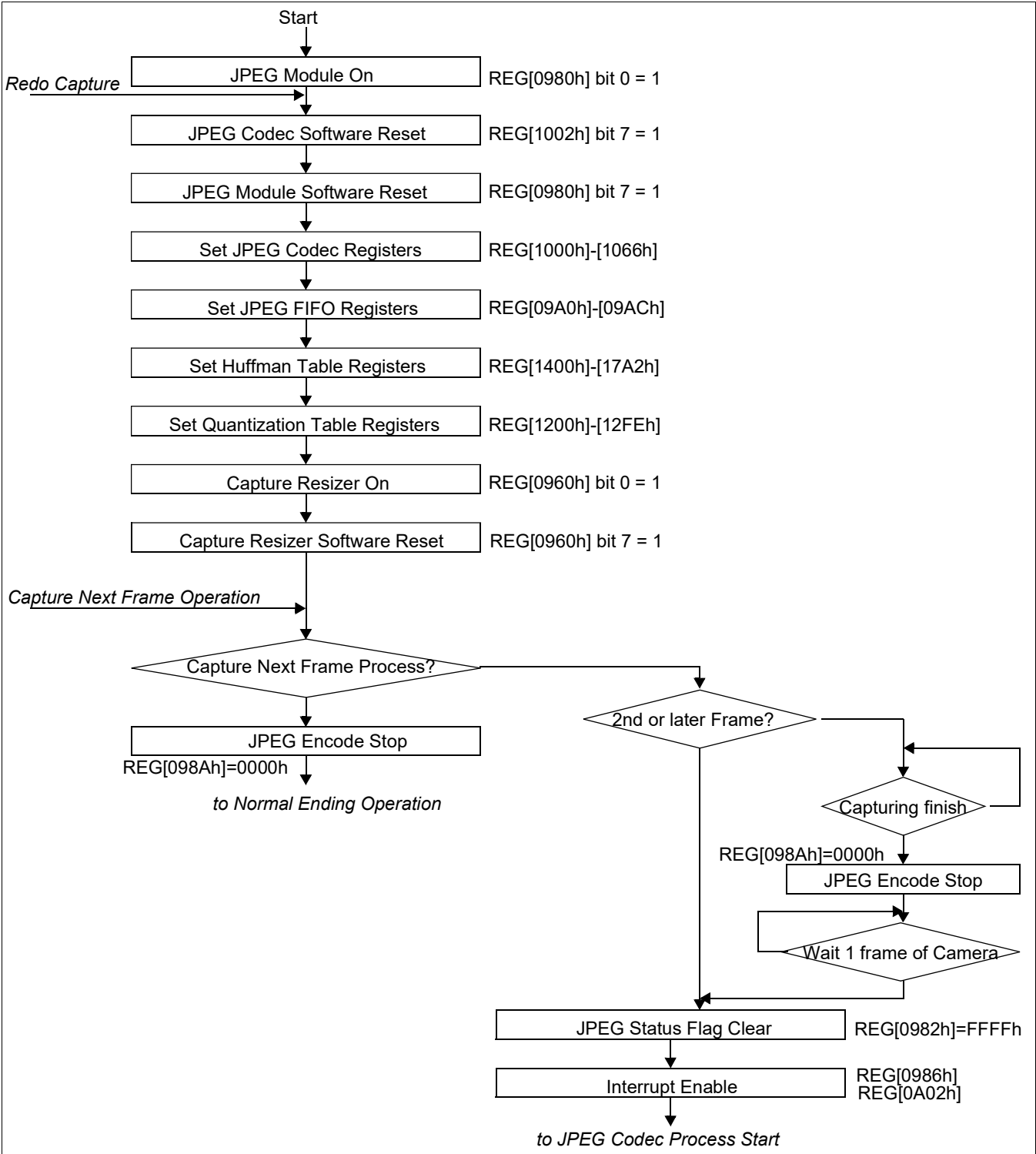


Figure 19-2: JPEG Encoding Process (1 of 4)

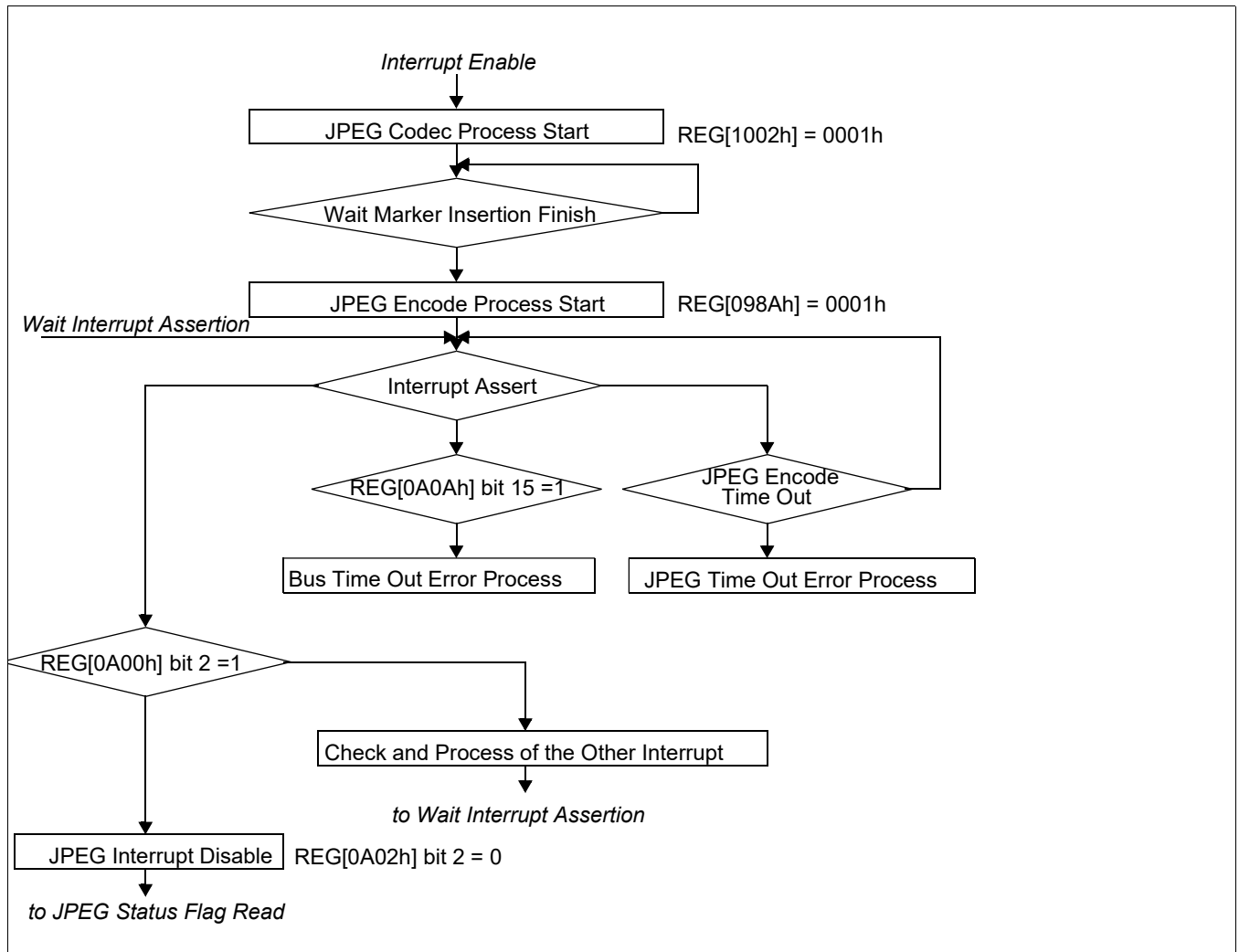


Figure 19-3: JPEG Encoding Process (2 of 4)

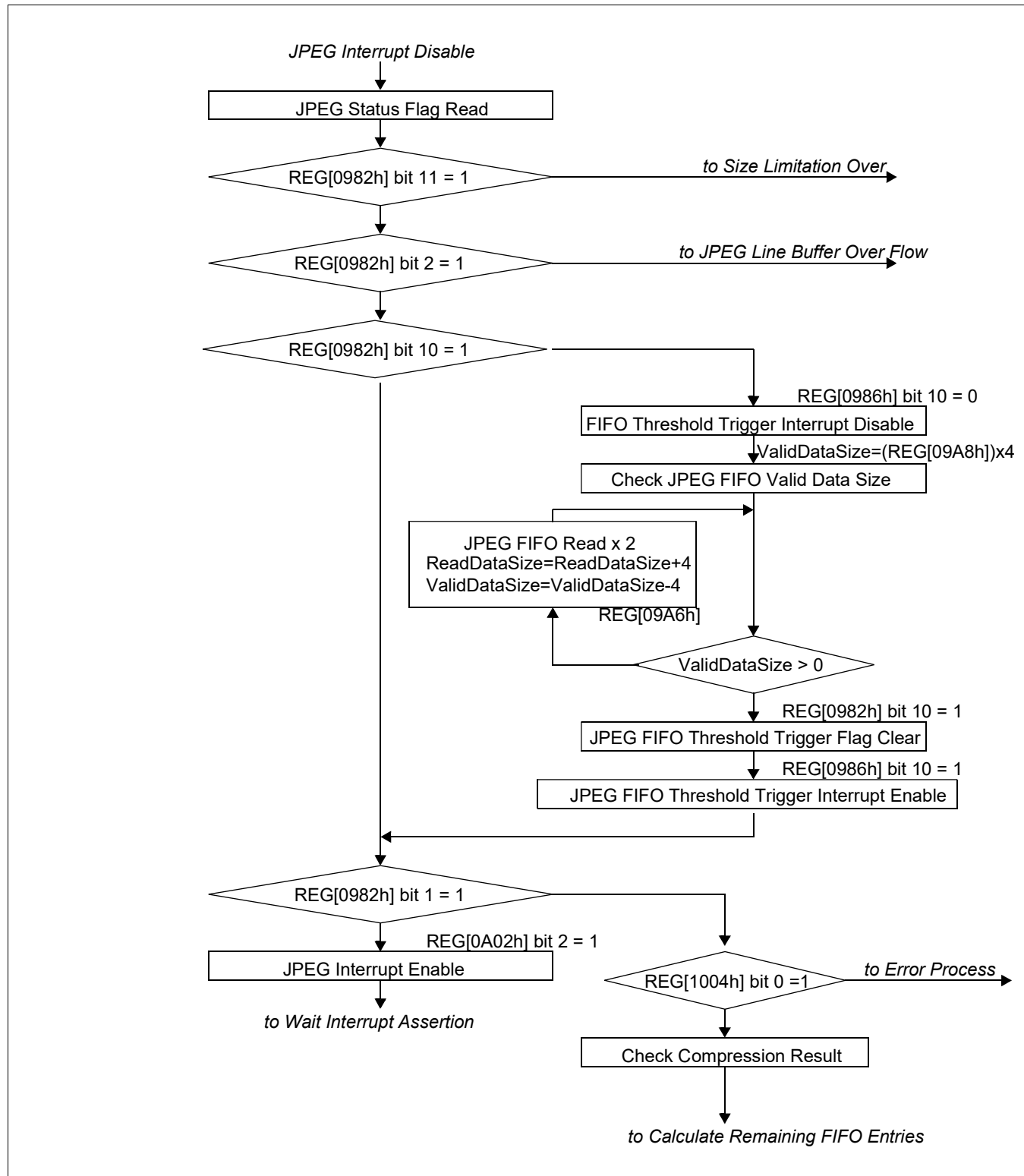
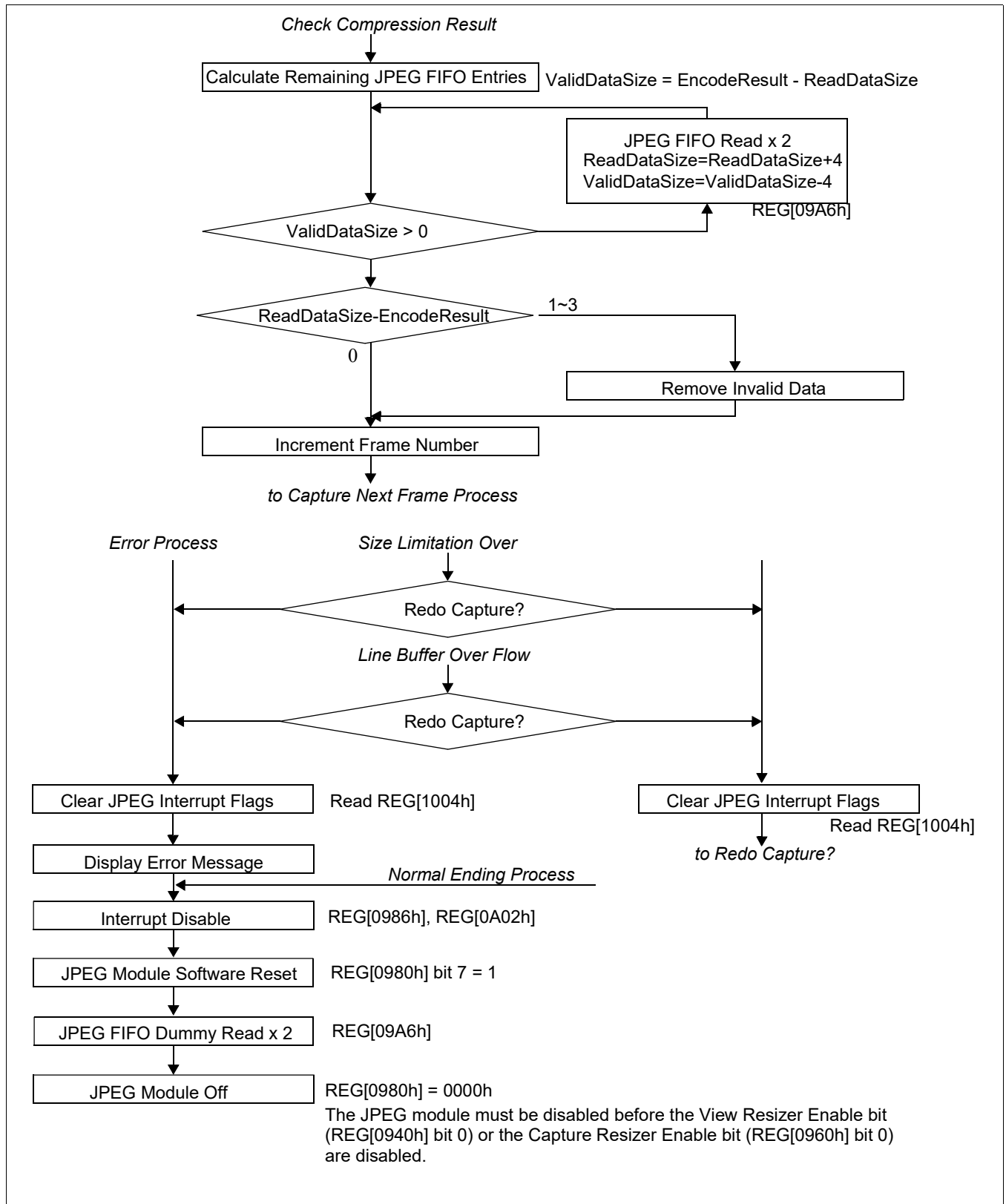


Figure 19-4: JPEG Encoding Process (3 of 4)



1. Initialize the camera interface registers (REG[0100h]-[0124h]).
2. Enable the JPEG module, set REG[0980h] bits 3-0 = 0001.
3. Initialize the JPEG Codec registers.
  - a. Software reset the JPEG codec, set REG[1002h] bit 7 = 1.
  - b. Select the operation mode for encoding, set REG[1000h] bit 2 = 0.
  - c. Set the desired quantization table number (REG[1006h]) and the huffman table number (REG[1008h]).
  - d. Select the DRI setting (REG[100Ah]-[100Ch]).
  - e. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]).
  - f. Set the Insertion Marker Data in REG[1020h]-[1066h]. When REG[1000h] bit 3 = 1, the data in these registers is written to the JPEG file. Unused bits must be written as FFh.
  - g. Initialize Quantization Table No. 0 (REG[1200h]-[127Eh]) and Quantization Table No. 1 (REG[1280h]-[12FEh]) with the following sequence.

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  |
| 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 |
| 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 |
| 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 |

- h. Set DC Huffman Tables and the AC Huffman Tables according to ISO/IEC 10918 attachment K, each numerical formula is specified as follows:

DC Huffman Table No. 0 Register 0 (REG[1400h-141Eh]) is set as A  
 DC Huffman Table No. 0 Register 1 (REG[1420h-1436h]) is set as B  
 AC Huffman Table No. 0 Register 0 (REG[1440h-145Eh]) is set as C  
 AC Huffman Table No. 0 Register 1 (REG[1460h-15A2h]) is set as D  
 DC Huffman Table No. 1 Register 0 (REG[1600h-161Eh]) is set as E  
 DC Huffman Table No. 1 Register 1 (REG[1620h-1636h]) is set as F  
 AC Huffman Table No. 1 Register 0 (REG[1640h-165Eh]) is set as G  
 AC Huffman Table No. 1 Register 1 (REG[1660h-17A2h]) is set as H

|    |                                   |          |
|----|-----------------------------------|----------|
| A: | 00h, 01h, 05h, ....., 00h, 00h    | 16 byte  |
| B: | 00h, 01h, 02h, ....., 0Ah, 0Bh    | 12 byte  |
| C: | 00h, 02h, 01h, 03h, .....01h, 7Dh | 16 byte  |
| D: | 01h, 02h, 03h, ....., F9h, FAh    | 162 byte |
| E: | 00h, 03h, 01h, ....., 00h, 00h    | 16 byte  |
| F: | 00h, 01h, 02h, ....., 0Ah, 0Bh    | 12 byte  |
| G: | 00h, 02h, 01h, 02h, ..., 02h, 77h | 16 byte  |
| H: | 00h, 01h, 02h, ....., F9h, FAh    | 162 byte |

4. Set the JPEG module registers.
- Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
  - Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:  
  

$$\text{JPEG FIFO size} = ((\text{REG}[09A4h] \text{ bits } 3-0) + 1) \times 4\text{K bytes.}$$

Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2  

$$(2 + 1) \times 4\text{KB} = 12\text{K bytes}$$
  - Set the Encode Size Limit (REG[09B0h]-[09B2h]) in bytes. To generate an interrupt when the encode size limit is exceeded use the Encode Size Limit Violation Flag (REG[0982h] bit 11).
  - Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).
  - Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).
5. Set the capture resizer registers. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 3e.

6. Start the encode process.
  - a. Clear all status bits by writing REG[0982h] as FFFFh
  - b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0E07h.
  - c. Start the JPEG operation (REG[1002h] bit 0 = 1)
  - d. Start capturing (REG[098Ah] bit 0 = 1)

After setting REG[1002h] bit 0 = 1, 2ms (internal system clock = 50Mhz) is required to generate the Markers. If REG[098Ah] bit 0 is set to 1 before 2ms, capturing will start only after generating the Markers (after 2 ms has passed).

### Host CPU Process

7. Wait for the JPEG FIFO Threshold condition to be met. This can be done using the JPEG FIFO Threshold Interrupt (see REG[0986h]) or by polling the JPEG FIFO Threshold Status bits (REG[0982h] bits 13-12). If the interrupt method is used, the interrupt should be disabled after it is asserted.
8. Confirm the FIFO Valid Data Size (REG[09A8h]).
9. Read the JPEG FIFO Read/Write register twice (REG[09A6h]). Two reads from the 16-bit FIFO read/write register are required to get the entire 32-bit FIFO entry.
10. If using the interrupt method, the interrupt should be re-enabled again.
11. Loop steps 7 through 9 continuously until the FIFO Valid Data Size reaches 0 (REG[09A8h] = 0) and the JPEG Operation Status is idle (REG[1004h] bit 0 = 0).
12. When the encode process finishes, check the actual file size with the Encode Size Result registers (REG[09B4h]-[09B6h]).
13. Confirm the process is complete with the JPEG Codec Interrupt Flag (REG[0982h] bit 1).
14. Stop the JPEG codec using the JPEG Start/Stop Control bit (REG[098Ah] bit 0 = 0).

### 19.2.2 Memory Image JPEG Encoding Process

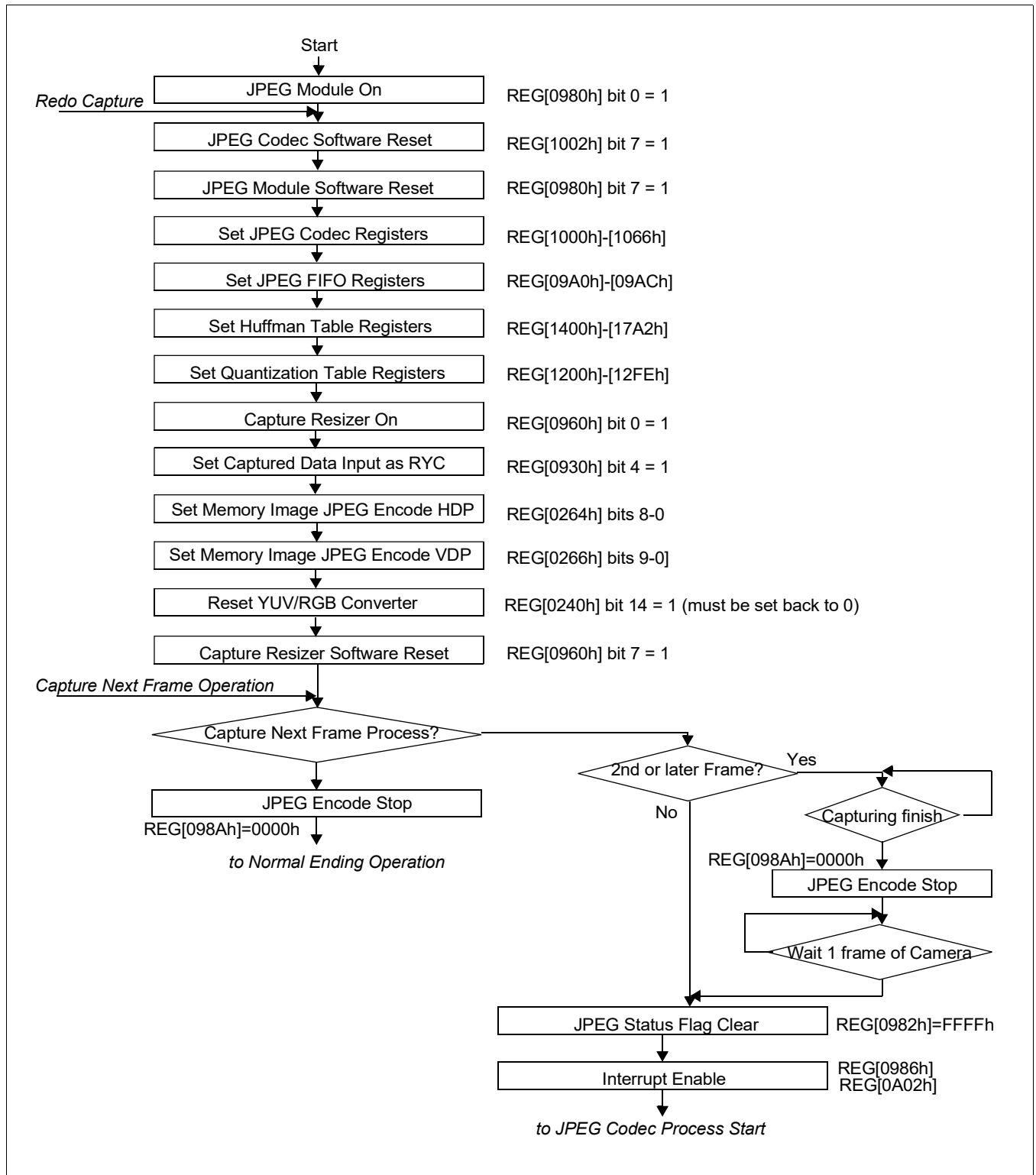


Figure 19-6: Memory Image JPEG Encoding Process (1 of 4)

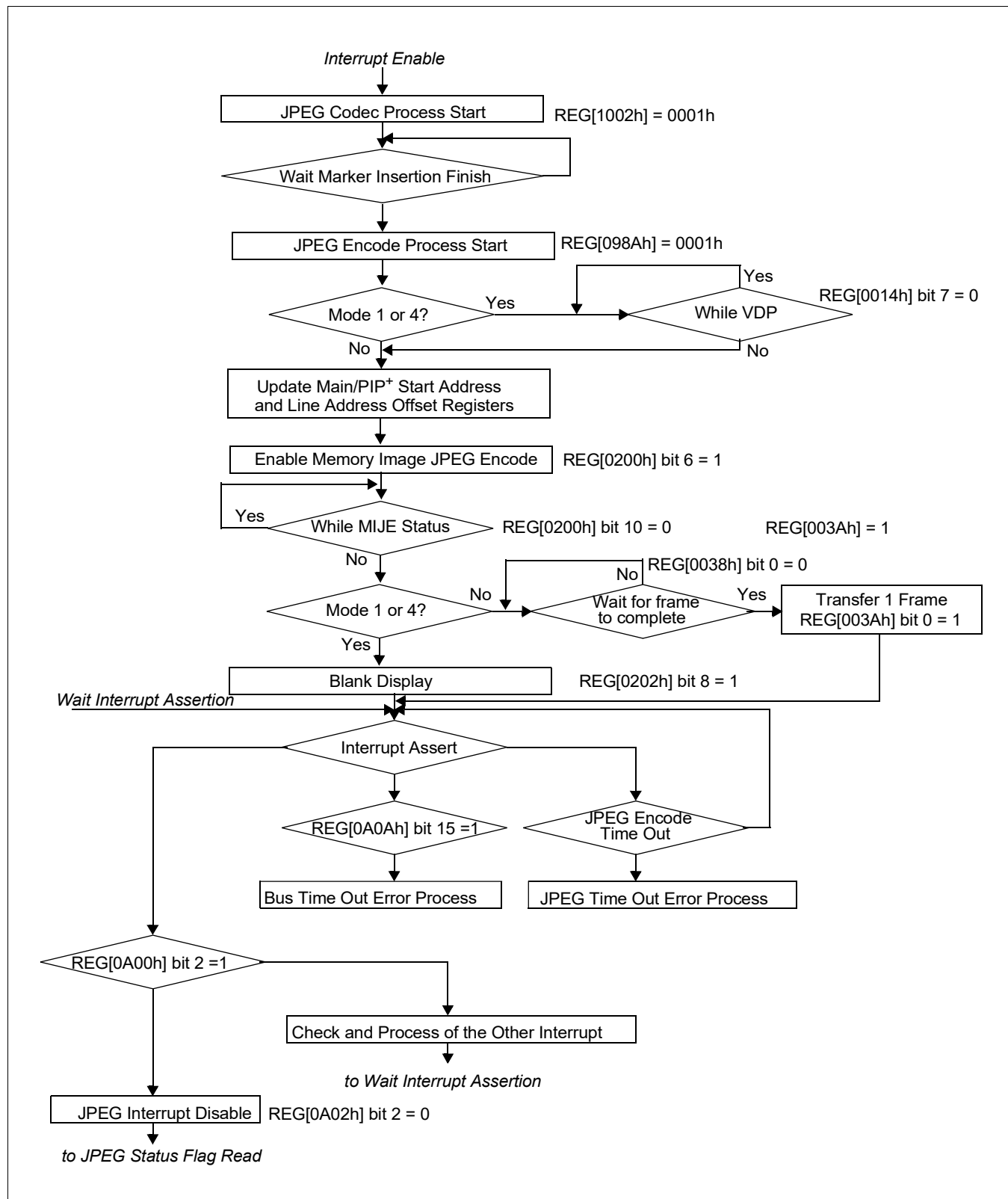
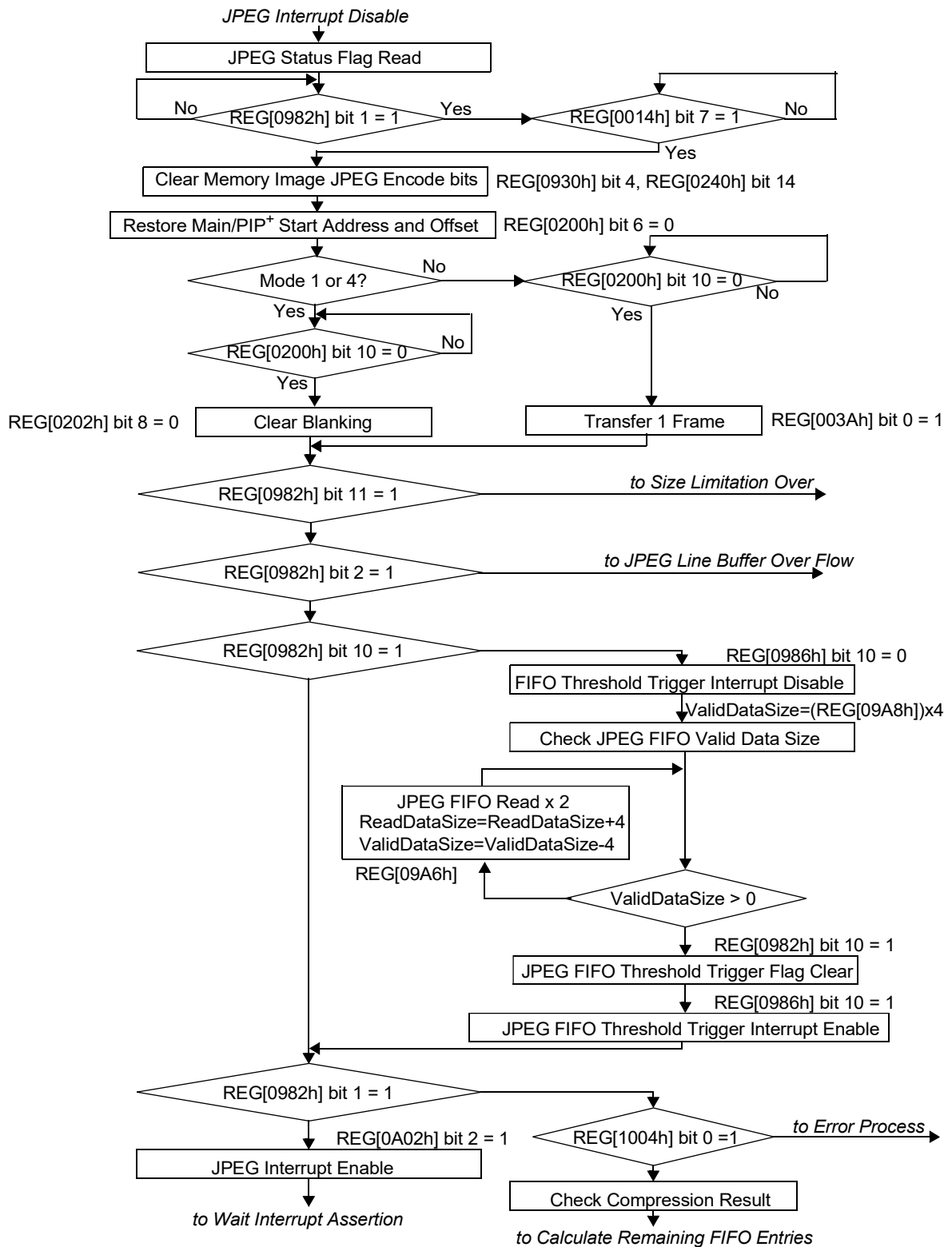


Figure 19-7: Memory Image JPEG Encoding Process (2 of 4)



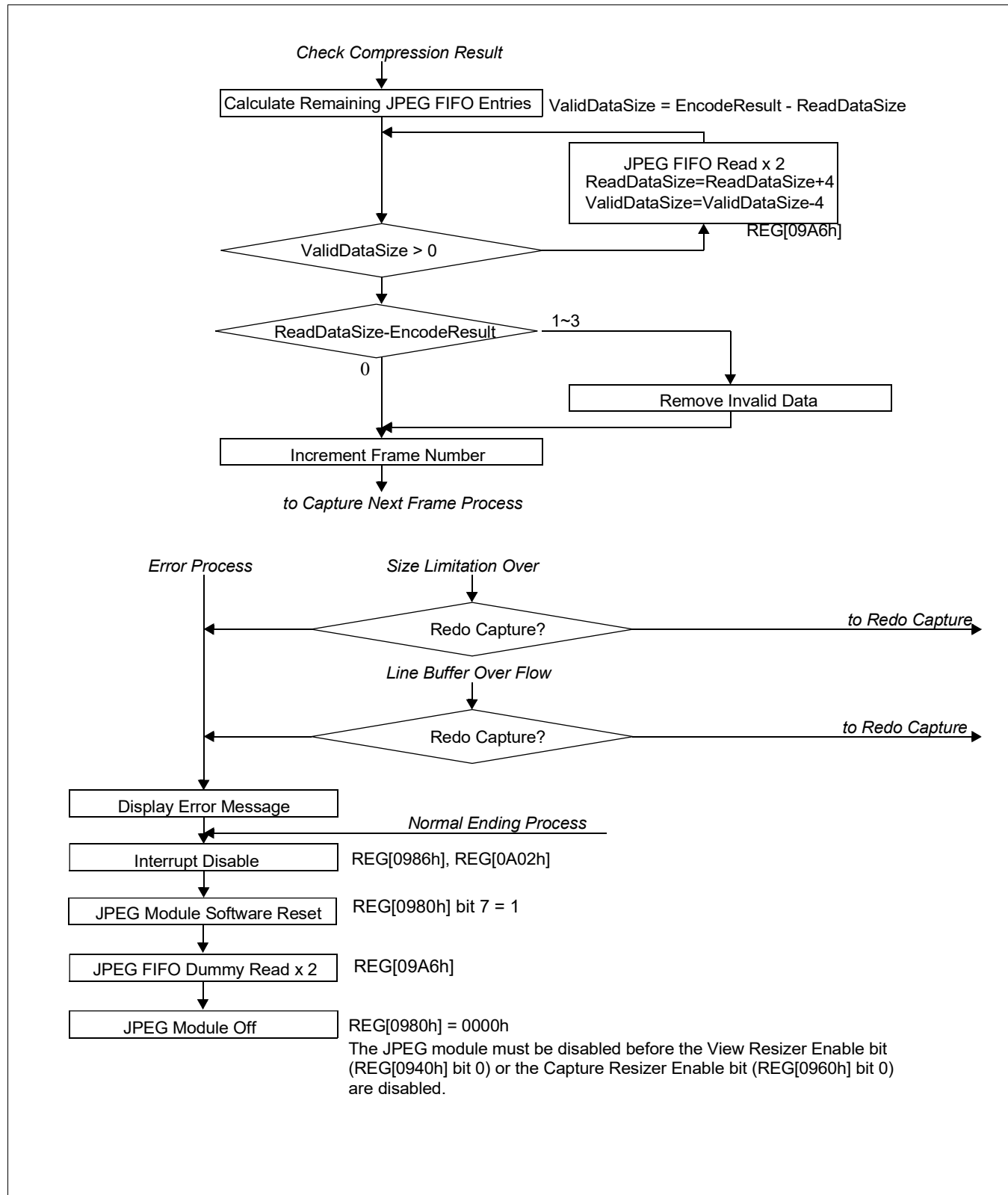


Figure 19-9: Memory Image JPEG Encoding Process (4 of 4)

### 19.2.3 Memory Image JPEG Encoding Process from Host I/F (RGB format)

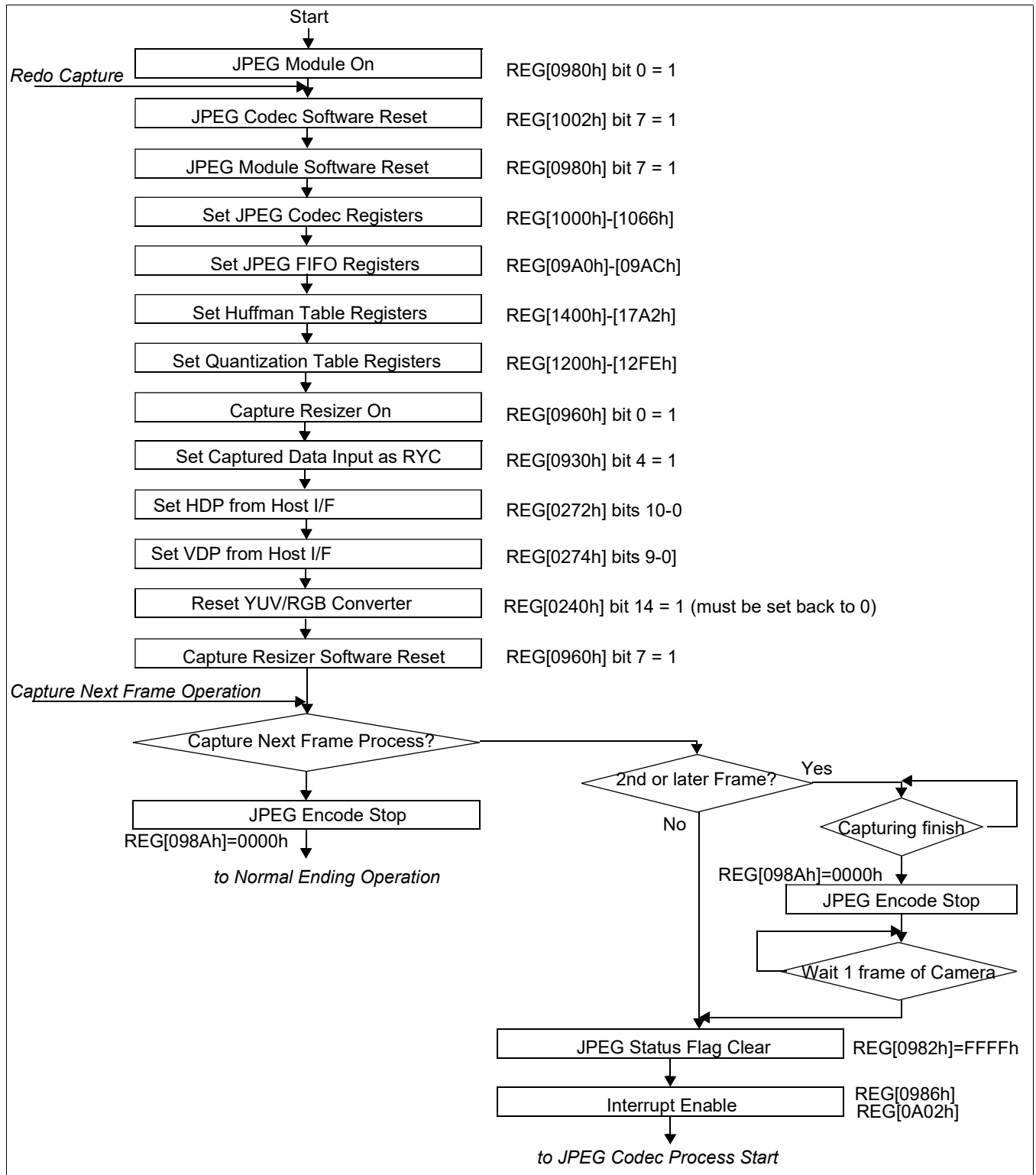


Figure 19-10: Memory Image JPEG Encoding Process from Host I/F (RGB format) (1 of 4)

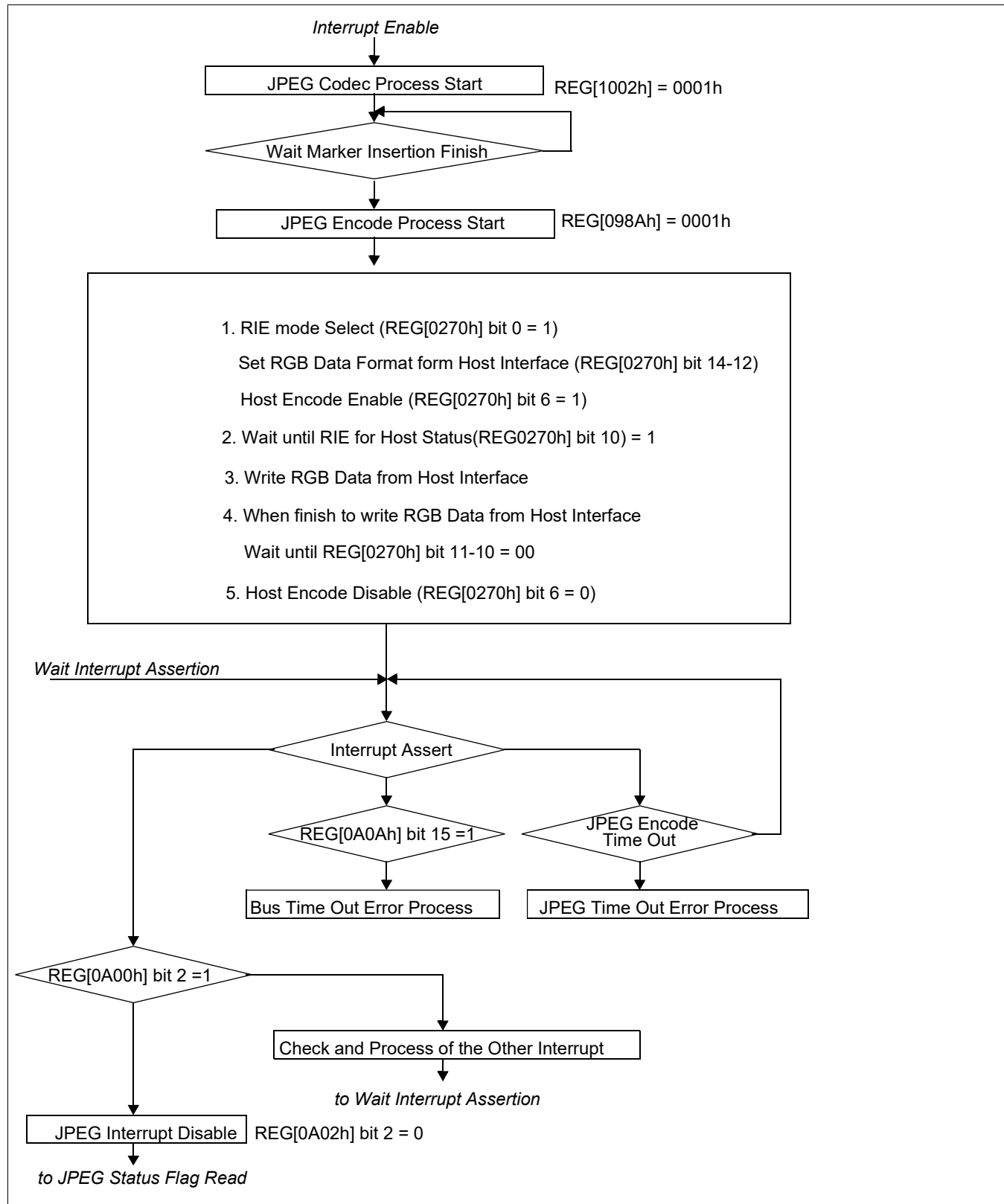


Figure 19-11: Memory Image JPEG Encoding Process from Host I/F (RGB format) (2 of 4)

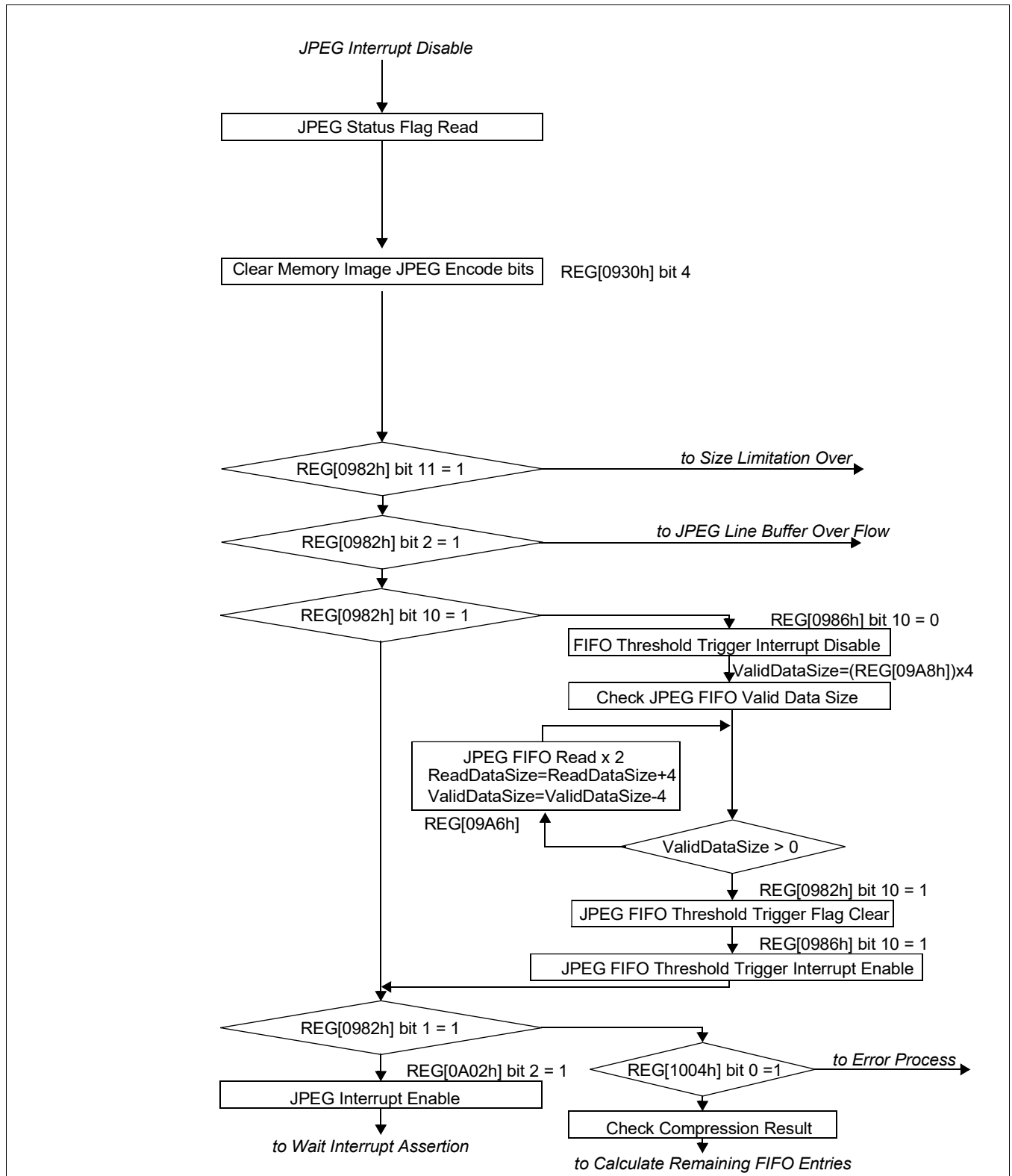


Figure 19-12: Memory Image JPEG Encoding Process from Host I/F (RGB format) (3 of 4)

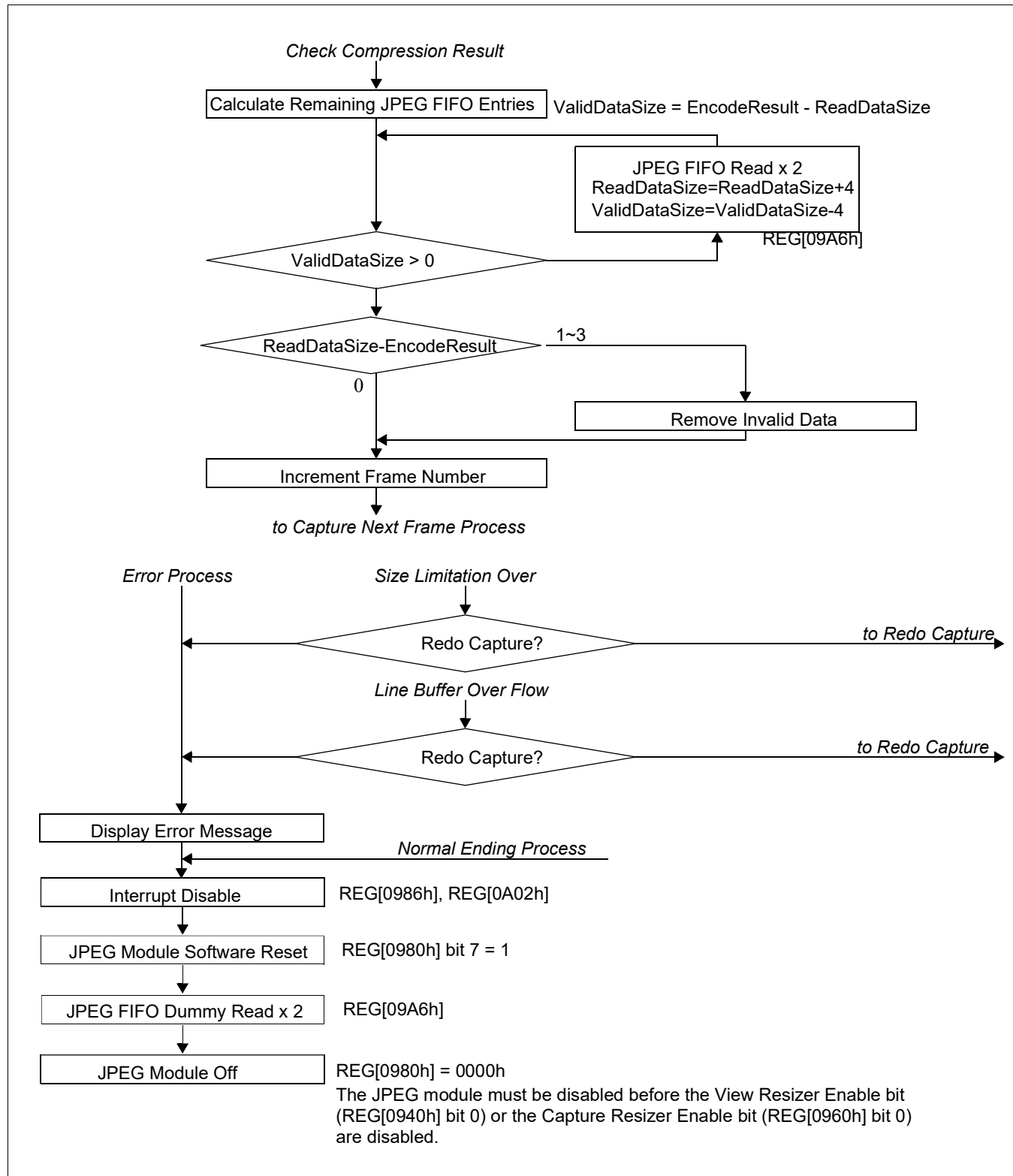


Figure 19-13: Memory Image JPEG Encoding Process from Host I/F (RGB format) (4 of 4)

## 19.2.4 JPEG Decoding Process

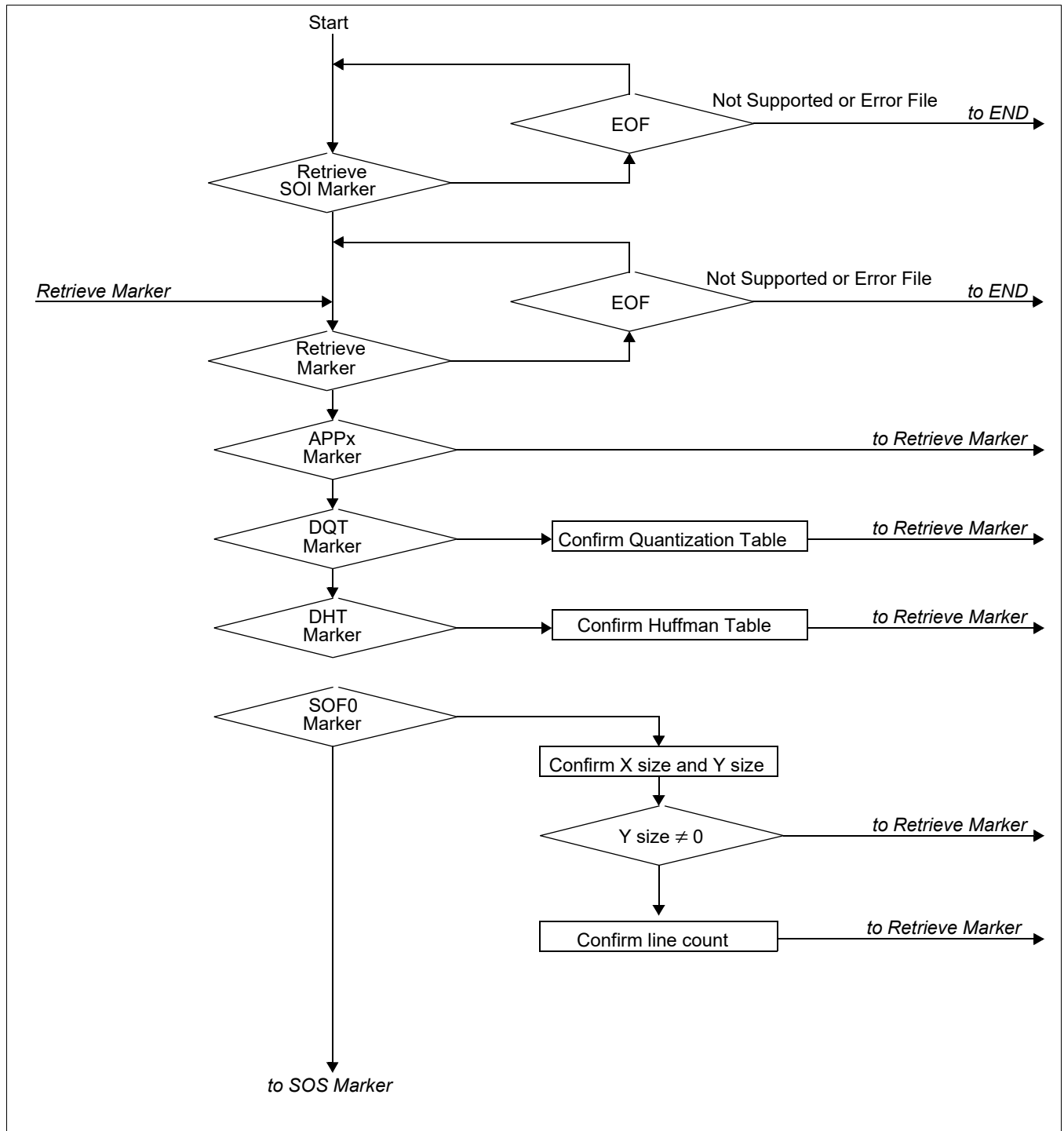


Figure 19-14: JPEG Decoding Process (1 of 6)

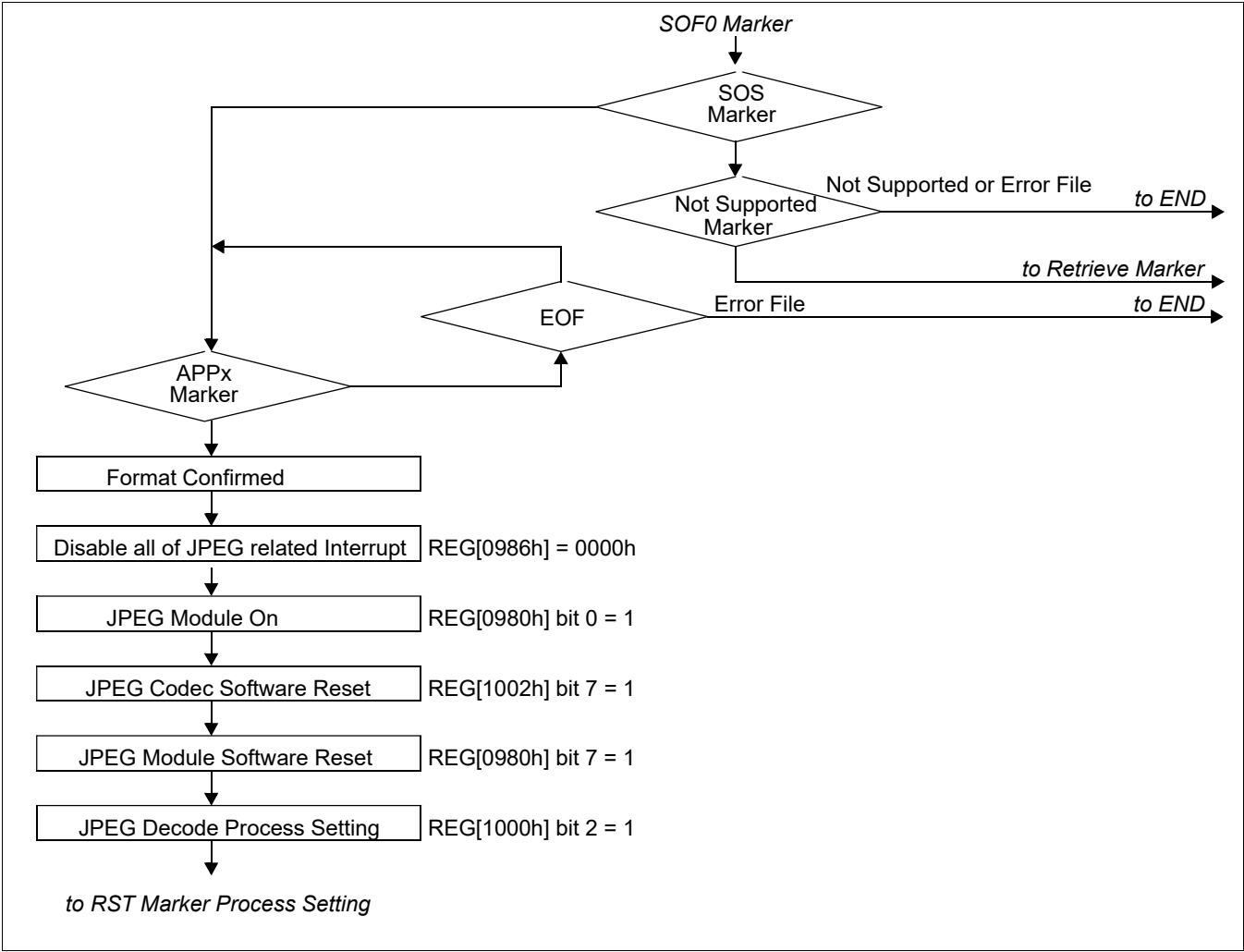


Figure 19-15: JPEG Decoding Process (2 of 6)

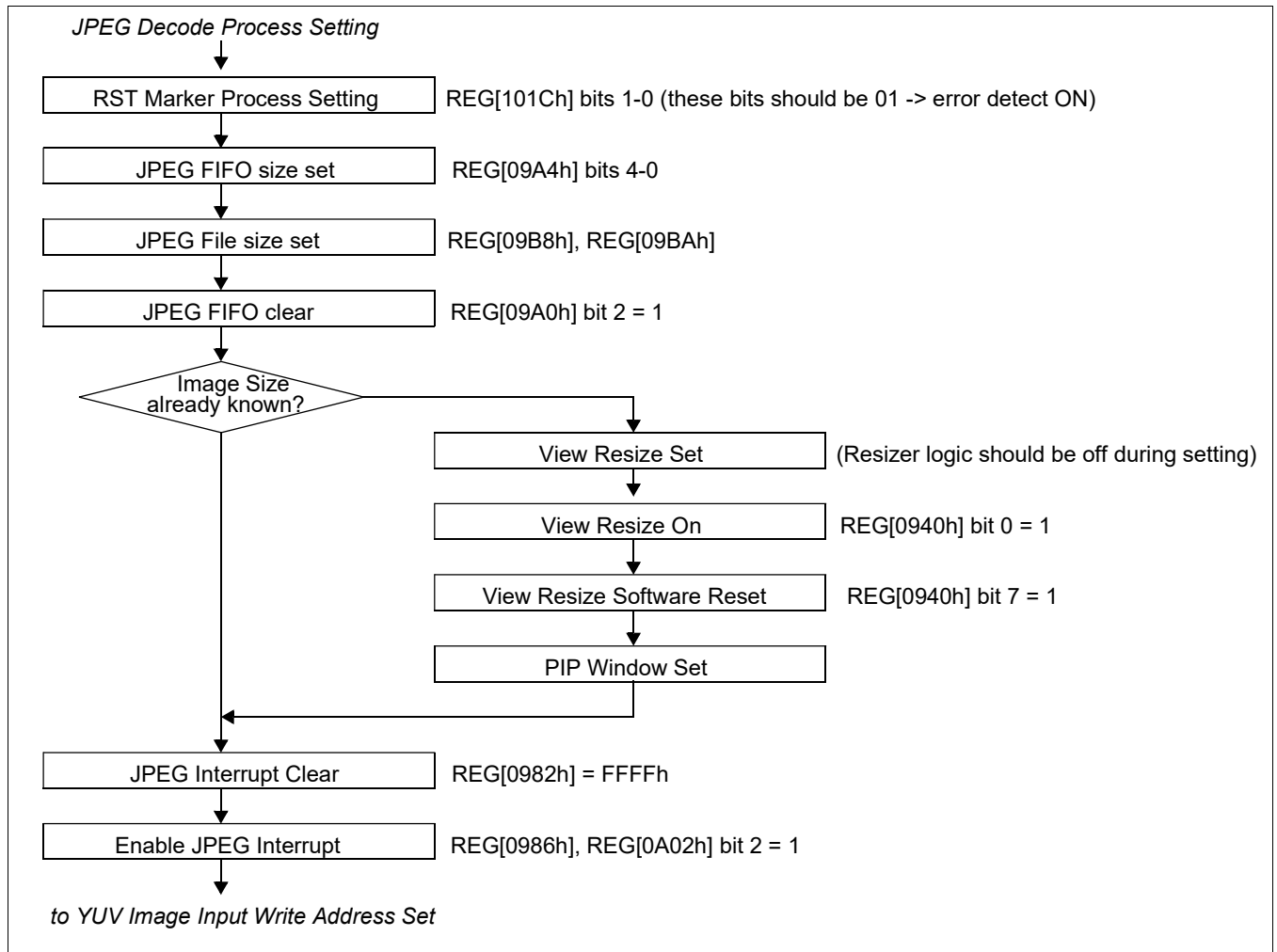


Figure 19-16: JPEG Decoding Process (3 of 6)

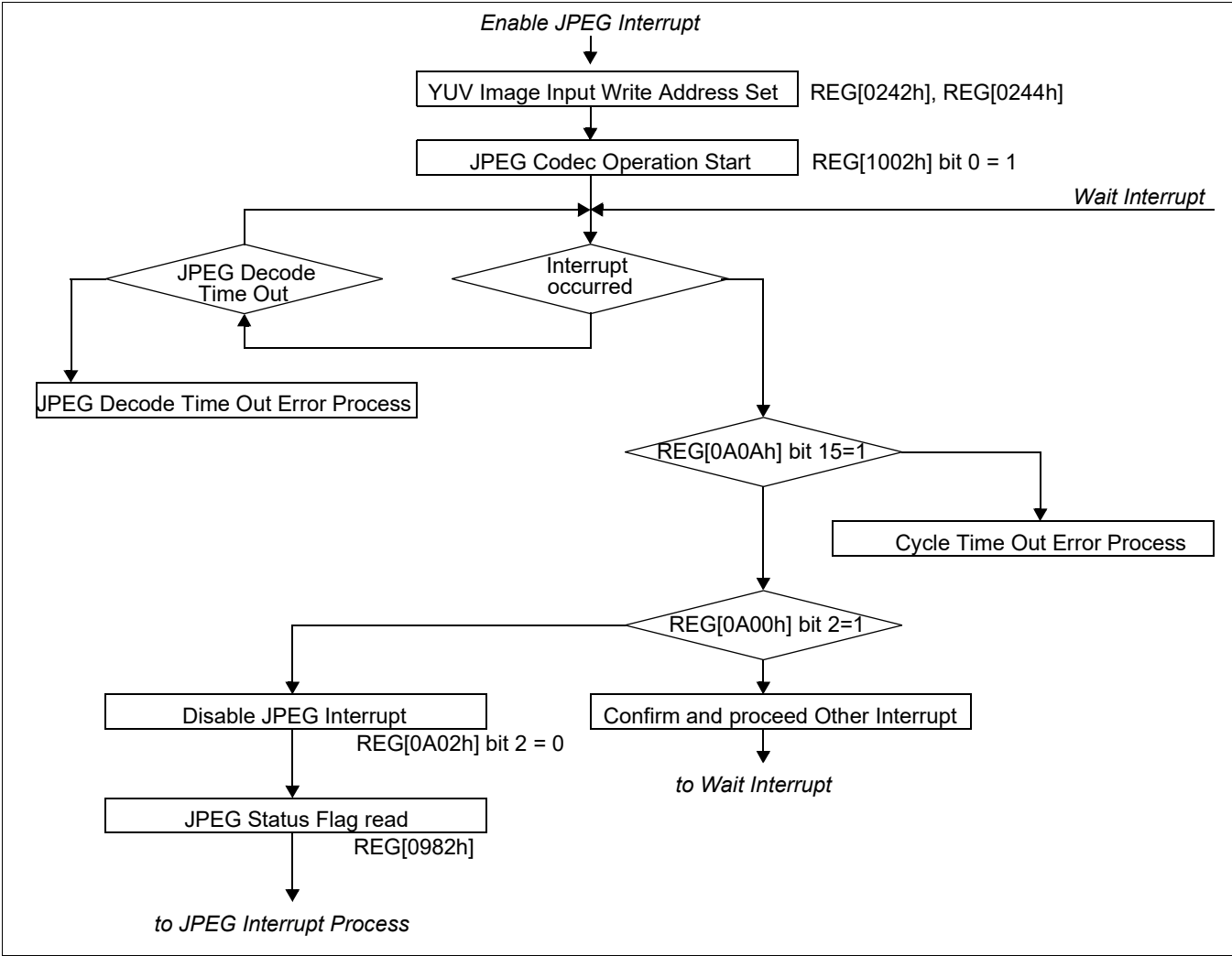


Figure 19-17: JPEG Decoding Process (4 of 6)

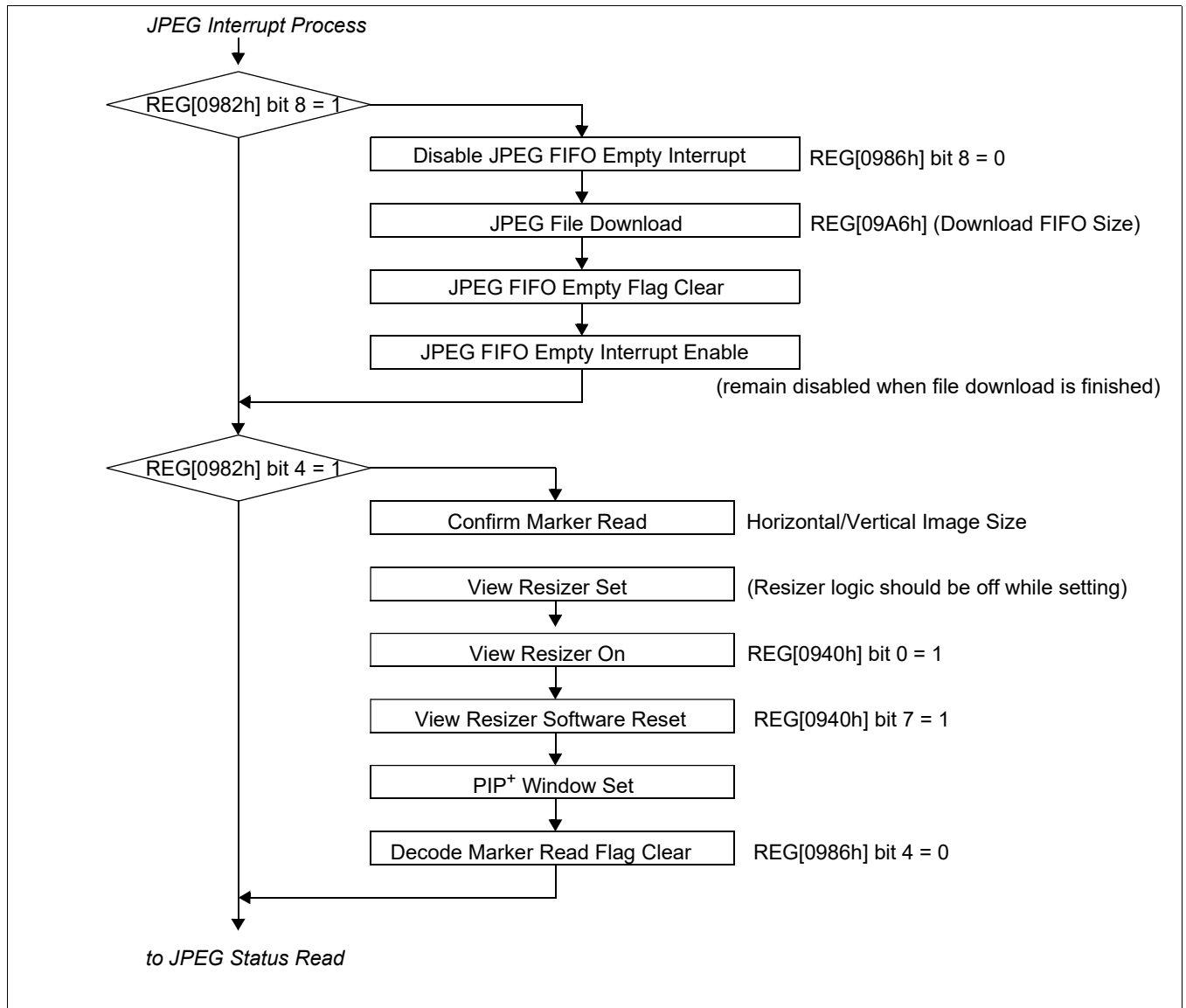


Figure 19-18: JPEG Decoding Process (5 of 6)

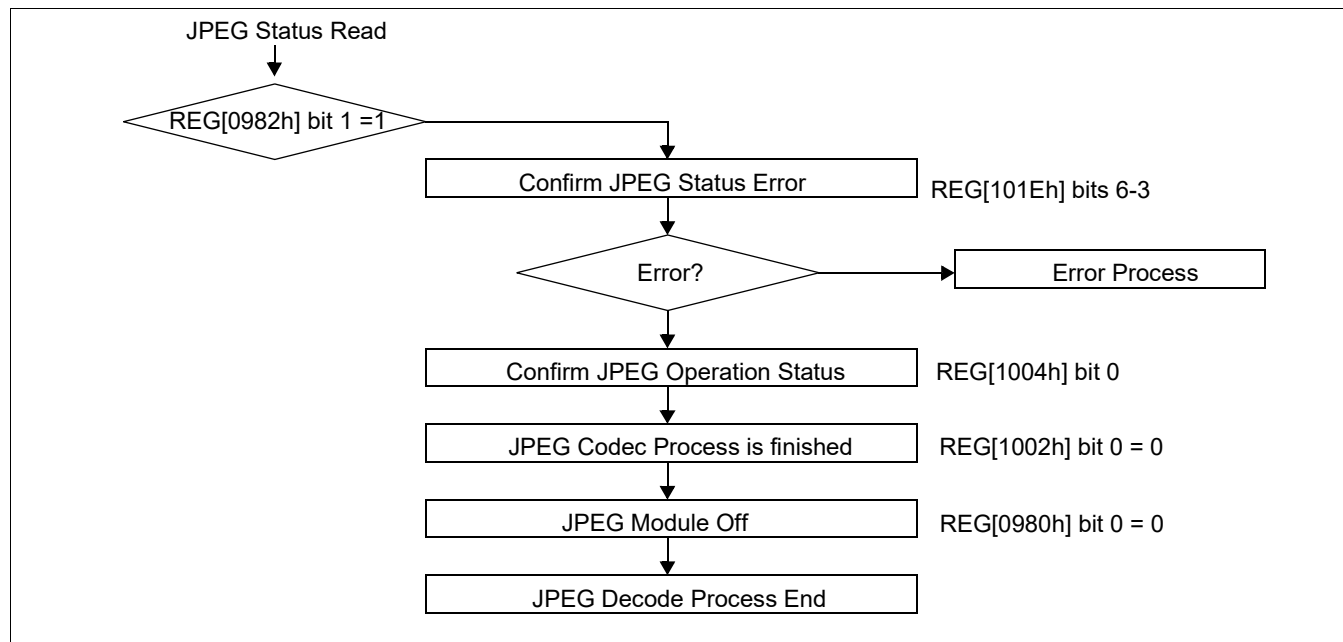


Figure 19-19: JPEG Decoding Process (6 of 6)

1. Enable the JPEG codec, set REG[0980h] bits 3-0 to 0001.
2. Initialize the JPEG Codec registers.
  - a. Software reset the JPEG codec, set REG[1002h] bit 7 to 1.
  - b. Select the operation mode for JPEG decoding, set REG[1000h] bit 2 = 1b.
  - c. Set the RST Marker Operation Setting, set REG[101Ah].
3. Set the JPEG module registers.
  - a. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
  - b. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:  

$$\text{JPEG FIFO size} = ((\text{REG}[09A4h] \text{ bits } 3-0) + 1) \times 4\text{K bytes}.$$

Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2  
 $(2 + 1) \times 4\text{KB} = 12\text{K bytes}$
  - c. specify the JPEG file size, set REG[09B8h]-[09BAh].
  - d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).

4. If the image size and the YUV format are already known, set the registers for the view resizer. If they are not known, read the data after stopping the JPEG decode process using the Decode Marker Read Interrupt (REG[0986h] bit 4).
5. Start decoding process.
  - a. Clear all status bits, set REG[0982h] to FFFFh
  - b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0133h.
  - c. Start the JPEG operation (REG[1002h] bit 0 = 1).

## Host CPU Process

6. After confirming FIFO valid data size (REG[09A8h]), write data to the JPEG FIFO.
7. Wait for FIFO Empty by interrupt or polling.  
If the Decode Marker Read Interrupt is enabled, there is an interrupt between steps 6 and 7. After reading data from the registers, disable the interrupt enable and clear the interrupt. Then set the registers for the view resizer.
8. Repeat steps 6 and 7 until the end of the JPEG file is detected.
9. If the JPEG Decode Complete Interrupt is enabled, there is an interrupt when the end of file marker is written to the JPEG FIFO.
10. Verify that the JPEG decode operation is complete (REG[1004h] bit 0 = 0).

### Note

When accessing the JPEG FIFO, an even number of accesses is needed for both encoding and decoding.

For the encoding process, there will be up to 3 bytes of data that is not needed. Discard this data and compare the data read to the final compressed file size in the Encode size result register (REG[09B4h]-[09B6h]).

For the decoding process, 32-bit unit data should always be written to the JPEG FIFO. Pad the end of the JPEG data stream with 00s to create 32-bits of data for the last JPEG FIFO entry.

### Note

If the JPEG FIFO is accessed after the JPEG process has completed or before the JPEG process has started, any data is considered invalid and ignored.

### 19.2.5 YUV Data Capture

1. Set the JPEG module registers.
  - a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 011, for YUV 4:2:0 set REG[0980h] bits 3-1 = 111.
  - b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] bit 7 = 1 and bit 0 = 1).
  - c. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:  
  
$$\text{JPEG FIFO size} = ((\text{REG}[09A4\text{h}] \text{ bits } 3-0) + 1) \times 4\text{K bytes.}$$
  
  
Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2  
$$(2 + 1) \times 4\text{KB} = 12\text{K bytes}$$
  - d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).
  - e. Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).
2. Set the YUV capture size.
  - a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Start capturing YUV data.
  - a. Clear all status bits by writing REG[0982h] to FFFFh.
  - b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0605h.
  - c. To enable the JPEG FIFO for YUV Capture Mode, set REG[1002h] bit 0 as 1. The JPEG FIFO is now ready to receive YUV data.
  - d. Start capturing (REG[098Ah] bit 0 = 1).

At this stage, it is the Host CPU's task to access the JPEG FIFO in the same way as for a JPEG Encode process. YUV data capture continues until a 0 is written to REG[098Ah] bit 0.

## 19.2.6 YUV Data Display

1. Set the JPEG module registers.
  - a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 001, for YUV 4:2:0 set REG[0980h] bits 3-1 = 101.
  - b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
2. Set the YUV data display size.
  - a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Set the JPEG Line Buffer registers (If the JPEG Line Buffer empty interrupt is used).
  - a. Set REG[09C6h] bit 0 = 1 and set REG[0986h] bit 0 = 1.
  - b. Clear the JPEG Line Buffer status bits (REG[09C0h] = FFFFh).
5. Start YUV data input.
  - a. Clear all JPEG status bits (REG[0982h] = FFFFh).
  - b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0001h.
  - c. Write YUV data to the JPEG Line Buffer Write Port (REG[09E0h]) when the JPEG Line Buffer is empty. The following table shows the maximum data size which can be sent at one time. The minimum line unit for YUV 4:2:2 is 1, for YUV 4:2:0 it is 2. After writing the YUV data to the JPEG Line Buffer, clear the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0 = 1).

| Line Size | The maximum data size |
|-----------|-----------------------|
| > 256     | Line Data Size x 16   |
| ≤ 256     | Line Data Size x 32   |
| ≤ 128     | Line Data Size x 64   |
| ≤ 64      | Line Data Size x 128  |
| ≤ 32      | Line Data Size x 256  |

- d. Continue writing YUV data until all the data is sent to the JPEG Line Buffer.

### 19.2.7 Exit Sequence

The exit sequence is the same for all cases: JPEG Decode, JPEG Encode, YUV Data Capture, and YUV Data Display.

1. Check the JPEG Operation Status bit (REG[1004h] bit 0).
2. For JPEG decode only, check the JPEG Error Status bits (REG[101Eh] bits 6-3).
3. Disable all interrupts, set REG[0986h] to 0000h.
4. Clear all status bits, set REG[0982h] to FFFFh.
5. Clear the JPEG Operation Select bit, write a 0 to REG[1000h] bit 2.
6. Perform a JPEG Software Reset, write a 1 to REG[0980h] bit 7.
7. Disable the JPEG codec, write a 0 to REG[0980h] bit 0.

## 20 Camera Interface

The S1D13715 is designed with a 2-port Camera interface. However, only one camera port can be used at a time (when Camera1 is enabled, Camera2 is disabled). Type 1 cameras are defined as cameras that supply horizontal and vertical sync information and typically are programmed through an I<sup>2</sup>C interface.

The Camera2 interface also supports MPEG Codec Interface input.

### 20.1 Camera1/2 Type 1 Camera

The Type 1 external camera module connected to either of the camera ports must satisfy the following conditions:

- The camera module must work synchronously with the S1D13715 camera clock output.
- The camera module must output VSYNC and HSYNC to the S1D13715 unless ITU-R BT 656 mode is used. ITU-R BT 656 mode uses embedded VSYNC/HSYNC signals in the YUV data stream. The S1D13715 fully satisfies the ITU-R BT656-4 requirements.
- The camera data must be 8-bit YUV 4:2:2. The following YUV 4:2:2 data formats are supported: UYVY, VYUY, YUYV, and YUYV

The following ranges for the camera YUV input data are supported.

*Table 20-1: YUV Input Data Ranges*

| YUV Straight        | YUV Offset             | YCbCr Straight       | YCbCr Offset           |
|---------------------|------------------------|----------------------|------------------------|
| $0 \leq Y \leq 255$ | $0 \leq Y \leq 255$    | $16 \leq Y \leq 235$ | $16 \leq Y \leq 235$   |
| $0 \leq U \leq 255$ | $-128 \leq U \leq 127$ | $16 \leq U \leq 240$ | $-113 \leq U \leq 112$ |
| $0 \leq V \leq 255$ | $-128 \leq V \leq 127$ | $16 \leq V \leq 240$ | $-113 \leq V \leq 112$ |

- The input data rate is determined by the camera module pixel clock output and must be a maximum of 1/3 of the system clock. For example, when the system clock is 54MHz, the camera module can have a maximum pixel clock output of 18MHz.

### 20.2 Strobe Control Signal

When the camera interface is enabled, a strobe feature is available. The strobe output is controlled using REG[0120h]-[0124h]. The strobe control signal output pin is GPIO20 and must be enabled using the Strobe Port Enable bit (REG[0124h] bit 3).

#### 20.2.1 Generating a Strobe Pulse

To generate a strobe pulse (GPIO20):

1. Enable the camera interface and ensure that the CM1VREF and CM1REF signals are present. ITU-R BT656 data format must not be enabled (REG[0110h] bit 5 = 0).
2. Set the JPEG Operation Mode bits (REG[0980h] bits 3-1 to 111 (JPEG Encode/Decode is bypassed)).
3. Enable the JPEG Module (REG[0980h] bit 0 = 1).
4. Configure the Strobe Line Delay (REG[0120h]), Strobe Pulse Width (REG[0122h], and Strobe Pulse Polarity (REG[0124h] bit 1).
5. Enable the strobe control signal output port by setting the Strobe Port Enable bit (REG[0124h] bit 3 = 1).
6. Enable the strobe signal (GPIO20) by setting the Strobe Enable bit (REG[0124] bit 0 = 1). This bit must remain enabled for the entire duration of the delay value (REG[0124h] bits 7-4), otherwise the strobe will be disabled immediately when the Strobe Enable bit is set to 0.
7. Generate a strobe signal (GPIO20) by setting the JPEG Start/Stop Control bit to 1 (REG[098A] bit 0 = 1).

Before generating another strobe signal, the strobe must be disabled (REG[0124h] bit 0 = 0) and then enabled again (REG[0124h] bit 0 = 1). Then generate the strobe pulse again by setting the JPEG Start/Stop Control bit to 1 (REG[098A] bit 0 = 1).

## 20.2.2 Strobe Timing

The strobe pulse (GPIO20) begins on the falling edge of CM1HREF after CM1VREF as specified by the Strobe Line Delay Timing bits (REG[0120h] bits 15-0). A zero delay (REG[0120h] bits 15-0 = 0h) starts the strobe pulse (GPIO20) on the first falling edge of CM1HREF after CM1VREF.

### Note

Both the Line Delay and Pulse Width signals are specified by counting HREFs which leads to an inherent timing delay if the HREF signal stops. This inherent delay must be considered when programming the Line Delay (REG[0120h]) and Pulse Width (REG[0122h]) registers.

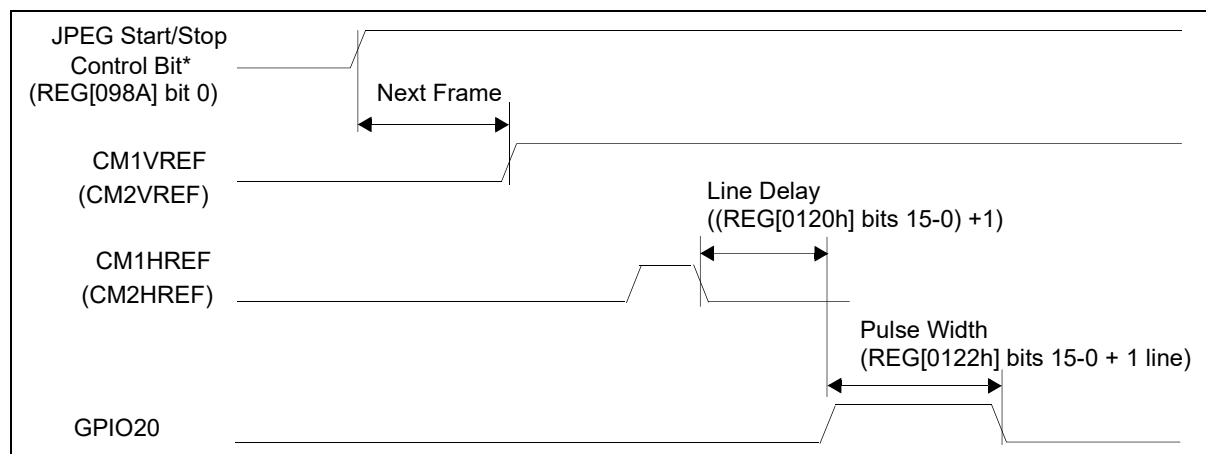


Figure 20-1: Strobe Signal Output Timing

### Note

The line delay (REG[0120h] bits 15-0) may be set greater than the period of the CM1VREF signal.

### 20.3 MPEG Codec Interface

The Camera2 interface can be selected to receive inputted YUV Data from a MPEG Codec Interface chip. The YUV data, along with horizontal and vertical sync signals, pixel clock output, and a display blank signal, enable the MPEG Codec Interface chip to encode image data into MPEG format. The following registers and bits control the MPEG Codec Interface.

- MPEG Codec Interface: REG[0106] bits 7-6 = 01.
- MPEG Codec Interface Vertical Height: REG[0128] bits 9-0.
- MPEG Codec Interface Horizontal Height: REG[012A] bits 9-0.
- MPEG Codec Interface Pixel Clock Output (CM2CLKOUT): REG[0104] bits 3-0.

## 21 Indirect Host Interface

The S1D13715 supports four indirect host interfaces which can be selected using CNF[4:2] (see Table 5-9: “Summary of Power-On/Reset Options,” on page 43). For an overview of the indirect host interface, see Section 1.4.2, “Indirect Addressing Host Interfaces” on page 14. For timing details, see Section 7.3, “Host Interface Timing” on page 60.

### 21.1 Using the Indirect Interface

Accessing the S1D13715 through the indirect interface is a two step process. See Section 21.2, “Example Sequences” on page 399 for example sequences of register read/writes, memory writes, and memory reads.

First, a “Command Write” (or register address) is written to the Indirect Interface Memory Access Port register (REG[0028h] where it is stored until the next Command Write. For Command Writes, the data bus width must be 16-bit.

Next, a “Data Read/Write” is done that specifies the data to be stored or read from the register specified in the “Command Write” cycle. “Data Read/Write” accesses to registers must be 16-bit accesses.

To access the internal memory, the memory address must be written to the Indirect Interface Memory Access registers (REG[0022h]-[0024h]) by “Command Write” and “Data Read/Write” accesses. Once the memory address is stored in these registers, a “Command Write” to the Memory Access Port Register REG[0028] must be done to enable memory accesses. Then “Data Read/Write” accesses to memory can be performed and they can be either 8-bit or 16-bit accesses. Once the memory “Data Read/Write” is complete, the address stored in REG[0022h] - 0024h] is incremented based on the Auto Increment bits (REG[0026h] bits 1-0).

If the auto increment feature is enabled (REG[0026h] bits 1-0 = 00 or 01), the S1D13715 can support a memory burst transfer where the host can “Data Read/Write” memory data continuously without issuing a “Command Write” each time. For the first access the host must set the memory address registers (REG[0022h] - REG[0024h]), but after that, the host can read/write data continuously without issuing a “Command Write”.

#### Note

When the indirect interface is enabled, the S1D13715 uses REG[002Ah], instead of the 2D BitBLT Data Memory Mapped Region Register (REG[10000h]).

### 21.2 Example Sequences

#### Note

All example sequences are shown using the Indirect 80 Type 3 host interface (CNF[4:2] = 011).

21.2.1 Register Read/Write Example Sequence

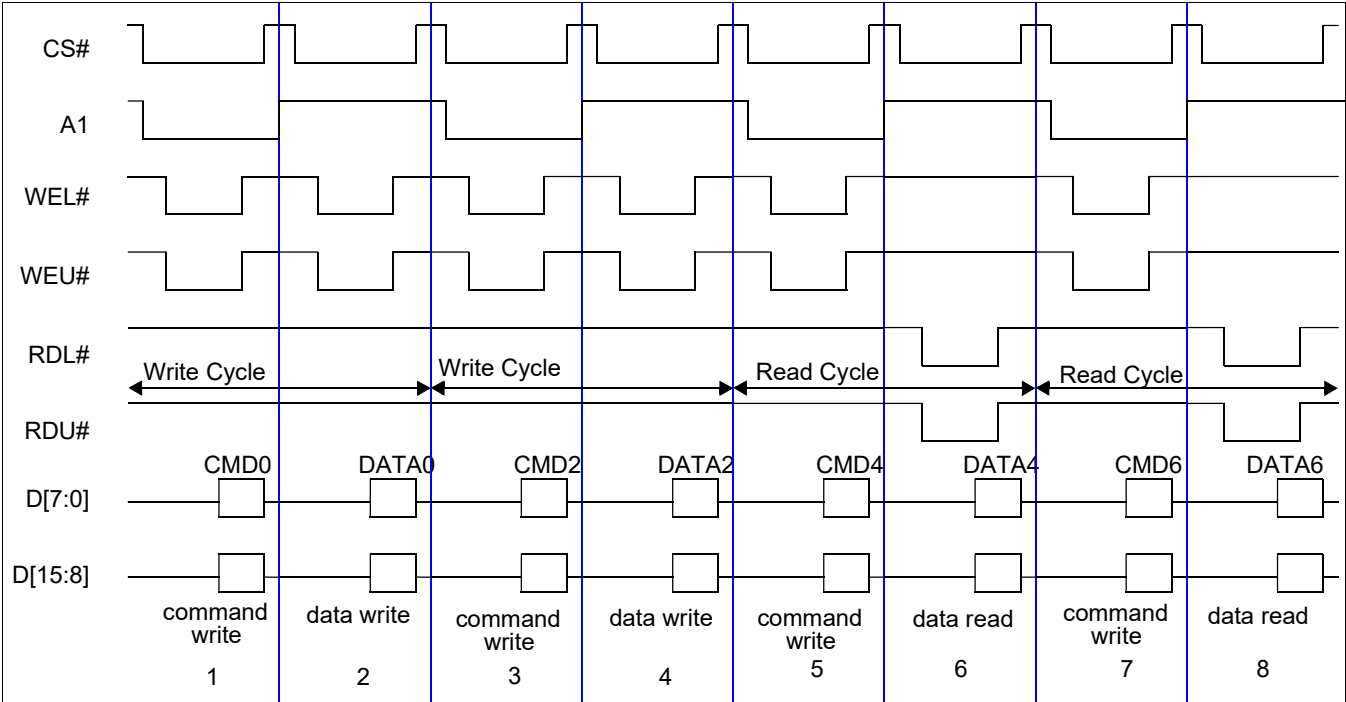


Figure 21-1: Register Read/Write” Example Sequence

1. Write the desired register number.
2. Write the data to be placed in the register.
3. Write the next register number.
4. Write the data to be placed in the register.
5. Write the desired register number.
6. Read the data from the register.
7. Write the desired register number.
8. Read the data from the register.
9. ....

**Note**  
The data bus width for all register accesses must be 16-bit.

## 21.2.2 Memory Write Example Sequence

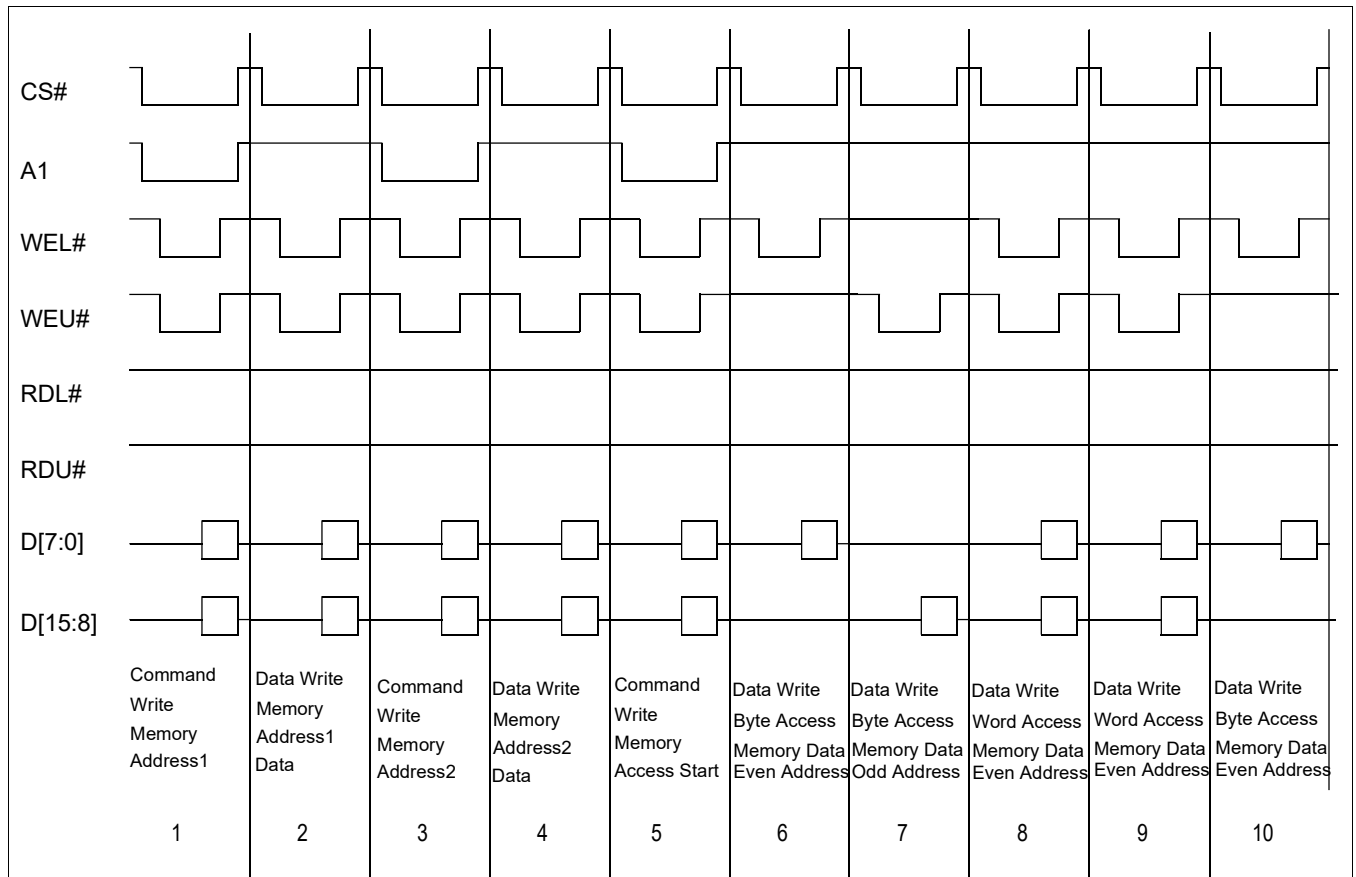


Figure 21-2: Memory Write Example Sequence

1. Write the register number of the Indirect Interface Memory Address Register 1 (REG[0022h]). The data bus width must be 16-bit.
2. Write the lower memory address (MA[15:0]) as data to REG[0022h]. The data bus width must be 16-bit.
3. Write the register number of the Indirect Interface Memory Address Register 2 (REG[0024h]). The data bus width must be 16-bit.
4. Write the upper memory address (MA[18:16]) as data to REG[0024h]. The data bus width must be 16-bit.
5. Write the register number of the Indirect Interface Memory Access Port register (REG[0028h]). This write triggers burst memory access beginning with the next access.

6. Write the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an even address and is in the lower byte. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a low byte access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
7. Write the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an odd address and is in the higher byte. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a high byte access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
8. Write the memory data. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
9. Write the memory data. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
10. ....

11. If another Command Write is made, burst memory access mode (or auto increment) is stopped and a register access takes place. Note that the Indirect Interface Memory Address registers (REG[0022h] -[0024h]) store the last incremented memory address until it is changed.

**Note**

To begin (or trigger) memory accesses, a Command Write to the Indirect Interface Memory Access Port register (REG[0028h]) is required, however, a data write to the register is not required. A Command Write to REG[0028h] indicates that burst memory accesses will start from the next data write.

### 21.2.3 Memory Read Example Sequence

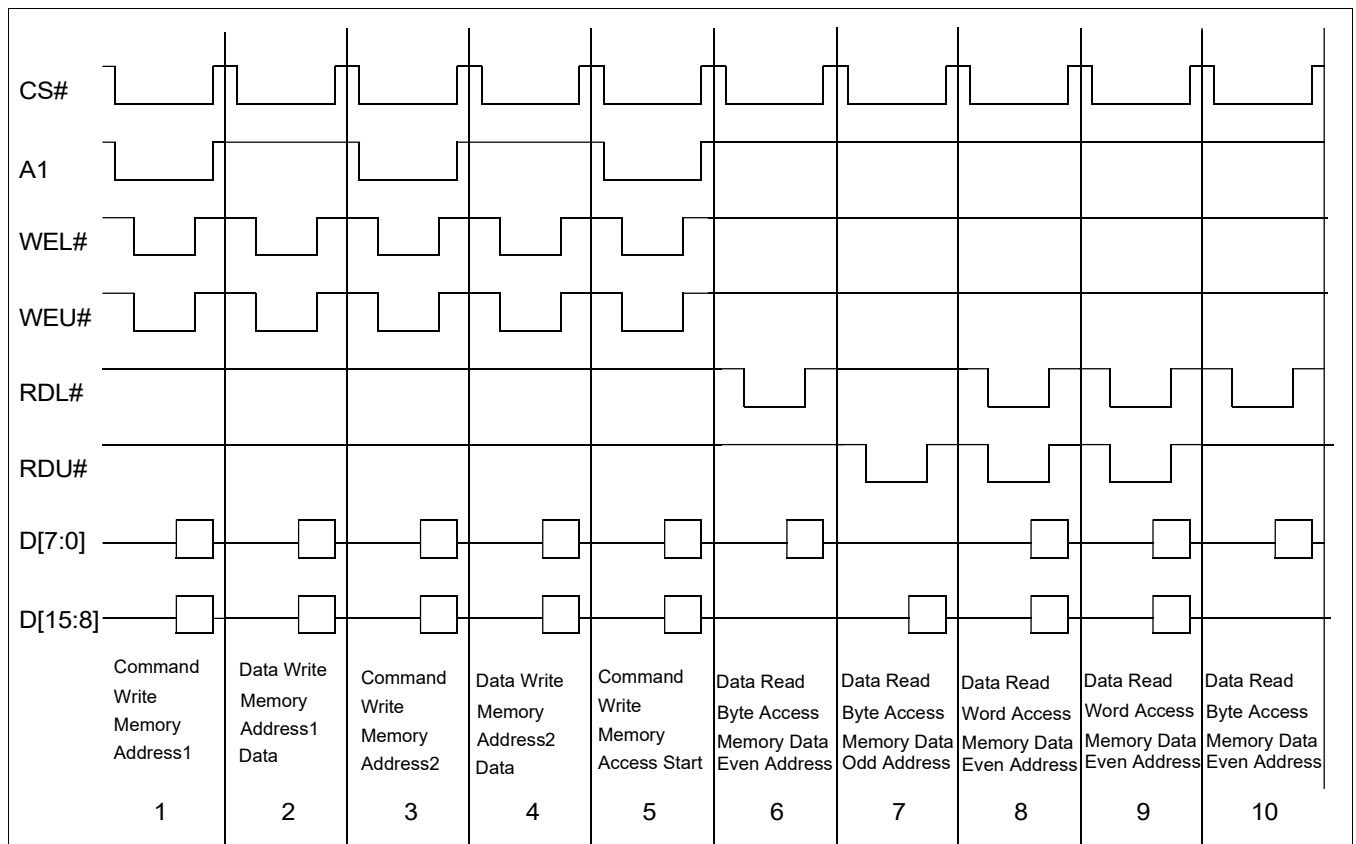


Figure 21-3: Memory Read Example Sequence

1. Write the register number of the Indirect Interface Memory Address Register 1 (REG[0022h]). The data bus width must be 16-bit.
2. Write the lower memory address (MA[15:0]) as data to REG[0022h]. The data bus width must be 16-bit.
3. Write the register number of the Indirect Interface Memory Address Register 2 (REG[0024h]). The data bus width must be 16-bit.

4. Write the upper memory address (MA[18:16]) as data to REG[0024h]. The data bus width must be 16-bit.
5. Write the register number of the Indirect Interface Memory Access Port register (REG[0028h]). This write triggers burst memory access beginning with the next access.
6. Read the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an even address and is in the lower byte. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a low byte access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
7. Read the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an odd address and is in the higher byte. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a high byte access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
8. Read the memory data. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
  - if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
9. Read the memory data. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
  - if REG[0026h] bits 1-0 = 00, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.

- if REG[0026h] bits 1-0 = 01, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
- if REG[0026h] bits 1-0 = 10, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

10. ....

11. If another Command Write is made, burst memory access mode (or auto increment) is stopped and a register access takes place. Note that the Indirect Interface Memory Address registers (REG[0022h] - [0024h]) store the last incremented memory address until it is changed.

**Note**

It is possible to perform a memory data write after a data read and vice versa without issuing another Command Write.

# 22 Mechanical Data

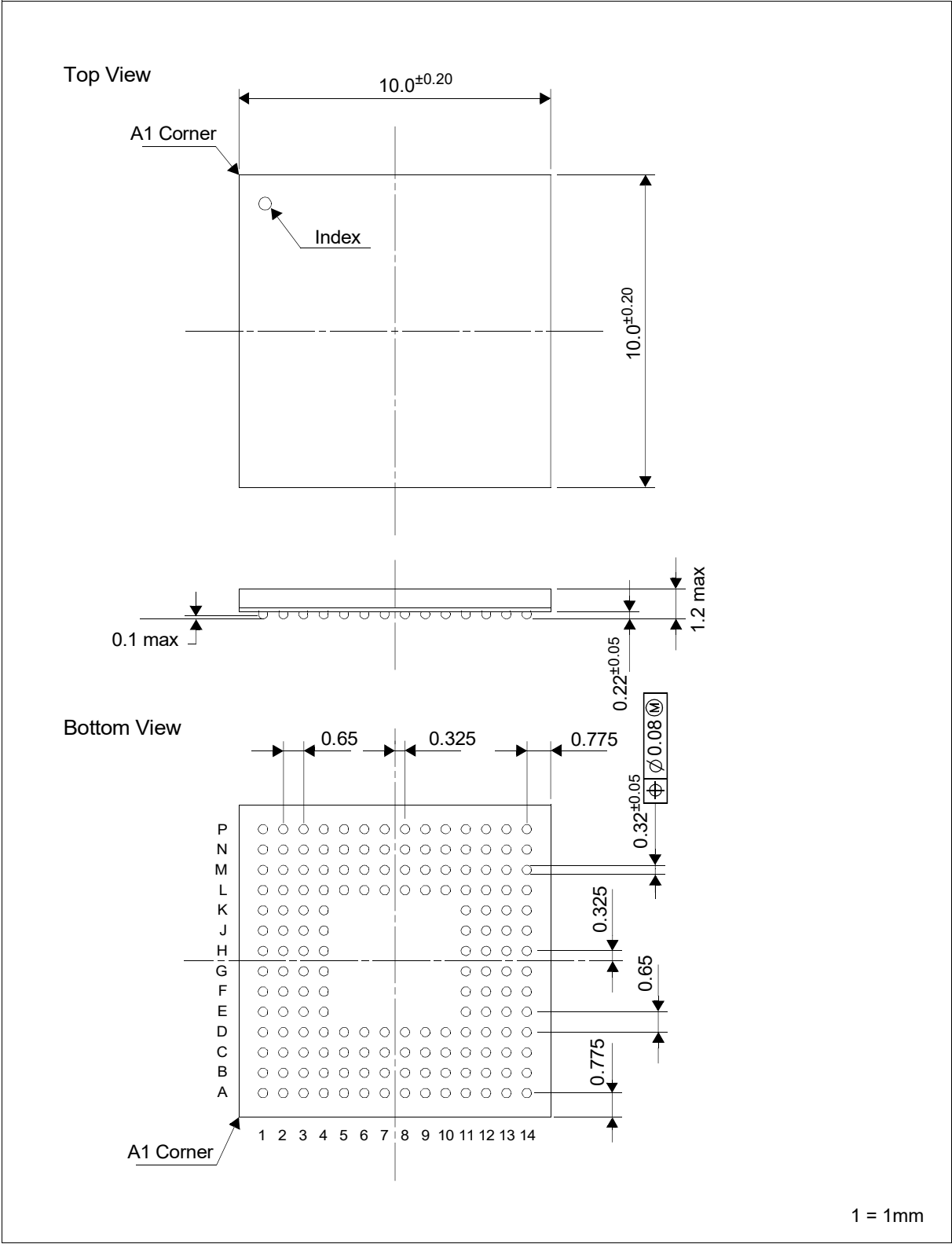


Figure 22-1: S1D13715 PFBGA 160-pin Package

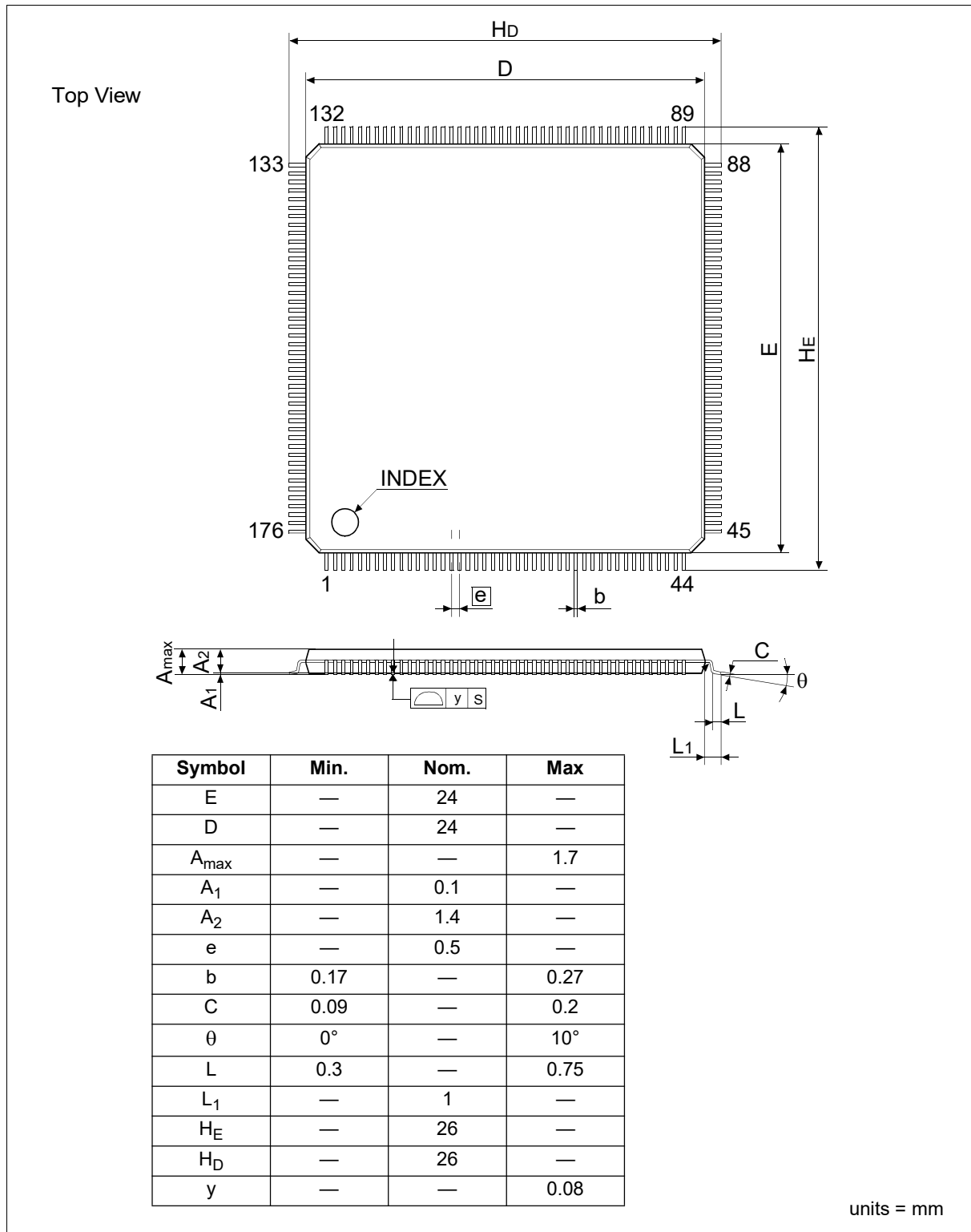


Figure 22-2: S1D13715 QFP21 176-Pin Package

# 23 Change Record

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X52A-A-001-07 | Revision 7.4 - Issued: April 12, 2018 <ul style="list-style-type: none"><li>• removed FCBGA package information</li><li>• clarified naming of section 7.5.1 and 7.5.2 AC Camera Timings to match the available product names</li><li>• updated Sales and Technical Support Section</li><li>• updated some formatting</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                  |
| X52A-A-001-07 | Revision 7.3 - Issued: June 12, 2008 <ul style="list-style-type: none"><li>• all changes from the last revision of the spec are highlighted in Red</li><li>• set revision to 7.3 to align with Japans numbering system</li><li>• globally add the QFP21-176 pin package</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| X52A-A-001-07 | Revision 7.02 - Issued: September 19, 2007 <ul style="list-style-type: none"><li>• all changes from the last revision of the spec are highlighted in Red</li><li>• section 24, updated the Sales and Technical Support addresses</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| X52A-A-001-07 | Revision 7.01 <ul style="list-style-type: none"><li>• all changes from the last revision of the spec are highlighted in Red</li><li>• updated EPSON tagline to “Exceed Your Vision”</li><li>• section 5.3.1, for both FCBGA and PFBGA packages clarified the pin#’s used for AB[18:1] and DB[15:0]</li><li>• section 5.3.2, for both FCBGA and PFBGA packages clarified the pin#’s used for FPDAT[17:0]</li><li>• section 5.3.3, for both FCBGA and PFBGA packages clarified the pin#’s used for CM1DAT[7:0] and CM2DAT[7:0]</li><li>• section 5.3.5, for both FCBGA and PFBGA packages clarified the pin#’s used for CNF[6:0] and GPIO[21:0]</li><li>• section 24.1, updated Japan sales office name and Taiwan office address/phone</li></ul> |
| X52A-A-001-07 | Revision 7.0 <ul style="list-style-type: none"><li>• add section 7.1.2 PLL Clock</li><li>• REG[000Eh] bits 1-0, updated V-Divider bit description to clarify its effect on PLL jitter and power consumption</li><li>• REG[0010h] bits 15-12, updated VCO Kv Set bit description to clarify its effect on PLL jitter and power consumption</li></ul>                                                                                                                                                                                                                                                                                                                                                                                             |
| X52A-A-001-06 | Revision 6.0 <ul style="list-style-type: none"><li>• rename section 7.5.1 to “S1D13715B01 Camera Interface Timing”</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

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|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|               | <ul style="list-style-type: none"> <li>• add section 7.5.2 S1D13715B01 Camera Interface Timing</li> <li>• section 20.1 Camera1/2 Type 1 Camera - rewrite bulleted text “The input data rate is determined by...” for a max 1/3 system clock</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| X52A-A-001-05 | <p>Revision 5.0</p> <ul style="list-style-type: none"> <li>• correct PFBGA160 mechanical package information in spec</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| X52A-A-001-04 | <p>Revision 4.0</p> <ul style="list-style-type: none"> <li>• add PFBGA160 package information to spec</li> <li>• REG[0116h] bit 4 - correct typos in figure 10-1, change “REG[0114h] bit 4” to “REG[0116h] bit 4” and “REG[0114h] bit 5” to “REG[0116h] bit 6”</li> <li>• section 11.1 Power-On/Power-Off Sequence - add “Software Reset” to Figure 11-1: Power On/Power-Off Sequence after “Hardware Reset” and remove the “Clock Source Select” block as per</li> <li>• section 11.1.2 Reset - rewrite software reset description</li> <li>• section 11.1.3 Standby Mode - rewrite standby mode description</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| X52A-A-001-03 | <p>Revision 3.0</p> <ul style="list-style-type: none"> <li>• section 1.5.3 Serial LCD Interface - delete “... except that the LCD Module VSYNC Input is not supported for serial interface panels” from end of section</li> <li>• section 1.6 Display Features - add Mirror to section</li> <li>• section 1.9.1 Encoder - add “..., or to encode YUV data sent by the Host CPU” to the third paragraph</li> <li>• section 1.9.2 Decoder - add “..., or to send the resulting YUV decoded data back to the Host CPU” to the first paragraph</li> <li>• section 2.2 Host CPU Interface- add bullet “M/R# and CS# inputs select between memory and register address space in 2 CS# mode” and bullet “CPU parallel port for direct control of a parallel LCD”</li> <li>• section 2.4 Display Modes- add bullet “Decoded by the internal JPEG decoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO”</li> <li>• section 2.8 Picture Input/Output Functions - add bullets “Host CPU can directly control parallel interface panels on LCD1 or LCD2” and “Encoded by the internal JPEG encoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO”</li> <li>• section 5.2.1 Host Interface - rewrite descriptions for SCS#, SCLK, SA0 and SI</li> <li>• section 5.2.2 LCD Interface - rewrite descriptions</li> <li>• section 10.1 Register Mapping - add “...(for 1 CS# mode), or CS# = 1 and M/R# = 0 (for 2 CS# mode)...” to first paragraph</li> <li>• REG[0028h] - change Command Write to Index Write in bit description</li> <li>• REG[0054h] - add “... for RGB displays requiring initialization through a serial interface” to all bit descriptions</li> </ul> |

- REG[0056h] bit 13 - rewrite bit description “When this bit = 1...”
- REG[0056h] bit 12 - rewrite bit description “When this bit = 1...”
- REG[0056h] bit 7 - add “When a manual transfer has been initiated...” to bit description
- REG[005Eh] bit 13 - rewrite bit description “When this bit = 1...”
- REG[005Eh] bit 12 - rewrite bit description “When this bit = 1...”
- REG[005Eh] bit 7 - add “When a manual transfer has been initiated...” to bit description
- REG[0110h] bit 8 - rename bit and add note to bit description
- REG[0114h] bit 8 - delete note in bit description
- REG[0116h] bit 1 - add “This bit is masked by the Camera Frame Capture Interrupt Enable...” to bit description
- REG[0120h] - change description to read “... the first HSYNC input of a camera frame...”
- REG[0200h] bit 6 - rewrite bit description
- REG[0124h] bits 7-4 - rewrite bit description
- REG[0124h] bit 0 - rewrite bit description
- REG[0200h] bit 12 - rewrite bit description
- REG[0200h] bit 7 - rewrite bit description
- REG[021Eh] bits 11-0 - add note to bit description
- REG[0220h] - add note to bit description
- REG[0222h] - add note to bit description
- REG[0224h] - add note to bit description
- REG[0226h] - add note to bit description
- REG[0240h] bit 5 - rewrite bit description
- REG[0240h] bit 4 - rename bit and rewrite bit description
- REG[0260h] bit 4 - rename bit and rewrite bit description
- REG[0930h] bit 3 - add note to bit description
- REG[0930h] bits 1-0 - rewrite description for bits 1-0 = 01 in table
- REG[094Ch] bits 13-8 - rewrite bit description
- REG[094Ch] bits 5-0 - rewrite bit description
- REG[096Ch] bits 13-8 - rewrite bit description
- REG[096Ch] bits 5-0 - rewrite bit description
- REG[0980h] bit 4 - add “The YUV data range depends on the interface...” to bit description

- REG[0982h] bit 11 - add note “The Encode Size Limit Violation Flag can only be cleared...” to bit description
- REG[0982h] bit 10 - add note “The JPEG FIFO Threshold Trigger Flag can only be cleared...” to bit description
- REG[0982h] bit 9 - add note “The JPEG FIFO Full Flag can only be cleared...” to bit description
- REG[0982h] bit 8 - add note “The JPEG FIFO Empty Flag can only be cleared...” to bit description
- REG[0982h] bit 0 - add “or Host Decode/Encode...” to bit description
- REG[0984h] bit 14 - add note to bit description
- REG[0984h] bits 13-12 - add note to bit description
- REG[09A2h] - remove reserved bits 14 - 8 and mark them n/a
- REG[09A2h] bits 3-2 - changes to table
- REG[09C0h] bit 2 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C0h] bit 1 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C0h] bit 0 - rewrite bit description
- REG[09C2h] bit 2 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C2h] bit 1 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C2h] bit 0 - rewrite bit description
- REG[09C4h] bit 0 - changes to “When this bit = 1...” in bit description
- section 12.2, removed separate lines about FPCS2#, FPSO, FPSCLK
- section 19.1.1, added information about terminate cycles when read from an empty FIFO or write to a full FIFO takes place
- section 19.2.1 JPEG Encoding Process - changes made to Figure 19-5 JPEG Encoding Process (4 of 4) - add “Clear JPEG Interrupt Flags”

X52A-A-001-02

Revision 2.0

- Section 5.2.5 Miscellaneous - re-write note “When CNF1 = 0 (GPIO pins...)” adding more information
- Section 7.3 - Replace all Host Bus timing
- Section 7.3 - Replace all Host Bus timing
- REG[0128h] - add register equation “REG[0128h] bits 9-0 = Vertical Total -1”
- REG[012Ah] - add register equation “REG[0128h] bits 9-0 = Horizontal Total -1”

# Change Record

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|               |                                                                                       |
|---------------|---------------------------------------------------------------------------------------|
| X52A-A-001-01 | Revision 1.0                                                                          |
|               | <ul style="list-style-type: none"><li>Released as Revision 1.0 (2003/07/22)</li></ul> |

## 24 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

[https://global.epson.com/products\\_and\\_drivers/semicon/products/display\\_controllers/](https://global.epson.com/products_and_drivers/semicon/products/display_controllers/)



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