International
IOR Rectifier

IRAM336-025SB

iMOTION™ Series

3 Phase Inverter HIC
2A, 500V

Integrated Power Hybrid IC for
Appliance Motor Drive Applications

Description

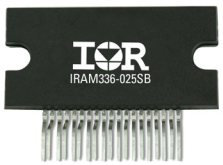
International Rectifier's IRAM336-025SB is a multi-chip Hybrid IC developed for low power appliance motor control applications such as Fans, Pumps, and refrigerator compressors. The compact Single in line (SIP-S) package minimizes PCB space.

Several built-in protection features such as temperature feedback, shoot through prevention, under voltage lockout, and shutdown input makes this a very robust solution. The combination of highly efficient high voltage MOSFETs and the industry benchmark 3-phase HVIC driver (3.3V/5V input compatible) and thermally enhanced package makes this a highly competitive solution.

The bootstrapped power supplies for the high side drivers can be generated using internal bootstrap diodes eliminating the need for isolated power supplies. This feature reduces the component count, board space, and cost of the system.

Features

- Motor Power up to 250W / 85~253 Vac.
- Integrated Gate Drivers and Bootstrap Diodes.
- Over-current Shut-Down function.
- Under-voltage lockout for all switches.
- Matched propagation delay for all channels.
- Schmitt-triggered input logic.
- Cross-conduction prevention logic.
- Lower di/dt gate driver for better noise immunity.



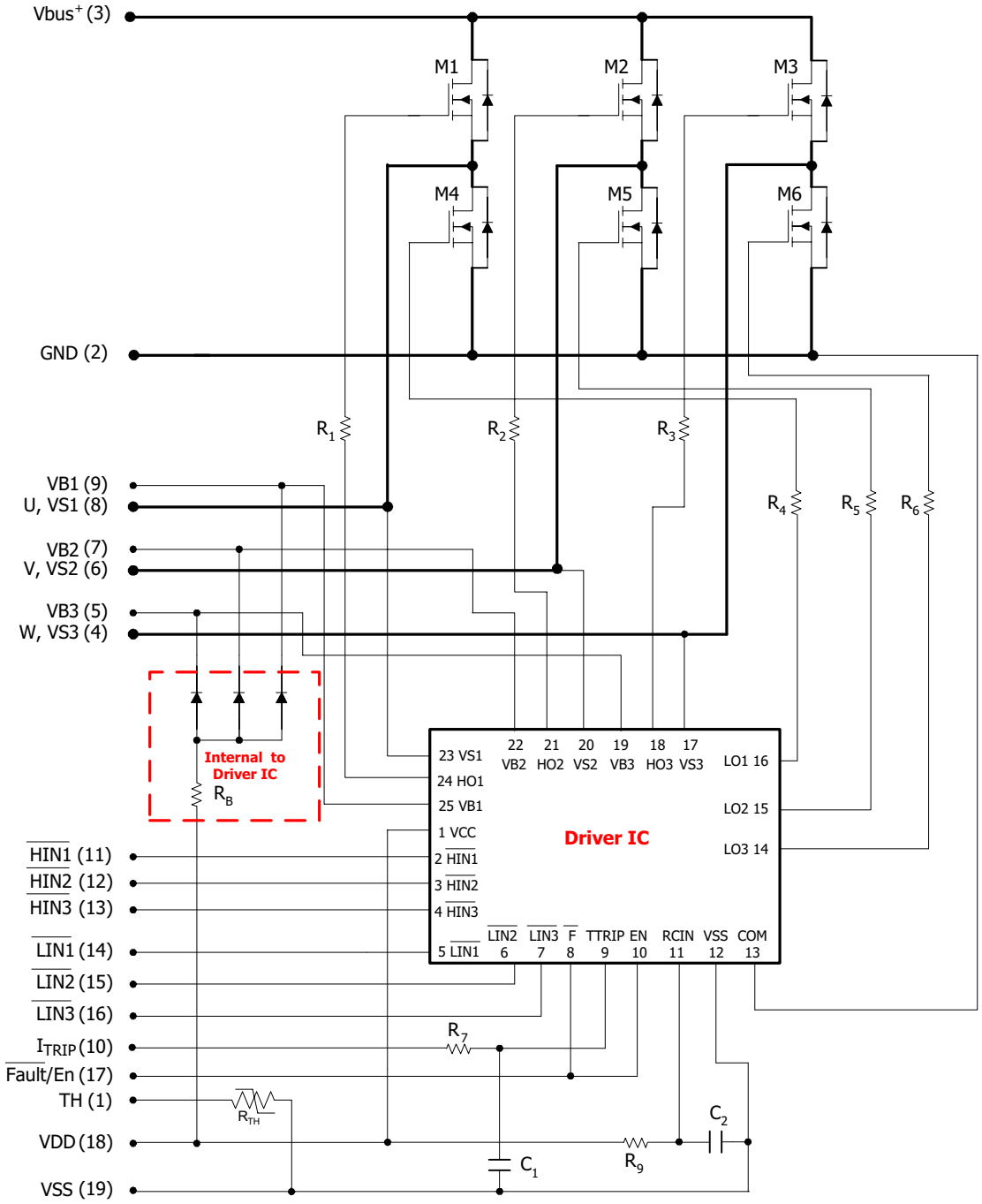
Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}.

V_{DSS}	MOSFET Blocking Voltage	500	V
Vbus	Positive DC Bus Input Voltage	400	V
I_o @ T_C=25°C	RMS Phase Current	2.0	A
I_o @ T_C=100°C	RMS Phase Current (Note 1)	1.0	
I_{pk} @ T_C=25°C	Maximum Peak Current (tp<100µs)	6.0	
P_d	Maximum Power dissipation per Fet @ T_C =25°C	15	W
T_J (MOSFET & IC)	Maximum Operating Junction Temperature	+150	°C
T_C	Operating Case temperature Range	-20 to +100	
T_{STG}	Storage Temperature Range	-40 to +125	
T	Mounting torque (M3 screw)	0.6	Nm

Note 1: Sinusoidal Modulation at V^+=360V, T_J=150°C, F_{PWM}=20kHz, F_{MOD}=50Hz, MI=0.8, PF=0.6, See Figure 5.

Internal Electrical Schematic – IRAM336-025SB



Absolute Maximum Ratings (Continued)

Absolute Maximum Ratings indicate substained limits beyond which damage to the device may occur. All voltage paramaters are absolute voltages referenced to V_{SS}.

$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3}$ - 20	$V_{B1,2,3}$ +0.3	V	
$V_{B1,2,3}$	High side floating supply voltage	-0.3	500	V	
V_{DD}	Low Side and logic fixed supply voltage	-0.3	20	V	
V_{IN}, $V_{F/EN}$, V_{ITRIP}	Input voltage LIN, HIN, Fault/EN, I_{Trip}	-0.3	Lower of (V_{SS}+15V) or V_{DD}+0.3V	V	

MOSFET Characteristics

V_{BIAS} (V_{CC}, V_B) = 15V and T_A = 25°C unless otherwise specified. The V_{DD} parameter is referenced to V_{SS}.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	---	---	V	V_{IN}=5V, I_D=250µA
I_{DSS}	Drain-to-Source Leakage Current	---	5	100	µA	V_{IN}=5V, V^+=500V
$R_{DS(ON)}$	Drain-to-Source On Resistance	---	2.2	2.7	Ω	I_D=1.0A, V_{DD}=15V
		---	5.5	---		I_D=1.0A, V_{DD}=15V, T_J=150°C
V_{FM}	Diode Forward Voltage Drop	---	0.87	1.0	V	I_F=1.0A
		---	0.76	---		I_F=1.0A, T_J=150°C

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to V_{SS}. The V_S offset is tested with all supplies biased at 15V differential.

Symbol	Definition	Min	Typ	Max	Units
V^+	Positive Bus Input Voltage	---	---	360	V
$V_{B1,2,3}$	High side floating supply voltage	V_S+10	V_S+15	V_S+20	
V_{DD}	Low side and logic fixed supply voltage	10	15	20	V
V_{ITRIP}	I_{TRIP} input voltage	V_{SS}	---	V_{SS}+5	
V_{IN}, $V_{F/EN}$, V_{ITRIP}	Logic input voltage LIN, HIN, Fault/EN, I_{TRIP} - Note 2	V_{SS}	---	V_{SS}+5	V
F_p	Maximum PWM Carrier Frequency	---	---	20	KHz

Note 2: Logic operational for V_s from COM-5V to V_{SS}+500V. Logic state held for V_s from V_{SS}-5V to V_{SS}-V_{BS}. (please refer to DT97-3 for more details).

Static Electrical Characteristics (T_J= 25°C Unless Otherwise Specified)

V_{BIAS} (V_{DD}, $V_{BS1,2,3}$)=15V, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (Static Electrical Characteristics are Based on Driver IC Data Sheet).

Symbol	Definition	Min	Typ	Max	Units
$V_{EN,th+}$	Enable Positive going threshold	---	---	2.5	V
$V_{EN,th-}$	Enable Negative going threshold	0.8	---	---	V
V_{DDUV+}, V_{BSUV+}	V_{DD} and V_{BS} supply undervoltage, Positive going threshold	8	8.9	9.8	V
V_{DDUV-}, V_{BSUV-}	V_{DD} and V_{BS} supply undervoltage, Negative going threshold	7.4	8.2	9	V
I_{QBS}	Quiescent V_{BS} supply current	---	70	120	µA
I_{QDD}	Quiescent V_{DD} supply current	---	3	4	mA
I_{LK}	Offset Supply Leakage Current	---	---	50	µA
R_B	Internal BS Diode R_{ON} (see Integrated BS Functionality page 10)	---	200	---	Ω

Dynamic Electrical Characteristics (T_J= 25°C Unless Otherwise Specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output propagation turn-on delay time (see fig.13a)	---	750	---	ns	I_D=1.5A, V^+=360V
T_{OFF}	Input to Output propagation turn-off delay time (see fig. 13b)	---	920	---	ns	

Thermal and Mechanical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{th(J-C)}$	Thermal resistance, per FET	---	5.8	8.0	°C/W	Flat, Insulation Material.

Internal NTC - Thermistor Characteristics

Parameter	Definition	Min	Typ	Max	Units	Conditions
R_{25}	Resistance	97	100	103	kΩ	T_C = 25°C
R_{125}	Resistance	2.25	2.52	2.8	kΩ	T_C = 125°C
B	B-constant (25-50°C)	4208	4250	4293	k	$R_2 = R_1 e^{[B(1/T2 - 1/T1)]}$
Temperature Range		-40	---	125	°C	
Typ. Dissipation constant		---	1	---	mW/°C	T_C = 25°C

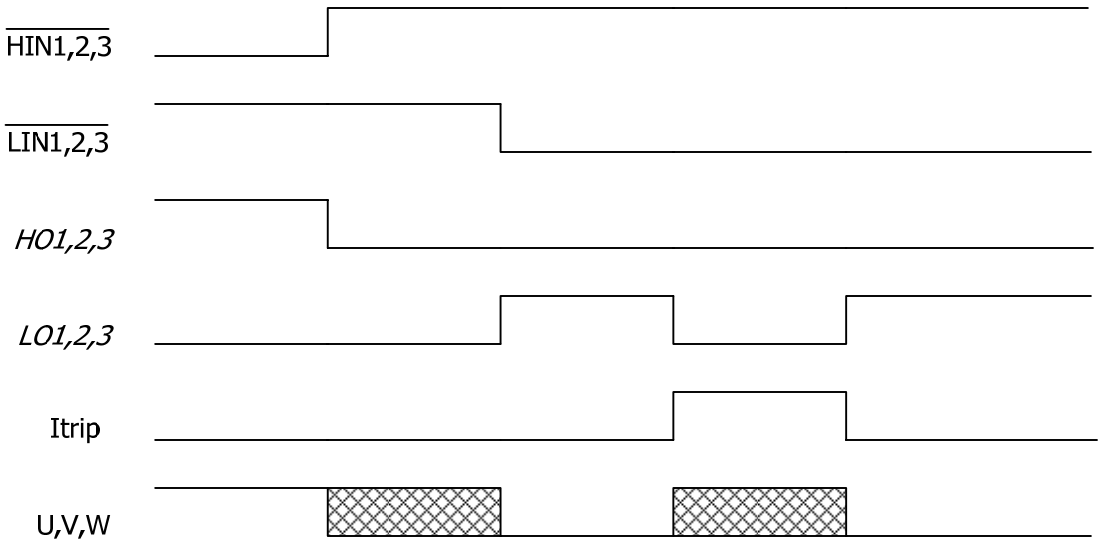
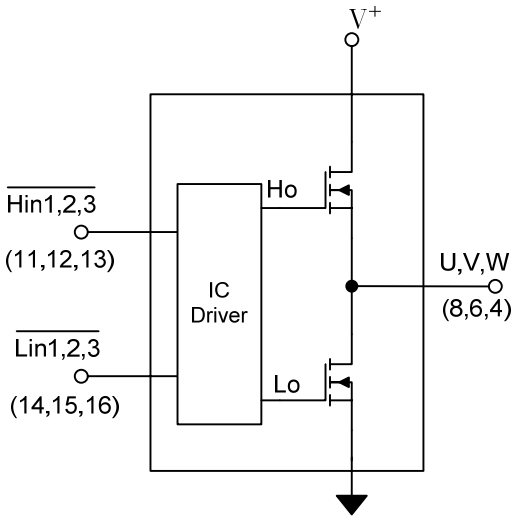


Figure 1. Input/Output Timing Diagram

Note 3: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.



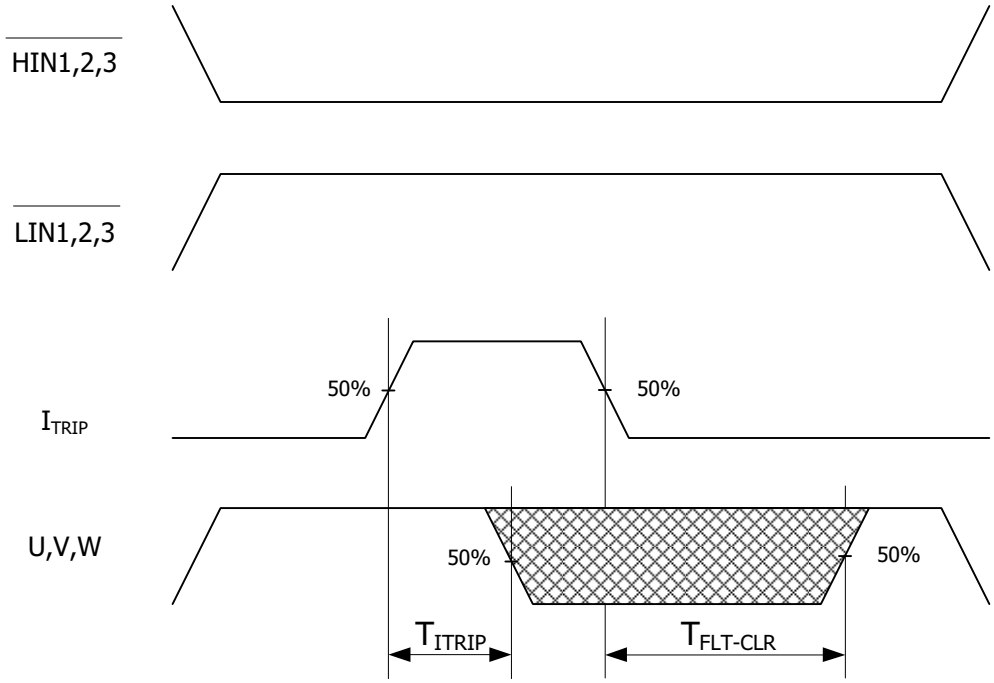


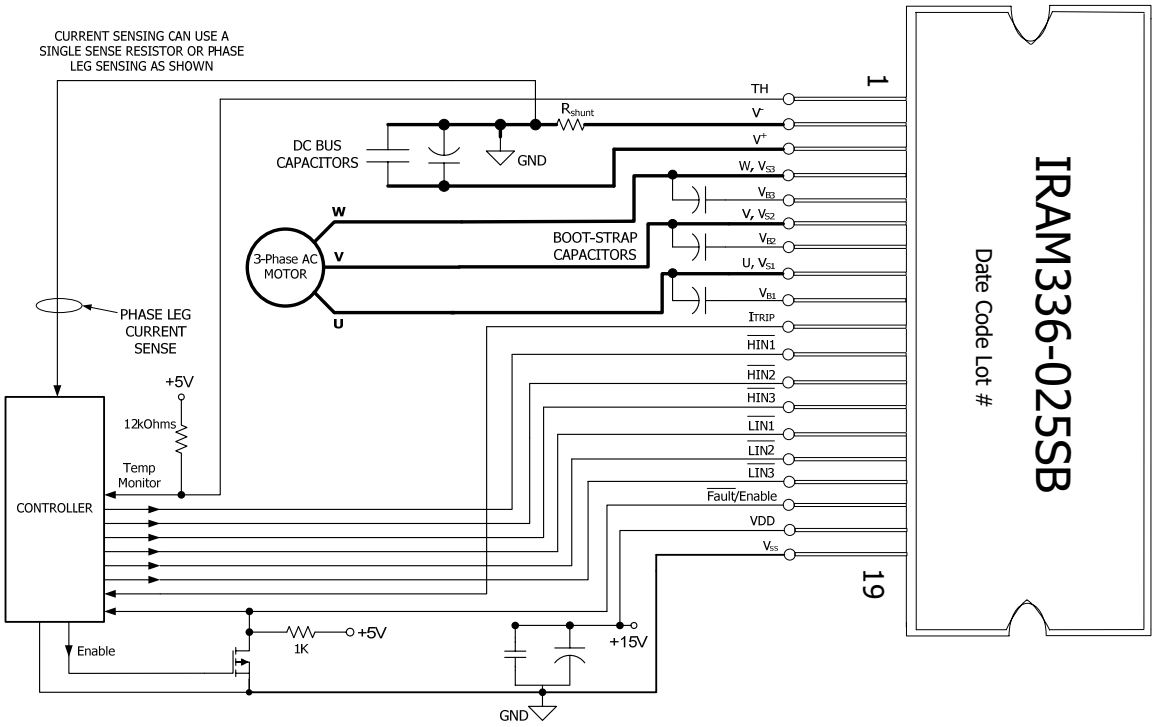
Figure 2. I_{TRIP} Timing Waveform

Note 4: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

Input-Output Logic Level Table

$\overline{\text{FLT- EN}}$	I_{TRIP}	$\overline{\text{HIN1,2,3}}$	$\overline{\text{LIN1,2,3}}$	U,V,W
1	0	0	1	V^+
1	0	1	0	0
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off

Typical Application Circuit – IRAM336-025SB



Application Circuit Recommendation

1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

2. In order to provide good decoupling between VCC-VSS and Vb-Vs terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are strongly recommended.

3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a or application note AN-1044 or Figure 12.

4. WARNING! Please note that after approx. 8ms the FAULT is automatically reset (see Dynamic Characteristics Table on page 5). PWM generator must be disabled within automatic reset time ($T_{FLT-CLR}$) to guarantee shutdown of the system, over-current condition must be cleared before resuming operation.

5. The case of the module is connected to the negative DC Bus and is NOT Isolated. It is recommended to provide isolation material between case and heat sink to avoid electrical shock.

Module Pin-Out Description

Pin	Name	Description
1	TH	Temperature Feedback
2	V^-	Negative Bus Input Voltage
3	V^+	Positive Bus Input Voltage
4	W,V_{S3}	Output 3 - High Side Floating Supply Offset Voltage
5	V_{B3}	High Side Floating Supply Voltage 3
6	V,V_{S2}	Output 2 - High Side Floating Supply Offset Voltage
7	V_{B2}	High Side Floating Supply voltage 2
8	U,V_{S1}	Output 1 - High Side Floating Supply Offset Voltage
9	V_{B1}	High Side Floating Supply voltage 1
10	I_{TRIP}	Current Feedback & Shut-down Function
11	$\overline{H_{IN1}}$	Logic Input High Side Gate Driver - Phase 1
12	$\overline{H_{IN2}}$	Logic Input High Side Gate Driver - Phase 2
13	$\overline{H_{IN3}}$	Logic Input High Side Gate Driver - Phase 3
14	$\overline{L_{IN1}}$	Logic Input Low Side Gate Driver - Phase 1
15	$\overline{L_{IN2}}$	Logic Input Low Side Gate Driver - Phase 2
16	$\overline{L_{IN3}}$	Logic Input Low Side Gate Driver - Phase 3
17	$\overline{FAULT}$/EN	Fault Indicator & Enable Function
18	V_{DD}	+15V Main Supply
19	V_{SS}	Negative Main Supply

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Integrated Bootstrap Functionality

The internal Driver IC in the IRAM336-025SB embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.

There is one bootstrap FET for each channel and it is connected between each of the floating supply (VB1, VB2, VB3) and Vcc as shown in Figure 3.

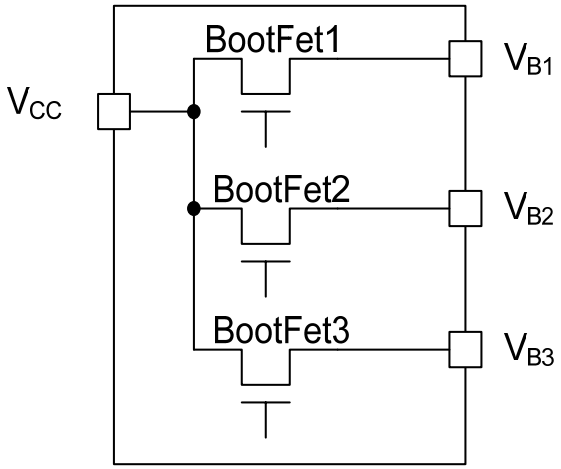


Figure 3. Simplified BootFet Connection

The Bootstrap FET of each channel follows the state of the respective low side output stage (i.e., bootFet is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 1.1(V_{cc}). In that case the bootstrap FET stays off until the V_s voltage returns below that threshold (see Fig. 4).

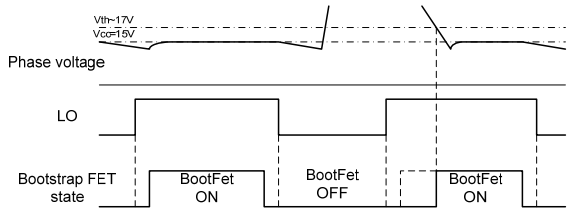


Figure 4. State Diagram

Bootstrap FET is suitable for most PWM modulation schemes and can be used either in parallel with the external bootstrap network (diode+resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- When used in non-complementary PWM schemes (typically 6-step modulations).
- At a very high PWM duty cycle due to the bootstrap FET equivalent resistance (R_{BS}, see page 5).

In these cases, better performances can be achieved by using an external bootstrap network.

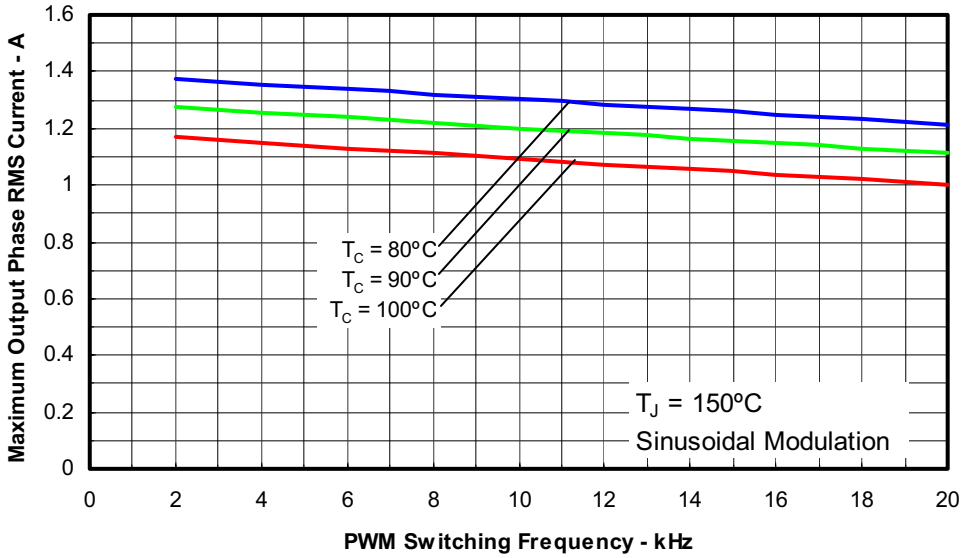


Figure 5. Maximum Sinusoidal Phase Current vs. PWM Switching Frequency
Sinusoidal Modulation, V^+=360V, T_J=150°C, F_{MOD}=50Hz, MI=0.8, PF=0.6

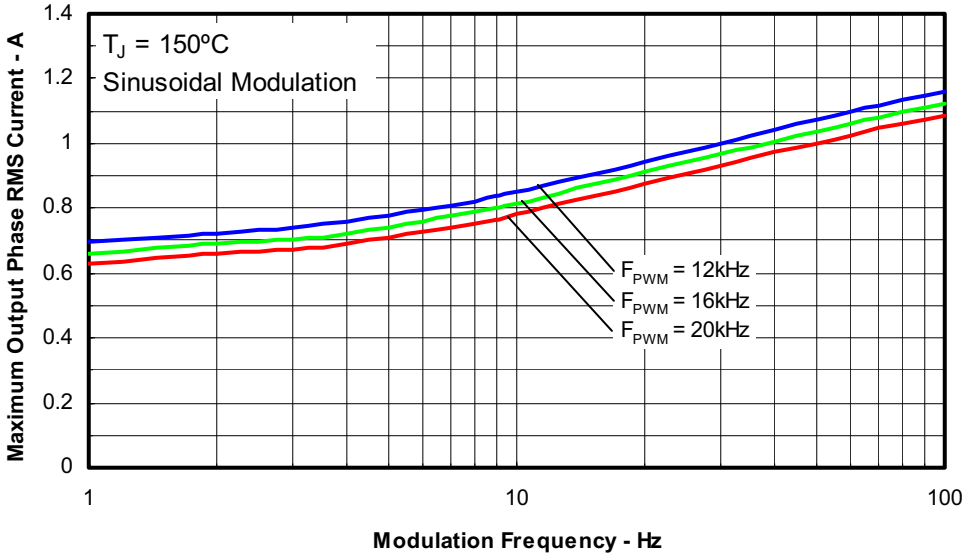


Figure 6. Maximum Sinusoidal Phase Current vs. Modulation Frequency
Sinusoidal Modulation, V^+=360V, T_J=150°C, MI=0.8, PF=0.6

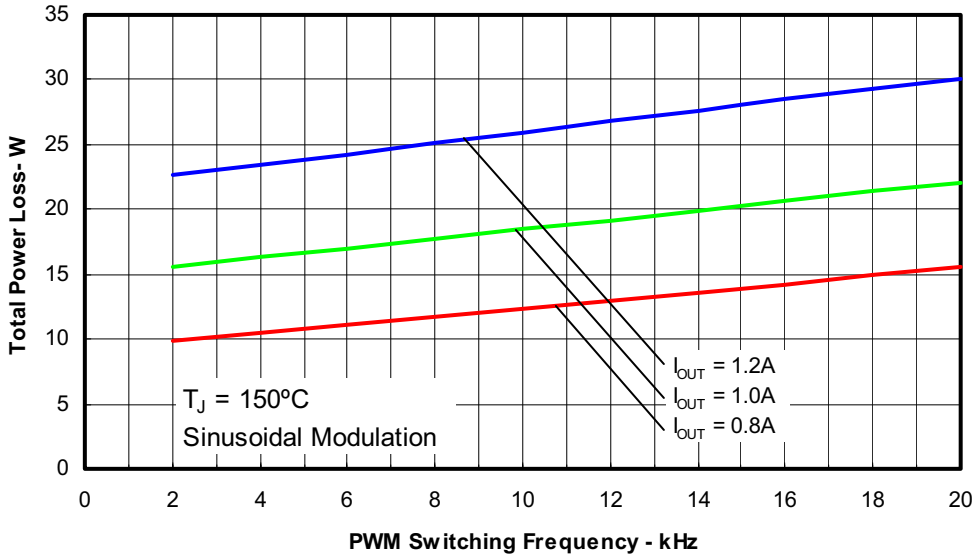


Figure 7. Total Power Losses vs. PWM Switching Frequency
Sinusoidal Modulation, V^+=360V, T_J=150°C, MI=0.8, PF=0.6

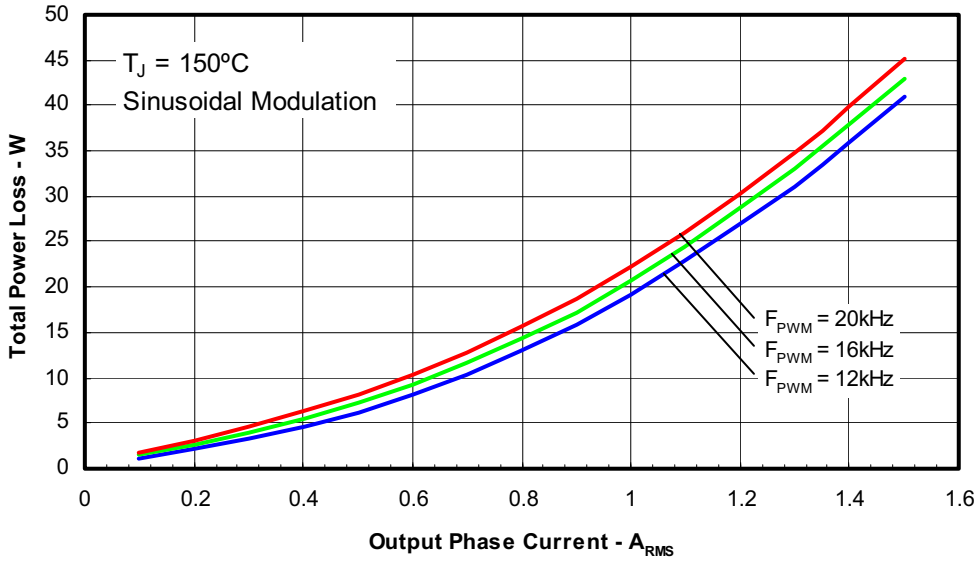


Figure 8. Total Power Losses vs. Output Phase Current
Sinusoidal Modulation, V^+=360V, T_J=150°C, MI=0.8, PF=0.6

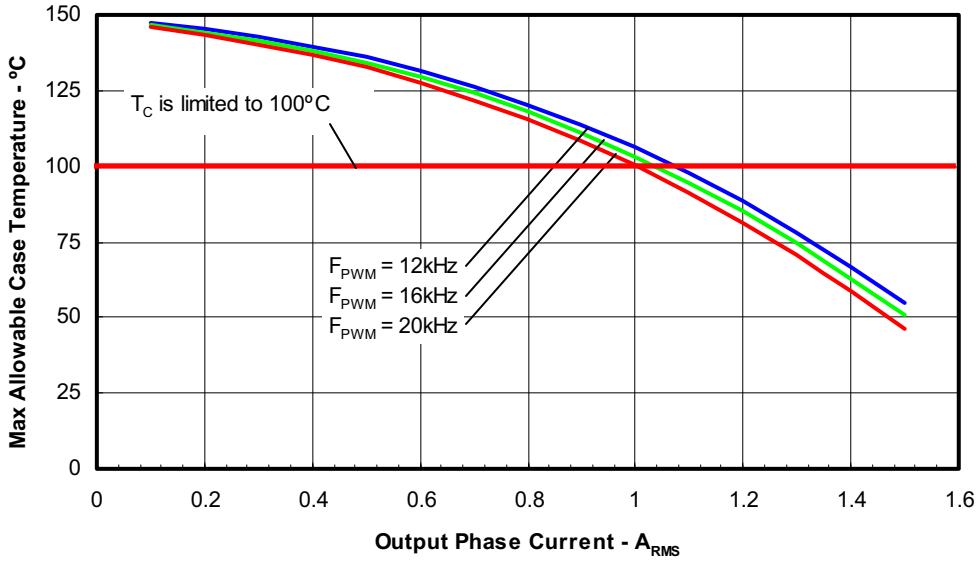


Figure 9. Maximum Allowable Case Temperature vs. Output RMS Current per Phase Sinusoidal Modulation, V^+=360V, T_J=150°C, MI=0.8, PF=0.6

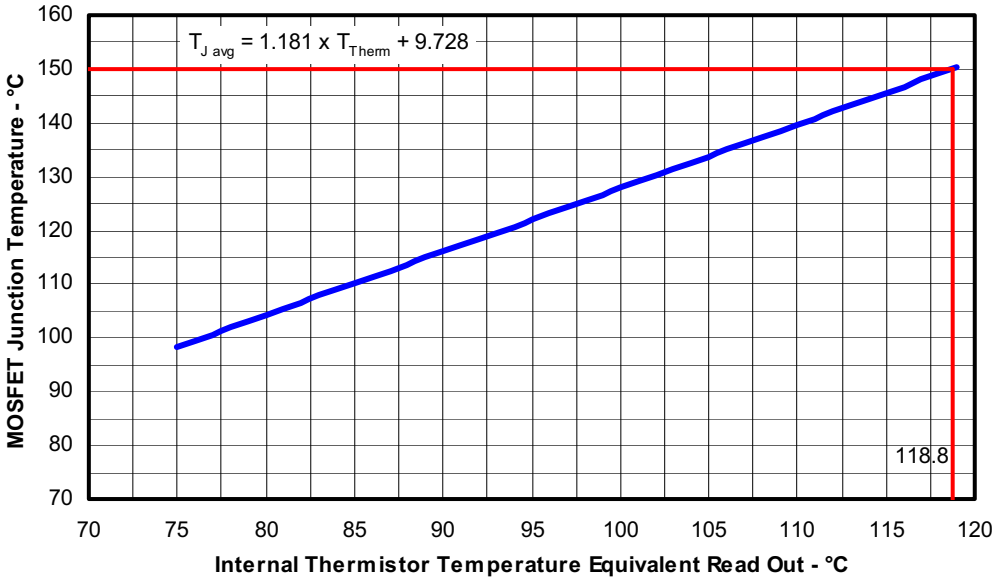
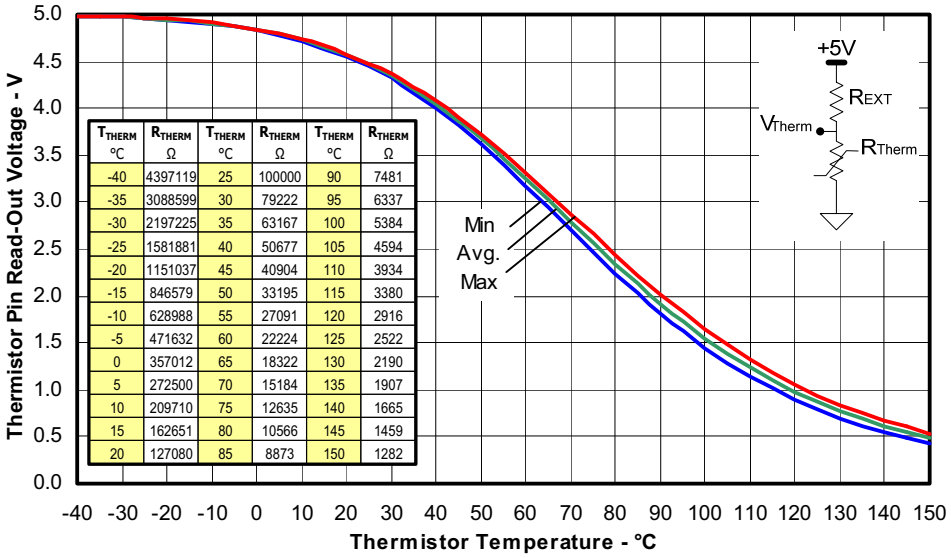


Figure 10. Estimated Maximum MOSFET Junction Temperature vs. Thermistor Temperature Sinusoidal Modulation, V^+=360V, T_J=150°C, F_{PWM}=20KHz, F_{MOD}=50Hz, MI=0.8, PF=0.6



T_{THERM} °C	R_{THERM} Ω	T_{THERM} °C	R_{THERM} Ω	T_{THERM} °C	R_{THERM} Ω
-40	4397119	25	100000	90	7481
-35	3088599	30	79222	95	6337
-30	2197225	35	63167	100	5384
-25	1581881	40	50677	105	4594
-20	1151037	45	40904	110	3934
-15	846579	50	33195	115	3380
-10	628988	55	27091	120	2916
-5	471632	60	22224	125	2522
0	357012	65	18322	130	2190
5	272500	70	15184	135	1907
10	209710	75	12635	140	1665
15	162651	80	10566	145	1459
20	127080	85	8873	150	1282

Figure 11. Thermistor Readout vs. Temperature (12Kohm pull-up resistor, 5V) and Normal Thermistor Resistance values vs. Temperature Table.

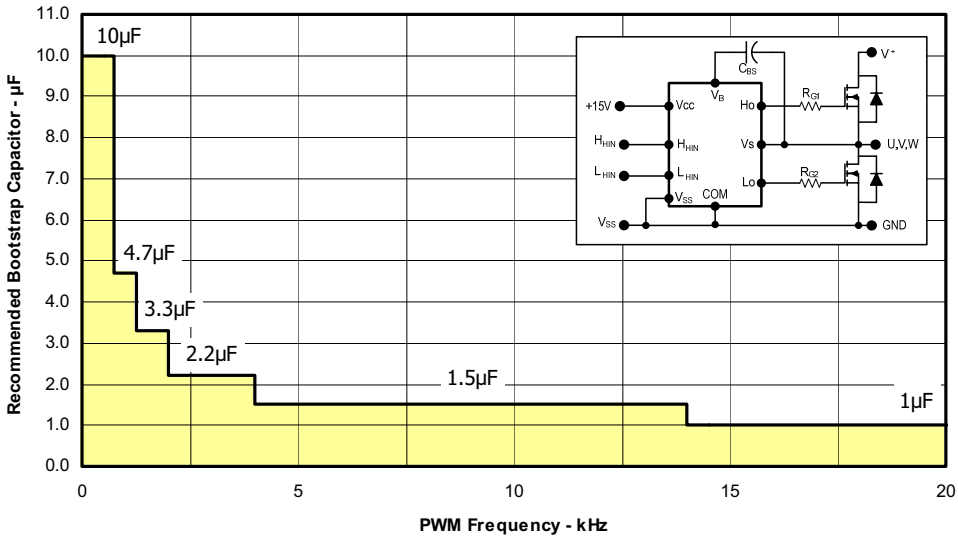


Figure 12. Recommended Bootstrap Capacitor Value vs. Switching Frequency

Figure 13. Switching Parameter Definitions

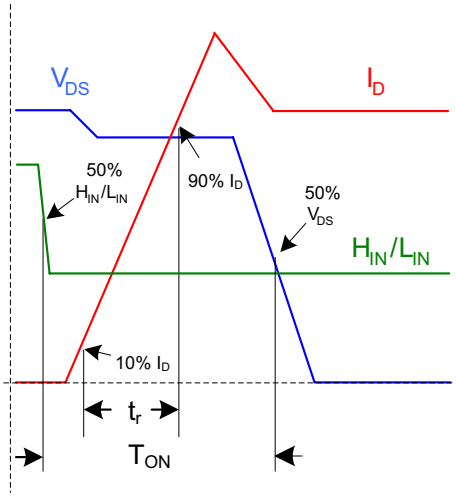


Figure 13a. Input to Output propagation turn-on delay time.

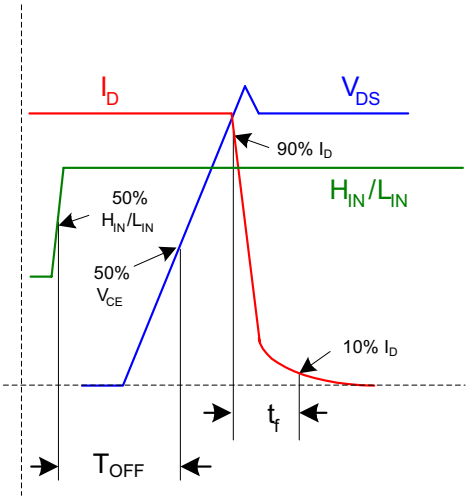


Figure 13b. Input to Output propagation turn-off delay time.

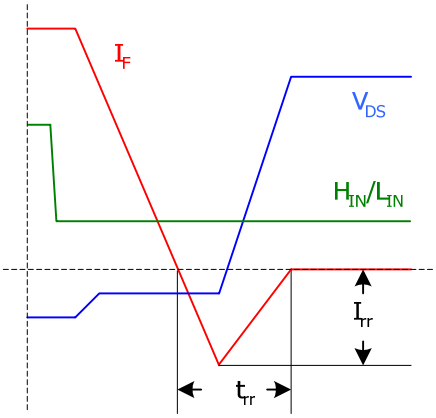
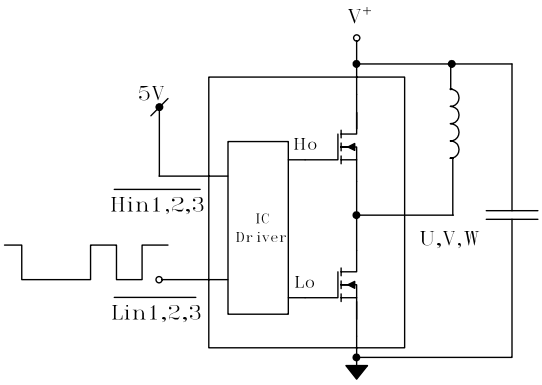


Figure 13c. Diode Reverse Recovery.



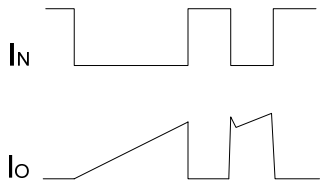
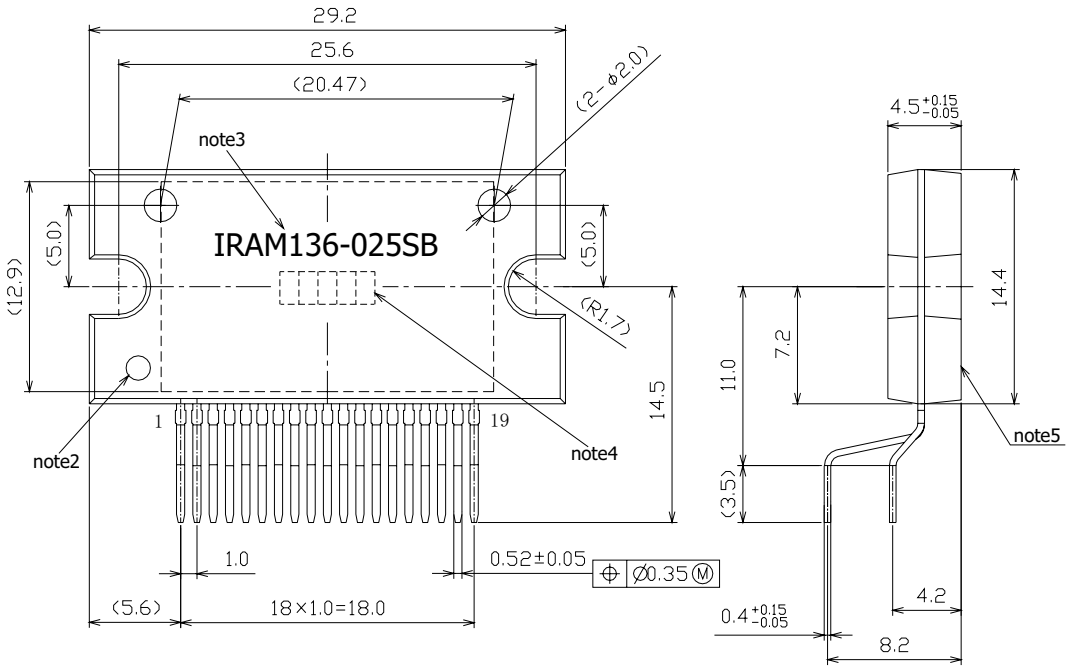
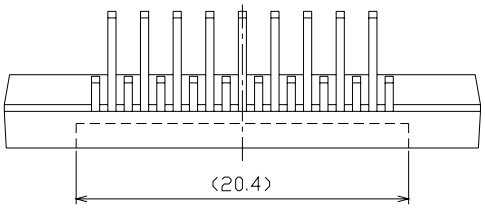


Figure CT1. Switching Loss Circuit

Package Outline IRAM336-025SB





note1: Unit Tolerance is ±0.4mm,
Unless Otherwise Specified.
note2: Mirror Surface Mark indicates Pin1 Identification.
note3: Characters Font in this drawing differs from Font shown on Module.
note4: Lot Code Marking.
Characters Font in this drawing differs from Font shown on Module.
note5: Non-Isolated Back Side.

Data and Specifications are subject to change without notice.
For mounting instruction see AN-1049.

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