CS4360

24-Bit, 192 kHz 6 Channel D/A Converter

Features

- 24-Bit Conversion
- 102 dB Dynamic Range
- -91 dB THD+N
- Low Clock Jitter Sensitivity
- Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- ATAPI Mixing
- Logic Levels between 5.0 V and 1.8 V
- +3.3 V or +5 V Analog Power Supply
- 116 mW with 3.3 V Supply
- Popguard Technology® for Control of Clicks and Pops

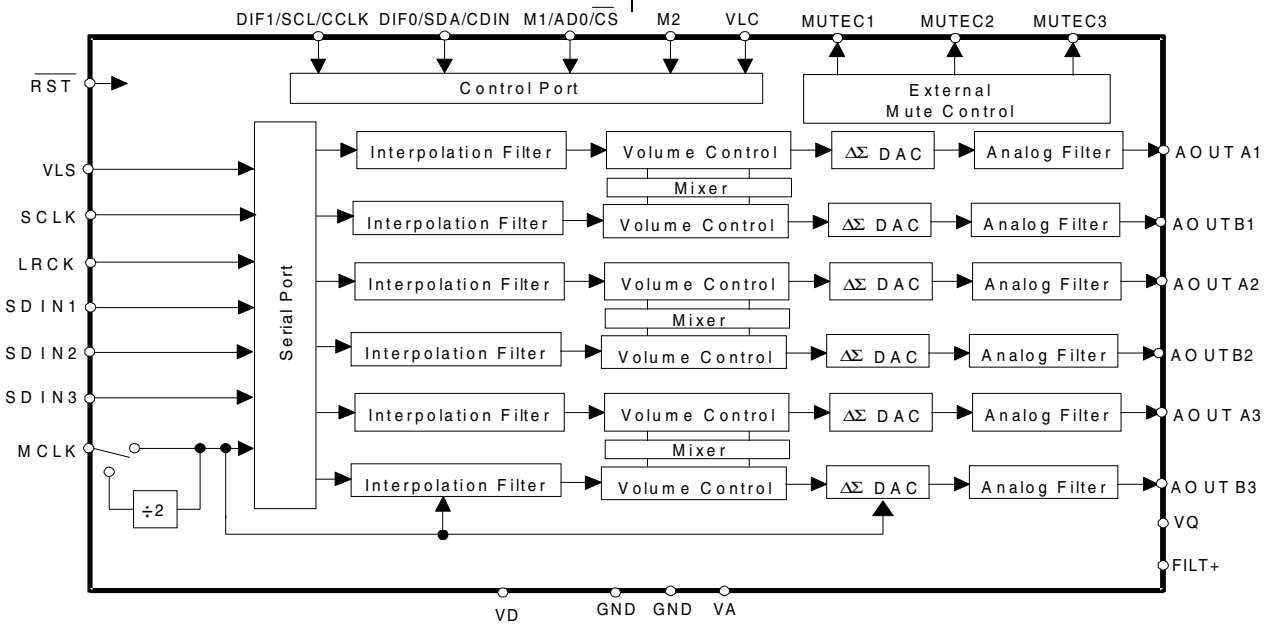
Description

The CS4360 is a complete 6-channel digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4360 accepts data at audio sample rates from 4 kHz to 20 0kHz, consumes very little power and operates over a wide power supply range. These features are ideal for cost-sensitive, multi-channel audio systems including DVD players, A/V receivers, set-top boxes, digital TVs and VCRs, mini-component systems, and mixing consoles.

ORDERING INFORMATION

CS4360-KZ	-10 to 70 °C	28-pin TSSOP
CS4360-DZ	-40 to 85 °C	28-pin TSSOP
CDB4360		Evaluation Board



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com/**

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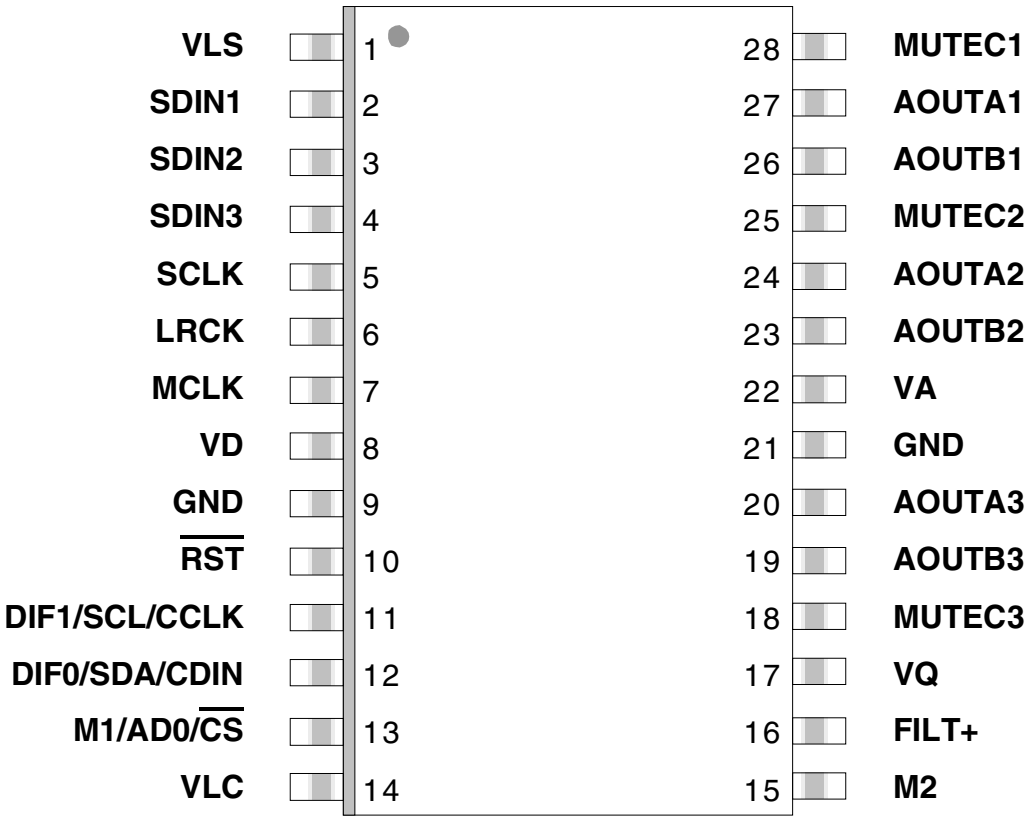
1. PIN DESCRIPTION



Pin Name	#	Pin Description
VLS	1	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface.
SDIN1 **SDIN2** **SDIN3**	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	5	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	6	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	8	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	9 21	**Ground** (*Input*)
$\overline{\text{RST}}$	10	**Reset** (*Input*) - Powers down device and resets all internal resisters to their default settings.
VLC	14	**Control Port Interface Power** (*Input*) **-** Positive power for the control port interface.
FILT+	16	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VA	22	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
AOUTB3 **AOUTA3** **AOUTB2** **AOUTA2** **AOUTB1** **AOUTA1**	19 20 23 24 26 27	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the *Analog Characteristics and Specifications* table.
MUTEC3 **MUTEC2** **MUTEC1**	18 25 28	**Mute Control** (*Output*) - Control signal for optional mute circuit.
Control Port Definitions		
SCL/CCLK	11	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	12	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Input for SPI data.
AD0/$\overline{\text{CS}}$	13	**Address Bit / Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI mode.
Stand-Alone Definitions		
DIF1 **DIF0**	11 12	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data.
M1 **M2**	13 15	**Mode Selection** (*Input*) - Determines the operational mode of the device.

2. TYPICAL CONNECTION DIAGRAM

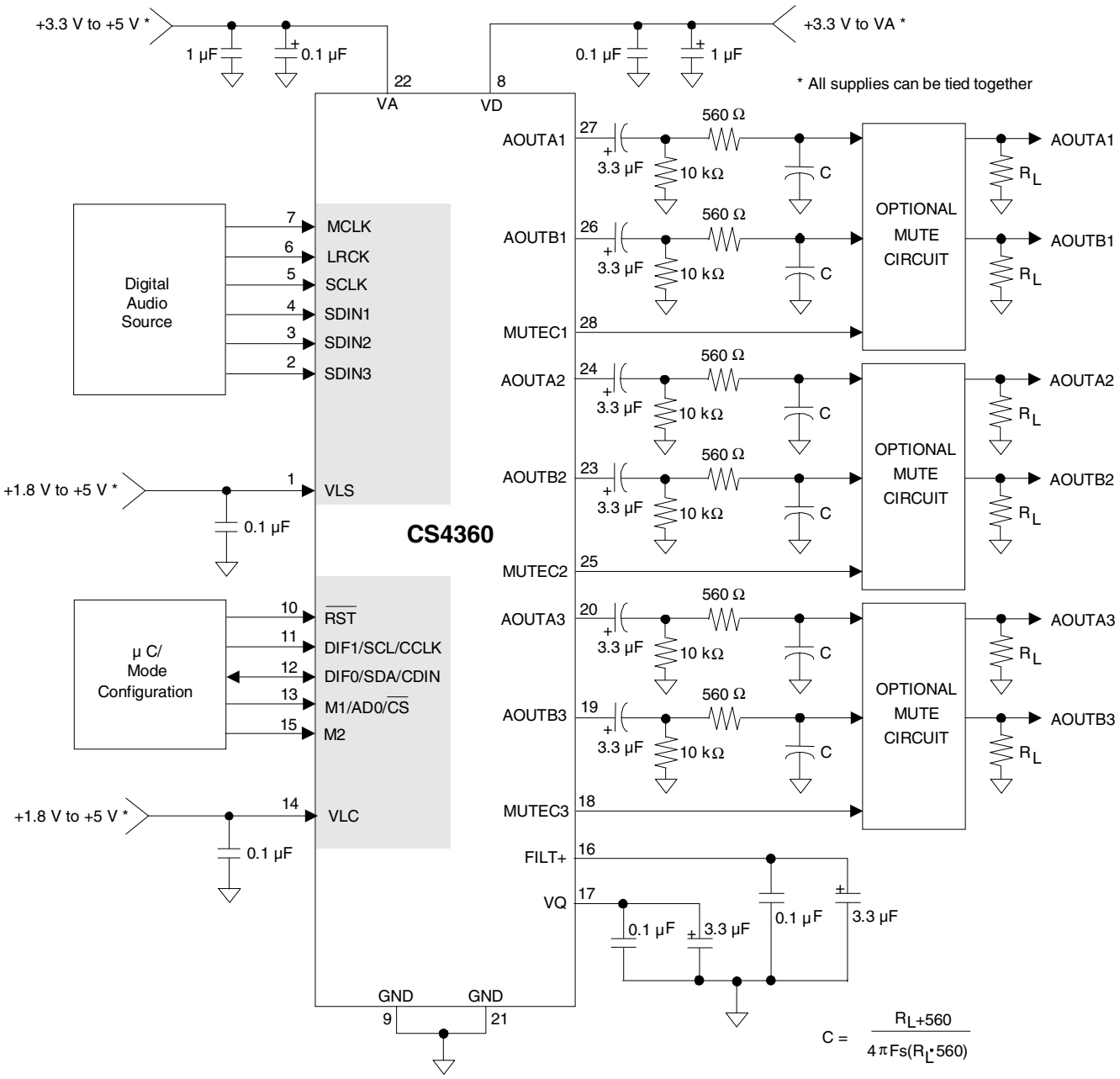


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

(Typical performance characteristics are derived from measurements taken at T_A = 25°C. Min/Max performance characteristics and specifications are guaranteed over the operating temperature and voltages.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to GND.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply						
Analog	3.3 V Nominal	VA	3.0	3.3	3.6	V
(Note 1)	5.0 V Nominal		4.5	5	5.5	V
Digital	2.5 V Nominal	VD	2.25	2.5	2.75	V
(Note 1)	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V
Serial Audio Interface	1.8 V Nominal	VLS	1.7	1.8	1.9	V
	2.5 V Nominal		2.25	2.5	2.75	V
	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V
Control Port Interface	1.8 V Nominal	VLC	1.7	1.8	1.9	V
	2.5 V Nominal		2.25	2.5	2.75	V
	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to GND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Audio Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Digital Input Voltage	Serial Audio Interface	V_{IND_S}	-0.3	VLS+0.4	V
	Control Port Interface	V_{IND_C}	-0.3	VLC+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Nominal VD supply must be less than or equal to the nominal VA supply.

2. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4360-KZ) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2). All supplies = VA = 5.0 V or 3.3 V.)

Parameter		5.0 V Min	5.0 V Typ	5.0 V Max	3.3 V Min	3.3 V Typ	3.3 V Max	Unit
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB

Notes: 3. One-half LSB of triangular PDF dither is added to data.

ANALOG CHARACTERISTICS (CS4360-KZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation	(1 kHz)		-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.60•VA	0.66•VA	0.72•VA	Vpp
Output Impedance		Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance	(Note 4)	R_L	-	3	-	kΩ
Maximum Load Capacitance	(Note 4)	C_L	-	100	-	pF

4. Refer to Figure 3.

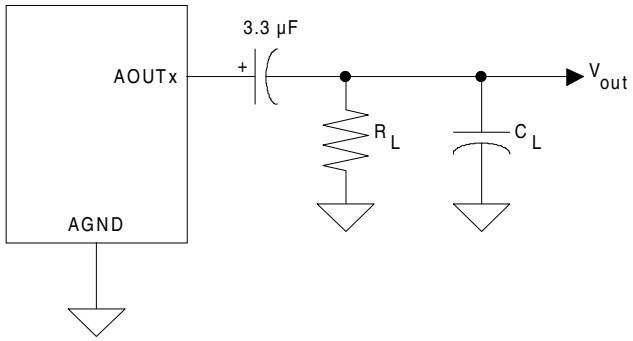


Figure 2. Output Test Load

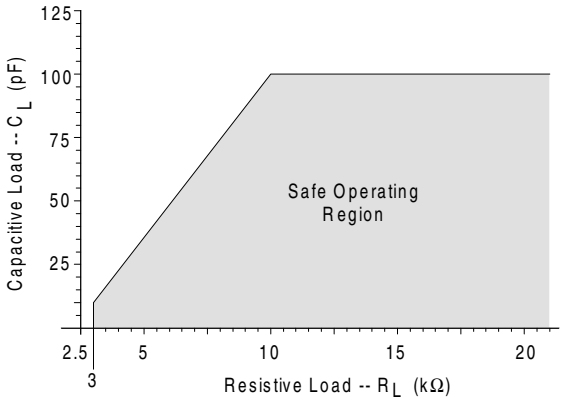


Figure 3. Maximum Loading

ANALOG CHARACTERISTICS (CS4360-DZ) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2). All supplies = VA = 5.0 V and 3.3 V.)

Parameter		VA = 5.0 V Min	VA = 5.0 V Typ	VA = 5.0 V Max	VA = 3.3 V Min	VA = 3.3 V Typ	VA = 3.3 V Max	Unit
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB

ANALOG CHARACTERISTICS (CS4360-DZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation	(1 kHz)		-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.60•VA	0.66•VA	0.72•VA	Vpp
Output Impedance		Z_{out}	-	100	-	Ω
AC-Load Resistance	(Note 4)	R_L	3	-	-	kΩ
Load Capacitance	(Note 4)	C_L	-	-	100	pF

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - (4 kHz to 50 kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.02	-	+0.035	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 5)	50	-	-	dB
Group Delay		-	9/Fs	-	s
De-emphasis Error (Relative to 1 kHz)	(Note 6)				
Control Port Mode	Fs = 32 kHz	-	-	+0.2/-0.1	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0/-0.22	dB
Stand-Alone Mode	Fs = 32 kHz	-	-	+1.5/-0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0.2/-0.4	dB
Double-Speed Mode - (50 kHz to 100 kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.1	-	0	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation	(Note 5)	55	-	-	dB
Group Delay		-	4/Fs	-	s
Quad-Speed Mode - (100 kHz to 200 kHz sample rates)					
Passband					
	to -3 dB corner	0	-	0.25	Fs
Frequency Response 10 Hz to 20 kHz		-0.7	-	0	dB
Group Delay		-	1.5/Fs	-	s

Notes: 5. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

6. De-emphasis is only available in Single-Speed Mode.

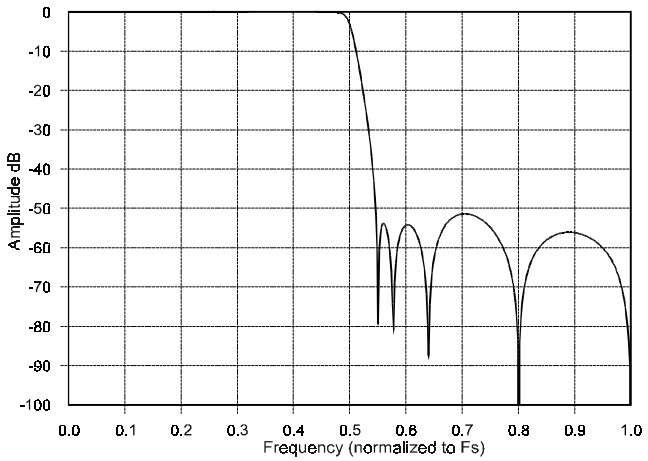


Figure 4. Single-Speed Stopband Rejection

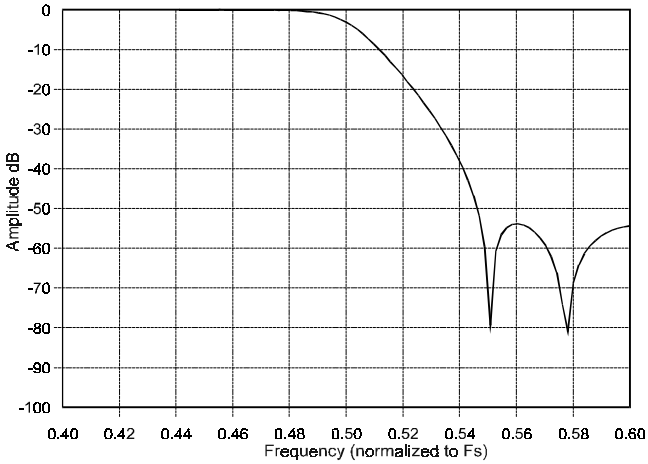


Figure 5. Single-Speed Transition Band

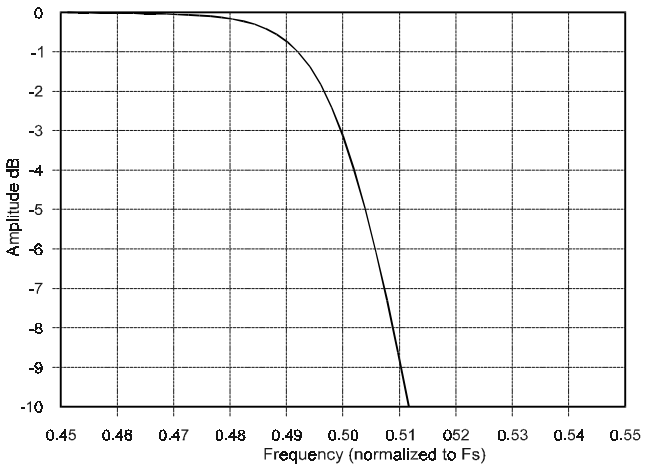


Figure 6. Single-Speed Transition Band (Detail)

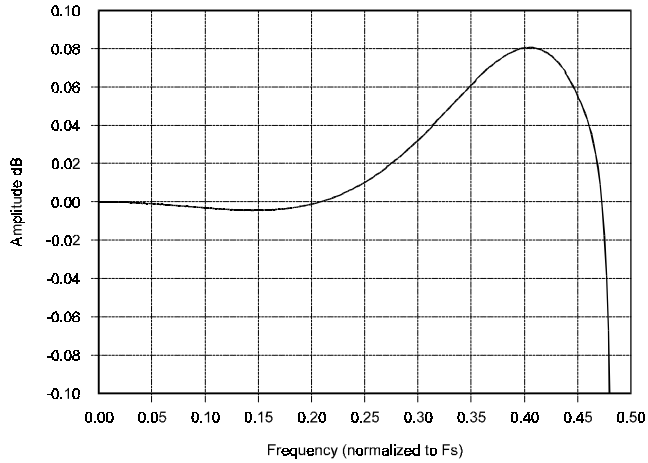


Figure 7. Single-Speed Passband Ripple

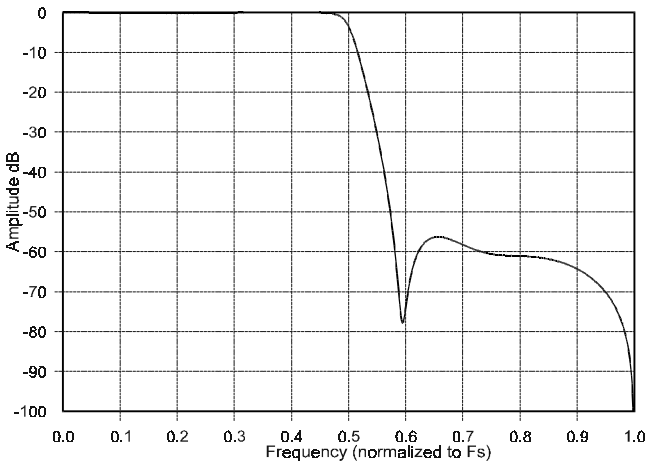


Figure 8. Double-Speed Stopband Rejection

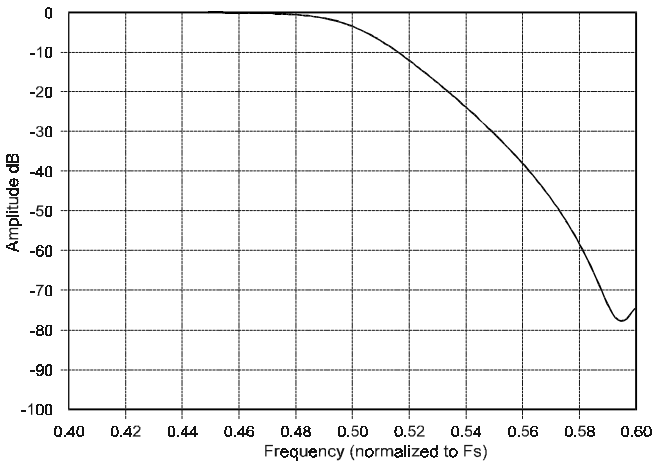


Figure 9. Double-Speed Transition Band

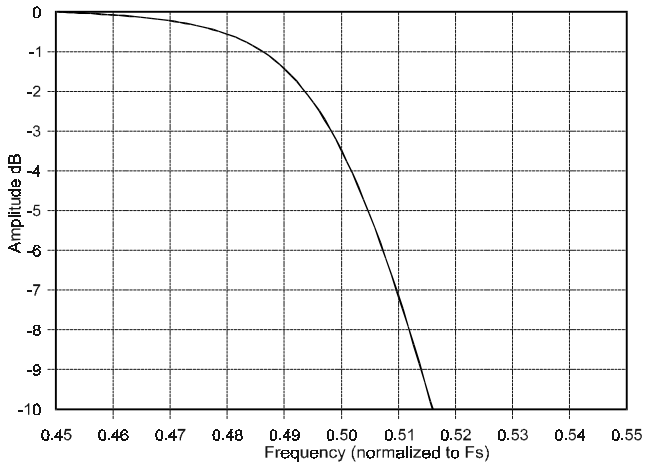


Figure 10. Double-Speed Transition Band (Detail)

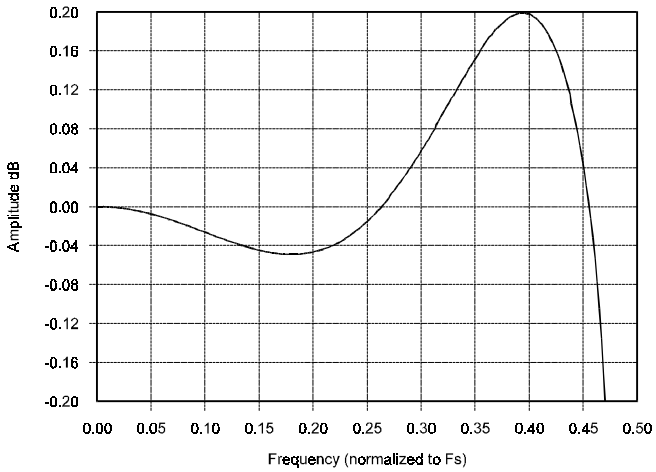


Figure 11. Double-Speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE (Inputs: Logic 0 = GND, Logic 1 = VLS.) .

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	51.2	MHz
MCLK Duty Cycle			40	60	%
Input Sample Rate	Single-Speed Mode	F_s	4	50	kHz
	Double-Speed Mode	F_s	50	100	kHz
	Quad-Speed Mode	F_s	100	200	kHz
LRCK Duty Cycle			45	55	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Frequency	Single-Speed Mode		-	128xFs	Hz
	Double-Speed Mode		-	64xFs	Hz
	Quad-Speed Mode (MCLKDIV = 0)		-	$\frac{MCLK}{2}$	Hz
	Quad-Speed Mode (MCLKDIV = 1)		-	$\frac{MCLK}{4}$	Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDINx valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDINx hold time		t_{sdh}	20	-	ns

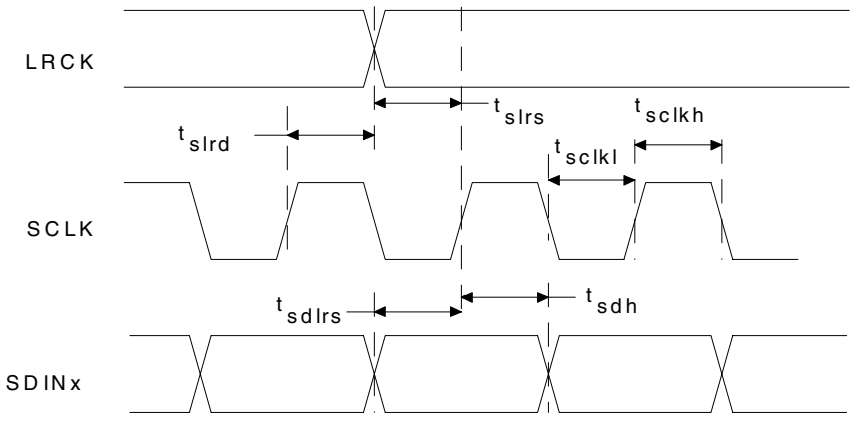


Figure 12. Serial Mode Input Timing

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (Inputs: Logic 0 = GND, Logic 1 = VLC)

Parameter		Symbol	Min	Max	Unit
I²C Mode					
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 7)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA		t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA		t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	(Note 8)	t_{ack}	-	(Note 9)	ns

Notes: 7. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

8. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

9. $\frac{5}{256 \times Fs}$ for Single-Speed Mode, $\frac{5}{128 \times Fs}$ for Double-Speed Mode, $\frac{5}{64 \times Fs}$ for Quad-Speed Mode.

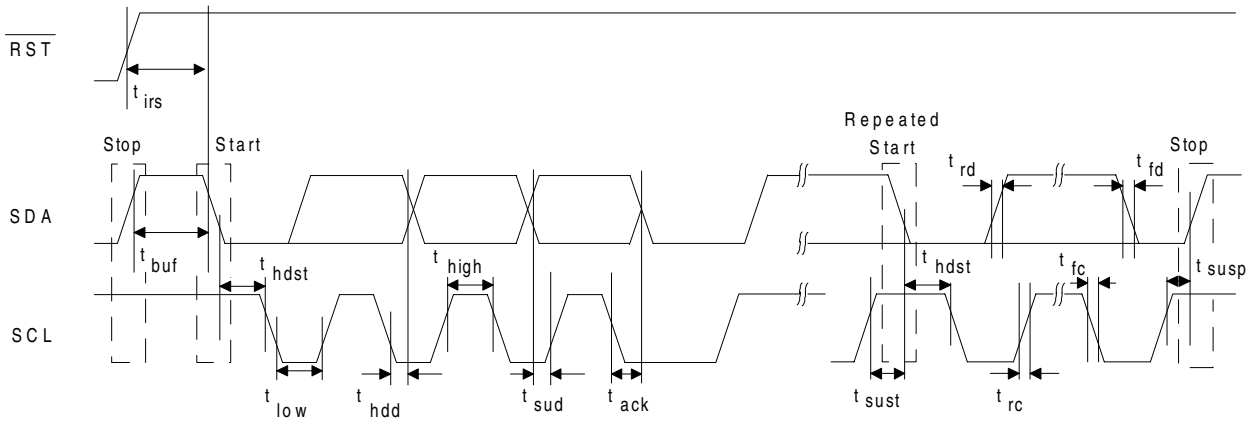


Figure 13. Control Port Timing - I²C Mode

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (Continued)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 10)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{MCLK}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{MCLK}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 11)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 12)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 12)	t_{f2}	-	100	ns

Notes: 10. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

11. Data must be held for sufficient time to bridge the transition time of CCLK.

12. For f_{sclk} < 1 MHz.

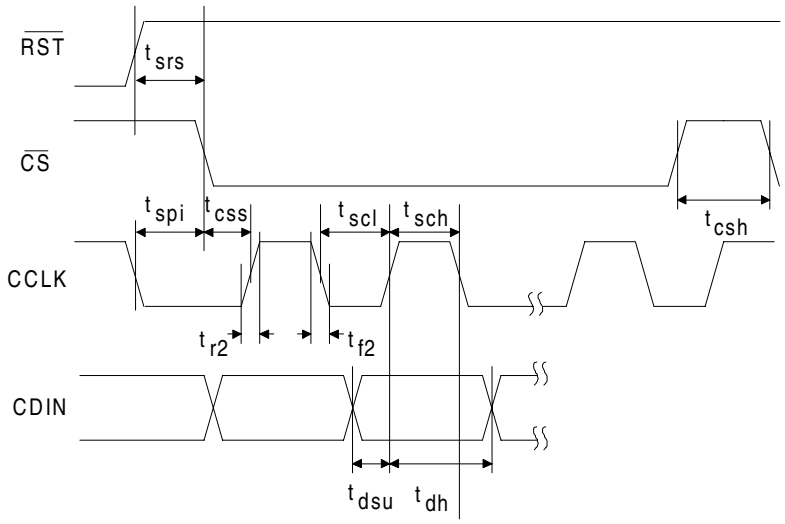


Figure 14. Control Port Timing - SPI Mode

DC ELECTRICAL CHARACTERISTICS (GND = 0 V; all voltages with respect to GND.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 13)						
Power Supply Current	VA = 5.0 V	I_A	-	22	-	mA
	VD = 5.0 V	I_D	-	25	-	mA
	VA = 3.3 V	I_A	-	21	-	mA
	VD = 3.3 V	I_D	-	14	-	mA
	VLS = 5.0 V	I_{LS}	-	6	-	µA
	VLC = 5.0 V	I_{LC}	-	2	-	µA
	VLS = 3.3 V	I_{LS}	-	2	-	µA
	VLC = 3.3 V (Note 14)	I_{LC}	-	1	-	µA
Power Dissipation	All Supplies = 5.0 V		-	235	265	mW
	All Supplies = 3.3 V		-	116	128	mW
Power-down Mode (Note 15)						
Power Supply Current	All Supplies = 5.0 V		-	16	-	µA
	All Supplies = 3.3 V		-	12	-	µA
Power Dissipation	All Supplies = 5.0 V		-	80	-	µW
	All Supplies = 3.3 V		-	40	-	µW
All Modes of Operation						
Power Supply Rejection Ratio (Note 16)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 13. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input sampled at the highest F_s for each speed mode, and open outputs, unless otherwise specified.

14. I_{LC} measured with no external loading on pin 12 (SDA).

15. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

16. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

DIGITAL INPUT CHARACTERISTICS (GND = 0 V; all voltages with respect to GND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

DIGITAL INTERFACE SPECIFICATIONS (GND = 0 V; all voltages with respect to GND.)

Parameters		Symbol	Min	Max	Units
1.8 V Logic					
High-Level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-Level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
2.5 V Logic					
High-Level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-Level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
3.3 V Logic					
High-Level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-Level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
5.0 V Logic					
High-Level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-Level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance	TSSOP (-KZ & -DZ)	θ_{JA}	-	40	-	°C/Watt
Ambient Operating Temperature (Power Applied)	-KZ	T_A	-10	-	+70	°C
	-DZ		-40	-	+85	°C

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode Select

4.1.1 Stand-Alone Mode

The device operates in one of four operational modes determined by the Mode pins in Stand-Alone mode. Sample rates outside the specified range for each mode are not supported.

M2	M1	Input Sample Rate (F_S)	MODE
0	0	4 kHz - 50 kHz	Single-Speed (without De-emphasis)
0	1	32 kHz - 48 kHz	Single-Speed (with De-emphasis)
1	0	50 kHz - 100 kHz	Double-Speed
1	1	100 kHz - 200 kHz	Quad-Speed

Table 1. CS4360 Stand-Alone Operational Mode

4.1.2 Control Port Mode

The device operates in one of three operational modes determined by the FM bits (see section 6.1.4) in Control Port mode. Sample rates outside the specified range for each mode are not supported.

FM1	FM0	Input Sample Rate (F_S)	MODE
0	0	4 kHz - 50 kHz	Single-Speed
0	1	50 kHz - 100 kHz	Double-Speed
1	0	100 kHz - 200 kHz	Quad-Speed
1	1	Reserved	Reserved

Table 2. CS4360 Control Port Operational Mode

4.2 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The LRCK, defined also as the input sample rate (F_s), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 3-5.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x*
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x*
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 5. Quad-Speed Mode Standard Frequencies

*Requires MCLKDIV bit = 1 in the Mode Control 2 register (address 0Ch)

4.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats in Stand-Alone mode, as illustrated in Table 6, and 1 of 6 formats in Control Port mode, as illustrated in Table 8.

4.3.1 Stand-Alone Mode

The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see Figures 15-17.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit Data	0	16
0	1	I^2S, up to 24-bit Data	1	15
1	0	Right Justified, 16-bit Data	2	17
1	1	Right Justified, 24-bit Data	3	17

Table 6. Digital Interface Format - Stand-Alone Mode

4.3.2 Control Port Mode

The desired format is selected via the DIF2, DIF1 and DIF0 bits in the Mode Control 2 register (see section 6.1.2). For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 15-17.

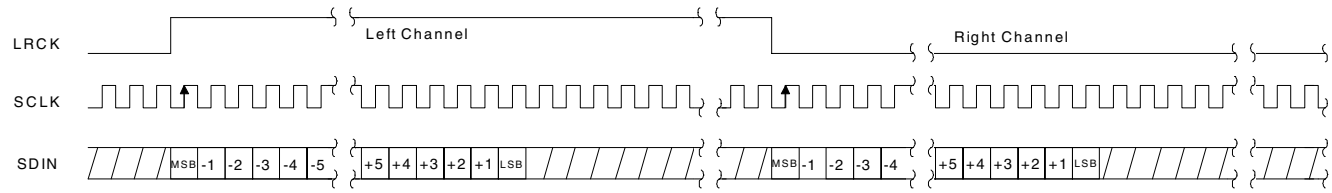


Figure 15. Left Justified up to 24-Bit Data

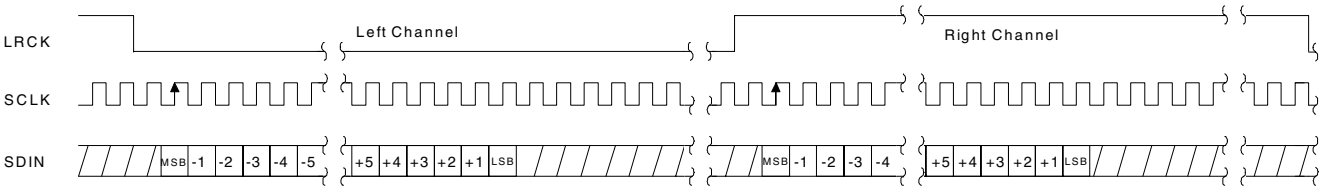


Figure 16. I²S, up to 24-Bit Data

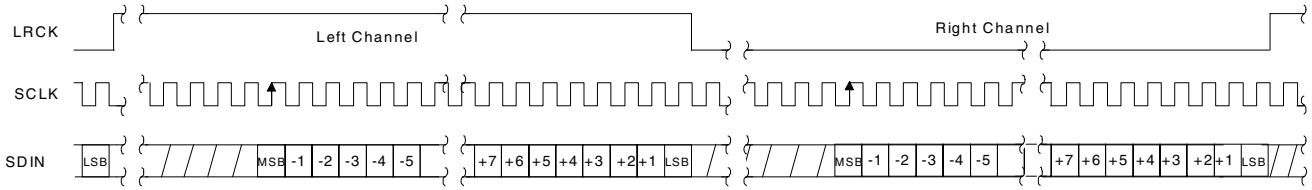


Figure 17. Right Justified Data

4.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 18 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

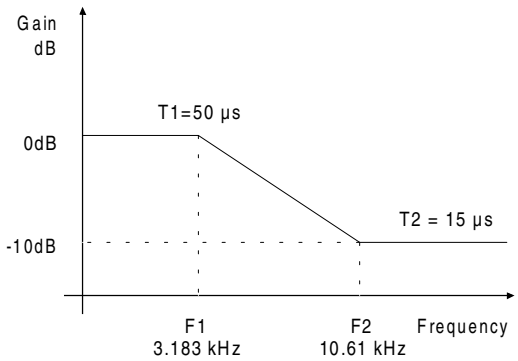


Figure 18. De-Emphasis Curve

Notes: De-emphasis is only available in Single-Speed Mode.

4.4.1 Stand-Alone Mode

The operational mode pins, M2 and M1, selects the 44.1 kHz de-emphasis filter. Please see section 4.1 for the desired de-emphasis control.

4.4.2 Control Port Mode

The Mode Control bits selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see section 6.1.3 for the desired de-emphasis control.

4.5 Recommended Power-up Sequence

4.5.1 Stand-Alone Mode

1) Hold $\overline{\text{RST}}$ low until the power supply and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in section 4.2. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the Stand-Alone power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.5.2 Control Port Mode

1) Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in section 4.2. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low.
3) Load the desired register settings while keeping the PDN bit set to 1.
4) Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximatel y 50µS when the POPG bit is set to 0. If the POPG bit is set to 1, see Section 4.6 for a complete description of power-up timing.

4.6 Popguard® Transient Control

The CS4360 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin or PDN bit is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.6.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTAx and AOUTBx, are clamped to GND. Following a delay of approximately 1000 LRCK cycles, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

4.6.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTAx and AOUTBx. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.6.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3. 3µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.7 Mute Control

The Mute Control pins go high during power-up initialization, reset, muting (see section 6.1.1 and 6.4.1), or if the MCLK to LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the CDB4360 data sheet for a suggested mute circuit.

4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4360 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA, VD, VLS and VLC connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4360 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The CDB4360 evaluation board demonstrates the optimum layout and power supply arrangements.

4.8.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin and referenced to analog ground.

4.8.2 Power Supply Sections

Each power supply pin provides power to specific sections of the CS4360. The logic voltage level for each section must adhere to the corresponding power supply voltage setting. For example: If VLC = 1.8 V; VLS = 3.3 V; VD = VA = 5 V; then the logic level for all mode configuration inputs must equal 1.8 V.

Pin #s	Description	Power Supply Reference
2, 3, 4, 5, 6, 7	Serial Audio Interface Inputs	VLS
10, 11, 12, 13, 15	Mode Configuration Inputs	VLC

Table 7. Power Supply Control Sections

4.9 Control Port Interface

The control port is used to load all the internal register settings (see section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

Notes: MCLK must be applied during all I²C communication.

4.9.1 Memory Address Pointer (MAP)

The MAP byte precedes the control port register byte during a write operation and is not available again until after a start condition is initiated. During a read operation the byte transmitted after the ACK will contain the data of the register pointed to by the MAP (see sections 4.9.1a and 4.9.3 for write/read details).

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.9.1a INCR (Auto Map Increment)

The device has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

Default = '0'
0 - Disabled
1 - Enabled

4.9.1b MAP0-3 (Memory Address Pointer)

Default = '0000'

4.9.2 I²C Mode

In the I²C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL. There is no CS pin. Pin AD0 enables the user to alter the chip address (001000[AD0][R/W]) and should be tied to VLC or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/CS pin after power-up, SPI mode will be selected.

4.9.2a I²C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 3.

1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/W bit.
2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4) If the INCR bit (see section 4.9.1a) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5) If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

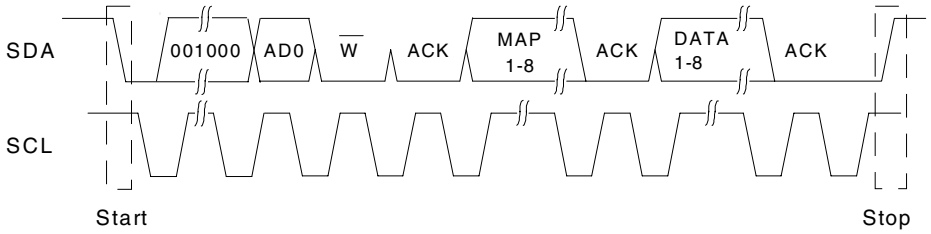


Figure 19. I²C Write

4.9.2b I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications. During this operation it is first necessary to write to the device, specifying the appropriate register through the MAP.

1) After writing to the MAP (see section 4.9.1), initiate a repeated START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2) Signal the end of the address byte by *not* issuing an acknowledge. The device will then transmit the contents of the register pointed to by the MAP. The MAP will contain the address of the last register written to the MAP.
3) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock but do not issue an ACK on the bytes clocked out of the device. After all the desired registers are read, initiate a STOP condition to the bus.
4) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further reads from other registers are desired, initiate a STOP condition to the bus.

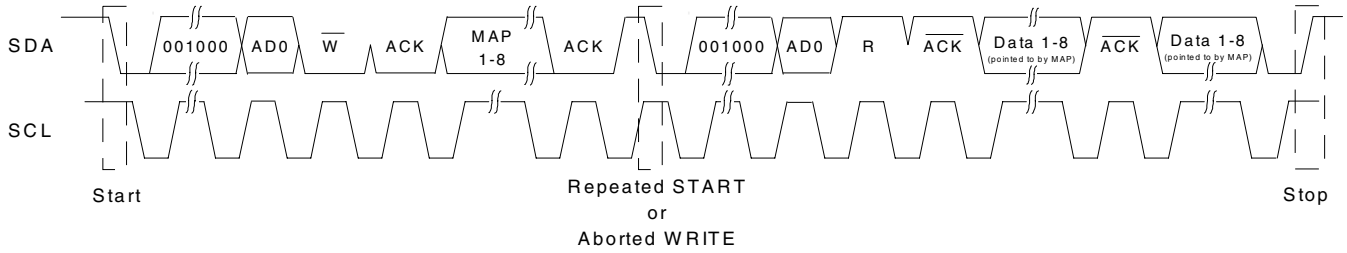


Figure 20. I²C Read

4.9.3 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 21 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.9.3a SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 3.

1) Bring $\overline{CS}$ low.
2) The address byte on the CDIN pin must then be 00100000.
3) Write to the memory address pointer, MAP. This byte points to the register to be written.
4) Write the desired data to the register pointed to by the MAP.
5) If the INCR bit (see section 4.9.1a) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.
6) If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and repeat the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.

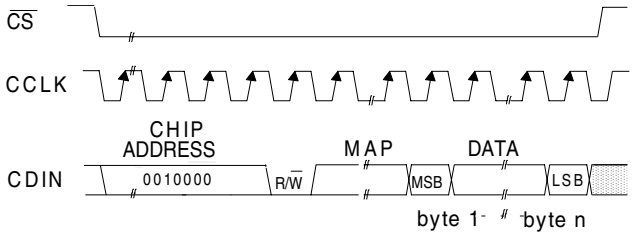


Figure 21. SPI Write

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
1h	Mode Control 1	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
	default	1	0	0	0	0	0	0	0
2h	Invert Signal	Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
3h	Mixing Control P1	Reserved	Reserved	Reserved	Reserved	P1ATAPI3	P1ATAPI2	P1ATAPI1	P1ATAPI0
	default	0	0	0	0	1	0	0	1
4h	Mixing Control P2	Reserved	Reserved	Reserved	Reserved	P2ATAPI3	P2ATAPI2	P2ATAPI1	P2ATAPI0
	default	0	0	0	0	1	0	0	1
5h	Mixing Control P3	Reserved	Reserved	Reserved	Reserved	P3ATAPI3	P3ATAPI2	P3ATAPI1	P3ATAPI0
	default	0	0	0	0	1	0	0	1
6h	Volume Control A1	A1_MUTE	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
7h	Volume Control B1	B1_MUTE	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
8h	Volume Control A2	A2_MUTE	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
9h	Volume Control B2	B2_MUTE	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
0Ah	Volume Control A3	A3_MUTE	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
0Bh	Volume Control B3	B3_MUTE	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
0Ch	Mode Control 2	SZC1	SZC0	CPEN	PDN	POPG	FREEZE	MCLKDIV	SNGLVOL
	default	1	0	0	1	1	0	0	0
0Dh	Revision Indicator	Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
	default	0	0	0	0	X	X	X	X

6. REGISTER DESCRIPTIONS

Note: All registers are read/write in I²C mode and write only in SPI, unless otherwise stated.

6.1 MODE CONTROL 1 (ADDRESS 01H)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
1	0	0	0	0	0	0	0

6.1.1 AUTO-MUTE (AMUTE) BIT 7

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Power and Muting Control register.

6.1.2 DIGITAL INTERFACE FORMAT (DIF) BIT 4-6

Default = 000 - Format 0 (Left Justified, up to 24-bit data)

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 15-17.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	15
0	0	1	I^2S, up to 24-bit data	1	16
0	1	0	Right Justified, 16-bit data	2	17
0	1	1	Right Justified, 24-bit data	3	17
1	0	0	Right Justified, 20-bit data	4	17
1	0	1	Right Justified, 18-bit data	5	17
1	1	0	Reserved	-	-
1	1	1	Reserved	-	-

Table 8. Digital Interface Formats - Control Port Mode

6.1.3 DE-EMPHASIS CONTROL (DEM) BIT 2-3

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15µs/50 µs digital de-emphasis filter response at 32, 44.1 or 4 8kHz sample rates. (See Figure 18.)

Note: De-emphasis is only available in Single-Speed Mode.

6.1.4 FUNCTIONAL MODE (FM) BIT 0-1

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Reserved

Function:

Selects the required range of input sample rates.

6.2 INVERT SIGNAL (ADDRESS 02H)

7	6	5	4	3	2	1	0
Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
0	0	0	0	0	0	0	0

6.2.1 INVERT SIGNAL POLARITY (INV_XX) BIT 0-5

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, these bits invert the signal polarity for each of their respective channels.

6.3 MIXING CONTROL PAIR 1 (CHANNELS A1 & B1) (ADDRESS 03H) MIXING CONTROL PAIR 2 (CHANNELS A2 & B2) (ADDRESS 04H) MIXING CONTROL PAIR 3 (CHANNELS A3 & B3) (ADDRESS 05H)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0
0	0	0	0	1	0	0	1

6.3.1 ATAPI CHANNEL MIXING AND MUTING (ATAPI) BIT 0-3

Default = 1001 - AOUTAx = L, AOUTBx = R (Stereo)

Function:

The CS4360 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 9 and Figure 22 for additional information.

Note: All mixing functions occur prior to the digital volume control. Mixing only occurs in channel pairs.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 9. ATAPI Decode

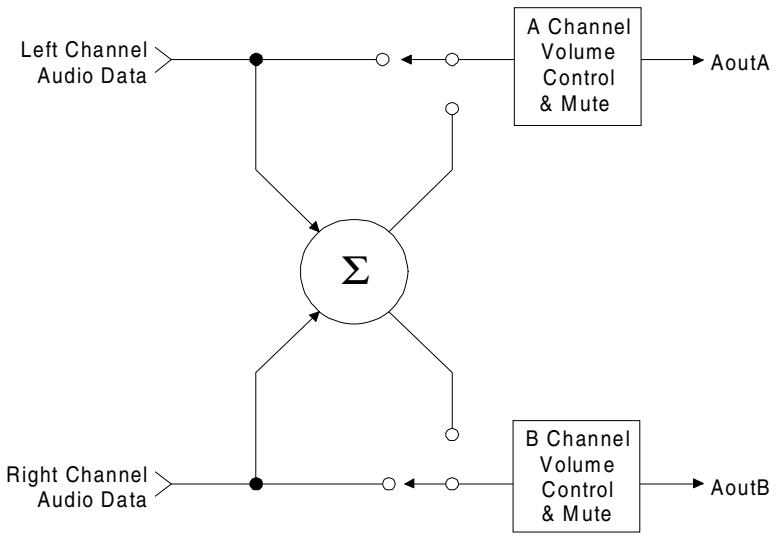


Figure 22. ATAPI Block Diagram

6.4 VOLUME CONTROL (ADDRESSES 06H - 0BH)

7	6	5	4	3	2	1	0
xx_MUTE	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

6.4.1 MUTE (MUTE) BIT 7

Default = 0
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits. The MUTEC pin will go active during the mute period if the Mute function is enabled for both channels in the pair.

6.4.2 VOLUME CONTROL (XX_VOL) BIT 0-6

Default = 0

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from 0 to -119 dB. Volume settings are decoded as shown in Table 10. The volume changes are implemented as dictated by the Soft Ramp and Zero Cross bits. All volume settings less than -119dB are equivalent to enabling the MUTE bit.

Binary Code	Decimal Value	Volume Setting
0001010	10	-10 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 10. Example Digital Volume Settings

6.5 MODE CONTROL 2 (ADDRESS 0DH)

7	6	5	4	3	2	1	0
SZC1	SZC0	CPEN	PDN	POPG	FREEZE	MCLKDIV	SNGLVOL
1	0	0	1	1	0	0	0

6.5.1 SOFT RAMP AND ZERO CROSS CONTROL (SZC) BIT 6-7

Default = 10
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp and Zero Cross

Function:

Immediate Change

When Immediate Change is selected all level changes will be implemented immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7ms t o 21.3 m s at 48kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/ 8dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Soft Ramp and Zero Cross

Soft Ramp and Zero Cross dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and will be implemented on successive signal zero crossings. The 1/8 dB level changes will occur after timeout periods between 512 and 1024 sample periods (10.7 ms to 21. 3ms at 4 8kHz sample rate) if the signal does not encounter zero crossings. The zero cross function is independently monitored and implemented for each channel.

6.5.2 CONTROL PORT ENABLE (CPEN) BIT 5

Default = 0
0 - Disabled
1 - Enabled

Function:

The Control Port will become active and reset to the default settings when this function is enabled.

6.5.3 POWER DOWN (PDN) BIT 4

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, but the contents of the control registers will be retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation in Control Port mode can occur.

6.5.4 POPGUARD® TRANSIENT CONTROL (POPG) BIT 3

Default = 1
0 - Disabled
1 - Enabled

Function:

The PopGuard® Transient Control allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-off when this function is enabled. Please see section 4.6 for implementation details.

6.5.5 FREEZE CONTROLS (FREEZE) BIT 2

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

6.5.6 MASTER CLOCK DIVIDE ENABLE (MCLKDIV) BIT 1

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

6.5.7 SINGLE VOLUME CONTROL (SNGLVOL) BIT 0

Default = 0
0 - Disabled
1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. When enabled, the volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored.

6.6 REVISION REGISTER (READ ONLY) (ADDRESS 0DH)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
0	0	0	0	X	X	X	X

6.6.1 REVISION INDICATOR (REV) [READ ONLY] BIT 0-3

Default = none
0001 - Revision A
0010 - Revision B
0011 - Revision C
etc.

Function:

This read-only register indicates the revision level of the device.

7. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

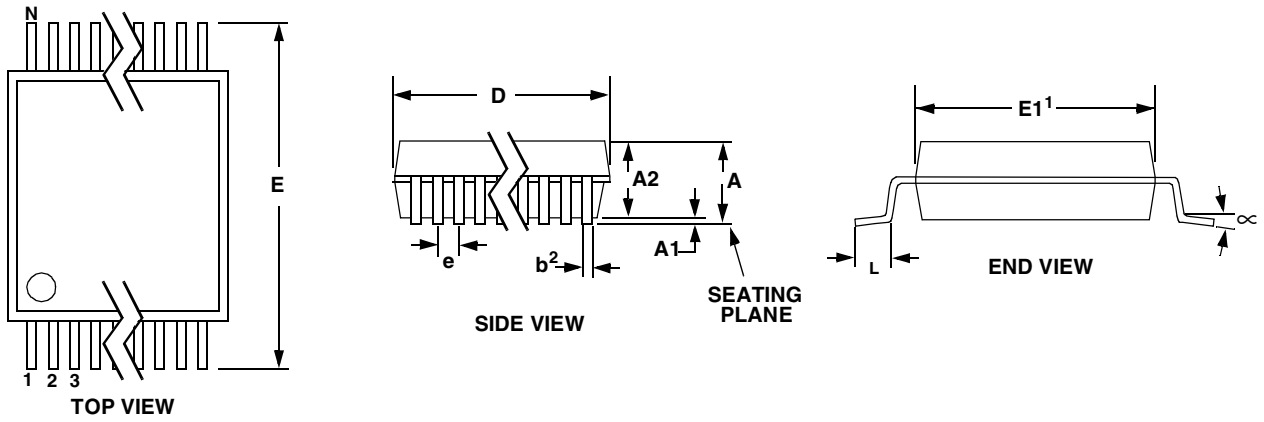
8. REFERENCES

1) CDB4360 Evaluation Board Datasheet

2) “The I²C Bus Specification: Version 2.1” Philips Semiconductors, January 2000. http://www.semiconductors.philips.com

9. PACKAGE DIMENSIONS

28L TSSOP (4. 4mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.47	--	--	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.029	0.50	0.60	0.75	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.0 7mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 a nd 0.25mm from lead tips.