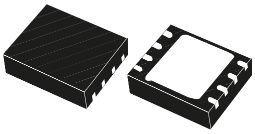
1 A ultra low-dropout regulator with reverse current protection



DFN8 (3 x 3 mm)

Maturity status link
LD59100

Features

- Input voltage range: 2.2 V to 5.5 V
- Ultra low-dropout: 200 mV typ. at 1 A
- NMOS topology
- Very high PSRR: 78 dB @ 100 Hz, 70 dB @ 100 kHz
- Very fast response to load variation
- Stable with 1 µF capacitor
- Thermal shutdown
- Current limit
- Adjustable from 1.2 V
- High output voltage accuracy: 1 % typ. (3 % max.)

Applications

- Post-regulation generic POL
- Portable equipment
- Industrial applications
- Telecom infrastructure

Description

The LD59100 is a 1 A LDO regulator designed for use in various environments. Its N-MOS topology allows reduction of the R_{dson} of the pass-element, maintaining a very low-dropout voltage even with very low input power supply voltage.

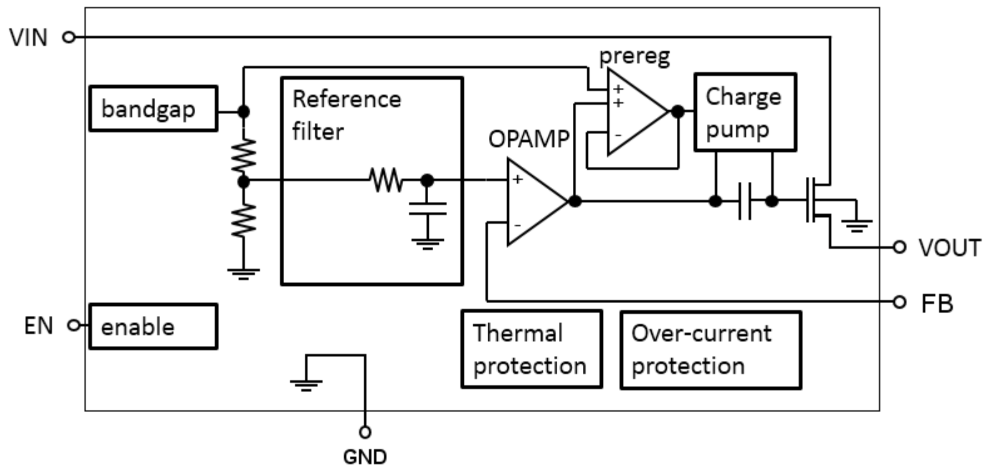
The device features very high PSRR characteristics over a wide frequency band, rendering it suitable for use as a secondary regulator for noise-sensitive applications.

The enable function can be used to further decrease the overall current consumption in shutdown mode.

The LD59100 embeds protection features, such as current limit, thermal shutdown and reverse output current protection.

1 Diagram

Figure 1. **Block diagram, adjustable version**



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2 Pin configuration

Figure 2. Pin connection (top view)

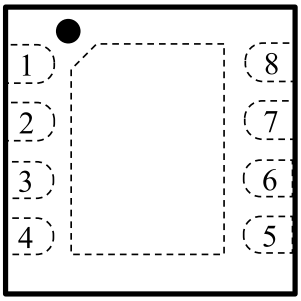

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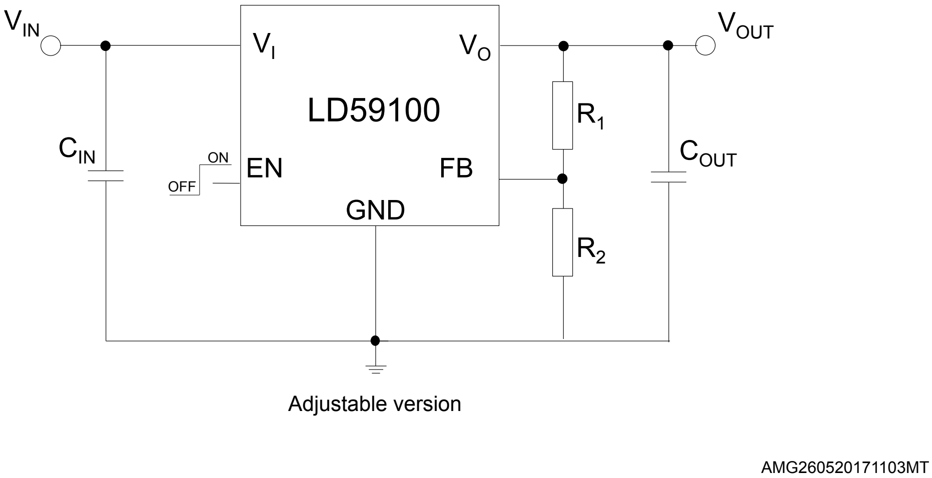
Table 1. Adjustable version: pin description

Pin DFN8-3x3	Symbol	Function
1	OUT	Regulated output voltage of the LDO
3	FB	Feedback to set the output voltage
4	GND	Ground
5	EN	Enable pin logic input: Low = shutdown, High = active
2, 6, 7	NC	Not connected
8	IN	Input pin
Tab	EXP	Exposed pad. Connect to GND on PCB.

3 Typical application

Figure 3. Typical application circuit for adjustable version



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 6	V
V_{OUT}	DC output voltage	- 0.3 to 5.5	V
V_{EN}	Enable input voltage	- 0.3 to 6	V
V_{FB}	Feedback pin voltage	- 0.3 to 6	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{ST}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	DFN8-3x3	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	10	°C/W

Table 4. Electrostatic discharge

Symbol	Parameter	DFN8-3x3	Unit
HBM	Human body model	+/-2	kV
CDM	Charged device model	+/-500	V

5 Electrical characteristics

$T_A = T_J$ = -40 °C to +125 °C, typical values refer to T_A = +25 °C, V_{EN} = 2.2 V, $V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 1 µF, unless otherwise specified (see note 1).

Table 5. Electrical characteristics for LD59100 adjustable

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.2		5.5	V
I_{OUT}	Guaranteed output current		0		1	A
V_{OUT}	Output voltage range		V_{FB}		5.5 - V_{DROP}	
	V_{OUT} accuracy	Nominal	-1		1	%
		$V_{IN} = V_{OUT(NOM)}$ + 0.5 V to 5.5 V	-3		3	%
		I_{OUT} = 0 mA to 1 A				
V_{FB}	Internal reference		1.192	1.204	1.216	V
I_{FB}	Adjustable pin leakage current			0.1	0.6	µA
ΔV_{OUT}	Static line regulation	$V_{IN} = V_{OUT(NOM)}$ + 0.5 V to 5.5 V		0.005		%/V
		I_{OUT} = 10 mA				
ΔV_{OUT}	Static load regulation	I_{OUT} = 1 mA to 1 A		0.0001		%/mA
V_{DROP}	Dropout voltage	I_{OUT} = 1 A, V_{OUT} > 2.4 V		200	500	mV
		$V_{IN} = V_{OUT(NOM)}$ - 0.1 V				
eN	Output noise voltage(1)	f = 10 Hz to 100 kHz, I_{OUT} = 10 mA C_{OUT} = 10 µF		27 x V_{OUT}		μV_{RMS}
SVR	Supply voltage rejection (2)	$V_{IN} = V_{OUT(NOM)}$ + 1 V+/-V_{RIPPLE} V_{RIPPLE} = 0.5 V, I_{OUT} = 10 mA f = 100 Hz		78		dB
		$V_{IN} = V_{OUT(NOM)}$ + 1 V+/-V_{RIPPLE} V_{RIPPLE} = 0.5 V, I_{OUT} = 10 mA f = 10 Hz		62		
		$V_{IN} = V_{OUT(NOM)}$ + 1 V+/-V_{RIPPLE} V_{RIPPLE} = 0.5 V, I_{OUT} = 10 mA f = 100 Hz		70		
		$V_{IN} = V_{OUT(NOM)}$ + 1 V+/-V_{RIPPLE} V_{RIPPLE} = 0.5 V, I_{OUT} = 1 A f = 100 Hz		58		
		$V_{IN} = V_{OUT(NOM)}$ + 1 V+/-V_{RIPPLE} V_{RIPPLE} = 0.5 V, I_{OUT} = 1 A f = 10 Hz		37		

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	I_{OUT} = 0 mA		130		µA
		I_{OUT} = 10 mA		140		
		I_{OUT} = 1 A		280		
		V_{IN} Input current in OFF mode V_{EN} = GND		0.02		
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current	R_L = 0		450		mA
I_{REV}	Reverse leakage current	V_{EN} < 0.5 V, 0 < V_{IN} < V_{OUT}		0.1		µA
V_{EN}	Enable input logic low				0.5	V
	Enable input logic high		1.7			
I_{EN}	Enable pin input current	V_{EN} = V_{IN} = 5.5 V		20		nA
T_{SHDN}	Thermal shutdown (2)			160		°C
	Hysteresis (2)			20		
T_{STR}	Start-up time	V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF		600		µs

1. *Values at below 0 °C are guaranteed by design and/or characterization tested at T_A = ~ T_J. Low duty cycle pulse techniques are used.*
2. *Guaranteed by design, not tested in production.*

6 Application information

6.1 Output voltage setting for adjustable version

In the adjustable version, the output voltage can be set from 1.204 V (V_{FB}) up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the FB pin and the output, thereby implementing remote voltage sensing. With reference to the typical circuit shown in Figure 4. Line regulation vs. temperature (V_{IN} = 2.5 to 5.5 V, V_{OUT} = V_{FB}, I_{OUT} = 10 mA), the resistor divider can be designed by using the following equation:

Equation 1

$$V_{OUT} = V_{FB}\left(1 + R_1/R_2\right), \, with \, V_{FB} = 1.204 \, V \, typ. \quad (1)$$

It is recommended to use resistors with values in the range of 10 kΩ to 100 kΩ. Lower values can also be suitable, but will result in an increase in current consumption.

The following table shows an example of R_1, R_2 choices, among standard 1% resistors, to obtain the most common output voltages.

Table 6. Resistor divider settings for common output voltages

V_{OUT}	R_1	R_2
1.204 (V_{FB})	Short	Open
1.5	23.2 kΩ	95.3 kΩ
1.8	28.0 kΩ	56.2 kΩ
2.5	39.2 kΩ	36.5 kΩ
2.8	44.2 kΩ	33.2 kΩ
3	46.4 kΩ	30.9 kΩ
3.3	52.3 kΩ	30.1 kΩ

6.2 Input and output capacitors

Input capacitor

An input capacitor with a minimum value of 1 µF must be located as close as possible to the input pin of the device and returned to a clean analog ground. A good quality, low-ESR ceramic capacitor is recommended. This capacitor helps to ensure stability of the control loop, reduces the effects of inductive sources and improves ripple rejection. A capacitance value larger than 1 µF can be used in the case of fast load transients in the application.

Output capacitor

The LD59100 requires a capacitor connected to its output, to keep the control loop stable and reduce the risk of ringing and oscillations. The control loop is designed to be stable with any good quality ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 µF and equivalent series resistance in the 5 mΩ to 1 Ω range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region. There is no maximum limit to the output capacitance, provided that the above conditions are respected.

7 Typical characteristics

$C_{IN} = C_{OUT} = 1\ \mu F$, $V_{EN} = V_{IN} = 2.5\ V$, $V_{OUT} = V_{FB}$, $T_J = 25\ °C$, unless otherwise specified.

Figure 4. **Line regulation vs. temperature (V_{IN} = 2.5 to 5.5 V, $V_{OUT} = V_{FB}$, I_{OUT} = 10 mA)**

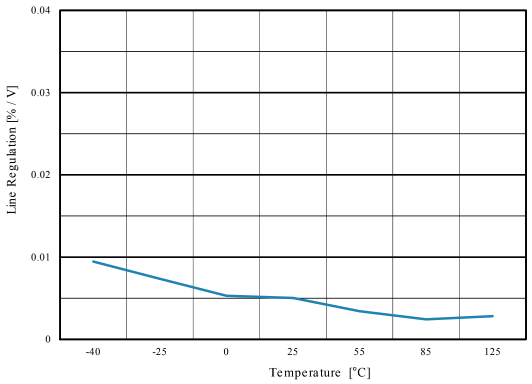


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Figure 5. **Load regulation vs. temperature (V_{IN} = 2.5 V, $V_{OUT} = V_{FB}$)**

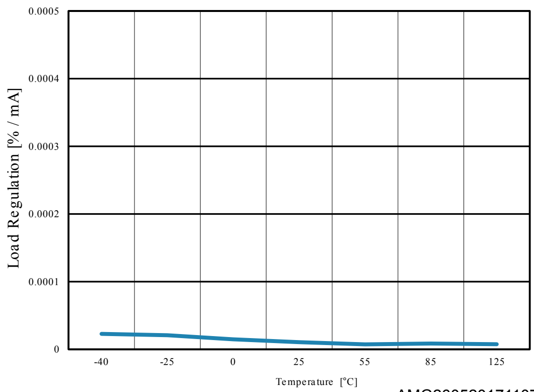

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Figure 6. **Reference voltage vs. temperature**

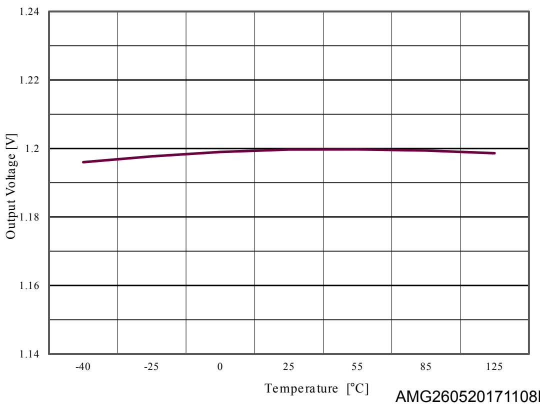

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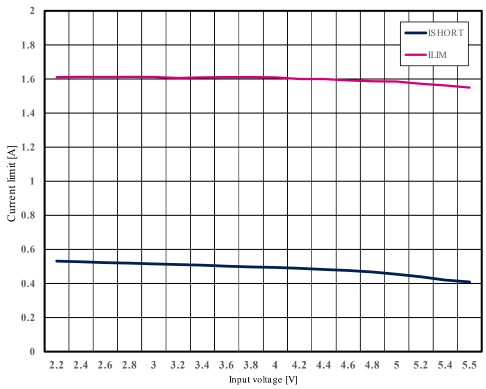
Figure 7. **Current limit vs. input voltage**



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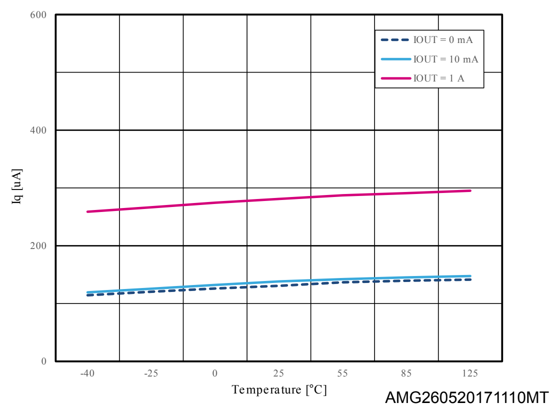


Figure 8. Quiescent current vs. temperature (V_{IN} = 2.2 V)

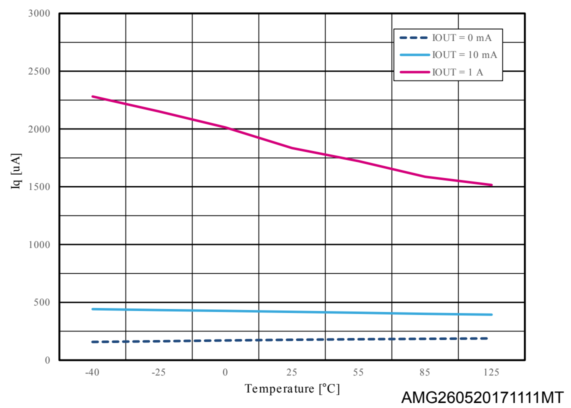


Figure 9. Quiescent current vs. temperature (V_{IN} = 5.5 V)

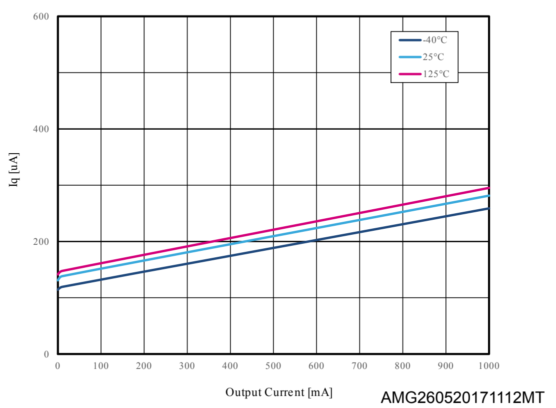


Figure 10. Quiescent current vs. output current

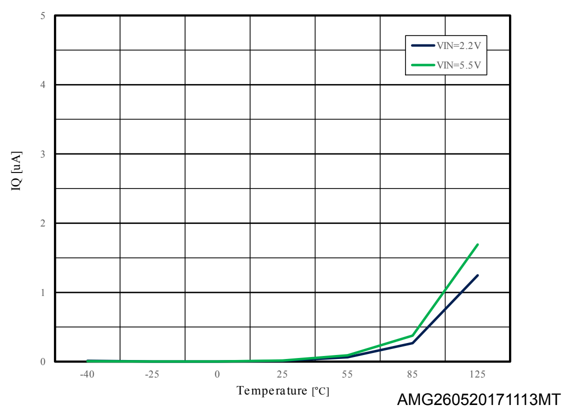


Figure 11. Off-state current vs. temperature

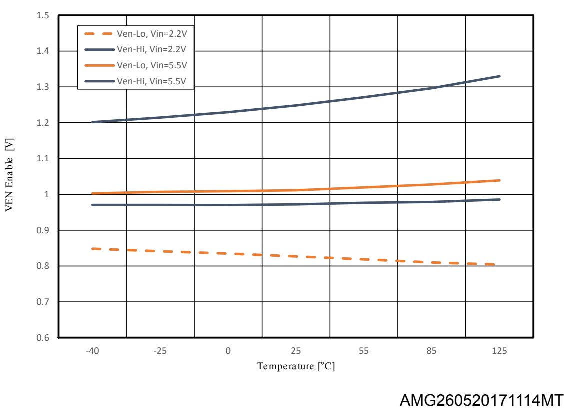


Figure 12. Enable thresholds vs. temperature

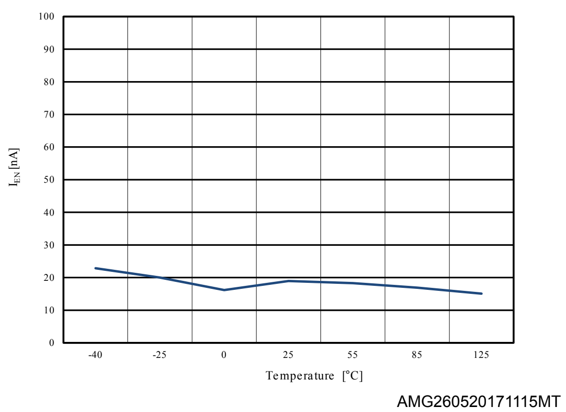


Figure 13. Enable pin current vs. temperature

Figure 14. **Feedback pin current vs. temperature**

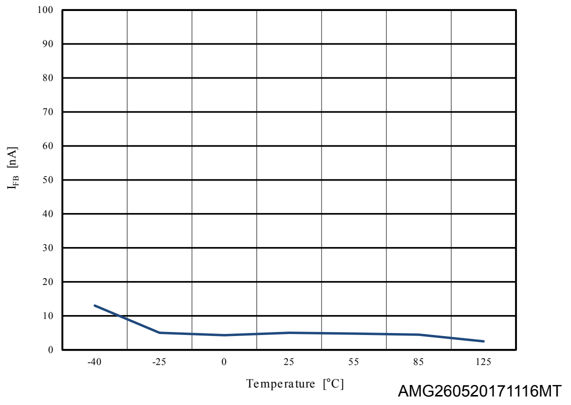


Figure 15. **Reverse current vs. temperature**

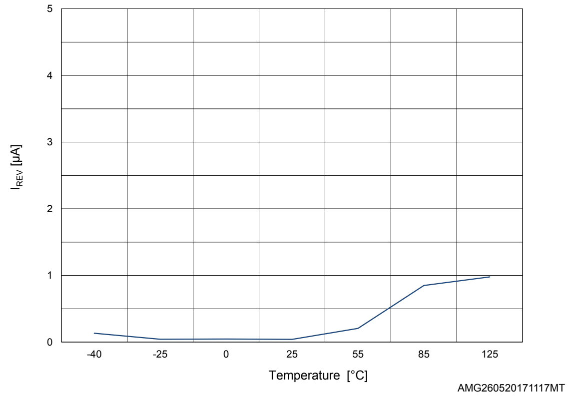


Figure 16. **Dropout voltage vs. temperature**

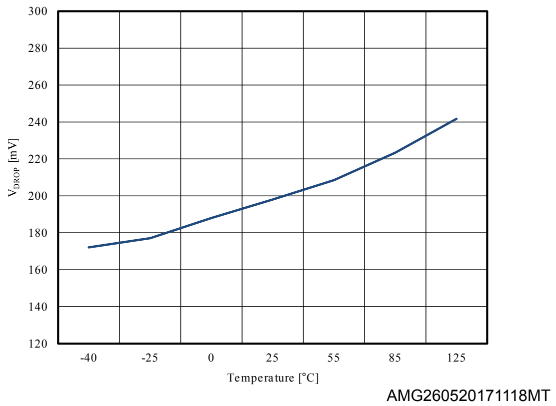


Figure 17. **Dropout voltage vs. output current**

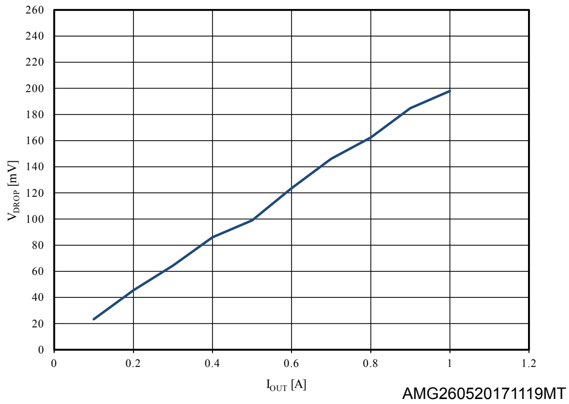


Figure 18. **Dropout voltage vs. input voltage**

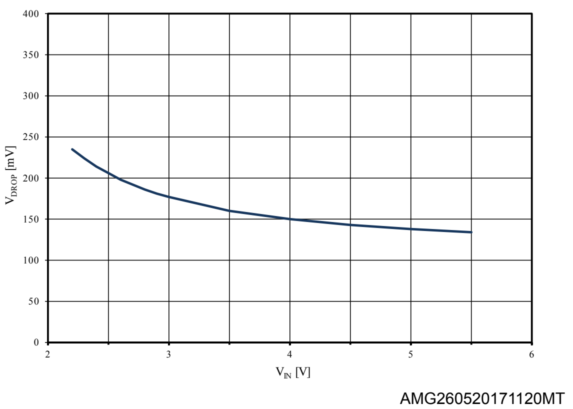


Figure 19. **R_{MS} noise vs. C_{FB}**

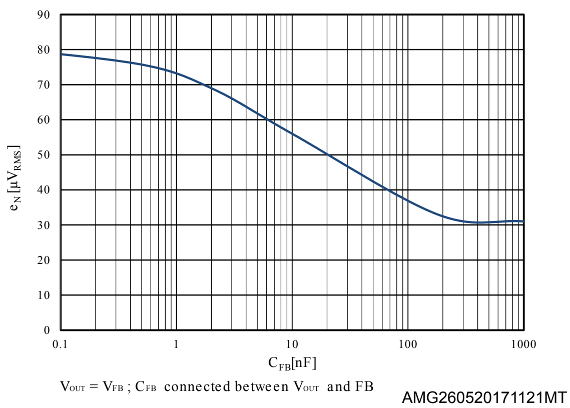
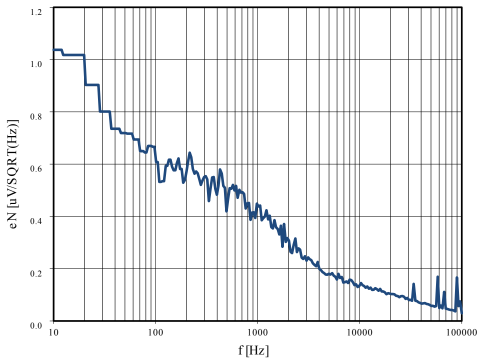


Figure 20. Noise spectral density



$V_{OUT} = V_{FB}$; $C_{OUT} = 10 \mu F$

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Figure 21. P_{SRR} vs. frequency

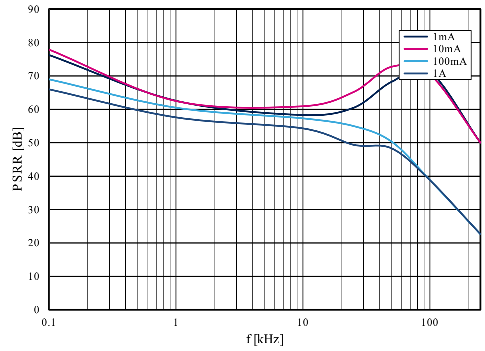

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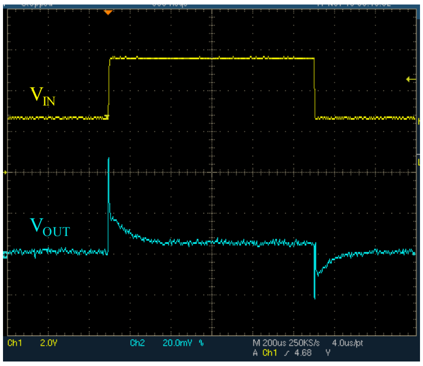
Figure 22. Line transient



V_{IN} from 2.5V to 5.5V, I_{OUT}=10mA, t_r=t_f=5µs, C_{IN}=C_{OUT}=1µF

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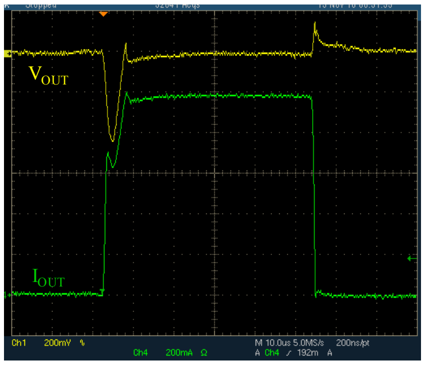
Figure 23. Load transient



V_{IN}=V_{OUT}+1V, I_{OUT} from 10mA to 1A, t_r=t_f=5µs, C_{IN}=C_{OUT}=1µF

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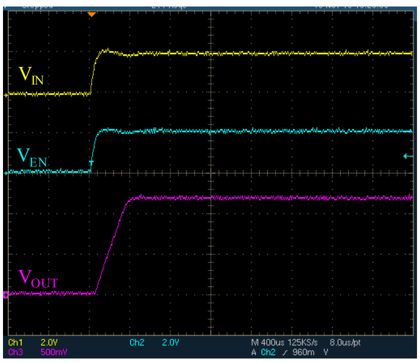
Figure 24. Startup waveform



V_{IN} = V_{EN} from 0 to 2.5V, I_{OUT}=10mA, t_r=5µs, C_{IN}=C_{OUT}=1µF

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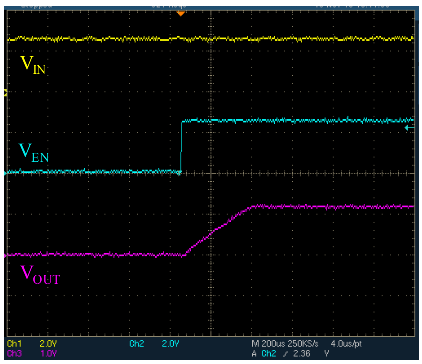
Figure 25. Enable transient



V_{IN} = 2.5V, V_{EN} from 0 to 2.5V, I_{OUT}=10mA, t_r=5µs, C_{IN}=C_{OUT}=1µF

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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN8 (3 x 3 mm) package information

Figure 26. DFN8 (3 x 3 mm) package outline

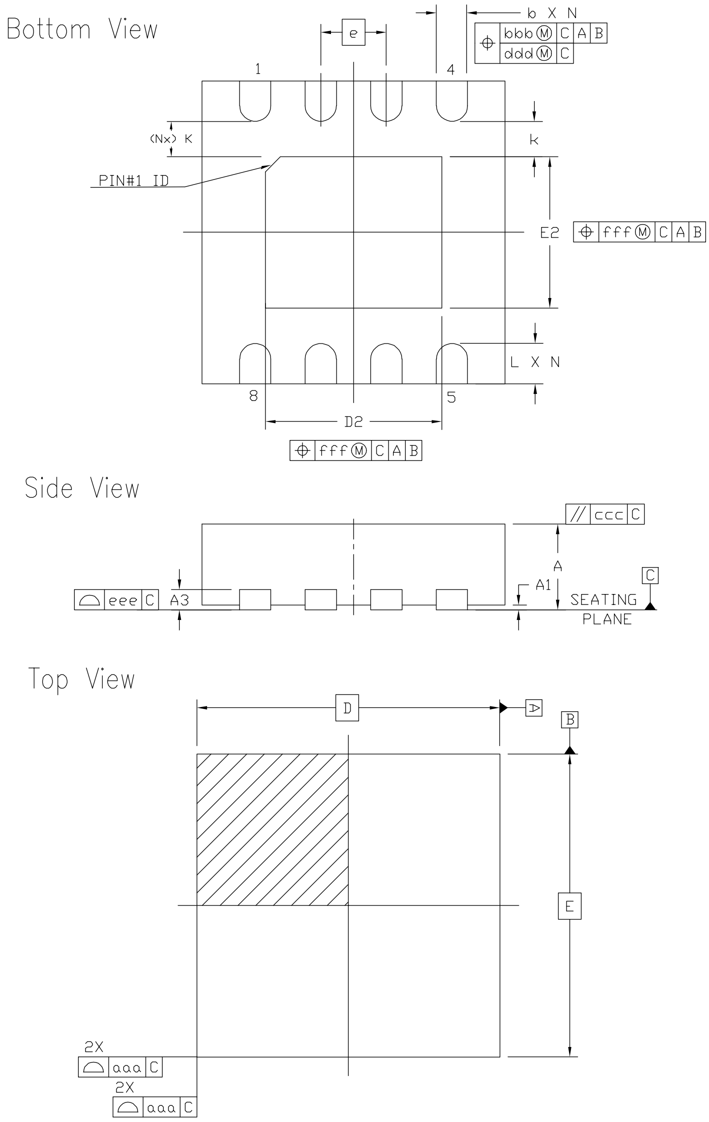
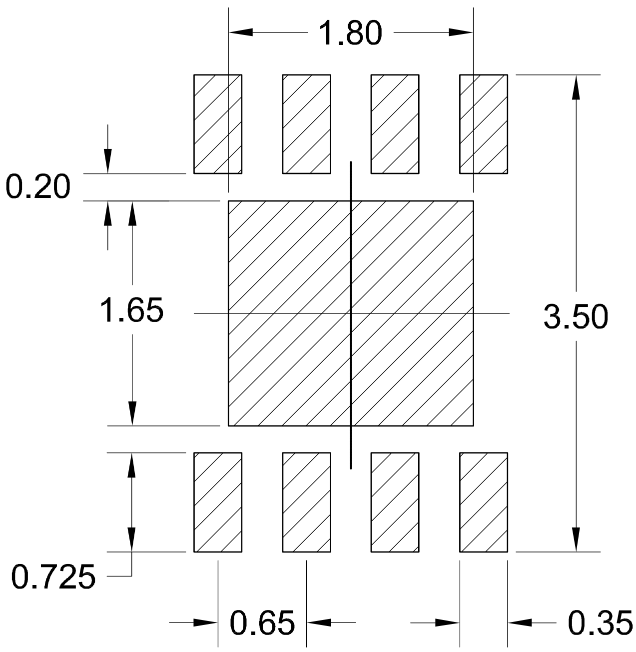


Table 7. **DFN8 (3 x 3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3		0.20 REF.	
b	0.28	0.31	0.34
D		3.00 BSC	
D2	1.70	1.75	1.80
e		0.65 BSC	
E		3.00 BSC	
E2	1.45	1.50	1.55
L	0.35	0.40	0.45
k	0.20		
N	8		

Figure 27. **DFN8 (3 x 3 mm) recommended footprint**



8.2 DFN8 (3 x 3 mm) packing information

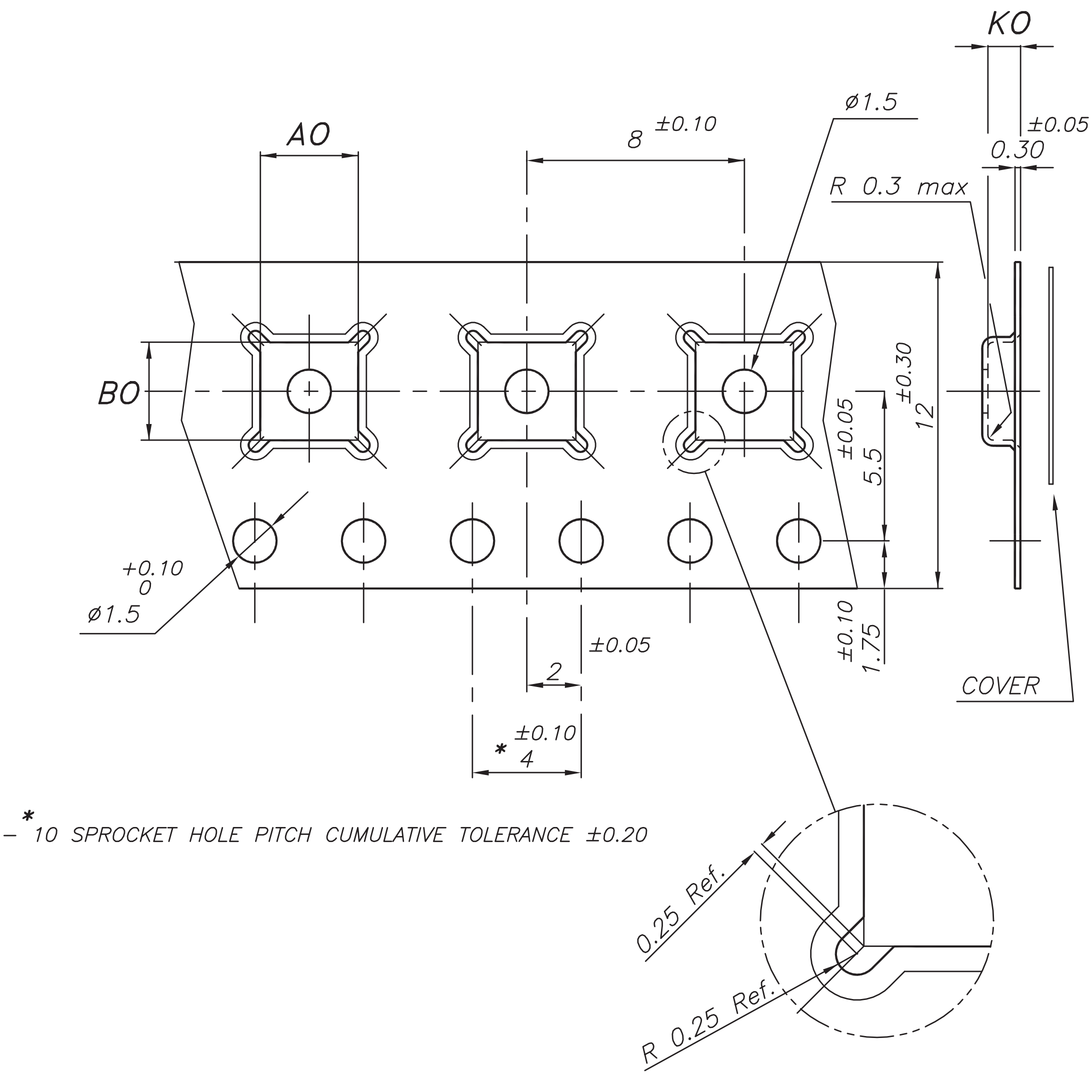
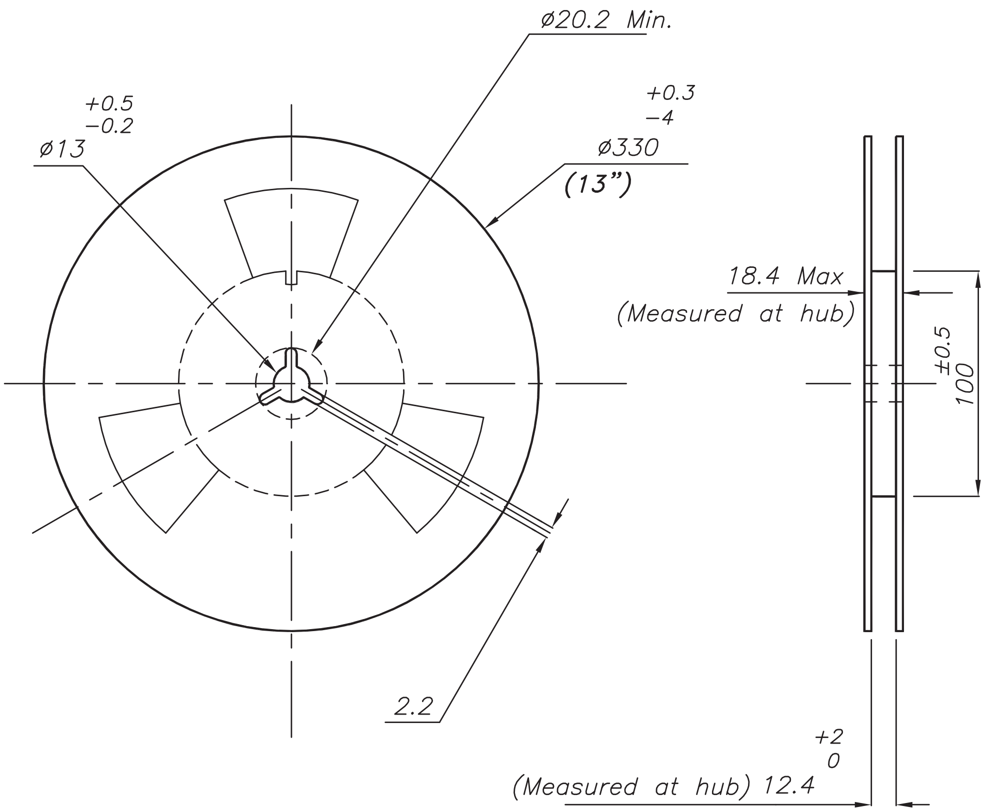


Figure 28. DFN8 (3 x 3 mm) tape outline

Table 8. DFN8 (3 x 3 mm) tape mechanical data

Dim.	mm
	Value
Ao	3.30 ±0.10
Bo	3.30 ±0.10
Ko	1.10 ±0.10

Figure 29. DFN8 (3 x 3 mm) reel outline



9 Ordering information

Table 9. Order codes

DFN8-3x3		Output voltage
Order code	Marking	
LD59100PUR	5910	Adjustable

Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Sep-2017	1	Initial release
21-Nov-2018	2	Updated Figure 15. Reverse current vs. temperature