

IRS2453(1)D(S) SELF-OSCILLATING FULL BRIDGE DRIVER IC

Features

- Integrated 600 V full-bridge gate driver
- CT, RT programmable oscillator
- 15.6V Zener clamp on V_{CC}
- Micropower startup
- Logic level latched shutdown pin
- Non-latched shutdown on CT pin ($1/6$ th V_{CC})
- Internal bootstrap FETs
- Excellent latch immunity on all inputs & outputs
- ESD protection on all pins
- 14-lead SOIC or PDIP package
- 0.5 or 1.0 μ s (typ.) internal deadtime
- RoHS compliant

Product Summary

Topology	Full-bridge
V_{OFFSET}	600 V
I_{O+} & I_{O-} (typical)	180 mA & 260 mA
Deadtime (typical)	1.0 μ s (IRS2453D) 0.5 μ s (IRS24531D)

Package Options



14 Lead PDIP
IRS2453DPbF



14 Lead SOIC
(Narrow Body)
IRS2453(1)DSPbF

Typical Connection Diagram

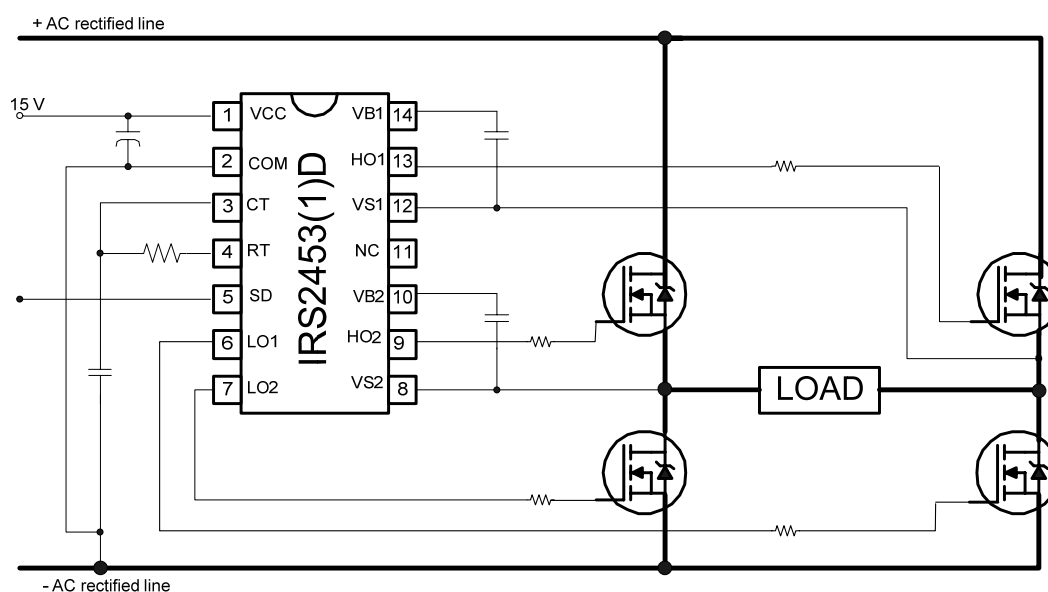


Table of Contents	Page
Description	3
Qualification Information	4
Absolute Maximum Ratings	5
Recommended Operating Conditions	6
Electrical Characteristics	7
Functional Block Diagram	9
Input/Output Pin Equivalent Circuit Diagram	10
Lead Definitions	11
Lead Assignments	11
Application Information and Additional Details	12
Package Details	15
Tape and Reel Details	16
Part Marking Information	17
Ordering Information	18

Description

The IRS2453(1)D is based on the popular IR2153 self-oscillating half-bridge gate driver IC, and incorporates a high voltage full-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers, and with an undervoltage lockout hysteresis greater than 1.5 V. The IRS2453(1)D also includes latched and non-latched shutdown pins.

Qualification Information[†]

Qualification Level		Industrial ^{††}	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC14	MSL2 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
		PDIP14	Not applicable (non-surface mount package style)
ESD	Machine Model	Class C (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{B1}, V_{B2}	High side floating supply voltage	-0.3	625	V
V_{S1}, V_{S2}	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO1}, V_{HO2}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{LO1}, V_{LO2}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{RT}	R_T pin voltage	-0.3	$V_{CC} + 0.3$	
V_{CT}	C_T pin voltage	-0.3	$V_{CC} + 0.3$	
V_{SD}	SD pin voltage	-0.3	$V_{CC} + 0.3$	
I_{RT}	R_T pin current	-5	5	mA
I_{CC}	Supply current ($\dagger$)	---	25	
dV_S/dt	Allowable offset voltage slew rate	-50	50	V/ns
P_D	Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$, 8-Pin DIP	---	1.0	W
P_D	Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$, 8-Pin SOIC	---	0.625	
$R_{\theta JA}$	Thermal resistance, junction to ambient, 8-Pin DIP	---	125	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance, junction to ambient, 8-Pin SOIC	---	200	
T_J	Junction temperature	-55	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

$\dagger$ This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS1}, V_{BS2}	High side floating supply voltage	$V_{CC} - 0.7$	V_{CLAMP}	V
V_{S1}, V_{S2}	Steady state high side floating supply offset voltage	-3.0 (†)	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	(††)	5	mA
T_J	Junction temperature	-25	125	°C

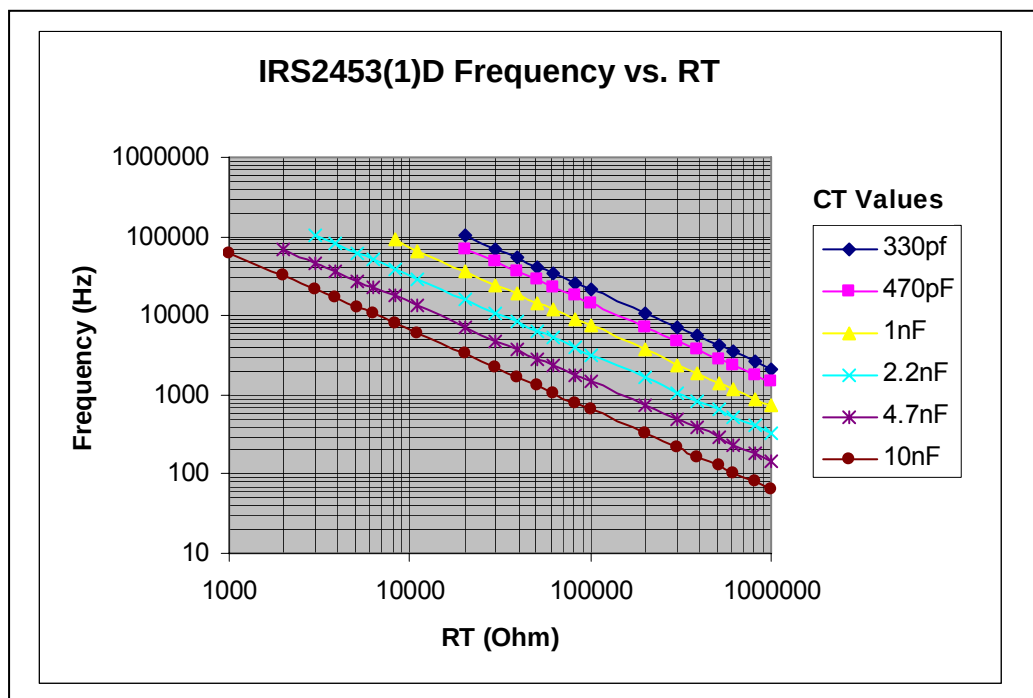
† It is recommended to avoid output switching conditions where negative-going spikes at the V_S node would decrease V_S below ground by more than -5V.

†† Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6 V zener diode clamping the voltage at this pin.

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_T	Timing resistor value	1	---	k Ω
C_T	C_T pin capacitor value	330	---	pF

VBIAS (V_{CC} , V_{BS}) = 14 V, V_S =0 V and T_A = 25 °C, CLO1=CLO2 = CHO1=CHO2 = 1 nF.



Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1 nF.

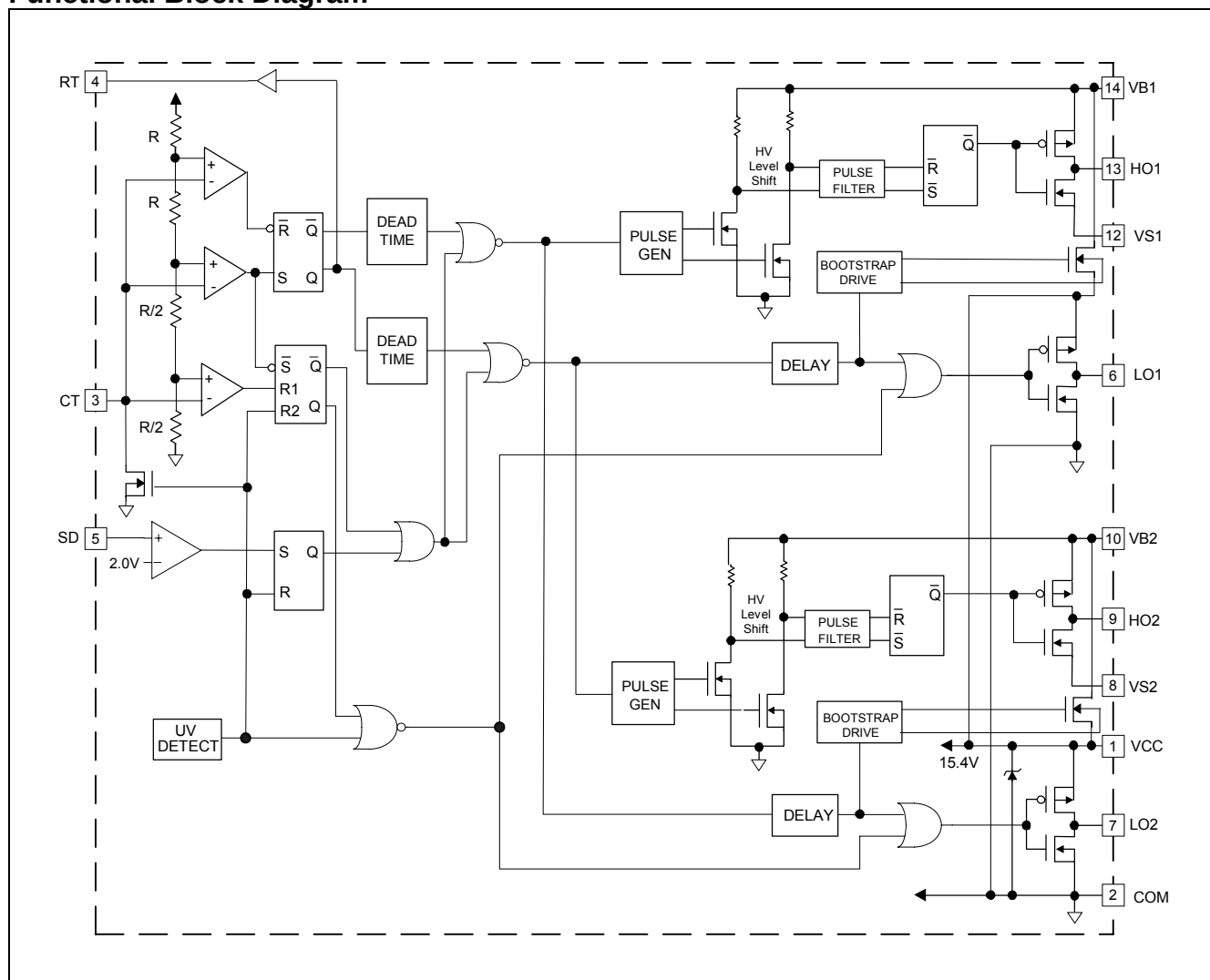
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	10.0	11.0	12.0	V	
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	8.0	9.0	10.0		
$V_{CCUVHYS}$	V_{CC} undervoltage lockout hysteresis	1.5	2.0	2.4		
I_{QCCUV}	Micropower startup V_{CC} supply current	---	140	200	μ A	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	---	1.3	2.0	mA	
I_{CC_20K}	V_{CC} supply current at f_{OSC} (R_T = 36.5 k Ω)	---	3.0	3.5		
I_{CCFLT}	V_{CC} supply current when $SD > V_{SD}$	---	360	500	μ A	
V_{CLAMP}	V_{CC} Zener clamp voltage	14.6	15.6	16.6	V	$I_{CC} = 5$ mA
Floating Supply Characteristics						
I_{QBS1UV} , I_{QBS2UV}	Micropower startup V_{BS} supply current	---	3	10	μ A	$V_{CC} \leq V_{CCUV-}$, $V_{CC} = V_{BS}$
I_{QBS1} , I_{QBS2}	Quiescent V_{BS} supply current	---	30	100		
V_{BS1UV+} , V_{BS2UV+}	V_{BS} supply undervoltage positive going threshold	8.0	9.0	10.0	V	
V_{BS1UV-} , V_{BS2UV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.0	9.0		
I_{LK1} , I_{LK2}	Offset supply leakage current	---	---	50	μ A	$V_B = V_S = 600$ V
Oscillator I/O Characteristics						
f_{OSC}	Oscillator frequency	19.6	20.2	20.8	kHz	$R_T = 36.5$ k Ω
		88	94	100		$R_T = 7.15$ k Ω
d	R_T pin duty cycle	48	50	52	%	$f_o < 100$ kHz
I_{CT}	C_T pin current	---	0.05	1.0	μ A	
I_{CTUV}	UV-mode C_T pin pulldown current	1	5	---	mA	$V_{CC} = 7$ V
V_{CT+}	Upper C_T ramp voltage threshold	---	9.3	---	V	
V_{CT-}	Lower C_T ramp voltage threshold	---	4.7	---		
V_{RT+}	High level R_T output voltage, $V_{CC} - V_{RT}$	---	10	50	mV	$I_{RT} = 100$ μ A $R_T = 140$ k Ω
		---	100	300		$I_{RT} = 1$ mA $R_T = 14$ k Ω
V_{RT-}	Low level R_T output voltage	---	10	50		$I_{RT} = 100$ μ A $R_T = 140$ k Ω
		---	100	300		$I_{RT} = 1$ mA $R_T = 14$ k Ω
V_{RTUV}	UV-mode R_T output voltage	---	0	100		$V_{CC} \leq V_{CCUV-}$

Electrical Characteristics

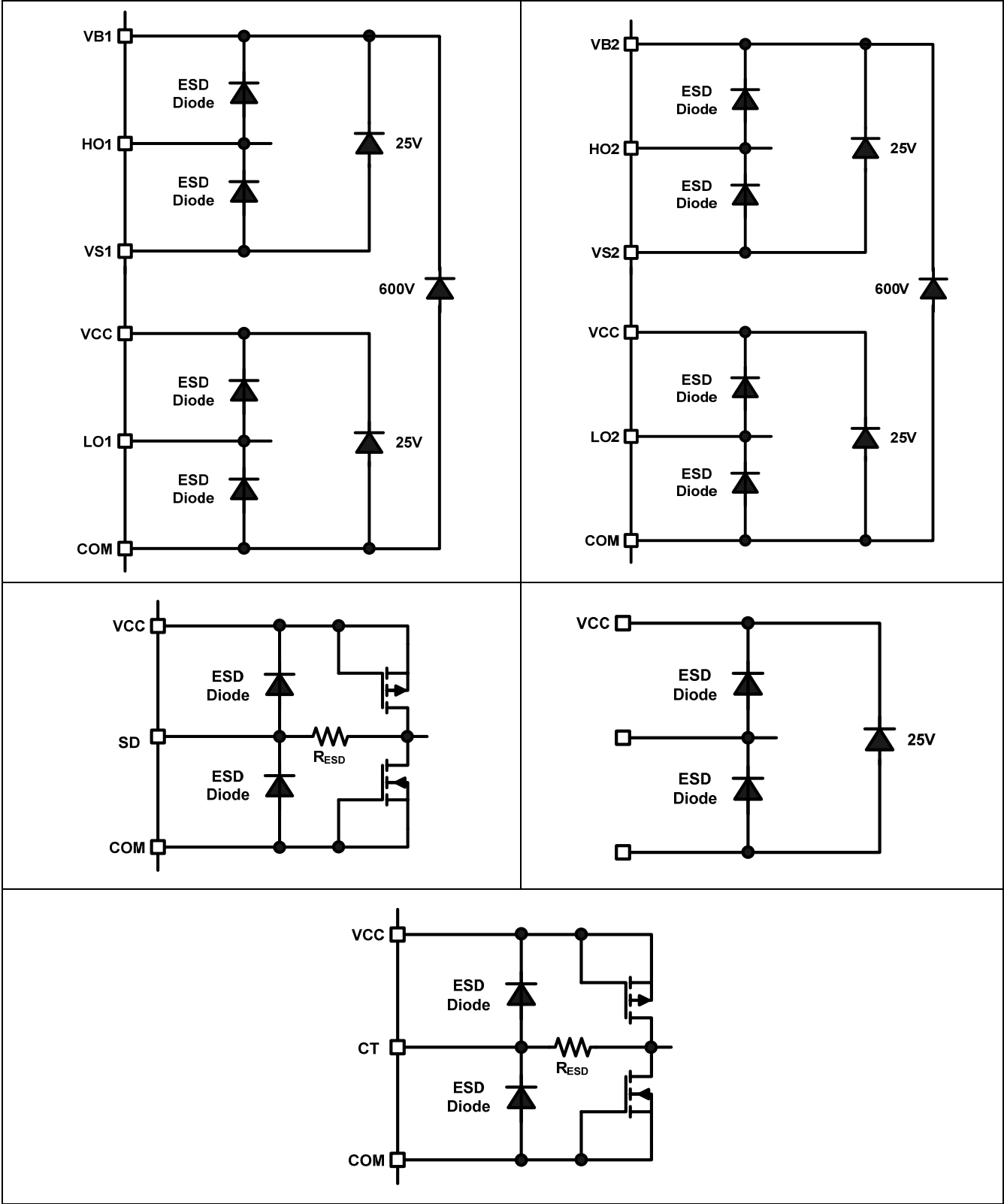
V_{BIAS} (V_{CC} , V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C, unless otherwise specified. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1 nF.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions	
Gate Driver Output Characteristics								
VOH	High level output voltage, VBIAS - VO		---	V _{CC}	---	V	IO = 0 A	
VOL	Low level output voltage, VO		---	COM	---			
VOL_UV	UV-mode output voltage, VO		---	COM	---		IO = 0 A, VCC ≤ VCC(UV)	
t _r	Output rise time		---	120	200	ns		
t _f	Output fall time		---	50	100			
t _{sd}	Shutdown propagation delay		---	250	---			
t _d	Output deadtime (HO or LO)	IRS2453D	0.8	1.0	1.40	μs		
		IRS24531D	0.4	0.5	0.7			
I _{O+}	Output source current		---	180	---	mA		
I _{O-}	Output sink current		---	260	---			
Shutdown								
V _{SD}	Shutdown threshold at SD pin (latched)		1.8	2.0	2.3	V		
VCTSD	CT voltage shutdown threshold (non latched)		2.2	2.3	2.5			
VRTSD	SD mode RT output voltage, VCC - VRT		---	10	50	mV	IRT = 100 μA, RT = 140 kΩ VCT = 0 V	
			---	100	300		IRT = 1 mA, RT = 14 kΩ VCT = 0 V	
Bootstrap FET Characteristics								
V _{B1_ON} V _{B2_ON}	VB when the bootstrap FET is on		13.7	14.0	---	V		
I _{B1_CAP} I _{B2_CAP}	VB source current when FET is on		40	55	---	mA	CBS=0.1 μF	
I _{B1_10 V} I _{B2_10 V}	VB source current when FET is on		10	12	---		VB=10 V	

Functional Block Diagram



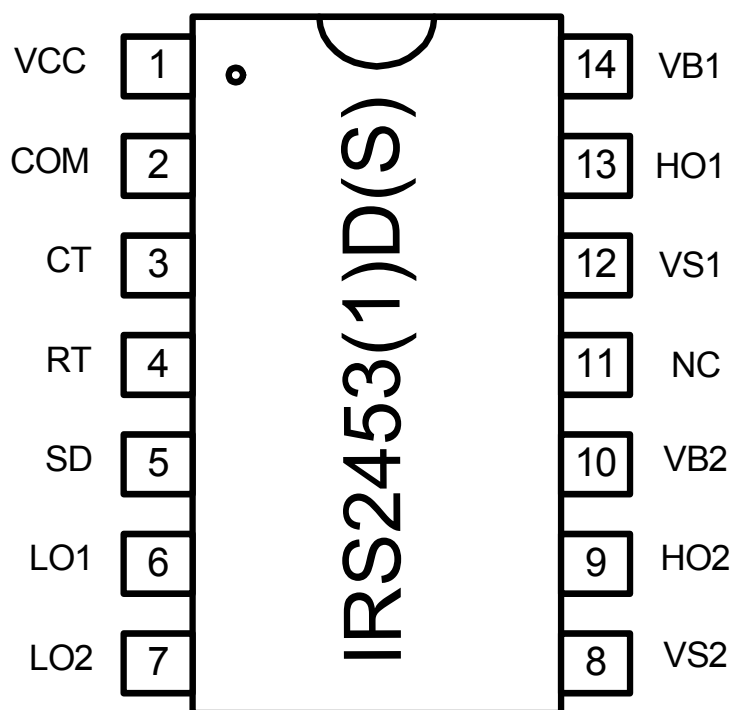
Input/Output Pin Equivalent Circuit Diagrams:



Lead Definitions

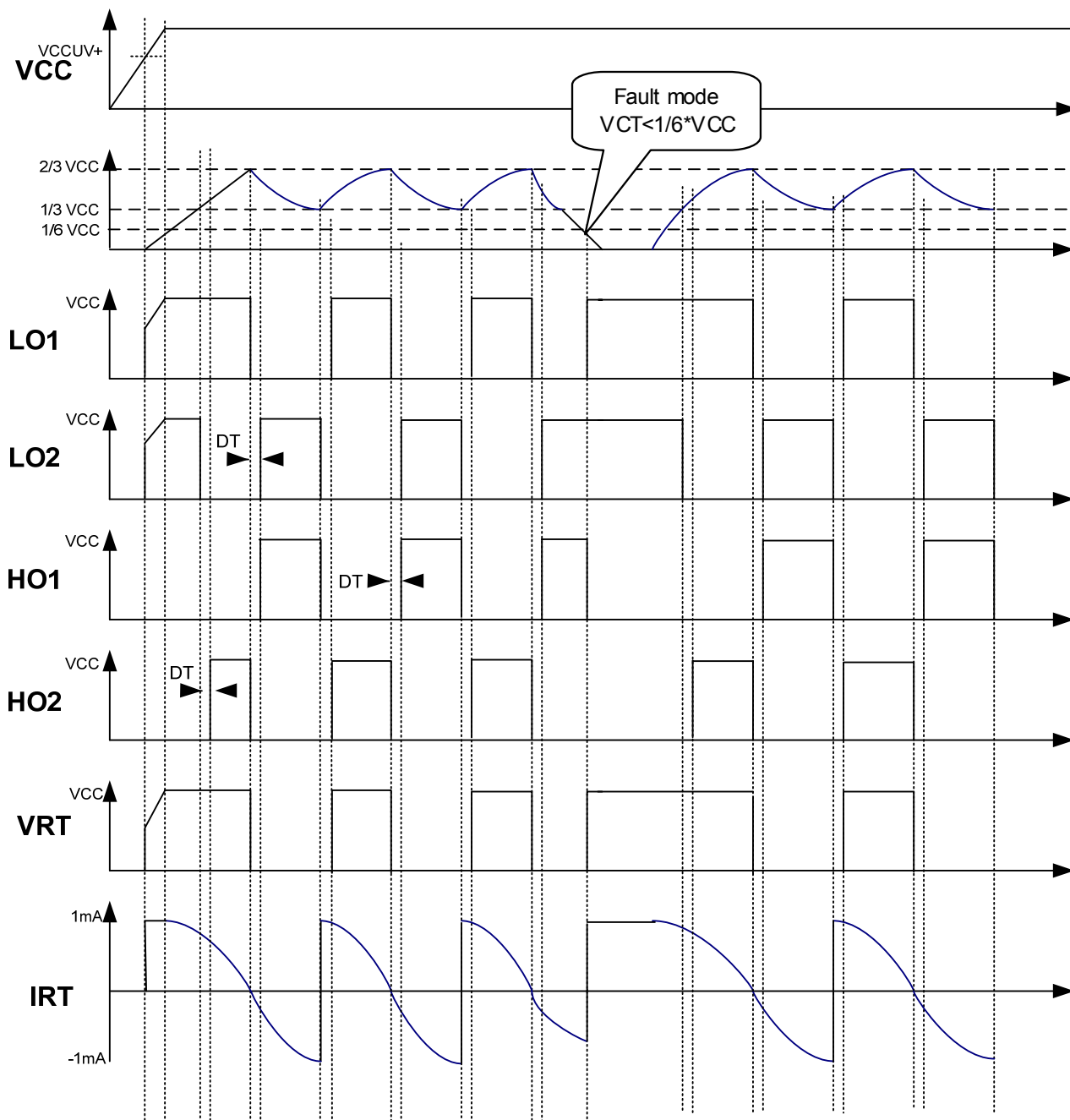
Pin	Symbol	Description
1	VCC	Logic and internal gate drive supply voltage
2	COM	IC power and signal ground
3	CT	Oscillator timing capacitor input
4	RT	Oscillator timing resistor input
5	SD	Shutdown input
6	LO1	Low side gate driver output
7	LO2	Low side gate driver output
8	VS2	High voltage floating supply return
9	HO2	High side gate driver output
10	VB2	High side gate driver floating supply
11	NC	No connect
12	VS1	High voltage floating supply return
13	HO1	High side gate driver output
14	VB1	High side gate driver floating supply

Lead Assignment



Application Information and Additional Details

Timing Diagram



Functional Description

Under-Voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when V_{CC} is below the turn-on threshold of the IC. The IRS2453(1)D under-voltage lock-out is designed to maintain an ultra low supply current of less than 150 μA , and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under-voltage lock-out mode, the high and low side driver outputs LO1, LO2, HO1, HO2 are all low. With V_{CC} above the V_{CCUV+} threshold, the IC turns on and the output begin to oscillate.

Normal Operating Mode

Once V_{CC} reaches the start-up threshold V_{CCUV+} , the MOSFET M1 opens, RT increases to approximately V_{CC} ($V_{CC}-V_{RT+}$) and the external CT capacitor starts charging. Once the CT voltage reaches V_{CT-} (about 1/3 of V_{CC}), established by an internal resistor ladder, LO1 and HO2 turn on with a delay equivalent to the deadtime (t_d). Once the CT voltage reaches V_{CT+} (approximately 2/3 of V_{CC}), LO1 and HO2 go low, RT goes down to approximately ground (V_{RT-}), the CT capacitor starts discharging and the deadtime circuit is activated. At the end of the deadtime, LO2 and HO1 go high. Once the CT voltage reaches V_{CT-} , LO2 and HO1 go low, RT goes to high again, the deadtime is activated. At the end of the deadtime, LO1 and HO2 go high and the cycle starts over again.

The frequency is best determined by the graph, Frequency vs. RT, page 3, for different values of CT. A first order approximate of the oscillator frequency can also be calculated by the following formula::

$$f \approx \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays.

Bootstrap MOSFET

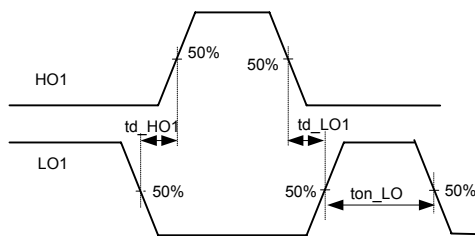
The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal bootstrap FET only turns on when the corresponding LO is high. To guarantee that the high-side supply is charged up before the first pulse on HO1 and HO2, LO1 and LO2 are both on when CT ramps between zero and 1/3* V_{CC} . LO1 and LO2 are also on when CT is grounded below 1/6* V_{CC} to ensure that the bootstrap capacitor is charged when CT is brought back over 1/3* V_{CC} .

Non-Latched Shutdown

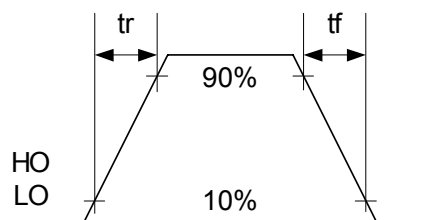
If CT is pulled down below V_{CTSD} (approximately 1/6 of V_{CC}) by an external circuit, CT doesn't charge up and oscillation stops. All outputs are held low and the bootstrap FETs are off. Oscillation will resume once CT is able to charge up again to V_{CT-} .

Latched Shutdown

When the SD pin is brought above 2 V, the IC goes into fault mode and all outputs are low. V_{CC} has to be recycled below V_{CCUV-} to restart the IC. The SD pin can be used for over-current or over-voltage protection using appropriate external circuitry.

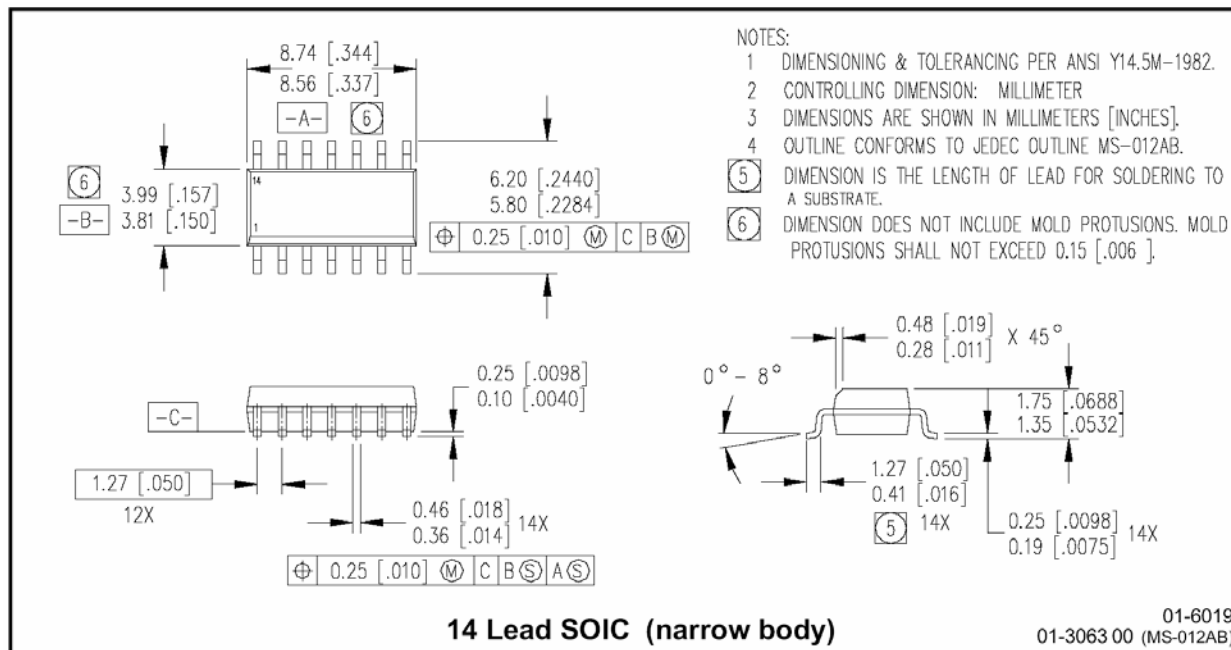
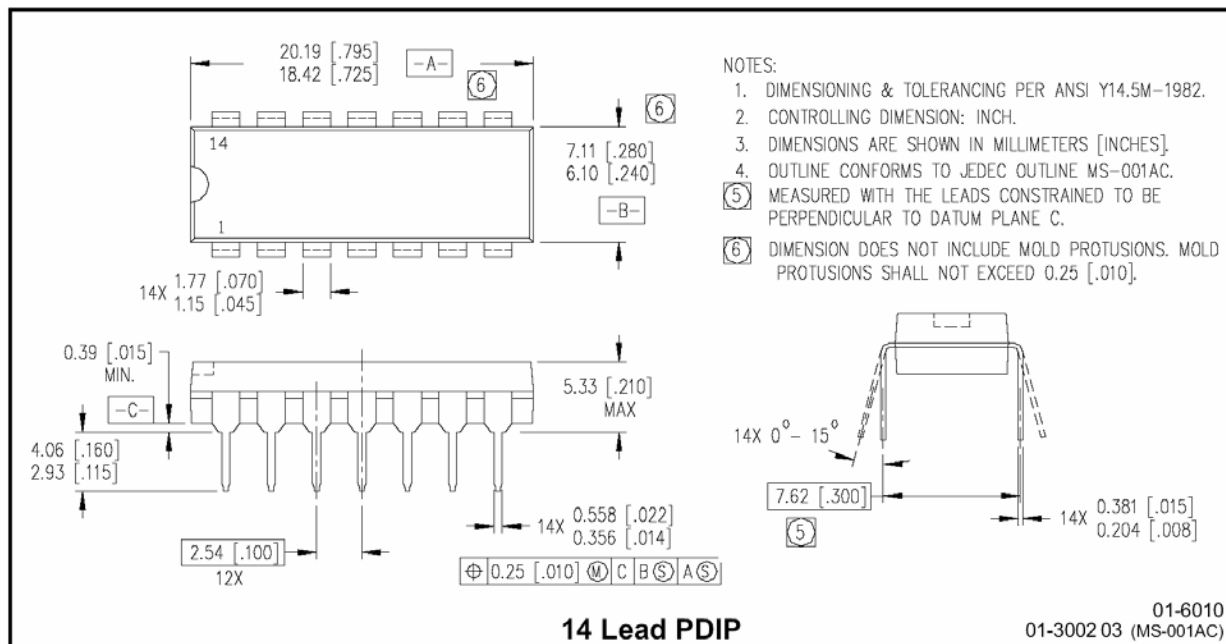


Deadtime Waveform

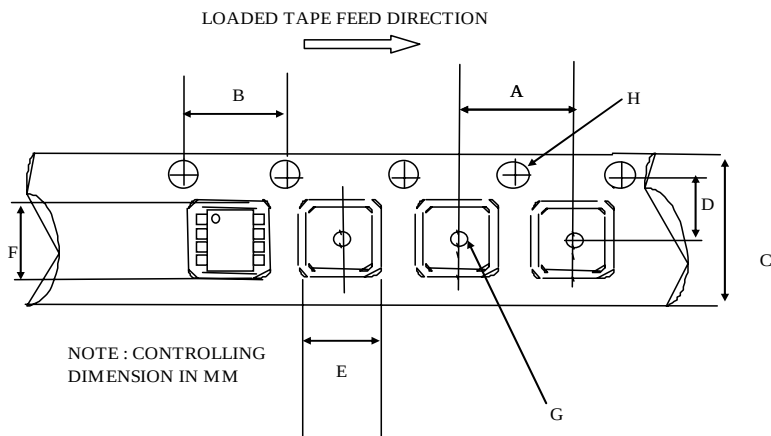


Rise and Fall Time Waveform

Package Details

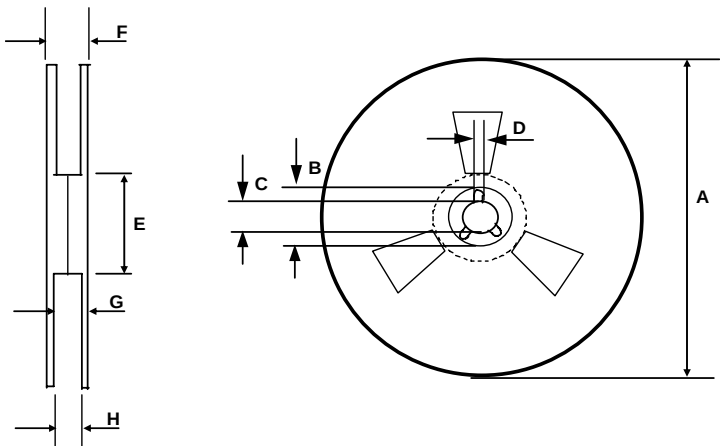


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 14SOICN

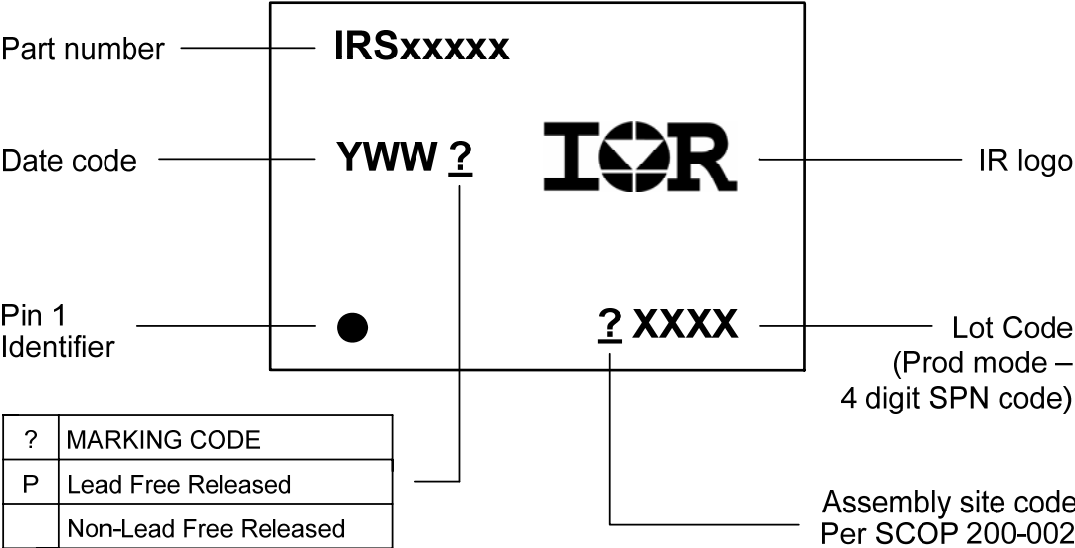
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2453D(S)	PDIP14	Tube/Bulk	25	IRS2453DPBF
	SOIC14N	Tube/Bulk	55	IRS2453DSPBF
		Tape and Reel	2500	IRS2453DSTRPBF
IRS24531DS	SOIC14N	Tube/Bulk	55	IRS24531DSPBF
		Tape and Reel	2500	IRS24531DSTRPBF

The information provided in this document is believed to be accurate and reliable. However, International Rectifier assumes no responsibility for the consequences of the use of this information. International Rectifier assumes no responsibility for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of International Rectifier. The specifications mentioned in this document are subject to change without notice. This document supersedes and replaces all information previously supplied.

For technical support, please contact IR's Technical Assistance Center

<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:

233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105