



64-Position OTP Digital Potentiometer

AD5273

FEATURES

64 Positions

OTP (One-Time-Programmable)¹ Set-and-Forget

Resistance Setting

1 k Ω , 10 k Ω , 50 k Ω , 100 k Ω End-to-End Terminal Resistance

Compact Standard SOT23-8 Package

Ultralow Power: $I_{DD} = 5 \mu A$ Max

Fast Settling Time: $t_s = 5 \mu s$ Typ in Power-Up

I²C Compatible Digital Interface

Computer Software² Replaces μC in Factory Programming

Applications

Wide Temperature Range: $-40^{\circ}C$ to $+105^{\circ}C$

5 V Programming Voltage

Low Operating Voltage, 2.7 V to 5.5 V

OTP Validation Check Function

APPLICATIONS

Systems Calibrations

Electronics Level Settings

Mechanical Trimmers[®] Replacement in New Designs

Automotive Electronics Adjustments

Transducer Circuits Adjustments

Programmable Filters up to 6 MHz BW³

GENERAL DESCRIPTION

The AD5273 is a 64-position, One-Time-Programmable (OTP) digital potentiometer⁴ that employs fuse link technology to achieve the permanent program setting. This device performs the same electronic adjustment function as most mechanical trimmers and variable resistors. It allows unlimited adjustments before permanently setting the resistance values. The AD5273 is programmed using a 2-wire, I²C compatible digital control. During the write mode, a fuse blow command is executed after the final value is determined, therefore freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). When this permanent setting is achieved, the value will not change regardless of the supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in the read mode.

NOTES

¹ One-Time-Programmable—Unlimited adjustments before permanent setting.

² ADI cannot guarantee the software to be 100% compatible in all systems due to the wide variations in computer configurations.

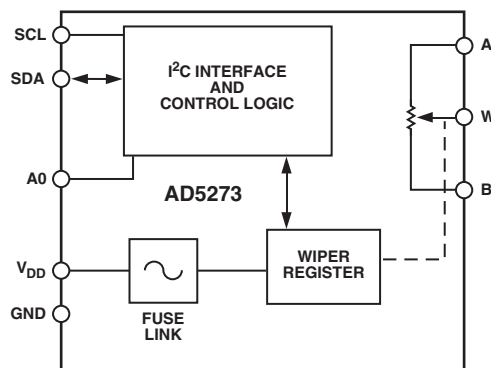
³ Applies to 1 k Ω parts only.

⁴ The terms digital potentiometer, VR, and RDAC are used interchangeably.

REV.0

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FUNCTIONAL BLOCK DIAGRAM



In addition, for applications that program AD5273 at the factory, Analog Devices offers device programming software² running in Windows[®] NT, 2000, and XP operating systems. This software application effectively replaces any external I²C controllers, which in turn enhances users' systems time-to-market.

AD5273 is available in 1 k Ω , 10 k Ω , 50 k Ω , and 100 k Ω in compact SOT23 8-lead standard package and operates from $-40^{\circ}C$ to $+105^{\circ}C$.

Besides its unique OTP feature, the AD5273 lends itself well to general digital potentiometer applications due to its effective resolution, array resistance options, small footprint, and low cost.

An AD5273 evaluation kit and software are available. The kit includes the connector and cable that can be converted for further factory programming applications.

For applications that require dynamic adjustment of resistance settings with nonvolatile EEMEM, users should refer to AD523x and AD525x families of nonvolatile memory digital potentiometers.

AD5273—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 1 k Ω , 10 k Ω , 50 k Ω , 100 k Ω VERSIONS

($V_{DD} = 2.7\text{ V}$ to 5.5 V , $V_A \leq V_{DD}$, $V_B = 0\text{ V}$, $-40^\circ\text{C} < T_A < +105^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS						
RHEOSTAT MODE						
Resolution	N				6	Bits
Resistor Differential NL ² (10 k Ω , 50 k Ω , 100 k Ω)	R-DNL	$R_{WB}, V_A = \text{NC}$ $R_{WB}, V_A = \text{NC}$	-0.5 -1	+0.05 +0.25	+0.5 +1	LSB LSB
Resistor Nonlinearity ² (10 k Ω , 50 k Ω , 100 k Ω)	R-INL	$R_{WB}, V_A = \text{NC}$ $R_{WB}, V_A = \text{NC}$	-0.5 -5	+0.10 +2	+0.5 +5	LSB LSB
Nominal Resistance Tolerance ³ (10 k Ω , 50 k Ω , 100 k Ω)	ΔR_{AB}	$T_A = 25^\circ\text{C}$	-30		+30	%
Nominal Resistance (1 k Ω)	R_{AB}		0.8	1.2	1.6	k Ω
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		300		ppm/ $^\circ\text{C}$
Wiper Resistance	R_W	$I_W = V_{DD}/R$, $V_{DD} = 3\text{ V}$ or 5 V		60	100	Ω
DC CHARACTERISTICS						
POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity ⁴	DNL		-0.5	+0.1	+0.5	LSB
Integral Nonlinearity ⁴	INL		-0.5		+0.5	LSB
Voltage Divider						
Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 20 _H		10		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSE}	Code = 3F _H	-1		0	LSB
Zero-Scale Error	V_{WZSE}		-6		0	LSB
(10 k Ω , 50 k Ω , 100 k Ω)		Code = 00 _H	0		1	LSB
(1 k Ω)		Code = 00 _H	0		5	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	$V_{A,B,W}$		0		V_{DD}	V
Capacitance ⁶ A, B	$C_{A,B}$	$f = 5\text{ MHz}$, Measured to GND, Code = 20 _H			25	pF
Capacitance ⁶ W	C_W	$f = 1\text{ MHz}$, Measured to GND, Code = 20 _H			55	pF
Common Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	$V_{LOGIC} = 3\text{ V}$	2.1			V
Input Logic Low	V_{IL}	$V_{LOGIC} = 3\text{ V}$			0.6	V
Output Logic High (SDO)	V_{IH}		4.9			V
Output Logic Low (SDO)	V_{IL}				0.4	V
Input Logic Current	I_{IL}	$V_{IN} = 0\text{ V}$ or 5 V		0.01	1	μA
Input Capacitance ⁶	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply ⁷	V_{DD_OTP}	$T_A = 25^\circ\text{C}$	5		6	V
Supply Current	I_{DD}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		0.1	5	μA
OTP Supply Current ⁸	I_{DD_OTP}	$T_A = 25^\circ\text{C}$	100			mA
Power Dissipation ⁹	P_{DISS}	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$, $V_{DD} = 5\text{ V}$		0.2	0.3	mW
Power Supply Sensitivity	PSSR		-0.015		+0.015	%/%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS ^{6, 10, 11}						
Bandwidth –3 dB	BW_1 kΩ	R _{AB} = 1 kΩ, Code = 20 _H		6000		kHz
	BW_10 kΩ	R _{AB} = 10 kΩ, Code = 20 _H		600		kHz
	BW_50 kΩ	R _{AB} = 50 kΩ, Code = 20 _H		110		kHz
	BW_100 kΩ	R _{AB} = 100 kΩ, Code = 20 _H		60		kHz
Total Harmonic Distortion	THD _W	V _A = 1 V rms, R _{AB} = 1 kΩ, V _B = 0 V, f = 1 kHz		0.014		%
Adjustment Settling Time	t _{S1}	V _A = 5 V ± 1 LSB Error Band, V _B = 0, Measured at V _W		5		μs
OTP Settling Time ¹²	t _{S_OTP}	V _A = 5 V ± 1 LSB Error Band, V _B = 0, Measured at V _W		400		ms
Power-Up Settling Time – Post Fuses Blown	t _{S2}	V _A = 5 V ± 1 LSB Error Band, V _B = 0, Measured at V _W		5		μs
Resistor Noise Voltage	e _{N_WB}	R _{AB} = 1 kΩ, f = 1 kHz, Code = 20 _H		3		nV/√Hz
		R _{AB} = 20 kΩ, f = 1 kHz, Code = 20 _H		13		nV/√Hz
		R _{AB} = 50 kΩ, f = 1 kHz, Code = 20 _H		20		nV/√Hz
		R _{AB} = 100 kΩ, f = 1 kHz, Code = 20 _H		28		nV/√Hz
INTERFACE TIMING CHARACTERISTICS (applies to all parts ^{6, 11, 13})						
SCL Clock Frequency	f _{SCL}				400	kHz
t _{BUF} Bus Free Time between STOP and START	t ₁		1.3			μs
t _{HD;STA} Hold Time (repeated START)	t ₂	After this period, the first clock pulse is generated.				
t _{LOW} Low Period of SCL Clock	t ₃		0.6			μs
t _{HIGH} High Period of SCL Clock	t ₄		1.3			μs
t _{SU;STA} Setup Time for START Condition	t ₅		0.6		50	μs
t _{HD;DAT} Data Hold Time	t ₆				0.9	μs
t _{SU;DAT} Data Setup Time	t ₇		0.1			μs
t _F Fall Time of Both SDA and SCL Signals	t ₈				0.3	μs
t _R Rise Time of Both SDA and SCL Signals	t ₉				0.3	μs
t _{SU;STO} Setup Time for STOP Condition	t ₁₀		0.6			μs

NOTES

¹Typicals represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V.

²Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

³V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

⁴INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

⁵Resistor terminals A, B, W have no limitations on polarity with respect to each other.

⁶Guaranteed by design and not subject to production test.

⁷Different from operating power supply, power supply for OTP is used one time only.

⁸Different from operating current, supply current for OTP lasts approximately 400 ms for one time needed only.

⁹P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

¹⁰Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

¹¹All dynamic characteristics use V_{DD} = 5 V.

¹²Different from settling time after fuses are blown. The OTP settling time occurs once only.

¹³See Figure 1 for location of measured values.

Specifications subject to change without notice.

AD5273

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to GND	−0.3 V, +6.5 V
V _A , V _B , V _W to GND	GND, V _{DD}
A–B, A–W, B–W	
Intermittent ²	±20 mA
Continuous	±2 mA
Digital Input and Output Voltage to GND	0 V, V _{DD}
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T _{J MAX})	150°C
Storage Temperature	−65°C to +150°C

Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance ³ θ _{JA} , SOT-23	230°C/W

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

³ Package Power Dissipation = (T_{J MAX} − T_A)/θ_{JA}

ORDERING GUIDE

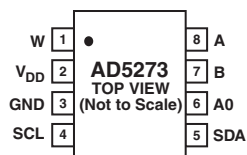
Model	Resistance R _{AB} (kΩ)	Package Code	Package Description	Full Container Quantities	Brand
AD5273BRJ1-REEL7	1	RJ	SOT23-8	3000	DYA
AD5273BRJ10-REEL7	10	RJ	SOT23-8	3000	DYB
AD5273BRJ50-REEL7	50	RJ	SOT23-8	3000	DYC
AD5273BRJ100-REEL7	100	RJ	SOT23-8	3000	DYD
AD5273BRJ1-R2	1	RJ	SOT23-8	250	DYA
AD5273BRJ10-R2	10	RJ	SOT23-8	250	DYB
AD5273BRJ50-R2	50	RJ	SOT23-8	250	DYC
AD5273BRJ100-R2	100	RJ	SOT23-8	250	DYD
AD5273EVAL	*	NA	NA	*	NA

*Users should order samples additionally as the evaluation kit comes with a socket but does not include the parts.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5273 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

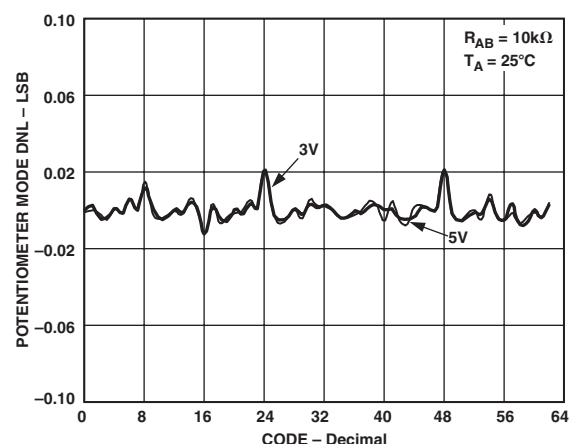
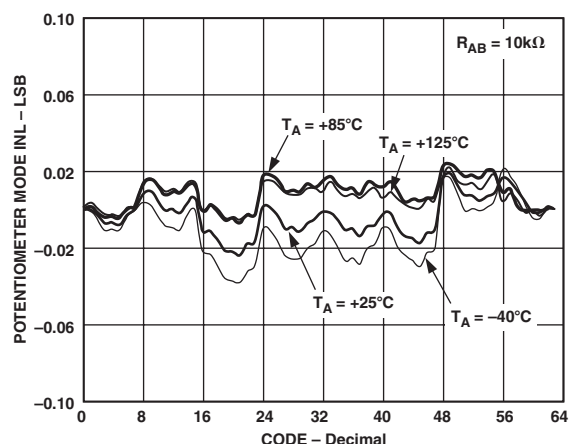
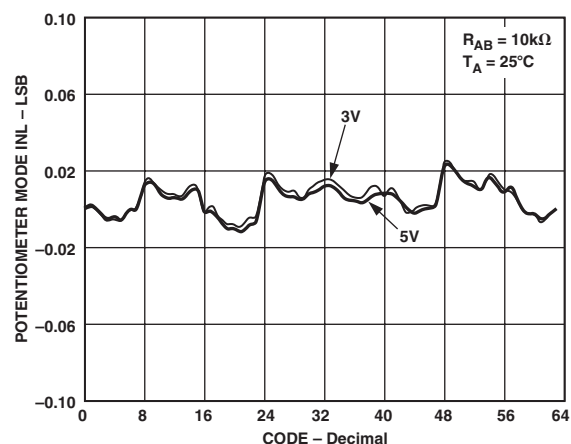
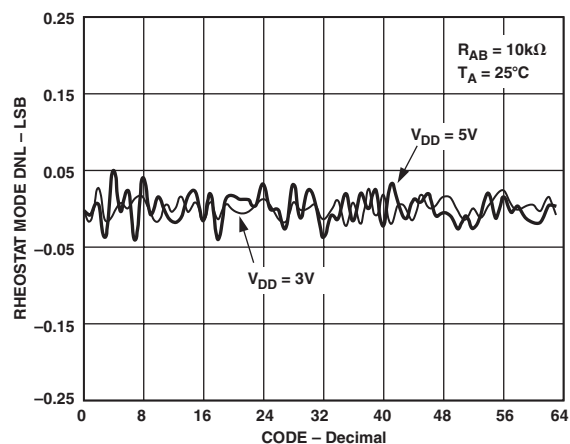
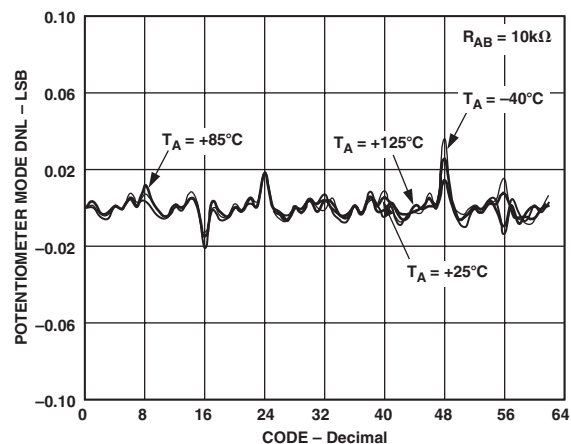
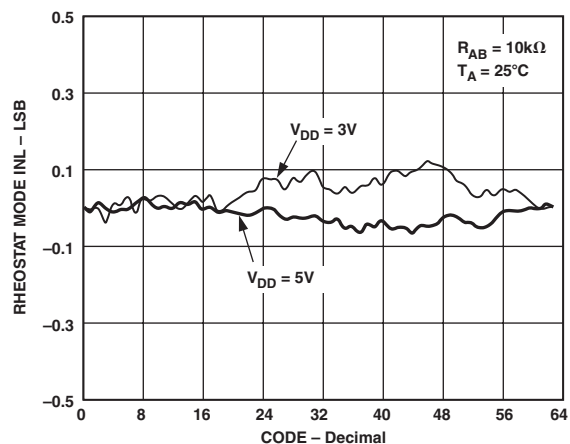


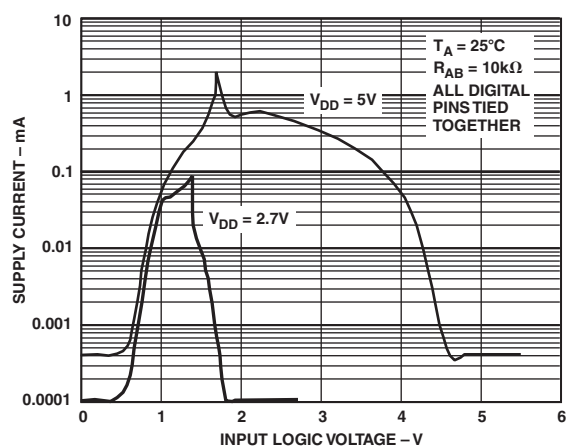
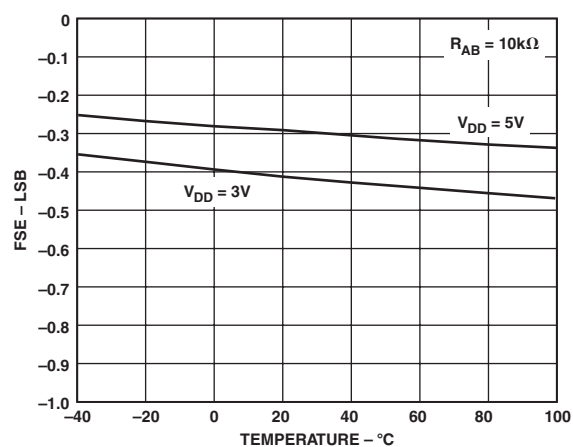
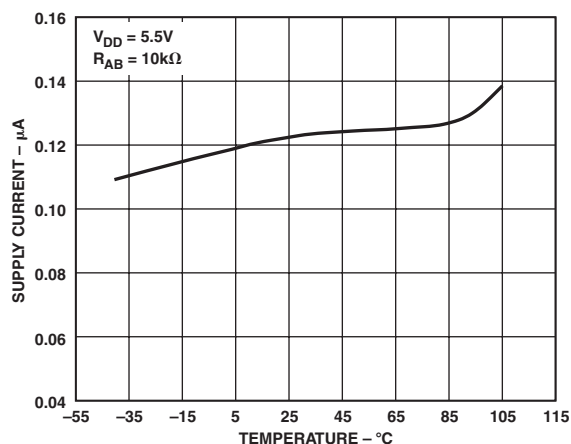
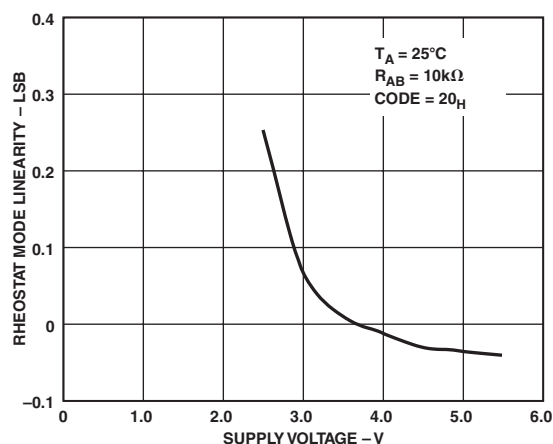
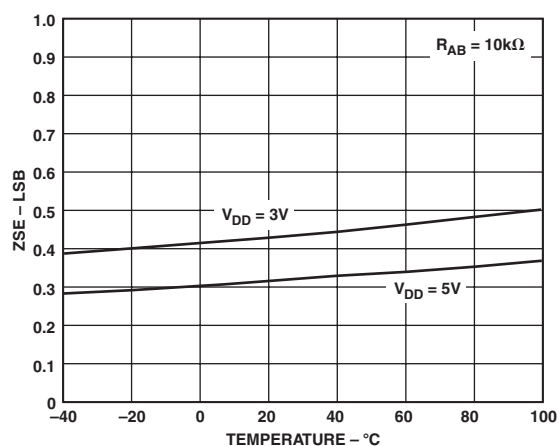
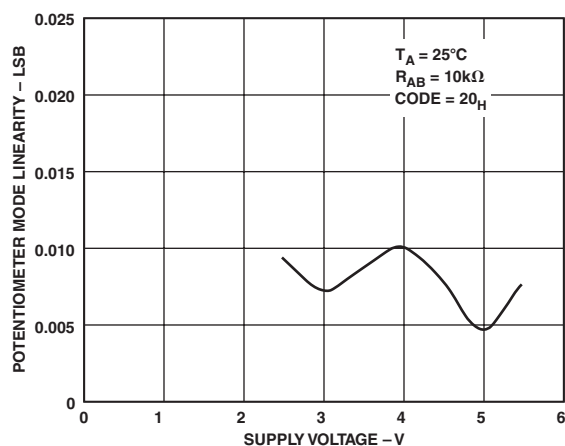


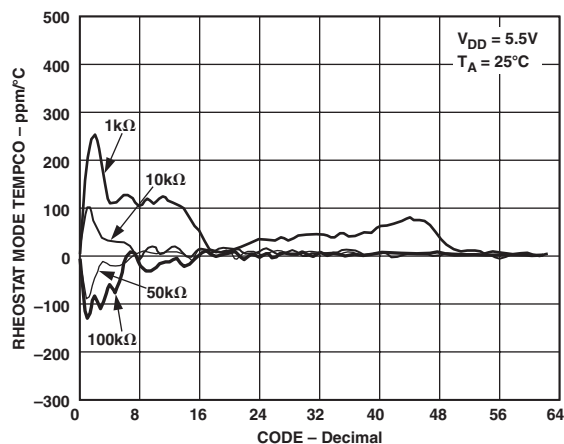
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W
2	V _{DD}	Positive Power Supply. Specified for non-OTP operation from 2.7 V to 5.5 V. For OTP programming, V _{DD} needs to be a minimum of 5 V.
3	GND	Common Ground
4	SCL	Serial Clock Input. Requires Pull-Up Resistor.
5	SDA	Serial Data Input/Output. Requires Pull-Up Resistor.
6	A0	I ² C Device Address Bit
7	B	Resistor Terminal B
8	A	Resistor Terminal A

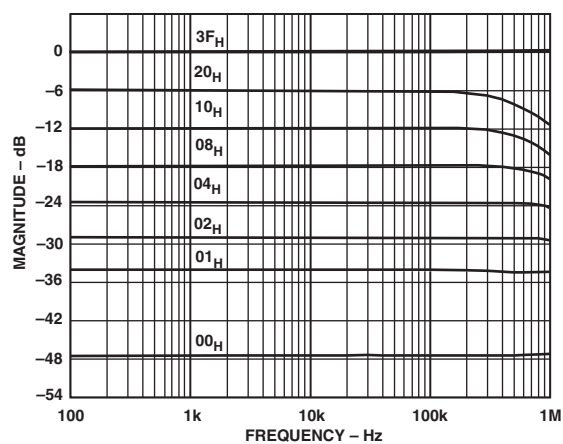
AD5273—Typical Performance Characteristics



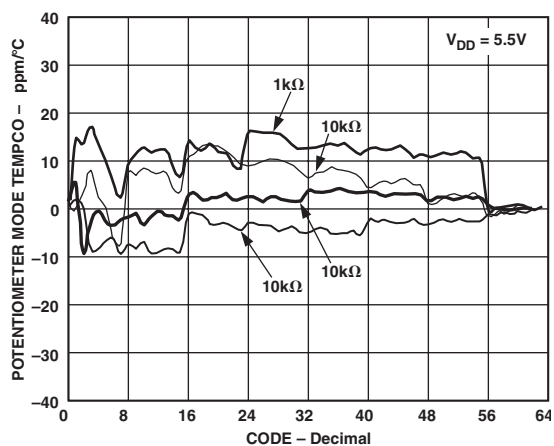




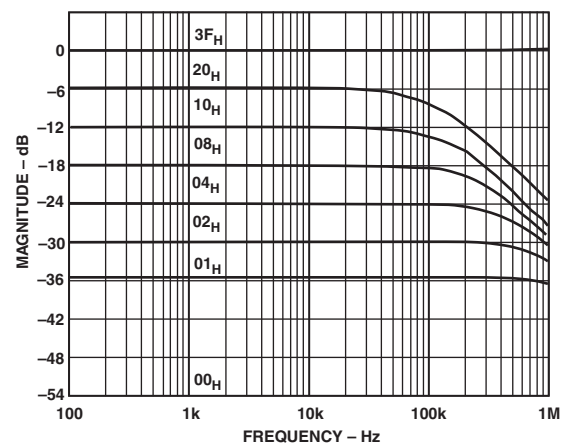
TPC 13. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code



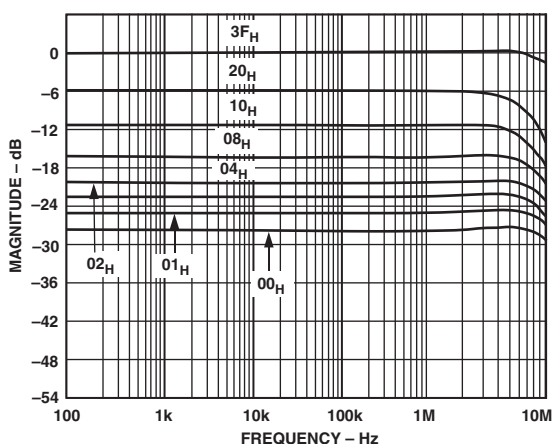
TPC 16. Gain vs. Frequency vs. Code, $R_{AB} = 10 \text{ k}\Omega$



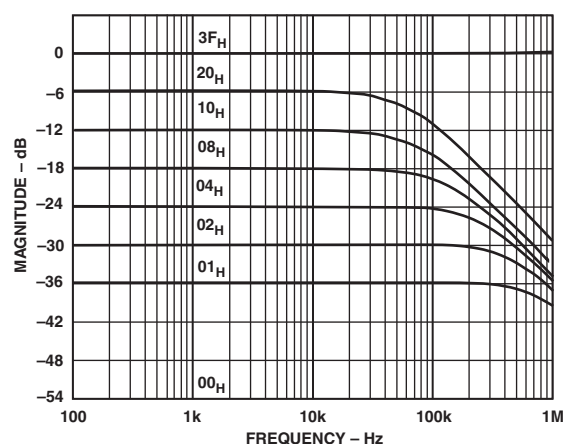
TPC 14. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code



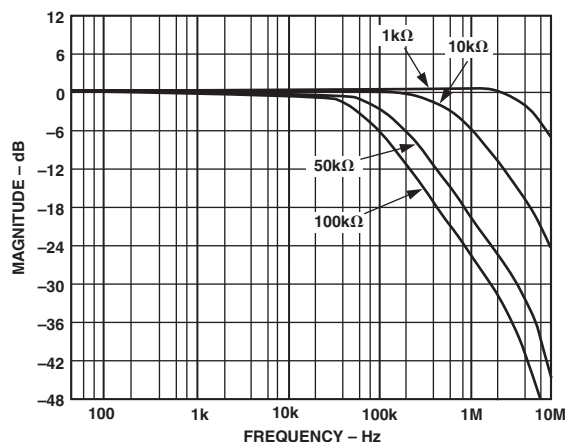
TPC 17. Gain vs. Frequency vs. Code, $R_{AB} = 50 \text{ k}\Omega$



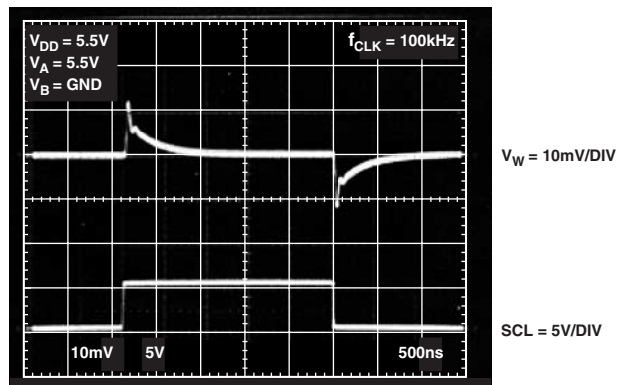
TPC 15. Gain vs. Frequency vs. Code, $R_{AB} = 1 \text{ k}\Omega$



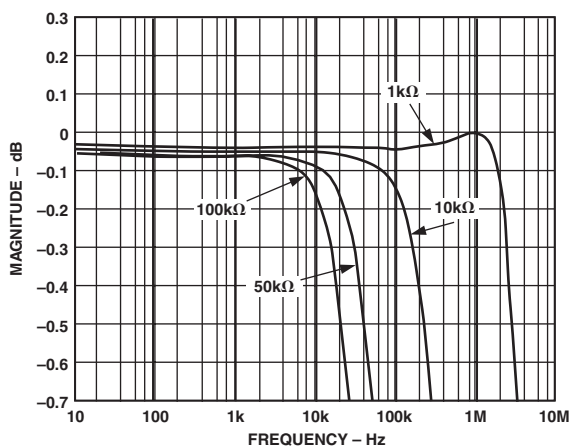
TPC 18. Gain vs. Frequency vs. Code, $R_{AB} = 100 \text{ k}\Omega$



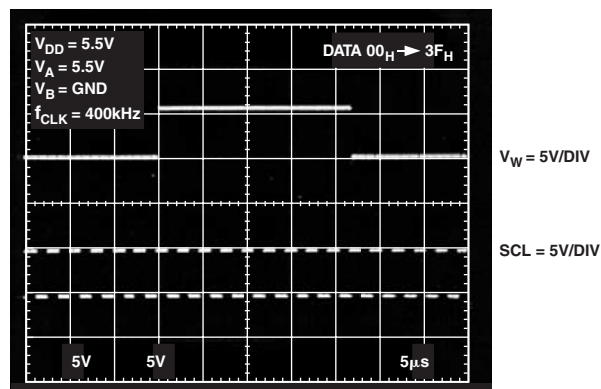
TPC 19. -3 dB Bandwidth



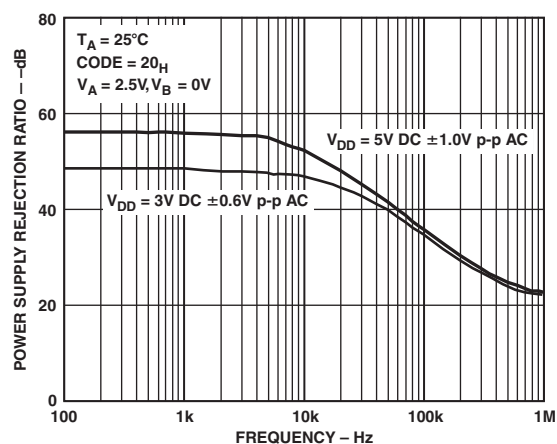
TPC 22. Digital Feedthrough vs. Time



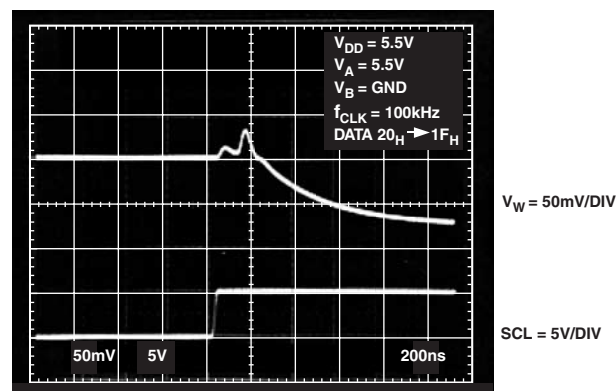
TPC 20. Normalized Gain Flatness vs. Frequency



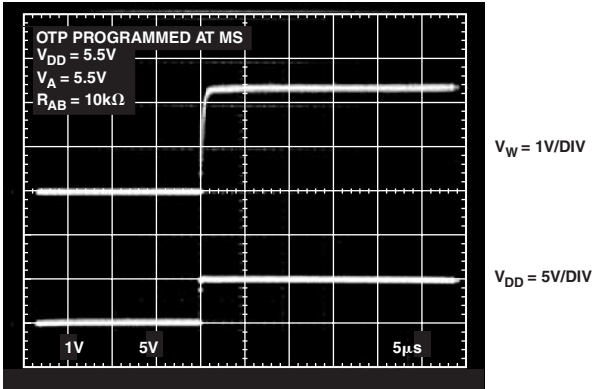
TPC 23. Large Settling Time



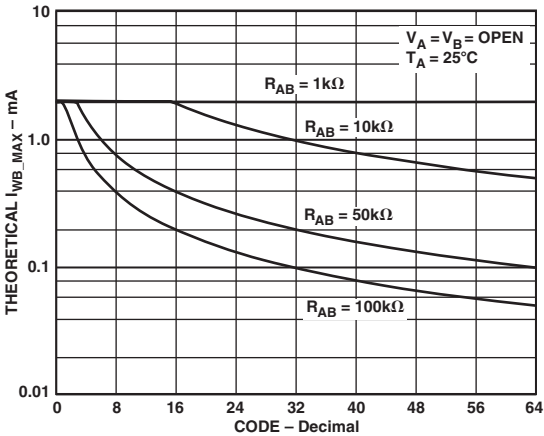
TPC 21. PSRR vs. Frequency



TPC 24. Midscale Glitch Energy



TPC 25. Power-Up Settling Time, after Fuses Blown



TPC 26. I_{WB_MAX} vs. Code

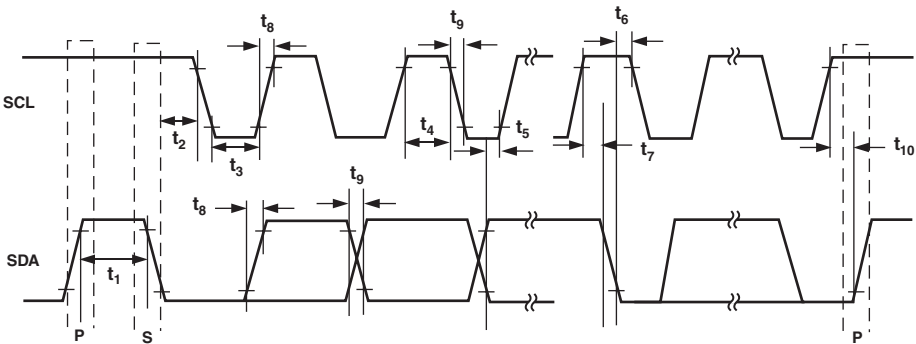


Figure 1. Interface Timing Diagram

Table I. SDA Write Mode Bit Format

S	0	1	0	1	1	0	A0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
SLAVE ADDRESS BYTE									INSTRUCTION BYTE									DATA BYTE										

Table II. SDA Read Mode Bit Format

S	0	1	0	1	1	0	A0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
SLAVE ADDRESS BYTE									DATA BYTE										

SDA BITS DEFINITIONS AND DESCRIPTIONS

S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don't Care
T = OTP Programming Bit. Logic 1 programs wiper position permanently.

D5, D4, D3, D2, D1, D0 = Data Bits
E1, E0 = OTP Validation Bits
0, 0 = Ready to Program
0, 1 = Test Fuse not Blown Successfully. (Check Setup.)
1, 0 = Fatal Error. Retry.
1, 1 = Programmed Successfully. No Further Adjustments Possible.

THEORY OF OPERATION

The AD5273 is a One-Time-Programmable (OTP), Set-and-Forget, 6-bit digital potentiometer. It is comprised of six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are programmed correctly.

One-Time-Programming (OTP)

AD5273 has an internal power-on preset that places the wiper in the midscale during power-on. After the wiper is adjusted to the desired position, the wiper setting can be permanently programmed by setting the T bit, MSB of the Instruction Byte, to 1 along with the proper coding. Refer to Table I.

The one-time program control circuit has two validation bits, E1 and E0, that can be read back in the Read mode for checking the programming status. Table III shows the validation status.

Table III. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully (For Setup Checking)
1	0	Fatal Error. Some fuses are not blown. Retry.
1	1	Successful. No further programming is possible.

The detailed programming sequence is explained further below. When the OTPT bit is set, the internal clock is enabled. The program will attempt to blow a test fuse. The operation stops if this fuse is not blown successfully. The validation bits, E1 and E0, show 01 and the users should check the setup. If the test fuse is blown successfully, the data fuses will be programmed next. The six data fuses will be programmed in six clock cycles. The output of the fuses is compared with the code stored in the DAC register. If they do not match, E1 E0 = 10 is issued as a fatal error and the operation stops. Users may retry with the same code. If the output and the stored code match, the programming lock fuse will be blown so that no further programming is possible. In the meantime, E1 E0 will issue 11 indicating the lock fuse is blown successfully. All the fuse latches are enabled at power on from this point on. Figure 2 shows a detailed functional block diagram.

DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE*

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 1 k Ω , 10 k Ω , 50 k Ω , and 100 k Ω . The final two or three digits of the part number determine the nominal resistance value, e.g., 1 k Ω = 1, 10 k Ω = 10; 50 k Ω = 50; 100 k Ω = 100. The nominal resistance (R_{AB}) of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact. The 6-bit data in the RDAC latch is decoded to select one of the 64 possible settings. Assuming that a 10 k Ω part is used, the wiper's first connection starts at the B terminal for data 00_H. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point and corresponds to 219 Ω ($R_{WB} = R_{AB}/63 + R_W = 159 + 60$) for data 01_H. The third connection is the next tap point representing 378 Ω ($159 \times 2 + 60$) for data 02_H, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω [$R_{AB} + R_W$]. Figure 3 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 6-bit RDAC register.

R_{AB} is the nominal end-to-end resistance.

R_W is the wiper resistance contributed by the on resistance of the internal switch.

Again, if $R_{AB} = 10$ k Ω and terminal A is opened, the following output resistance values R_{WB} will be set for the following RDAC latch codes.

D(DEC)	R_{WB} (Ω)	Output State
63	10060	Full-Scale ($R_{AB} + R_W$)
32	5139	Midscale
1	219	1 LSB
0	60	Zero-Scale (Wiper contact resistance)

*Applies to Potentiometer Mode only

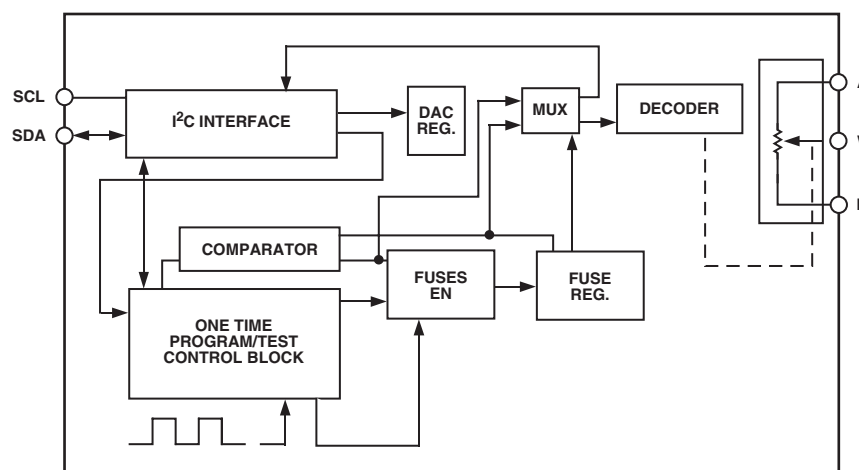


Figure 2. Detailed Functional Block Diagram

AD5273

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA} . When these terminals are used, terminal B can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{63-D}{63} \times R_{AB} + R_W \quad (2)$$

For $R_{AB} = 10 \text{ k}\Omega$ and terminal B is opened, the following output resistance R_{WA} will be set for the following RDAC latch codes.

D (DEC)	$R_{WA} (\Omega)$	Output State
63	60	Full-Scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero-Scale

The typical distribution of the nominal resistance R_{AB} from channel to channel matches within $\pm 1\%$. Device-to-device matching is process lot dependent and is possible to have $\pm 30\%$ variation.

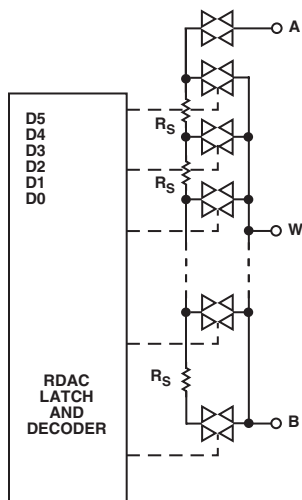


Figure 3. Equivalent RDAC Circuit

Voltage Output Operation

Similar to the D/A converter, the digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-B. Unlike the polarity of V_{DD} , which must be positive, voltage across A-B, W-A, and W-B can be at either polarity as long as the voltage across them is $\leq |V_{DD}|$.

If ignoring the effect of the wiper resistance for approximation, connecting terminal A to 5 V and terminal B to ground produces an output voltage at the wiper-to-B starting at 0 V up to 5 V. Each LSB of voltage is equal to the voltage applied across terminal A-B, divided by the 63 position of the potentiometer divider as:

$$V_W(D) = \frac{D}{63} V_A \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation overtemperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values, therefore, the temperature drift reduces to 10 ppm/ $^{\circ}\text{C}$.

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figures 4a and 4b. This applies to digital input pins SDA and SCL.

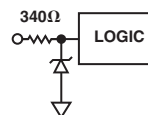


Figure 4a. ESD Protection of Digital Pins

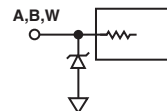


Figure 4b. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The V_{DD} of AD5273 defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} will be clamped by the internal forward-biased diodes. See Figure 5.

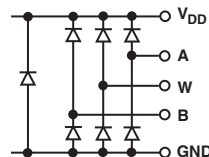


Figure 5. Maximum Terminal Voltages Set by V_{DD}

POWER-UP SEQUENCE

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (Figure 5), it is important to power V_{DD} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuits. The ideal power-up sequence is in the following order: GND, V_{DD} , digital inputs, and $V_{A/B/W}$. The order of powering V_A , V_B , V_W , and digital inputs is not important as long as they are powered after V_{DD} .

POWER SUPPLY CONSIDERATIONS

AD5273 employs fuse link technology, which requires an adequate current density to blow the internal fuses to achieve a given setting. As a result, the power supply, either an on-board linear regulator or rack-mount power supply, must be rated at 5 V with less than $\pm 5\%$ tolerance. The supply should be able to handle 100 mA of transient current, and lasts about 400 ms, during the one-time programming. A low ESR 1 μF to 10 μF tantalum or electrolytic

bypass capacitor should be applied at V_{DD} to minimize the transient disturbances during the programming as shown in Figure 6a. Once the programming is completed, the supply voltage can be reduced to 2.7 V with supply current of less than 1 μ A.

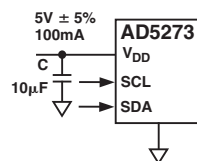


Figure 6a. OTP Power Supply Requirement

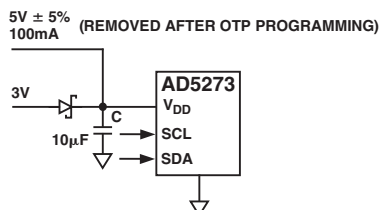


Figure 6b. External Power Supply Applied for Programming

For users who have an on-board 3 V supply for portable applications, a separate 5 V supply must be applied one time in the factories for programming and a low VF Schottky Diode should be designed with the AD5273 to isolate the supply voltages. Once the programming is done, the 5 V supply can be removed with V_{DD} maintained at 2.7 V for minimum operation. Figure 6b shows one such implementation.

CONTROLLING THE AD5273

There are two ways of controlling the AD5273. Users can either program the device with computer software or with external I²C controllers.

Software Programming

Due to the advantage of the one-time-programmable feature, most systems using the AD5273 will program the devices in the factories before shipping to the end users. As a result, ADI offers device programming software that can be implemented in the factory on computers running Windows NT, 2000, and XP platforms. The software can be downloaded from the AD5273 product folder at www.analog.com and is an executable file that does not require any programming languages or user programming skills. Figure 7 shows the software interface.

Write

The AD5273 starts at midscale after power up prior to any OTP programming. To increment or decrement the resistance, the user may simply move the scrollbar on the left. Once the desired setting is found, the user may press the Program Permanent button to lock the setting permanently. To write any specific values, the user should use the bit pattern control in the upper screen and press the Run button. The format of writing data to the device is shown in Table I. Once the desired setting is found, the user may turn the T bit to 1 and press the Run button to program the setting permanently.

Read

To read the validation bits and data out from the device, the user may simply press the Read button. The user may also set the bit pattern in the upper screen and press the Run button. The format of reading data out from the device is shown in Table II.

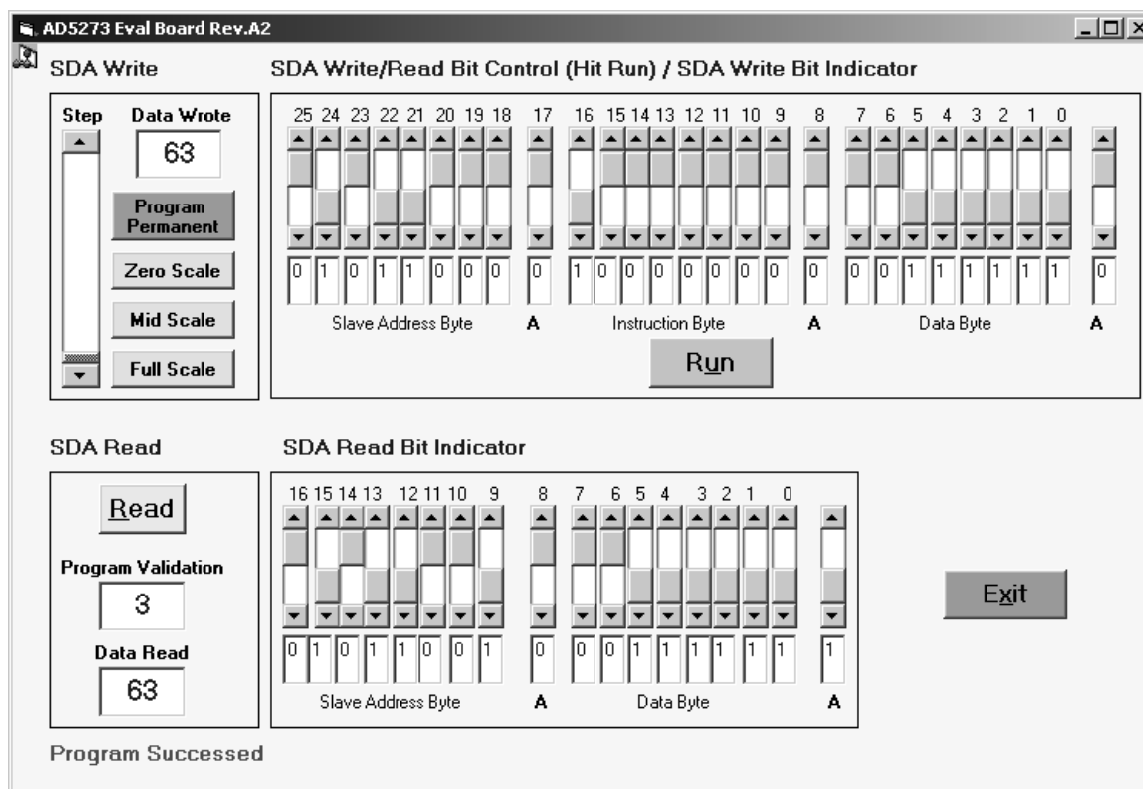


Figure 7. Computer Software

AD5273

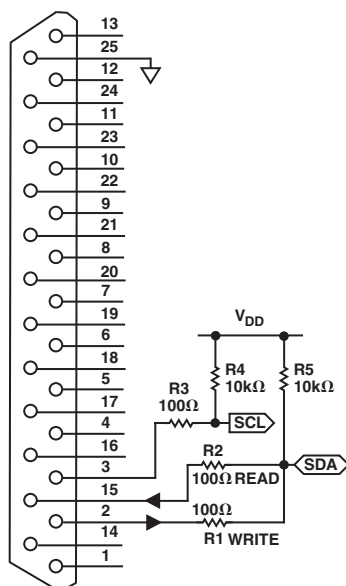


Figure 8. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND

In both Read and Write operations, the program generates the I²C digital signals through the parallel port LPT1 pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively, to control the device. See Figure 8.

To apply the device programming software in the factories, users may lay out the AD5273 SCL and SDA pads on the PCB such that the programming signals can be communicated to and from the parallel port. Figure 9 shows a recommended AD5273 PCB layout that pogo pins can be inserted for factory programming. 100 Ω resistors should also be put in series to the SCL and SDA pins to prevent damaging the PC parallel port. Pull-up resistors on SCL and SDA are also required.

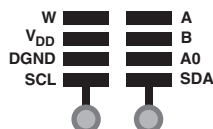


Figure 9. Recommended AD5273 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for programming. Refer to Figure 8.

For users who do not use the software solution, the AD5273 can be controlled via an I²C compatible serial bus and is connected to this bus as a slave device. Referring to Figures 10a, 10b, and 11, the 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when SDA goes from high to low while SCL is high, Figure 10a. The following byte is the Slave

Address byte, which consists of the 6 MSBs as slave address defined as 010110. The next bit is AD0; it is an I²C device address bit. Depending on the states of their AD0 bits, two AD5273s can be addressed on the same bus. (See Figure 12.) The last LSB is the R/W bit, which determines whether data will be read from or written to the slave device.

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. A Write operation contains one more Instruction byte than the Read operation. The Instruction byte in the Write mode follows the Slave Address byte. The MSB of the Instruction byte labeled T is the One Time Programming bit. After acknowledging the Instruction byte, the last byte in the Write mode is the Data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL. See Figure 10a.
3. In the Read mode, the Data byte follows immediately after the acknowledgment of the Slave Address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference with the Write mode, there are eight data bits followed by a No Acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL as shown in Figure 11.
4. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In the Write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition, Figures 10a and 10b. In the Read mode, the master will issue a No Acknowledge for the ninth clock pulse, i.e., the SDA line remains high. The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition. See Figure 11.

A repeated Write function gives the user flexibility to update the RDAC output a number of times, except after permanent programming, after addressing and instructing the part only once. During the Write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its Slave Address and Instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the Write mode has to be started with a new Slave Address, Instruction, and Data bytes again. Similarly, a repeated Read function of the RDAC is also allowed.

I²C Controller Programming

Write Bit Pattern Illustrations

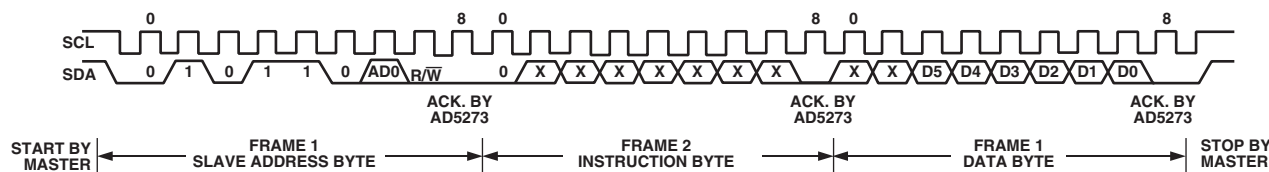


Figure 10a. Writing to the RDAC Register

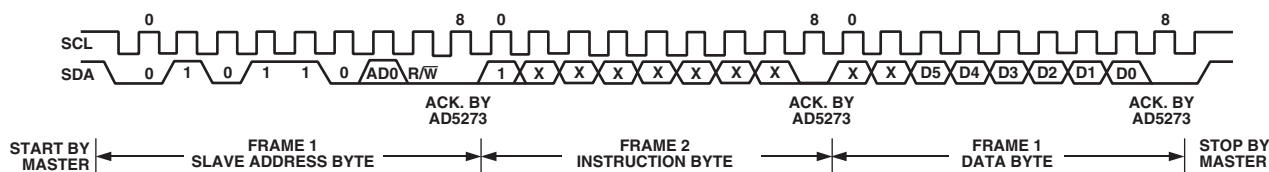


Figure 10b. Activating One Time Programming

Read Bit Pattern Illustration

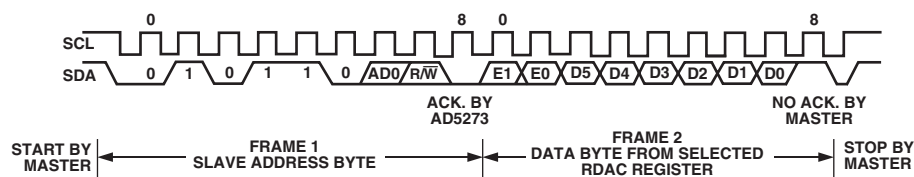


Figure 11. Reading Data From the RDAC Register

CONTROLLING TWO DEVICES ON ONE BUS

Figure 12 shows two AD5273 devices on the same serial bus. Each has a different slave address since the state of each AD0 pin is different. This allows each device to operate independently. The master device output bus line drivers are open-drain pull downs in a fully I²C compatible interface.

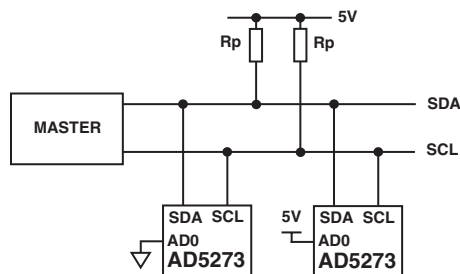


Figure 12. Two AD5273 Devices on One Bus

APPLICATIONS

Programmable Voltage Reference

For Voltage Divider mode operation, as shown in Figure 13, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB} . Not only does the buffer serve the purpose of impedance conversion, it also allows a heavier load to be driven.

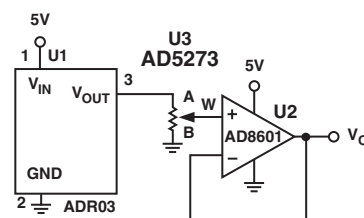


Figure 13. Programmable Voltage Reference

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment such as a laser diode driver or tunable laser, a boosted voltage source can be considered. See Figure 14.

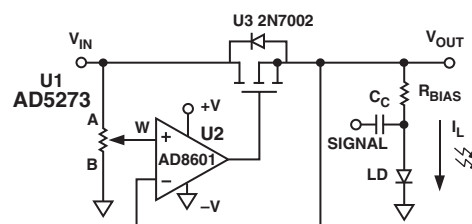


Figure 14. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch

AD5273

FET N_1 . N_1 power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at the A terminal of the digital potentiometer.

Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 15. The load current is simply the voltage across terminals B-to-W of the AD5273 divided by R_S . Notice at zero-scale, the A terminal of the AD5273 will be at -2.048 V, which makes the wiper voltage clamped at ground potential. Dependent on the load, Equation 5 is therefore valid only at certain codes. For example, when the compliance voltage V_L equals half of the V_{REF} , the current can be programmed from midscale to full-scale of the AD5273.

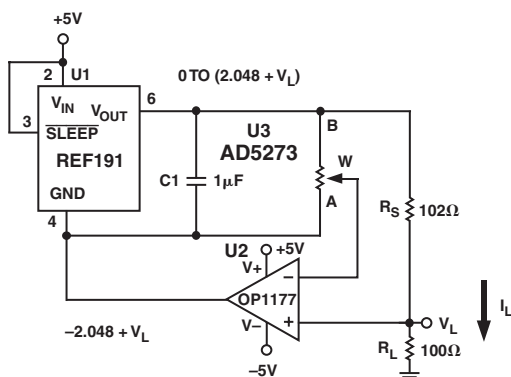


Figure 15. Programmable Current Source

$$I_L = \frac{(V_{REF} \times D) / 64}{R_S} \quad | \quad 32 \leq D \leq 63 \quad (5)$$

Gain Control Compensation

As seen in Figure 16, the digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications.

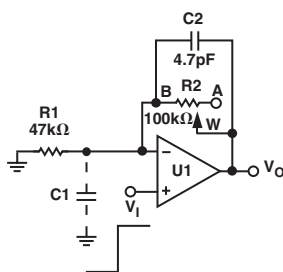


Figure 16. Typical Noninverting Gain Amplifier

In both applications, one of the digital potentiometer terminals is connected to the op amp inverting node with finite terminal capacitance $C1$. It introduces a zero for the $1/\beta_o$ term with 20 dB/dec whereas a typical op amp GBP has -20 dB/dec characteristics. A large $R2$ and finite $C1$ can cause this zero's frequency to fall well below the crossover frequency. Thus the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or in the worst case oscillate when

the input is a step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input. To reduce the effect of $C1$, users should also configure B or A rather than W terminal at the inverting node.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor $C2$ to cancel the effect caused by $C1$. Optimum compensation occurs when $R1 \times C1 = R2 \times C2$. This is not an option because of the variation of $R2$. As a result, one may use the relationship above and scale $C2$ as if $R2$ is at its maximum value. Doing so may overcompensate by slowing down the settling time when $R2$ is set at low values. As a result, $C2$ should be found empirically for a given application. In general, $C2$ in the range of a few pF to no more than a few tenths of a pF is adequate for the compensation.

There is also a W terminal capacitance connected to the output (not shown); its effect on stability is less significant so that the compensation may not be necessary unless the op amp is driving a large capacitive load.

Programmable Low-Pass Filter

In A/D conversion applications, it is common to include an anti-aliasing filter to band-limit the sampling signal. To minimize various system redesigns, users may use two 1 kΩ AD5273s to construct a generic second-order Sallen Key low-pass filter. Since the AD5273 is a single supply device, the input must be dc offset when an ac signal is applied to avoid clipping at ground. This is illustrated in Figure 17. The design equations are:

$$\frac{V_O}{V_I} = \frac{\omega_o^2}{S^2 + \frac{\omega_o}{Q}S + \omega_o^2} \quad (6)$$

$$\omega_o = \sqrt{\frac{1}{R1R2C1C2}} \quad (7)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (8)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where $Q = 0.707$, let $C1$ be twice the size of $C2$ and let $R1 = R2$. As a result, $R1$ and $R2$ can be adjusted to the same setting to achieve the desirable bandwidth.

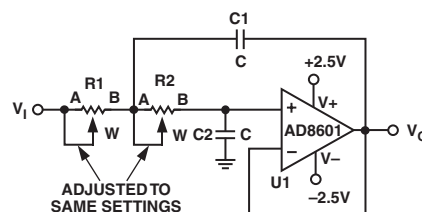


Figure 17. Sallen Key Low-Pass Filter

Level Shift for Different Voltages Operation

When users need to interface a 2.5 V controller with the AD5273, a proper voltage level shift must be employed so that the digital potentiometer can be read from or written to the controller; Figure 18 shows one of the implementations. M1 and M2 should be low threshold N-Ch Power MOSFETs such as FVD301N.

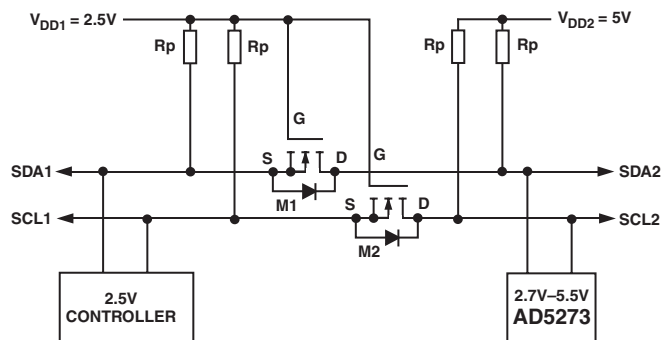


Figure 18. Level Shift for Different Voltage Operation

Resistance Scaling

The AD5273 offers 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ nominal resistances. For users who need to optimize the resolution with an arbitrary full-range resistance, the following techniques can be the solutions. Applicable only to the voltage divider mode, by paralleling a discrete resistor as shown in Figure 19, a proportionately lower voltage appears at terminal A–B. This translates into a finer degree of precision because the step size at terminal W will be smaller. The voltage can be found as:

$$V_W(D) = \frac{(R_{AB} // R2)}{R3 + R_{AB} // R2} \times \frac{D}{256} \times V_{DD} \quad (9)$$

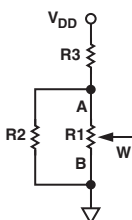


Figure 19. Lowering the Nominal Resistance

Figure 19 shows that the digital potentiometer changes steps linearly. On the other hand, log taper adjustment is usually preferred in applications like volume control. Figure 20 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to RAB, the more the pseudo log taper characteristic it behaves. The wiper voltage is simply:

$$V_W(D) = \frac{R_{WB}(D) // R2}{R_{WA}(D) + R_{WB}(D) // R2} \times V_I \quad (10)$$

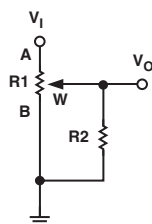


Figure 20. Resistor Scaling with Log Adjustment Characteristics

Resolution Enhancement

Borrowed from ADI's patented RDAC segmentation technique, users can configure three AD5273s to double the resolution. (See Figure 21.) First, U3 must be paralleled with a discrete resistor Rp that is chosen to be equal to a step resistance (Rp = RAB/64). We may see that adjusting U1 and U2 together forms the coarse 6-bit adjustment and adjusting U3 alone forms the finer 6-bit adjustment. As a result, the effective resolution becomes 12-bit.

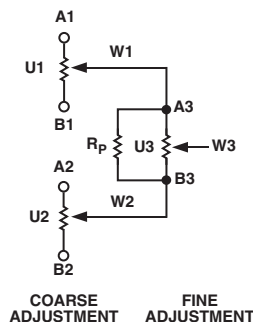


Figure 21. Double the Resolution in Rheostat Mode Operation

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5273 (1 kΩ resistor) measures 6 MHz at half scale. TPCs 15–18 provide the large signal BODE plot characteristics of the four available resistor versions 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. Figure 22 shows a parasitic simulation model. The code following Figure 22 provides a macro model net list for the 1 kΩ device:

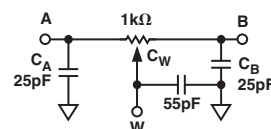


Figure 22. Circuit Simulation Model for RDAC = 1 kΩ

Macro Model Net List for RDAC

```
.PARAM D = 63, RDAC = 1E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A      0      25E-12
RWA     A      W      {(1-D/63)*RDAC+60}
CW      W      0      55E-12
RWB     W      B      {D/63*RDAC+60}
CB      B      0      25E-12
*
.ENDS DPOT
```

AD5273

EVALUATION BOARD

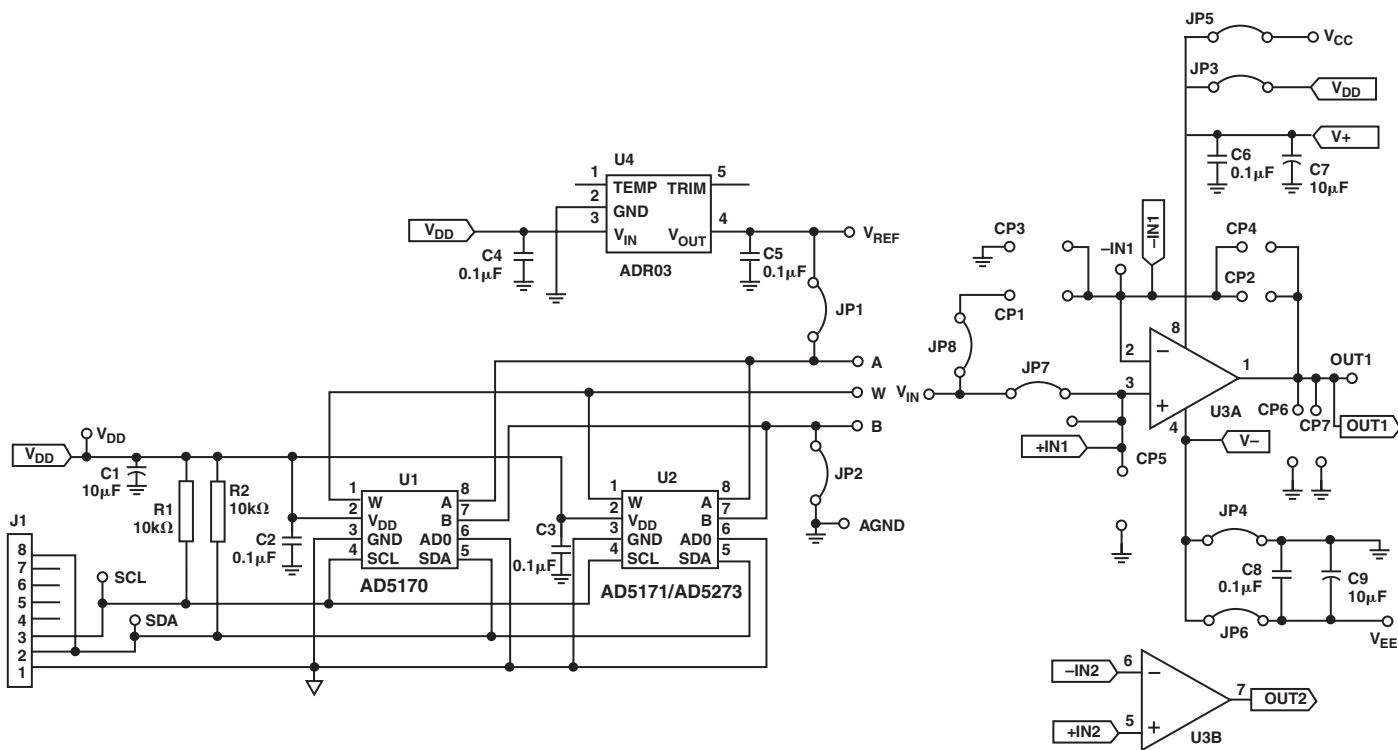


Figure 23. Evaluation Board Schematic

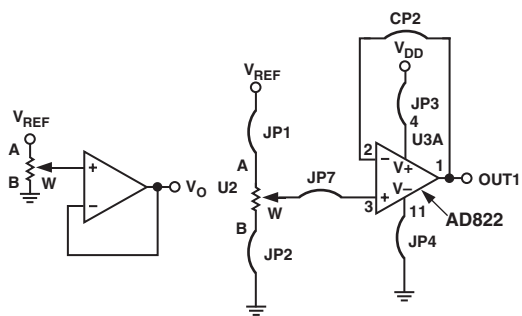


Figure 24. One of the Possible Configurations: Programmable Voltage Reference

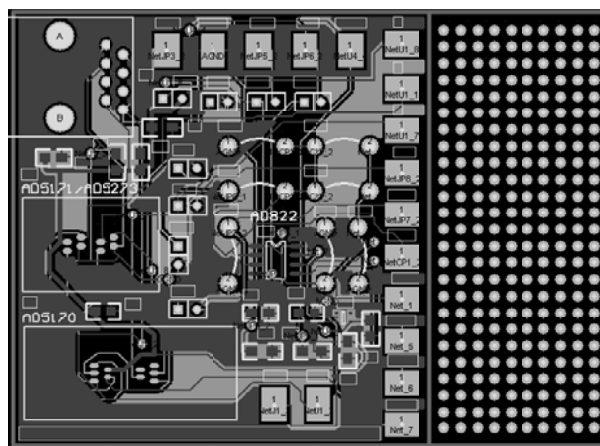


Figure 25. Evaluation Board

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE*

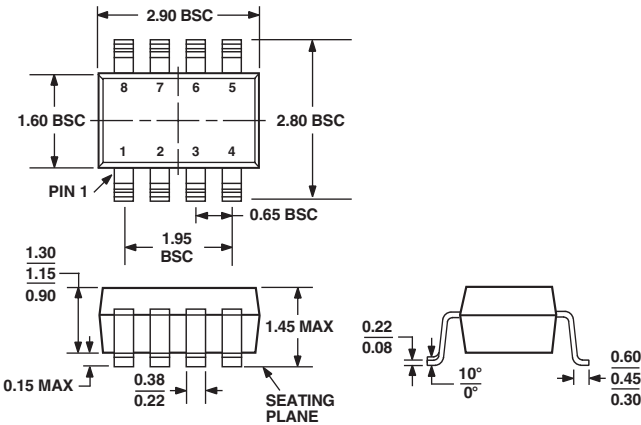
Part Number	Number of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (k Ω)	Resolution (No. of Wiper Positions)	Power Supply Current (I _{DD}) (μ A)	Packages	Comments
AD5201	1	$\pm 3, 5.5$	3-wire	10, 50	33	40	MSOP-10	Full AC Specs, Dual Supply, Power-On-Reset, Low Cost
AD5220	1	5.5	UP/DOWN	10, 50, 100	128	40	PDIP, SOIC-8, MSOP-8	No Rollover, Power-On-Reset
AD7376	1	$\pm 15, 28$	3-wire	10, 50, 100, 1000	128	100	PDIP-14, SOIC-16, TSSOP-14	Single 28 V or Dual ± 15 V Supply Operation
AD5200	1	$\pm 3, 5.5$	3-wire	10, 50	256	40	MSOP-10	Full AC Specs, Dual Supply, Power-On-Reset
AD8400	1	5.5	3-wire	1, 10, 50, 100	256	5	SOIC-8	Full AC Specs
AD5260	1	$\pm 5, 15$	3-wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ± 5 V Operation, TC < 50 ppm/ $^{\circ}$ C
AD5280	1	$\pm 5, 15$	2-wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ± 5 V Operation, TC < 50 ppm/ $^{\circ}$ C
AD5241	1	$\pm 3, 5.5$	2-wire	10, 100, 1000	256	50	SOIC-14, TSSOP-14	I ² C Compatible, TC < 50 ppm/ $^{\circ}$ C
AD5231	1	$\pm 2.75, 5.5$	3-wire	10, 50, 100	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ± 6 dB Settability
AD5222	2	$\pm 3, 5.5$	UP/DOWN	10, 50, 100, 1000	128	80	SOIC-14, TSSOP-14	No Rollover, Stereo, Power-On-Reset, TC < 50 ppm/ $^{\circ}$ C
AD8402	2	5.5	3-wire	1, 10, 50, 100	256	5	PDIP, SOIC-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5207	2	$\pm 3, 5.5$	3-wire	10, 50, 100	256	40	TSSOP-14	Full AC Specs, Dual Supply, Power-On-Reset, SDO
AD5232	2	$\pm 2.75, 5.5$	3-wire	10, 50, 100	256	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ± 6 dB Settability
AD5235	2	$\pm 2.75, 5.5$	3-wire	25, 250	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/ $^{\circ}$ C
AD5242	2	$\pm 3, 5.5$	2-wire	10, 100, 1000	256	50	SOIC-16, TSSOP-16	I ² C Compatible, TC < 50 ppm/ $^{\circ}$ C
AD5262	2	$\pm 5, 15$	3-wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ± 5 V Operation, TC < 50 ppm/ $^{\circ}$ C
AD5282	2	$\pm 5, 15$	3-wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ± 5 V Operation, TC < 50 ppm/ $^{\circ}$ C
AD5203	4	5.5	3-wire	10, 100	64	5	PDIP, SOIC-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5233	4	$\pm 2.75, 5.5$	3-wire	10, 50, 100	64	20	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ± 6 dB Settability
AD5204	4	$\pm 3, 5.5$	3-wire	10, 50, 100	256	60	PDIP, SOIC-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset
AD8403	4	5.5	3-wire	1, 10, 50, 100	256	5	PDIP, SOIC-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	$\pm 3, 5.5$	3-wire	10, 50, 100	256	60	PDIP, SOIC-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset

*For the most current information on digital potentiometers, check the website at: www.analog.com/digitalpotentiometers

OUTLINE DIMENSIONS

8-Lead Plastic Surface-Mount Package [SOT-23]
(RT-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178BA