

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC164FN

8-Bit Shift Register (S-IN, P-OUT)

The TC74AC164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

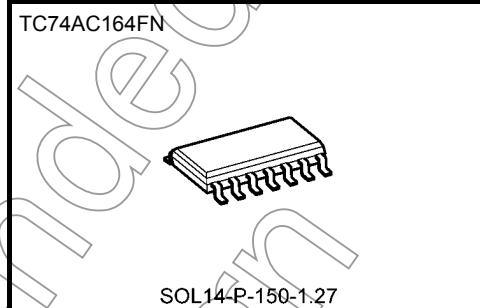
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding CLEAR input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Note: xxxFN (JEDEC SOP) is not available in Japan.



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Weight

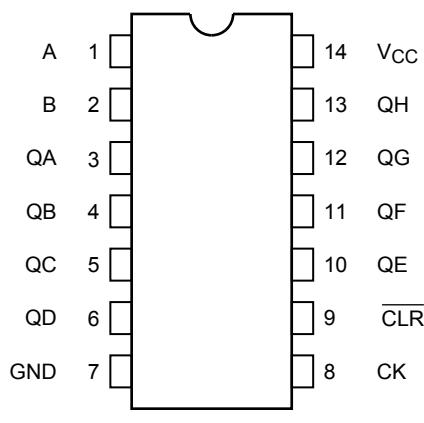
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: 0.12 g (typ.)

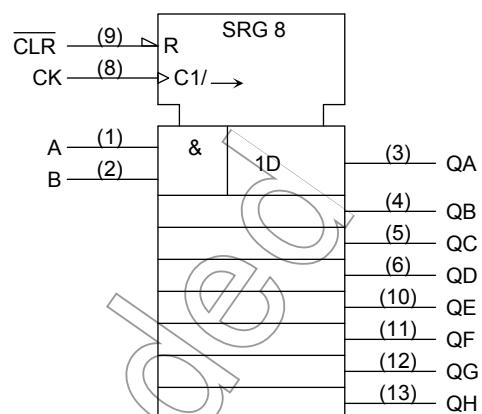
Features

- High speed: $f_{max} = 170$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Symmetrical output impedance:
 $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 V to 5.5 V
- Pin and function compatible with 74F164

Pin Assignment



IEC Logic Symbol



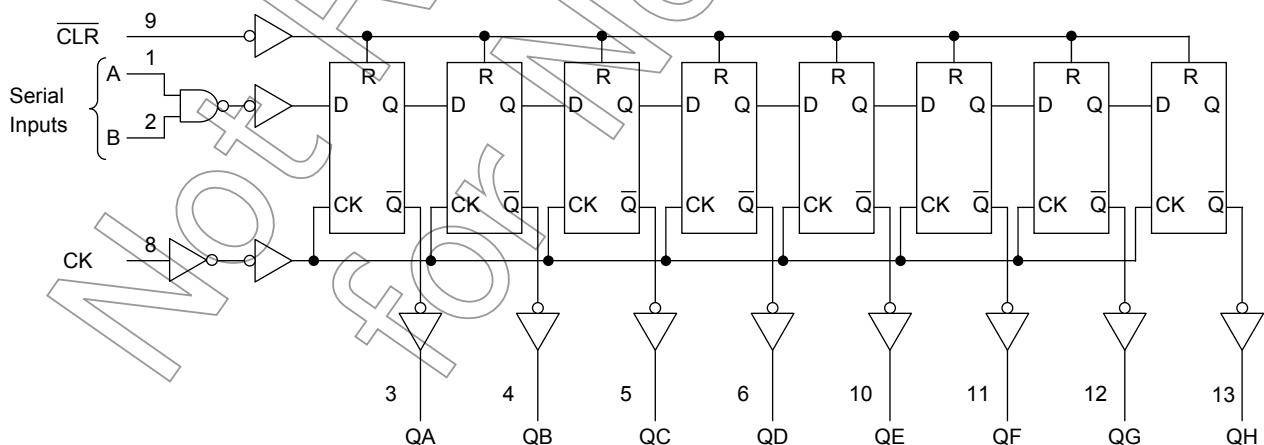
Truth Table

Inputs			Outputs				
$\overline{\text{CLR}}$	CK	Serial In		QA	QB	...	QH
		A	B	L	L	...	L
L	X	X	X	L	L	...	L
H		X	X	No Change			
H		L	X	L	QA _n	...	QG _n
H		X	L	L	QA _n	...	QG _n
H		H	H	QA _n	...	QG _n	

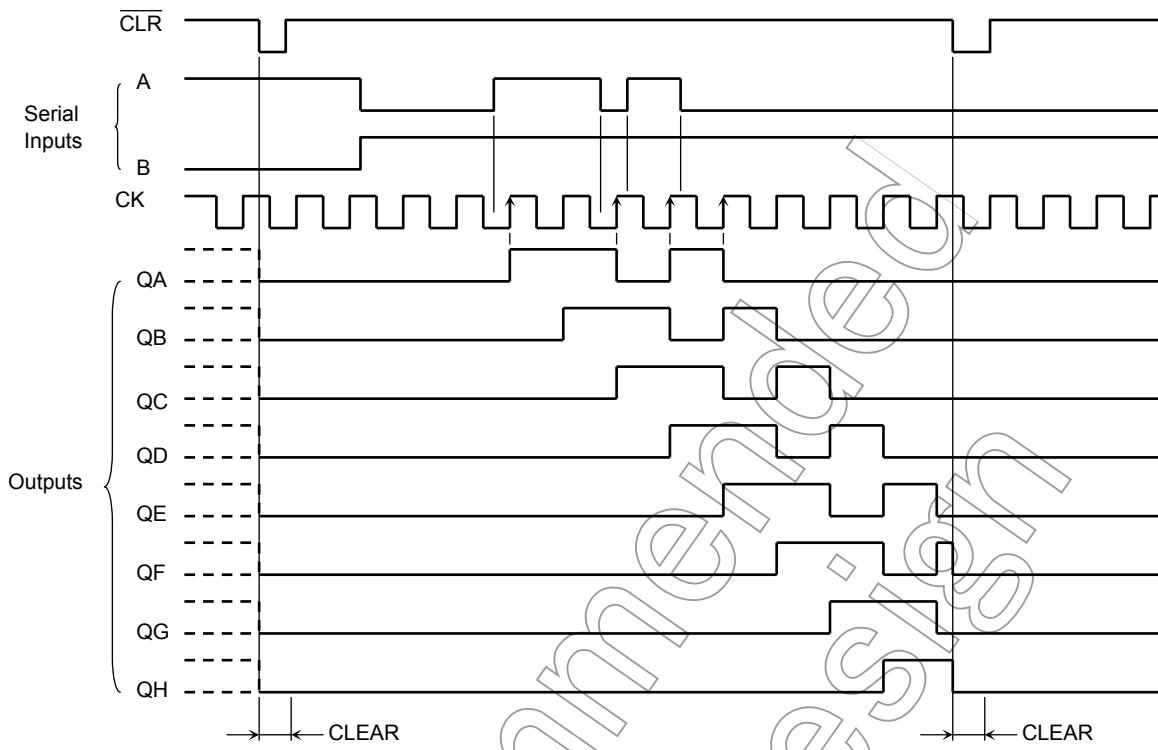
X: Don't care

QA_n to QG_n: The level of QA to QG, respectively, before the most recent positive edge of the clock.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 200	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 5.5	V
Input voltage	V _{IN}	0 to V _{CC}	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V _{CC} = 3.3 ± 0.3 V) 0 to 20 (V _{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
		V _{CC} (V)	Min	Typ.	Max	Min	Max		
High-level input voltage	V _{IH}	—	2.0	1.50	—	—	1.50	—	V
			3.0	2.10	—	—	2.10	—	
			5.5	3.85	—	—	3.85	—	
Low-level input voltage	V _{IL}	—	2.0	—	—	0.50	—	0.50	V
			3.0	—	—	0.90	—	0.90	
			5.5	—	—	1.65	—	1.65	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	2.0	1.9	2.0	—	1.9	—	V
			3.0	2.9	3.0	—	2.9	—	
			4.5	4.4	4.5	—	4.4	—	
			3.0	2.58	—	—	2.48	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	4.5	3.94	—	—	3.80	—	V
			5.5	—	—	—	3.85	—	
			2.0	—	0.0	0.1	—	0.1	
			3.0	—	0.0	0.1	—	0.1	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	4.5	—	0.0	0.1	—	0.1	μA
			3.0	—	—	—	—	—	
			4.5	—	—	—	—	—	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	3.0	—	—	0.36	—	0.44	μA
			4.5	—	—	0.36	—	0.44	
			5.5	—	—	—	—	1.65	

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		$T_a = 25^\circ C$		$T_a = -40$ to $85^\circ C$	Unit
			V_{CC} (V)	Limit	Limit		
Minimum pulse width (CK)	t_w (L)	—	3.3 ± 0.3	9.0	10.0	ns	
	t_w (H)		5.0 ± 0.5	5.0	6.0		
Minimum pulse width (\overline{CLR})	t_w (L)	—	3.3 ± 0.3	9.0	10.0	ns	
			5.0 ± 0.5	5.0	6.0		
Minimum set-up time	t_s	—	3.3 ± 0.3	7.0	7.0	ns	
			5.0 ± 0.5	4.0	4.0		
Minimum hold time	t_h	—	3.3 ± 0.3	1.0	1.0	ns	
			5.0 ± 0.5	1.0	1.0		
Minimum removal time (\overline{CLR})	t_{rem}	—	3.3 ± 0.3	8.5	8.5	ns	
			5.0 ± 0.5	5.0	5.0		

AC Characteristics ($C_L = 50$ pF, $R_L = 500$ Ω , input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		$T_a = 25^\circ C$			$T_a = -40$ to $85^\circ C$		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{PLH}	—	3.3 ± 0.3	—	9.6	16.3	1.0	18.6	ns
	t_{PHL}		5.0 ± 0.5	—	6.6	9.8	1.0	11.2	
Propagation delay time (\overline{CLR} -Q)	t_{PHL}	—	3.3 ± 0.3	—	8.0	15.4	1.0	17.5	ns
			5.0 ± 0.5	—	6.0	11.0	1.0	12.5	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	45	100	—	45	—	MHz
			5.0 ± 0.5	85	150	—	80	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}		(Note)	—	110	—	—	—	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

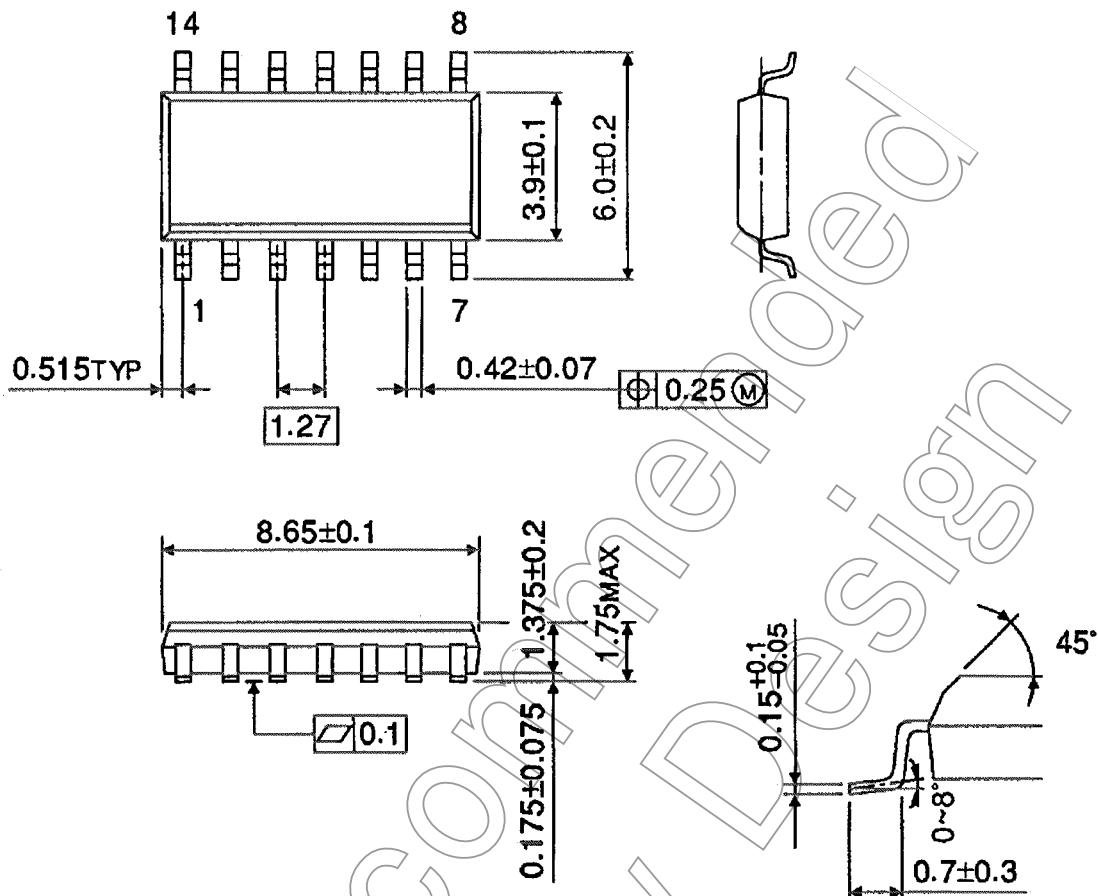
Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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