

May 1995

20A, 1000V N-Channel IGBT

Features

- 34A, 1000V
- Latch Free Operation
- Typical Fall Time 520ns
- High Input Impedance
- Low Conduction Loss

Description

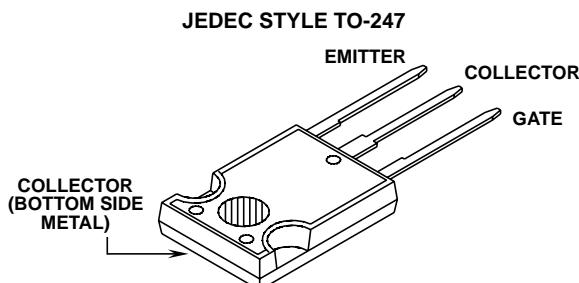
The HGTG20N100D2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

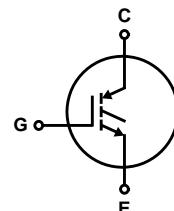
PART NUMBER	PACKAGE	BRAND
HGTG20N100D2	TO-247	G20N100D2

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 600V$, $T_C = +125^{\circ}C$, $R_{GE} = 25\Omega$.

INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Specifications HGTG20N100D2

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\text{mA}$, $V_{\text{GE}} = 0\text{V}$	1000	-	-	V	
Collector-Emitter Leakage Voltage	I_{CES}	$V_{\text{CE}} = \text{BV}_{\text{CES}}$, $T_C = +25^\circ\text{C}$	-	-	250	μA	
		$V_{\text{CE}} = 0.8 \text{ BV}_{\text{CES}}$, $T_C = +125^\circ\text{C}$	-	-	1.0	mA	
Collector-Emitter Saturation Voltage	$V_{\text{CE}(\text{SAT})}$	$I_C = I_{\text{C90}}$, $V_{\text{GE}} = 15\text{V}$, $T_C = +25^\circ\text{C}$	-	3.1	3.8	V	
		$T_C = +125^\circ\text{C}$	-	2.9	3.6	V	
		$I_C = I_{\text{C90}}$, $V_{\text{GE}} = 10\text{V}$, $T_C = +25^\circ\text{C}$	-	3.3	4.1	V	
		$T_C = +125^\circ\text{C}$	-	3.2	4.0	V	
Gate-Emitter Threshold Voltage	$V_{\text{GE}(\text{TH})}$	$I_C = 500\mu\text{A}$, $V_{\text{CE}} = V_{\text{GE}}$	$T_C = +25^\circ\text{C}$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{\text{GE}} = \pm 20\text{V}$	-	-	± 250	nA	
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{\text{C90}}$, $V_{\text{CE}} = 0.5 \text{ BV}_{\text{CES}}$	-	7.1	-	V	
On-State Gate Charge	$Q_{\text{G}(\text{ON})}$	$I_C = I_{\text{C90}}$, $V_{\text{GE}} = 15\text{V}$	-	120	160	nC	
		$V_{\text{CE}} = 0.5 \text{ BV}_{\text{CES}}$	-	163	212	nC	
Current Turn-On Delay Time	$t_{\text{D}(\text{ON})\text{I}}$	$L = 50\mu\text{H}$, $I_C = I_{\text{C90}}$, $R_G = 25\Omega$, $V_{\text{GE}} = 15\text{V}$, $T_J = +125^\circ\text{C}$, $V_{\text{CE}} = 0.8 \text{ BV}_{\text{CES}}$	-	100	-	ns	
Current Rise Time	t_{RI}		-	150	-	ns	
Current Turn-Off Delay Time	$t_{\text{D}(\text{OFF})\text{I}}$		-	500	650	ns	
Current Fall Time	t_{FI}		-	520	680	ns	
Turn-Off Energy (Note 1)	W_{OFF}		-	3.7	-	mJ	
Current Turn-On Delay Time	$t_{\text{D}(\text{ON})\text{I}}$	$L = 50\mu\text{H}$, $I_C = I_{\text{C90}}$, $R_G = 25\Omega$, $V_{\text{GE}} = 10\text{V}$, $T_J = +125^\circ\text{C}$, $V_{\text{CE}} = 0.8 \text{ BV}_{\text{CES}}$	-	100	-	ns	
Current Rise Time	t_{RI}		-	150	-	ns	
Current Turn-Off	$t_{\text{D}(\text{OFF})\text{I}}$		-	410	530	ns	
Current Fall Time	t_{FI}		-	520	680	ns	
Turn-Off Energy (Note 1)	W_{OFF}		-	3.7	-	mJ	
Thermal Resistance	$R_{\theta\text{JC}}$		-	0.7	0.83	$^\circ\text{C}/\text{W}$	

NOTE: 1. Turn-Off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{\text{CE}} = 0\text{A}$) The HGTG20N100D2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

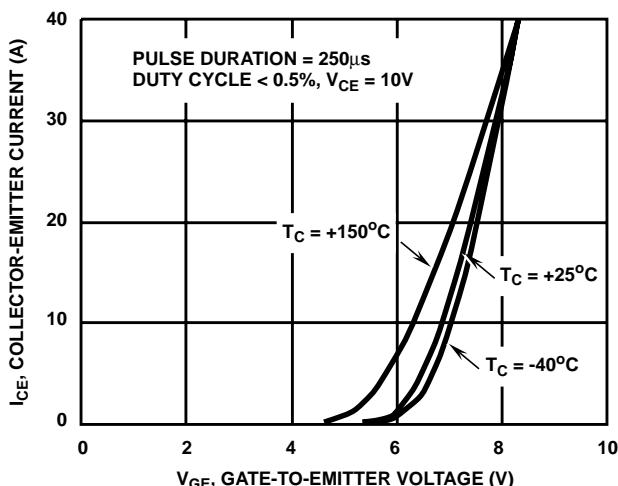


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

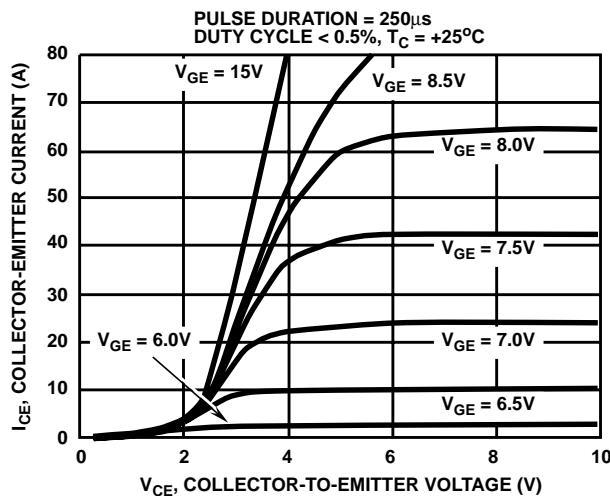


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

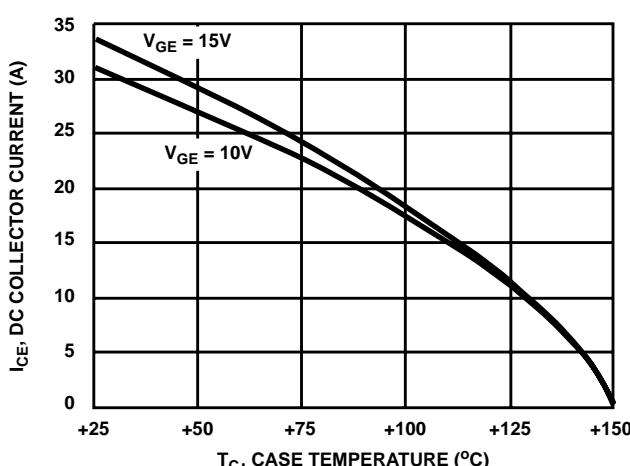


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

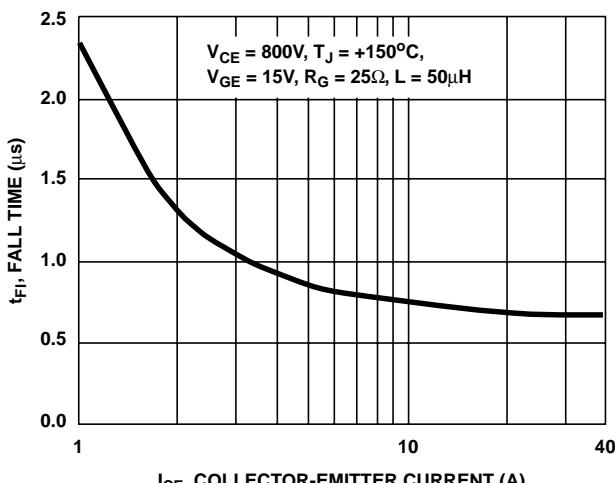


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

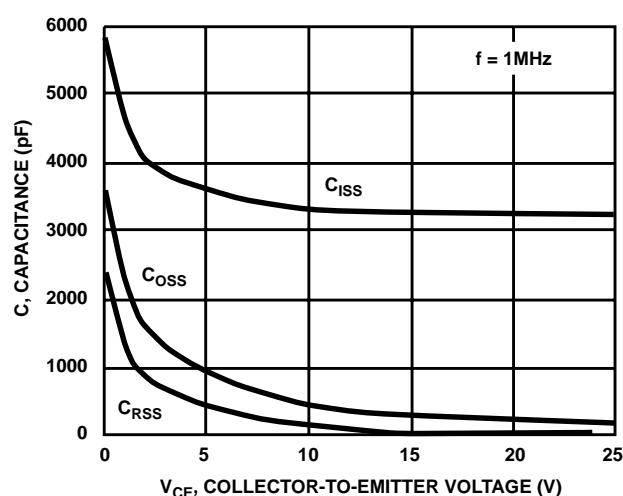


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

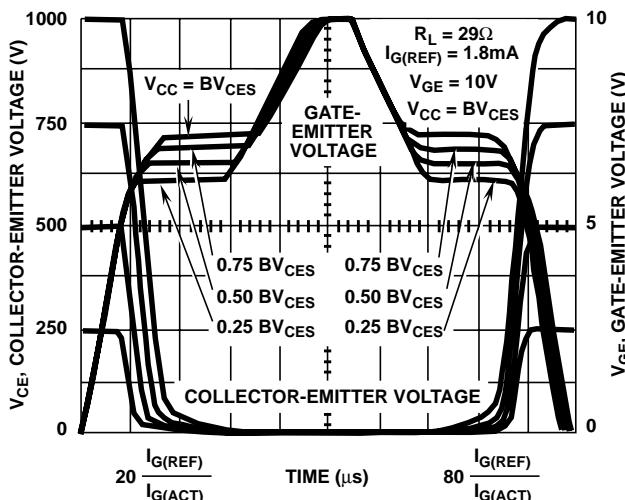


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

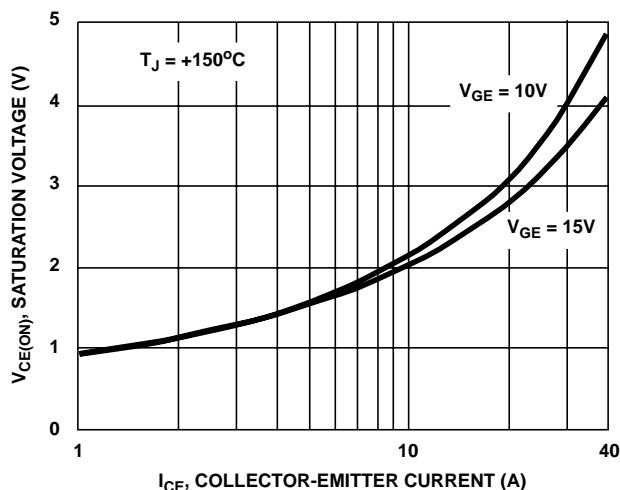


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

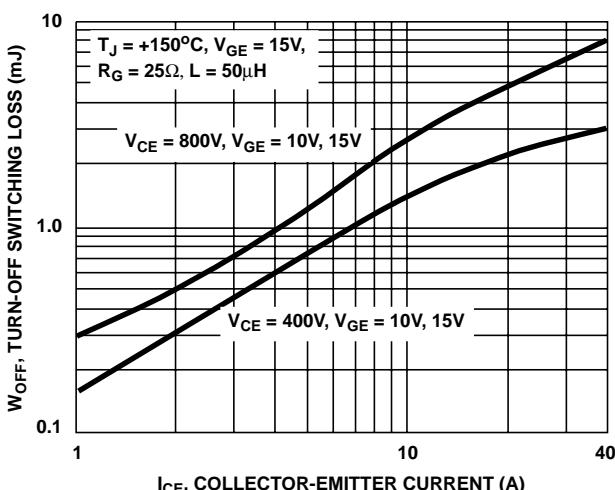


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

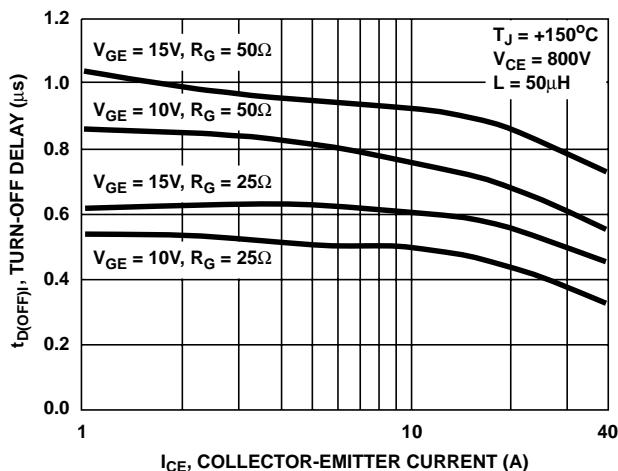


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT

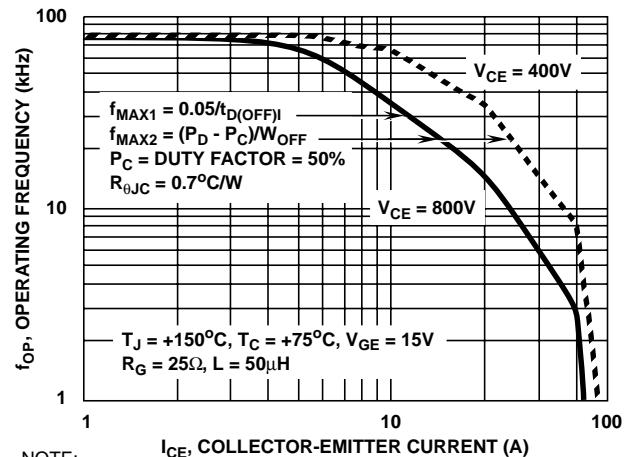


FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

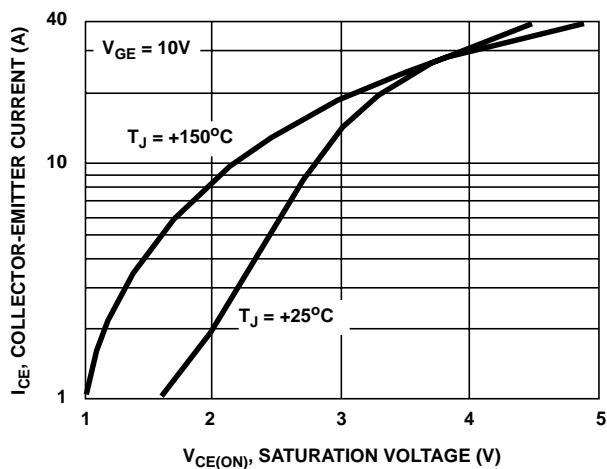


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

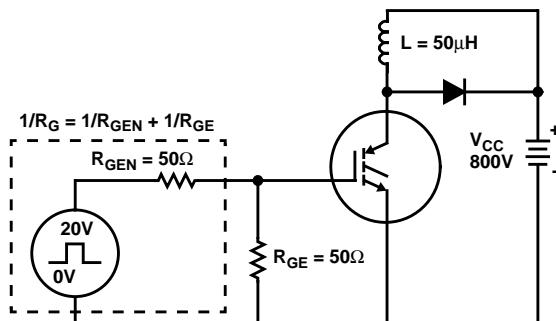


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device

turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX} . $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{eJC}$. The sum of device switching and conduction losses must not exceed P_D . A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \cdot I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \cdot W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.