

**1M X 9,
1M X 8 BIT FAST PAGE MODE
CMOS DYNAMIC RAM MEMORY MODULE**

HIGH PERFORMANCE V404J8/9	60/60L	70/70L	80/80L	10/10L
Max. <u>RAS</u> Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	160 ns	180 ns

LOW POWER V404J8/9L	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.8/2mA	0.8/1 mA	0.8/1 mA	0.8/1 mA

Features

- 1M x 8 and 1M x 9-bit organization
- Utilizes 1M x 4 and 1M x 1 CMOS DRAMs
- RAS access time: 60, 70, 80, 100 ns
- Low power dissipation
 - V404J8/9-80
 - Operating Current – 160/230 mA max.
 - TTL Standby Current – 4/6 mA max.
- Low CMOS Standby Current
 - V404J8/9 – 2/3 mA max.
 - V404J8/9L – 0.8/1 mA max.
- Battery Back-up Mode (V404J8/9L Only)
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh capability
- Refresh Interval
 - V404J8/9 – 1024 cycles/16ms
 - V404J8/9L – 1024 cycles/64ms
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in standard 30-lead single-in-line module

Description

The V404J8/9 are high speed 1,048,576 x 8/9 bit CMOS dynamic random access memory modules. The V404J8/9 offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V404J8/9L).

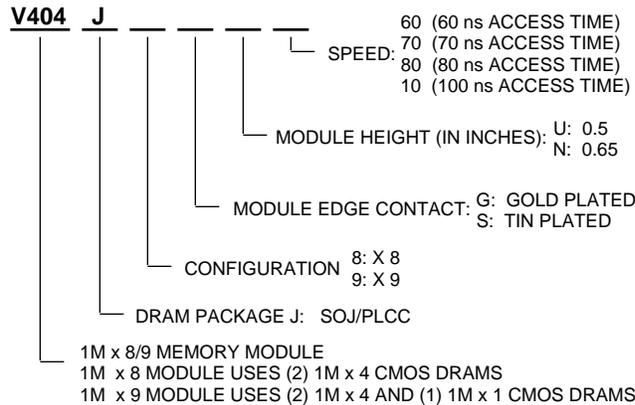
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 bits within a row with cycle times as short as 45 ns. Because of static circuitry, the CAS clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V404J8/9L ideally suited for high performance computing systems.

The V404J8/9L offer a maximum data retention power of 6.6/8.3 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles.

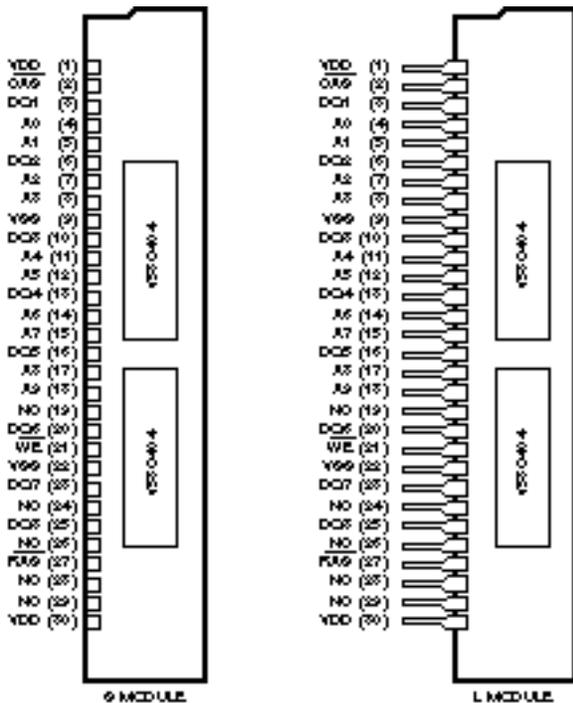
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)				Power	
	x 8	x 9	S	L	60	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•	•

Part Number Information



Pin Configuration
 x 8 Organization



Pin Names (x 8 Organization)

Name	Description
A0-A9	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobes
WE	Write Enable
DQ1-DQ8	Data In/Data Out
V _{DD}	5 V Supply
V _{SS}	Ground
NC	No Connection

Capacitance* (x8 Organization)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C _{IN}	Input Capacitance, Address Inputs		30	pF
C _{IN}	Input Capacitance, RAS, WE		30	pF
C _{IN(DQ)}	Input Capacitance, Data Inputs		15	pF
C _{IN(CAS)}	Input Capacitance, CAS		30	pF

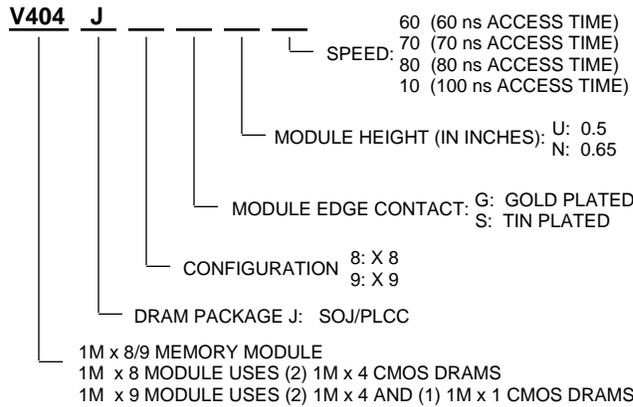
*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

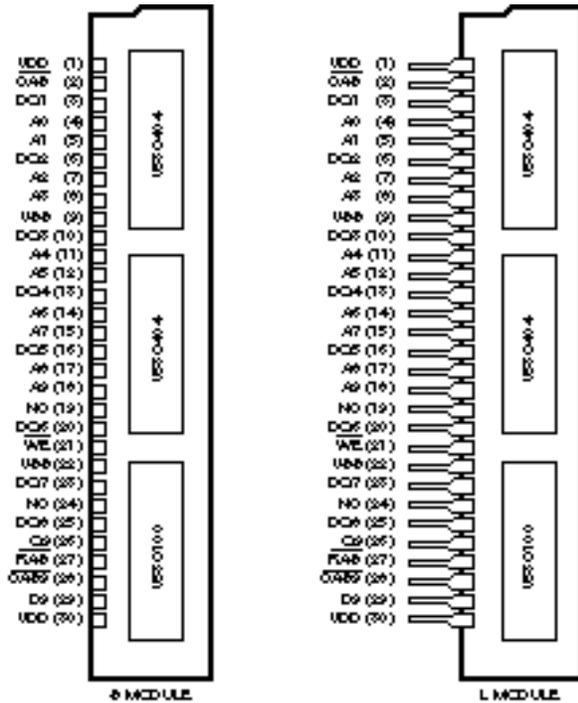
Ambient Temperature
 Under Bias -10°C to +80°C
 Storage Temperature (plastic) -55°C to +125°C
 Voltage Relative to V_{SS} -1.0 to +7.0 V
 Data Out Current 50 mA
 Power Dissipation 9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Part Number Information



Pin Configuration x 9 Organization



Pin Names (x 9 Organization)

Name	Description
A0-A9	Address Inputs
RAS	Row Address Strobe
CAS, CAS9	Column Address Strobes
WE	Write Enable
DQ1-DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V _{DD}	5 V Supply
V _{SS}	Ground
NC	No Connection

Capacitance* (x9 Organization)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C _{IN}	Input Capacitance, Address Inputs		30	pF
C _{IN}	Input Capacitance, RAS, WE		30	pF
C _{IN(DQ)}	Input Capacitance, Data Inputs		15	pF
C _{IN(CAS)}	Input Capacitance, CAS		30	pF
C _{IN(CAS9)}	Input Capacitance, CAS9		10	pF
C _{IN(D9)}	Input Capacitance, D9		10	pF
C _{O(Q9)}	Output Capacitance, Q9		10	pF
C _{O(VDD)}	Decoupling Capacitance	0.2		μF

Absolute Maximum Ratings*

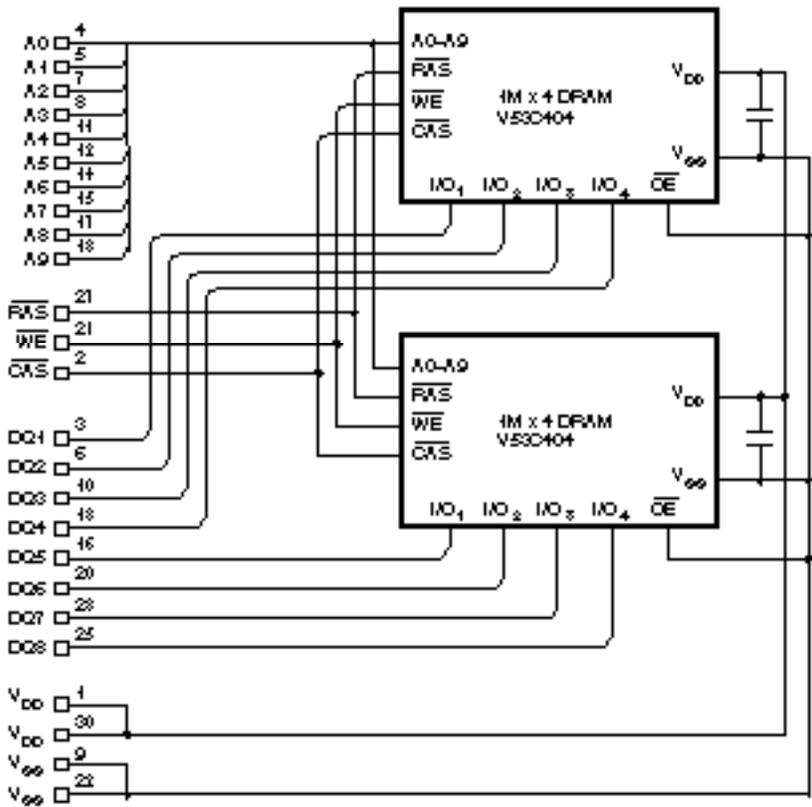
Ambient Temperature
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 Voltage Relative to V_{SS} -1.0 to +7.0 V
 Data Out Current 50 mA
 Power Dissipation 9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Note: Capacitance is sampled and not 100% tested.

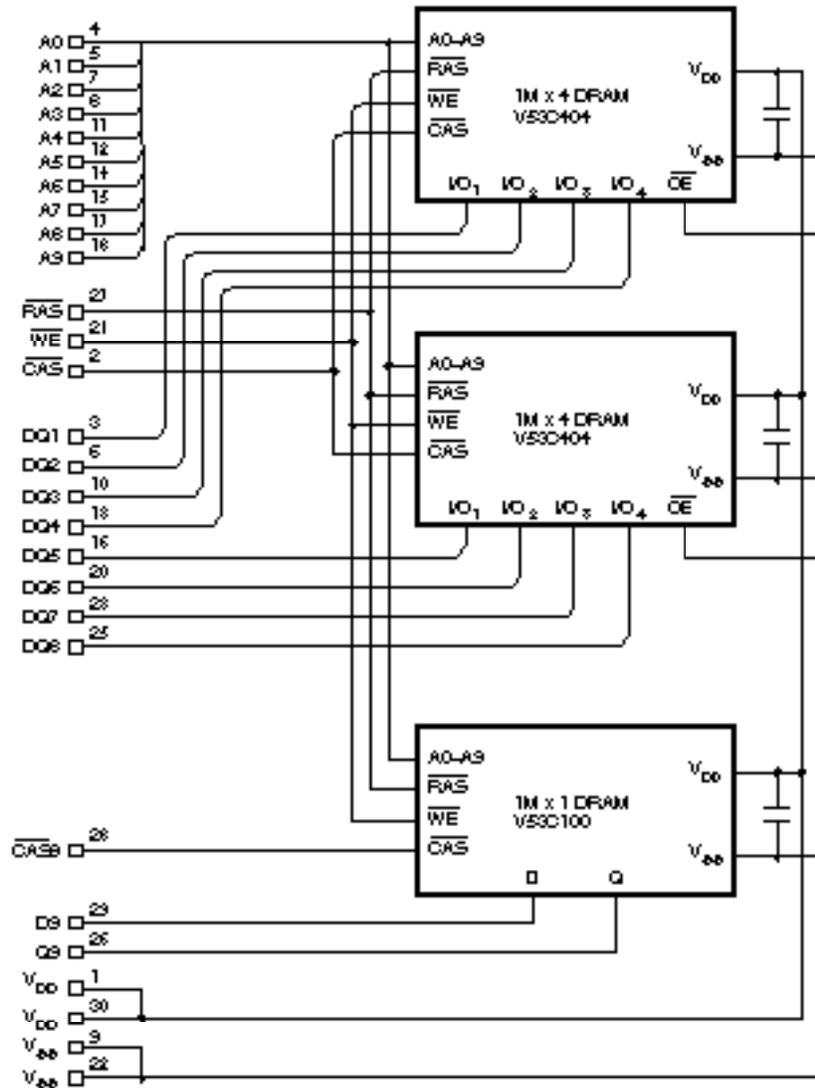
Functional Diagram

x 8 Organization



Functional Diagram

x 9 Organization



DC and Operating Characteristics (1-2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Power	Access Time	V404J8		V404J9		Unit	Test Conditions	Notes
				Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)			-20	20	-30	30	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			-10	10	-10	10	μA	$V_{SS} \leq V_{OUT} \leq V_{DD}$ <u>RAS</u> , <u>CAS</u> at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		60		190		280	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
			70		180		260			
			80		160		230			
			100		140		200			
I_{DD2}	V_{DD} Supply Current, TTL Standby				4		6	mA	<u>RAS</u> , <u>CAS</u> at V_{IH} other inputs $\geq V_{SS}$	
I_{DD3}	V_{DD} Supply Current, <u>RAS</u> -Only Refresh,		60		190		280	mA	$t_{RC} = t_{RC}(\text{min.})$	2
			70		180		260			
			80		160		230			
			100		140		200			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		60		190		270	mA	Minimum Cycle	1, 2
			70		160		250			
			80		140		200			
			100		120		175			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			10		13	mA	<u>RAS</u> = V_{IH} , <u>CAS</u> = V_{IL} other inputs $\geq V_{SS}$	
		LOW			8		10			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			2		3	mA	<u>RAS</u> $\geq V_{DD} - 0.2\text{ V}$ <u>CAS</u> $\geq V_{DD} - 0.2\text{ V}$ other inputs $\geq V_{SS}$	
		LOW			0.8		1			
I_{DD7}	Battery Back-up Data Retention Current (Only V404J8/9L)	LOW			1.2		1.5	mA	<u>CAS</u> -Before- <u>RAS</u> Refresh cycle $t_{RC} = 62.5\ \mu\text{s}$ CMOS clock levels	18
V_{IL}	Input Low Voltage			-1.0	0.8	-1.0	0.8	V		3
V_{IH}	Input High Voltage			2.4	$V_{DD}+1$	2.4	$V_{DD}+1$	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	$I_{OL} = 4.2\text{ mA}$	
V_{OH}	Output High Voltage			2.4		2.4			$I_{OH} = -5\text{ mA}$	

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted

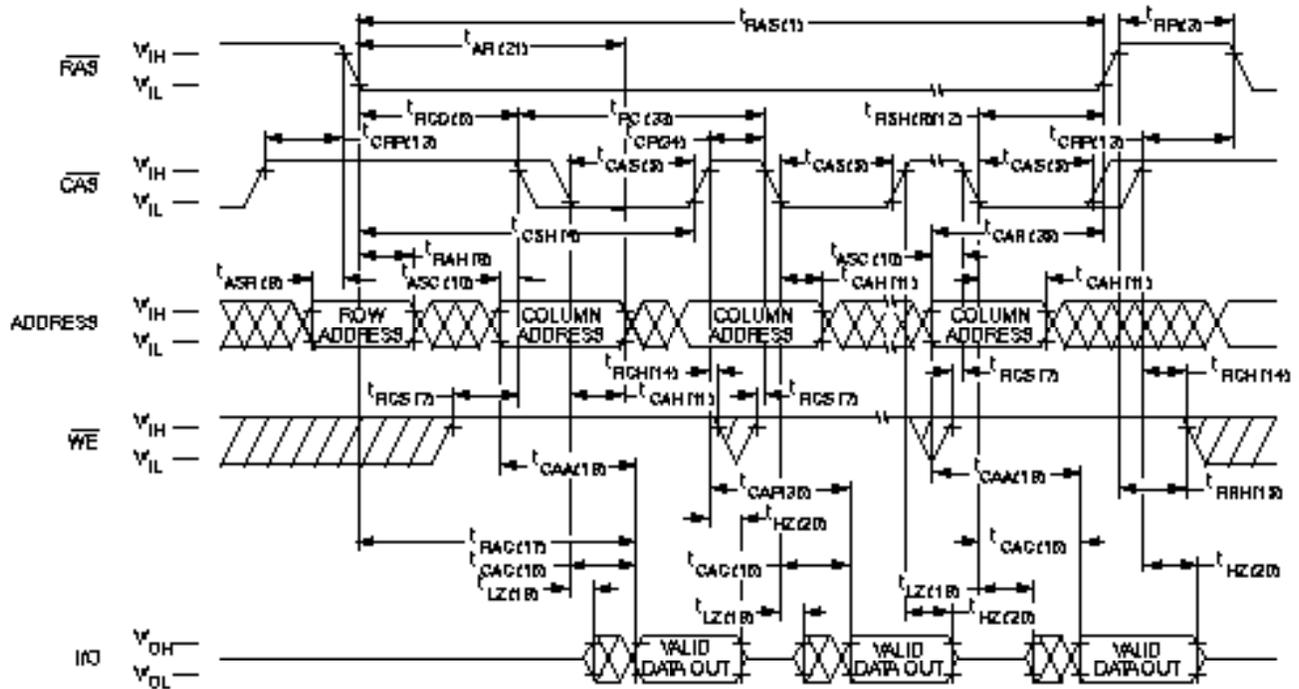
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	<u>RAS</u> Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	<u>RAS</u> Precharge Time	50		50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	<u>CAS</u> Hold Time	60		70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	<u>CAS</u> Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
6	t_{RL1CL1}	t_{RCD}	<u>RAS</u> to <u>CAS</u> Delay	20		20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	<u>RAS</u> Hold Time (Read Cycle)	15		20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	<u>CAS</u> to <u>RAS</u> Precharge Time	5		5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to <u>CAS</u>	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to <u>RAS</u>	0		0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from <u>CAS</u>		15		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from <u>RAS</u>		60		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		50	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	<u>CAS</u> to Low-Z Output	0		0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	<u>CAS</u> to High-Z Output	0	20	0	20	0	25	0	25	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from <u>RAS</u>	50		55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	<u>RAS</u> to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	11

AC Characteristics (Cont'd.)

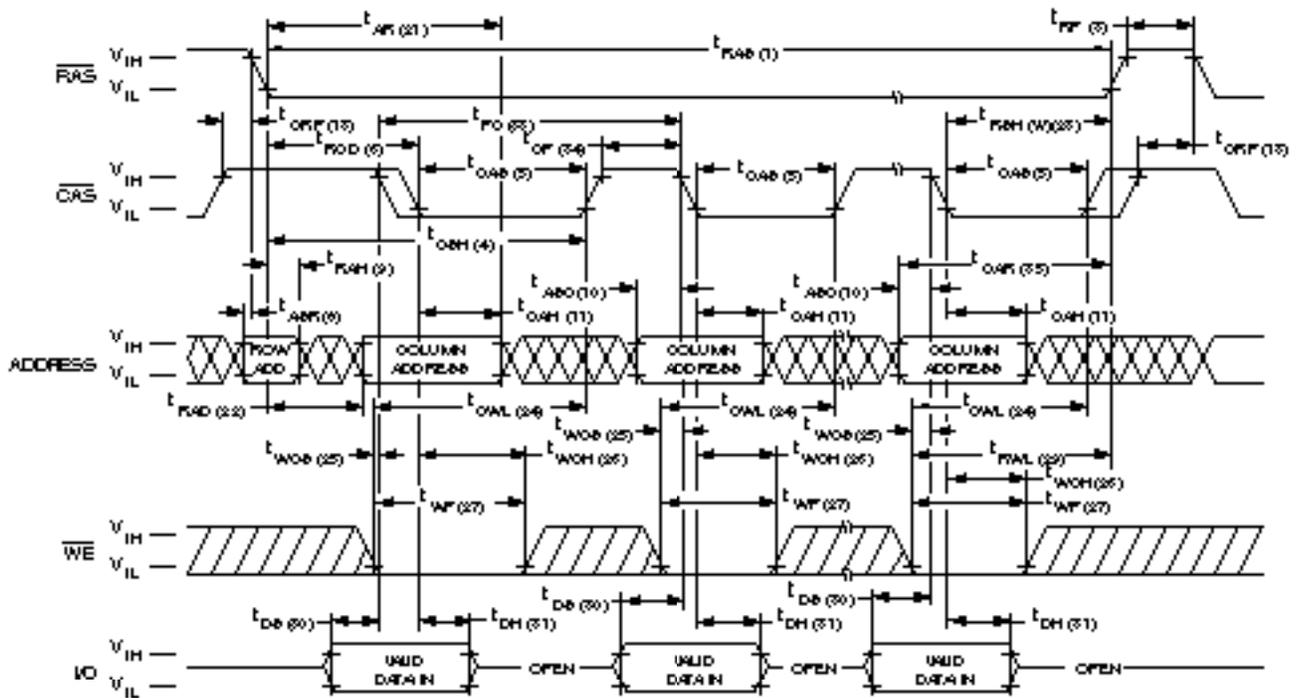
#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	<u>RAS</u> or <u>CAS</u> Hold Time in Write Cycle	15		20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to <u>CAS</u> Lead Time	15		20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	15		0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		10		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		10		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from <u>RAS</u>	50		55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to <u>RAS</u> Lead Time	15		20		20		25		ns	
30	$t_{D VWL2}$	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	<u>CAS</u> Pulse Width (RMW)	65		75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		65		ns	
34	t_{CH2CL2}	t_{CP}	<u>CAS</u> Precharge Time	10		10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to <u>RAS</u> Setup Time	30		35		40		50		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45		55	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to <u>RAS</u>	50		55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	<u>CAS</u> Setup Time <u>CAS</u> -before- <u>RAS</u> Refresh	5		5		5		5		ns	
39	t_{RH2CL2}	t_{RPC}	<u>RAS</u> to <u>CAS</u> Precharge Time	5		5		5		5		ns	
40	t_{RL1CH1}	t_{CHR}	<u>CAS</u> Hold Time <u>CAS</u> -before- <u>RAS</u> Refresh	15		15		15		15		ns	
41		t_{WRP}	Write to <u>RAS</u> Recharge Time	10		10		10		10		ns	
42		t_{WRH}	Write to <u>RAS</u> Hold Time	10		10		10		10		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
	t_{RI}		Refresh Interval (1024 Cycles)		16		16		16		16	ms	17

Waveforms of Fast Page Mode Read Cycle



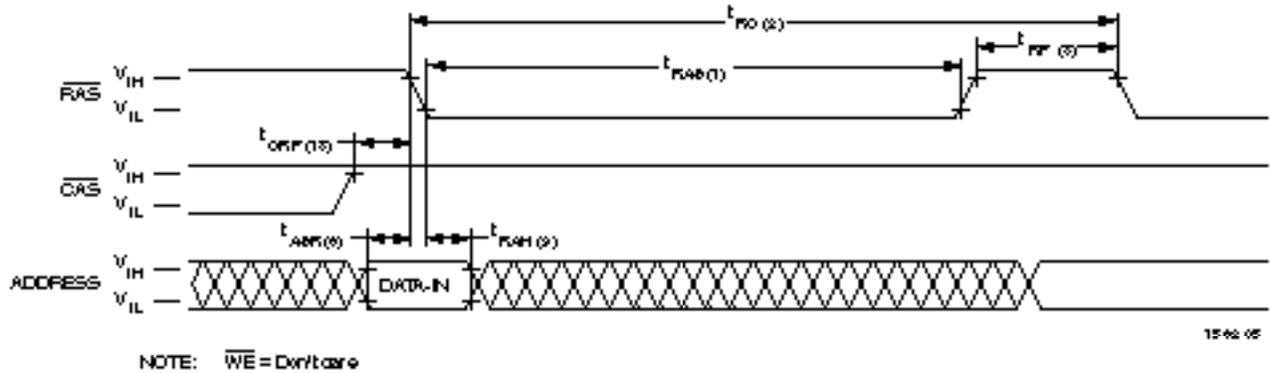
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Waveforms of Fast Page Mode Write Cycle

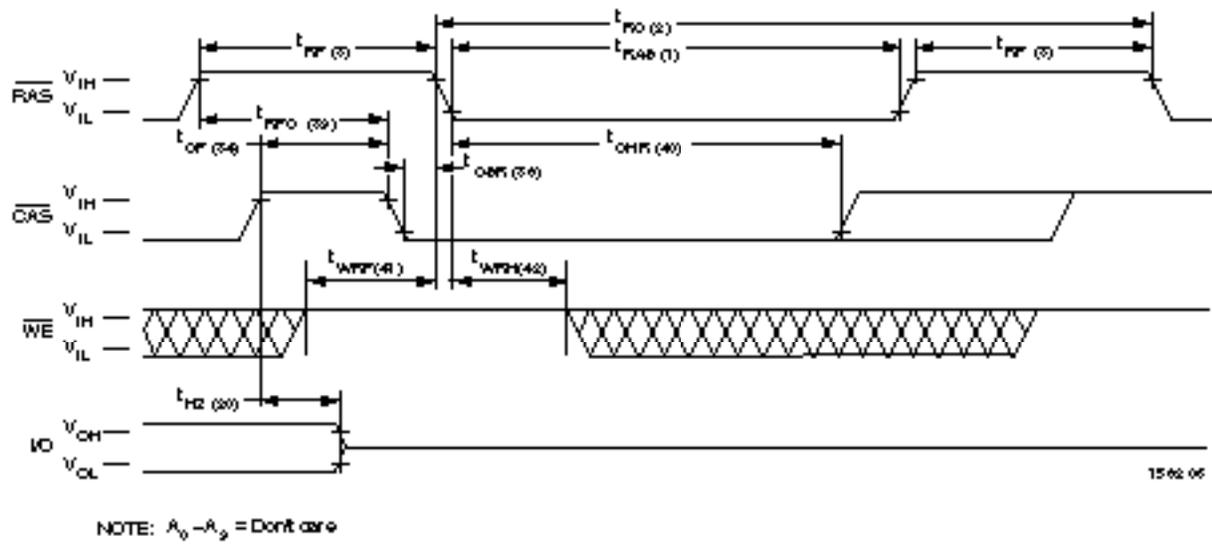


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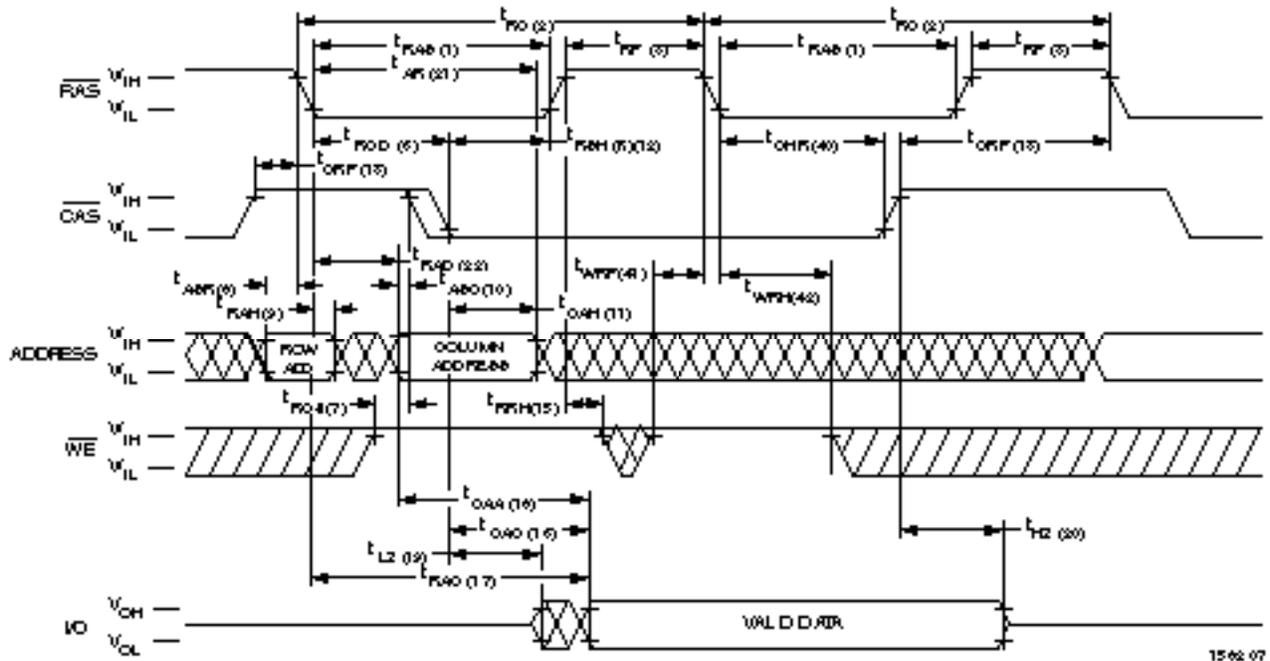
Waveforms of RAS-Only Refresh Cycle



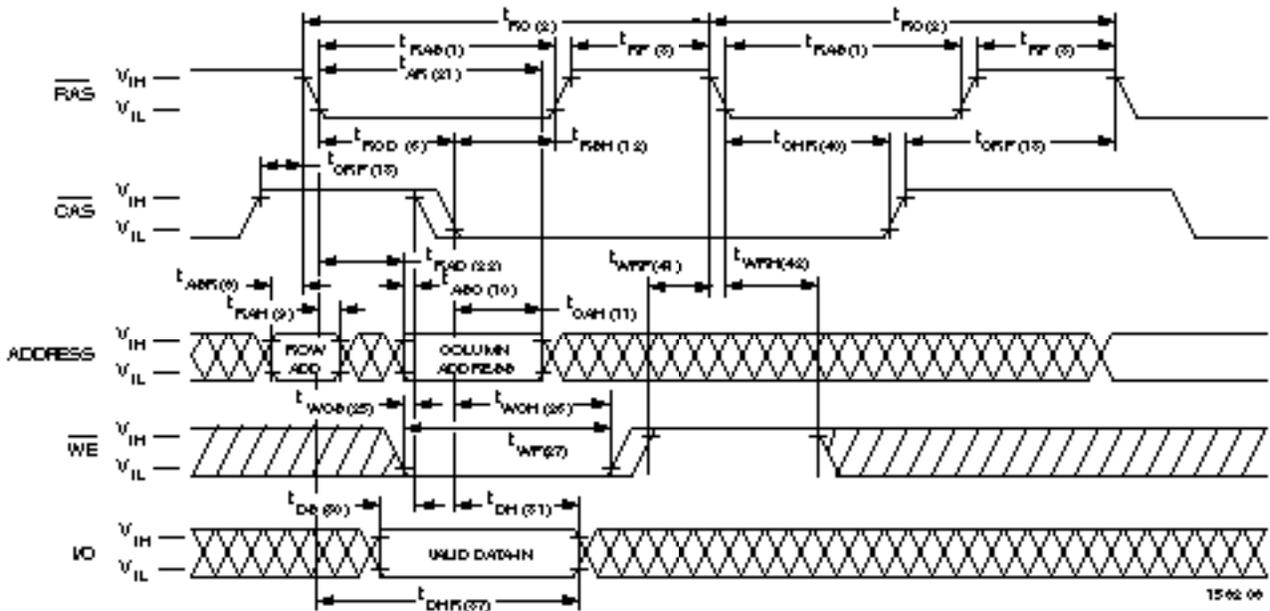
Waveforms of CAS-before-RAS Refresh Cycle



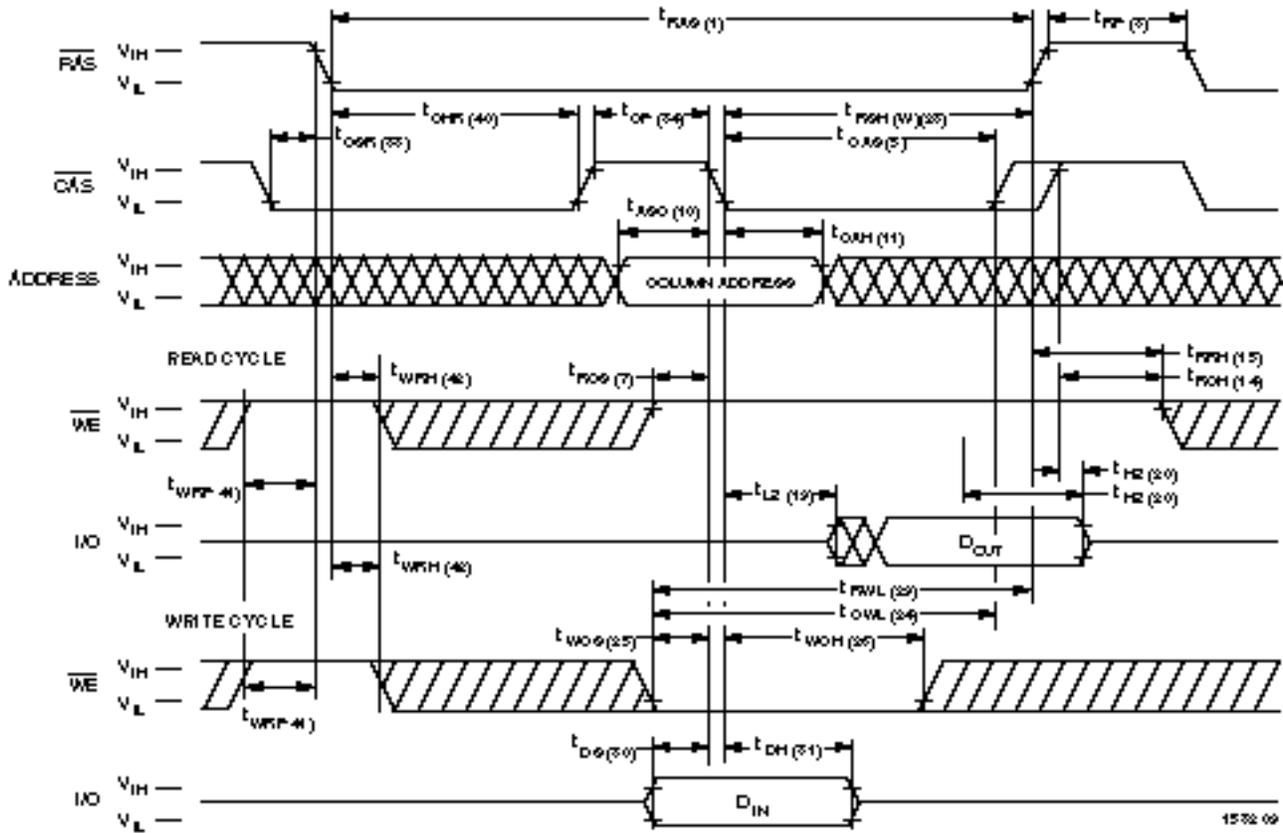
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of CAS-before-RAS Refresh Counter Test Cycle



Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{DD}$.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC} .
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC} .
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of CAS or WE.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume $t_T = 5$ ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit condition, and are not referenced to the output voltage levels.
17. An initial 200 μ s pause and 8 RAS-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under CAS-before-RAS refresh cycles.

$$t_{RC} = 62.5 \mu\text{s} \quad (62.5 \mu\text{s} \times 1024 = 64 \text{ ms})$$

$$t_{RAS} = t_{RAS} \text{ (min.) to } 1 \mu\text{s}$$

Input voltages : RAS and CAS

$$V_{IH} > V_{DD} - 0.2 \text{ V}$$

$$V_{IL} < 0.2 \text{ V}$$

WE and OE

$$V_{IN} > V_{DD} - 0.2 \text{ V}$$

All other inputs at stable V_{IH} or V_{IL}

Functional Description

The V404J8/9 are CMOS dynamic RAM modules for high data bandwidth, low power applications. The V404J8/9 reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe (RAS). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe (CAS). Because access time is primarily dependent on a valid column address rather than the precise time that the CAS edge occurs, the delay time from RAS to CAS has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing RAS low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable (WE) signal High during a RAS/CAS operation. The column address must be held for a minimum specified by t_{AR} . Data Out becomes valid only when t_{OAC} , t_{RAC} , t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC} , t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking WE and CAS low during a RAS operation. The column address is latched by CAS. The Write Cycle can be WE controlled or CAS controlled depending on whether WE or CAS falls later. Consequently, the input data must be valid at or before the falling edge of WE or CAS, whichever occurs last. In the CAS-controlled Write Cycle, when the leading edge of WE occurs prior to the CAS low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function.

Ending the Write with RAS or CAS will maintain the output in the High-Z state.

In the WE controlled Write Cycle, OE must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to refresh the memory:

1. By clocking each of the 1024 row addresses (A_0 through A_9) with RAS at least once every 16 ms. Any Read, Write, Read-Modify-Write or RAS-only cycle refreshes the addressed row.
2. Using a CAS-before-RAS Refresh Cycle. If CAS makes a transition from low to high to low after the previous cycle and before RAS falls, CAS-before-RAS refresh is activated. The V404J8/9 uses the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

CAS-before-RAS is a “refresh-only” mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A CAS-before-RAS counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V404J8/9 offers a CMOS standby mode that is entered by causing the RAS clock to swing between a valid V_{IL} and an “extra high” V_{IH} within 0.2 V of V_{DD} . While the RAS clock is at the “extra high” level, the V404J8/9 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
 t_{RX} = Refresh Interval / 1024

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining RAS low while performing successive CAS cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while CAS is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of CAS, eliminating t_{ASC} and t_T from the critical timing path. CAS latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of CAS, the access time is referenced to the CAS rising edge and is specified by t_{CAP} . If the column address is valid after the rising CAS edge, access is timed from the occurrence of a valid address and is specified by t_{CAA} . In both cases, the falling edge of CAS latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 20 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Data Output Operation

The V404J8/9 Input/Output is controlled by OE, CAS, WE and RAS. A RAS low transition enables the transfer of data to and from the selected row address in the Memory Array. A RAS high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a RAS low transition, a CAS low transition or CAS low level enables the internal I/O path. A CAS high transition or a CAS high level disables the I/O path and the output driver if it is enabled. A CAS low transition while RAS is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding

OE high. The OE signal has no effect on any data stored in the output latches. A WE low level can also disable the output drivers when CAS is low. During a Write cycle, if WE goes low at a time in relationship to CAS that would normally cause the outputs to be active, it is necessary to use OE to disable the output drivers prior to the WE low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 μs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

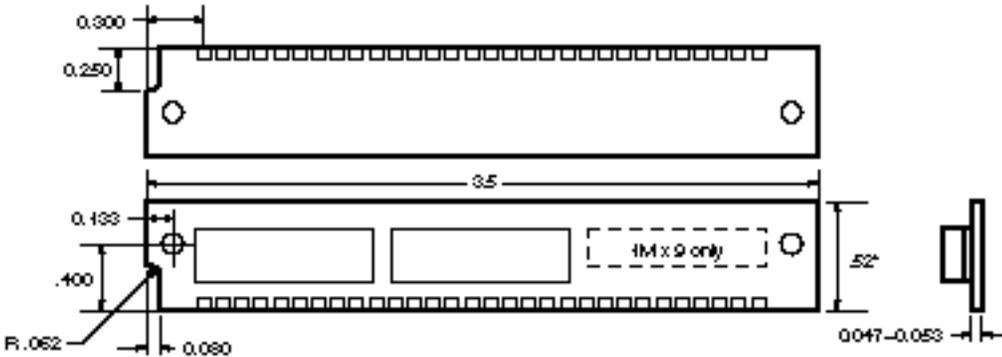
During Power-On, the V_{DD} current requirement of the V404J8/9 is dependent on the input levels of RAS and CAS. If RAS is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that RAS and CAS track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V404J8/9 Data Output Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
<u>CAS</u> -Controlled Write Cycle (Early Write)	High-Z
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
<u>RAS</u> -only Refresh	High-Z
<u>CAS</u> -before- <u>RAS</u> Refresh Cycle	Data remains as in previous cycle
<u>CAS</u> -only Cycles	High-Z

Package Dimensions

30-Pin SIMM #3



* 0.65" module also available
** Package dimensions subject to change without notice.

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

TAIWAN

5F NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 011-886-2-545-1213
FAX: 011-886-2-545-1214

JAPAN

KANAGAWA SCIENCE PARK
R&D C-4
100-1 SAKADO, TAKATSU-KU
KAWASAKI 213
PHONE: 011-04-4-812-4397
FAX: 011-04-4-812-4398

1 R&D ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 011-886-35-770055
FAX: 011-886-35-776520

HONG KONG

TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
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FAX: 011-852-664-7535

U.S. SALES OFFICES**NORTHWESTERN**

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RICHARDSON, TX 75081
PHONE: 214-690-1402
FAX: 214-690-0341

NORTHEASTERN

SUITE 306
71 SPITBROOK ROAD
NASHUA, NH 03062
PHONE: 603-891-2007
FAX: 603-891-3597

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