

128-common x 128-segment 4-level Gray Scale BITMAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6680** is a 128-common x 128-segment 4-level gray scale bit map LCD driver to display graphics or characters.

It contains 32,768-bit display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.

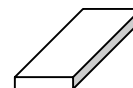
An image data from CPU through the serial or 8-bit parallel interface are stored into the 32,768-bit internal display data RAM and are displayed on the LCD panel through the commons and segments drivers.

The **NJU6680** features 4-level gray scale display function creating 4 types of gray scale (white / light gray / dark gray / black) and black & white display function.

The **NJU6680** contains a built-in OSC circuit for reducing external components. And it features Partial Display Function containing selectable active display block and optimizing the duty cycle ratio. This function dramatically reduces the operating current, setting the optimum boosted voltage combined with a programmable voltage booster circuit and an electrical variable resistor. As result, it reduces the operating current.

The operating voltage from 2.2V to 3.6V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE

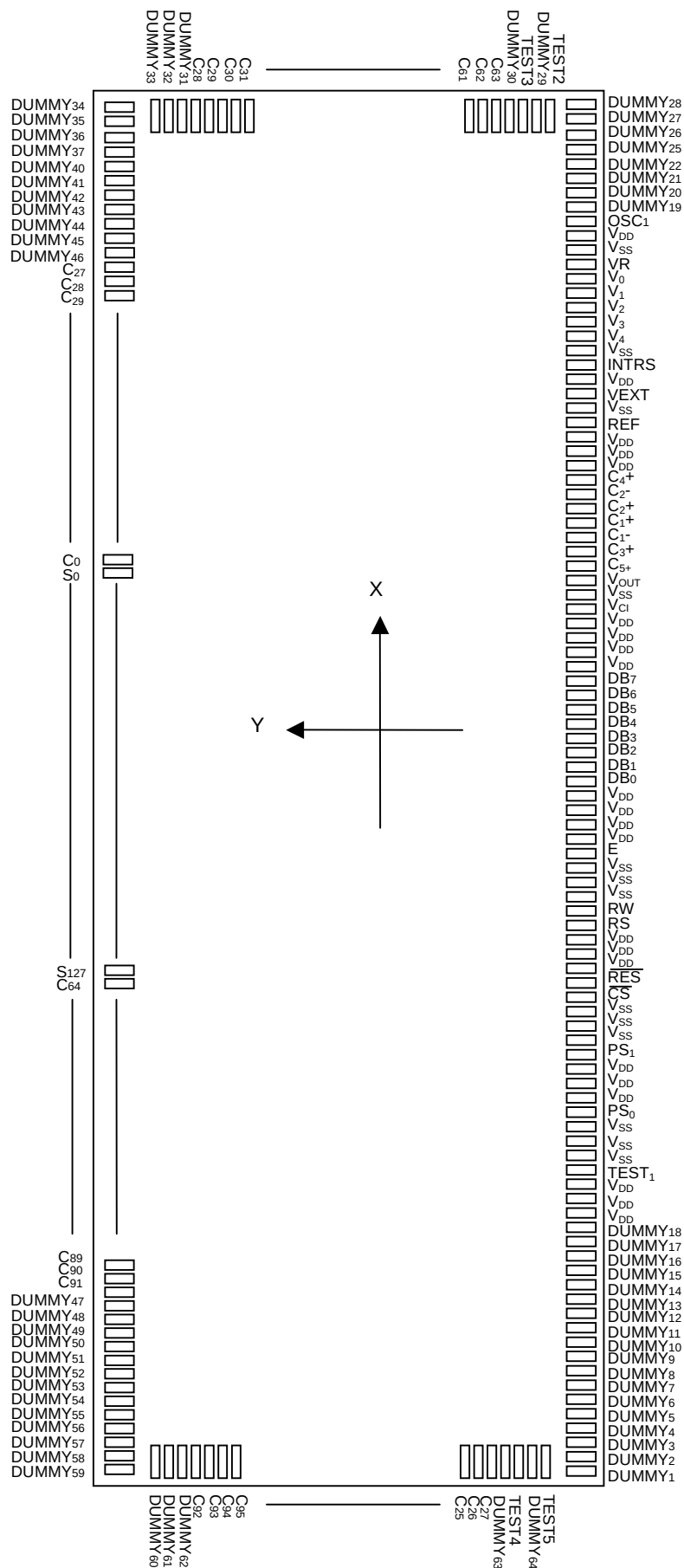


NJU6680CL

■ FEATURES

- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Method – 4-level Gray Scale / Black & White
- Display Data RAM – 32,768 bits ;(128-Com x 128-Seg) x 2bit
- LCD drivers – 128-common and 128-segment
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface (SI, SCL, RS, $\overline{CS}$)
- Partial Display Function
- Easy Vertical Scroll by setting the start line address of over size display data RAM
- Programmable Bias ratio selection ; 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12 bias
- Useful Instruction Sets
Status read, Display data write, Column address set, Page address set, Initial display line set, Initial COM₀ line set, Display ON/OFF, Entire display ON/OFF, Reverse display ON/OFF, N-line inversion set, N-line inversion OFF, ADC select, COM scan direction select, Internal resistor ratio set, Power control set, Partial display duty set, LCD bias set, Boost level set, Contrast level set, Power save mode ON, Power save mode OFF, Internal oscillator ON, Display data length set, Reset, FRC & PWM set, Grey scale mode set Display mode set.
- Power Supply Circuit for LCD; Programmable Booster Circuits (6 times maximum, Voltage boosting polarity : Positive Voltage (V_{SS} Common), Voltage Regulator, Voltage Follower (x 4))
- Precision Electrical Variable Resistance (64 Step)
- Low Operating Current $I_{OUT1}=400\mu A$ (TYP.)
- Operating Voltage 2.2 to 3.6 V
- LCD Driving Voltage 6.0 to 18.0V
- Package Outline Bumped Chip
- C-MOS Technology (Substrate : P)

PAD LOCATION



Chip Center	:X=0μm,Y=0μm
Chip Size	:X=13.11m,Y=3.08mm
Chip Thickness	:675um +/- 30um
Bump Size	:40μm x 83μm
Pad Pitch	:60μm (min)
Bump Height	:15μm (typ)
Bump Material	:Au
Voltage boosting polarity :	
Positive Voltage (V _{SS} Common)	
Substrate	: P

■ PAD Coordinates

Chip Size 13.11×3.08mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X(μm)	Y(μm)
1	DUMMY ₁	-6302	-1384
2	DUMMY ₂	-6242	-1384
3	DUMMY ₃	-6182	-1384
4	DUMMY ₄	-6122	-1384
5	DUMMY ₅	-6062	-1384
6	DUMMY ₆	-6002	-1384
7	DUMMY ₇	-5942	-1384
8	DUMMY ₈	-5882	-1384
9	DUMMY ₉	-5822	-1384
10	DUMMY ₁₀	-5762	-1384
11	DUMMY ₁₁	-5702	-1384
12	DUMMY ₁₂	-5642	-1384
13	DUMMY ₁₃	-5582	-1384
14	DUMMY ₁₄	-5522	-1384
15	DUMMY ₁₅	-5462	-1384
16	DUMMY ₁₆	-5402	-1384
17	DUMMY ₁₇	-5342	-1384
18	DUMMY ₁₈	-5282	-1384
19	V _{DD}	-5222	-1384
20	V _{DD}	-5162	-1384
21	V _{DD}	-5102	-1384
22	TEST ₁	-4897	-1384
23	V _{SS}	-4712	-1384
24	V _{SS}	-4652	-1384
25	V _{SS}	-4592	-1384
26	PS ₀	-4397	-1384
27	V _{DD}	-4209	-1384
28	V _{DD}	-4149	-1384
29	V _{DD}	-4089	-1384
30	PS ₁	-3892	-1384
31	V _{SS}	-3707	-1384
32	V _{SS}	-3647	-1384
33	V _{SS}	-3587	-1384
34	$\overline{\text{CS}}$	-3394	-1384
35	$\overline{\text{RES}}$	-3165	-1384
36	V _{DD}	-2982	-1384
37	V _{DD}	-2922	-1384
38	V _{DD}	-2862	-1384
39	RS	-2669	-1384
40	R/W	-2440	-1384
41	V _{SS}	-2257	-1384
42	V _{SS}	-2197	-1384
43	V _{SS}	-2137	-1384
44	E	-1940	-1384
45	V _{DD}	-1760	-1384
46	V _{DD}	-1700	-1384
47	V _{DD}	-1640	-1384
48	V _{DD}	-1580	-1384
49	DB ₀	-1370	-1384
50	DB ₁	-1150	-1384

PAD No.	Terminal	X(μm)	Y(μm)
51	DB ₂	-930	-1384
52	DB ₃	-710	-1384
53	DB ₄	-490	-1384
54	DB ₅	-270	-1384
55	DB ₆	-50	-1384
56	DB ₇	170	-1384
57	V _{DD}	362	-1384
58	V _{DD}	422	-1384
59	V _{DD}	482	-1384
60	V _{DD}	542	-1384
61	V _{CI}	739	-1384
62	V _{SS}	957	-1384
63	V _{OUT}	1067	-1384
64	C5 ⁺	1284	-1384
65	C3 ⁺	1547	-1384
66	C1 ⁻	1810	-1384
67	C1 ⁺	2073	-1384
68	C2 ⁺	2336	-1384
69	C2 ⁻	2599	-1384
70	C4 ⁺	2862	-1384
71	V _{DD}	3070	-1384
72	V _{DD}	3130	-1384
73	V _{DD}	3190	-1384
74	REF	3377	-1384
75	V _{SS}	3557	-1384
76	VEXT	3754	-1384
77	V _{DD}	3952	-1384
78	INTRS	4132	-1384
79	V _{SS}	4315	-1384
80	V ₄	4425	-1384
81	V ₃	4535	-1384
82	V ₂	4645	-1384
83	V ₁	4755	-1384
84	V ₀	4974	-1384
85	VR	5084	-1384
86	V _{SS}	5287	-1384
87	V _{DD}	5377	-1384
88	OSC ₁	5558	-1384
89	DUMMY ₁₉	5757	-1384
90	DUMMY ₂₀	5817	-1384
91	DUMMY ₂₁	5877	-1384
92	DUMMY ₂₂	5937	-1384
93	DUMMY ₂₃	5997	-1384
94	DUMMY ₂₄	6057	-1384
95	DUMMY ₂₅	6117	-1384
96	DUMMY ₂₆	6177	-1384
97	DUMMY ₂₇	6237	-1384
98	DUMMY ₂₈	6297	-1384
99	TEST ₂	6400	-1273
100	DUMMY ₂₉	6400	-1213

PAD No.	Terminal	X(um)	Y(um)
101	TEST ₃	6400	-1153
102	DUMMY ₃₀	6400	-1033
103	COM ₆₃	6400	-973
104	COM ₆₂	6400	-913
105	COM ₆₁	6400	-853
106	COM ₆₀	6400	-793
107	COM ₅₉	6400	-733
108	COM ₅₈	6400	-673
109	COM ₅₇	6400	-613
110	COM ₅₆	6400	-553
111	COM ₅₅	6400	-493
112	COM ₅₄	6400	-433
113	COM ₅₃	6400	-373
114	COM ₅₂	6400	-313
115	COM ₅₁	6400	-253
116	COM ₅₀	6400	-193
117	COM ₄₉	6400	-133
118	COM ₄₈	6400	-73
119	COM ₄₇	6400	-13
120	COM ₄₆	6400	47
121	COM ₄₅	6400	107
122	COM ₄₄	6400	167
123	COM ₄₃	6400	227
124	COM ₄₂	6400	287
125	COM ₄₁	6400	347
126	COM ₄₀	6400	407
127	COM ₃₉	6400	467
128	COM ₃₈	6400	527
129	COM ₃₇	6400	587
130	COM ₃₆	6400	647
131	COM ₃₅	6400	707
132	COM ₃₄	6400	767
133	COM ₃₃	6400	827
134	COM ₃₂	6400	887
135	COM ₃₁	6400	947
136	COM ₃₀	6400	1007
137	COM ₂₉	6400	1067
138	COM ₂₈	6400	1127
139	DUMMY ₃₁	6400	1187
140	DUMMY ₃₂	6400	1247
141	DUMMY ₃₃	6400	1307
142	DUMMY ₃₄	6270	1384
143	DUMMY ₃₅	6210	1384
144	DUMMY ₃₆	6150	1384
145	DUMMY ₃₇	6090	1384
146	DUMMY ₃₈	6030	1384
147	DUMMY ₃₉	5970	1384
148	DUMMY ₄₀	5910	1384
149	DUMMY ₄₁	5850	1384
150	DUMMY ₄₂	5790	1384

PAD No.	Terminal	X(um)	Y(um)
151	DUMMY ₄₃	5730	1384
152	DUMMY ₄₄	5670	1384
153	DUMMY ₄₅	5610	1384
154	DUMMY ₄₆	5550	1384
155	COM ₂₇	5490	1384
156	COM ₂₆	5430	1384
157	COM ₂₅	5370	1384
158	COM ₂₄	5310	1384
159	COM ₂₃	5250	1384
160	COM ₂₂	5190	1384
161	COM ₂₁	5130	1384
162	COM ₂₀	5070	1384
163	COM ₁₉	5010	1384
164	COM ₁₈	4950	1384
165	COM ₁₇	4890	1384
166	COM ₁₆	4830	1384
167	COM ₁₅	4770	1384
168	COM ₁₄	4710	1384
169	COM ₁₃	4650	1384
170	COM ₁₂	4590	1384
171	COM ₁₁	4530	1384
172	COM ₁₀	4470	1384
173	COM ₉	4410	1384
174	COM ₈	4350	1384
175	COM ₇	4290	1384
176	COM ₆	4230	1384
177	COM ₅	4170	1384
178	COM ₄	4110	1384
179	COM ₃	4050	1384
180	COM ₂	3990	1384
181	COM ₁	3930	1384
182	COM ₀	3870	1384
183	SEG ₀	3810	1384
184	SEG ₁	3750	1384
185	SEG ₂	3690	1384
186	SEG ₃	3630	1384
187	SEG ₄	3570	1384
188	SEG ₅	3510	1384
189	SEG ₆	3450	1384
190	SEG ₇	3390	1384
191	SEG ₈	3330	1384
192	SEG ₉	3270	1384
193	SEG ₁₀	3210	1384
194	SEG ₁₁	3150	1384
195	SEG ₁₂	3090	1384
196	SEG ₁₃	3030	1384
197	SEG ₁₄	2970	1384
198	SEG ₁₅	2910	1384
199	SEG ₁₆	2850	1384
200	SEG ₁₇	2790	1384

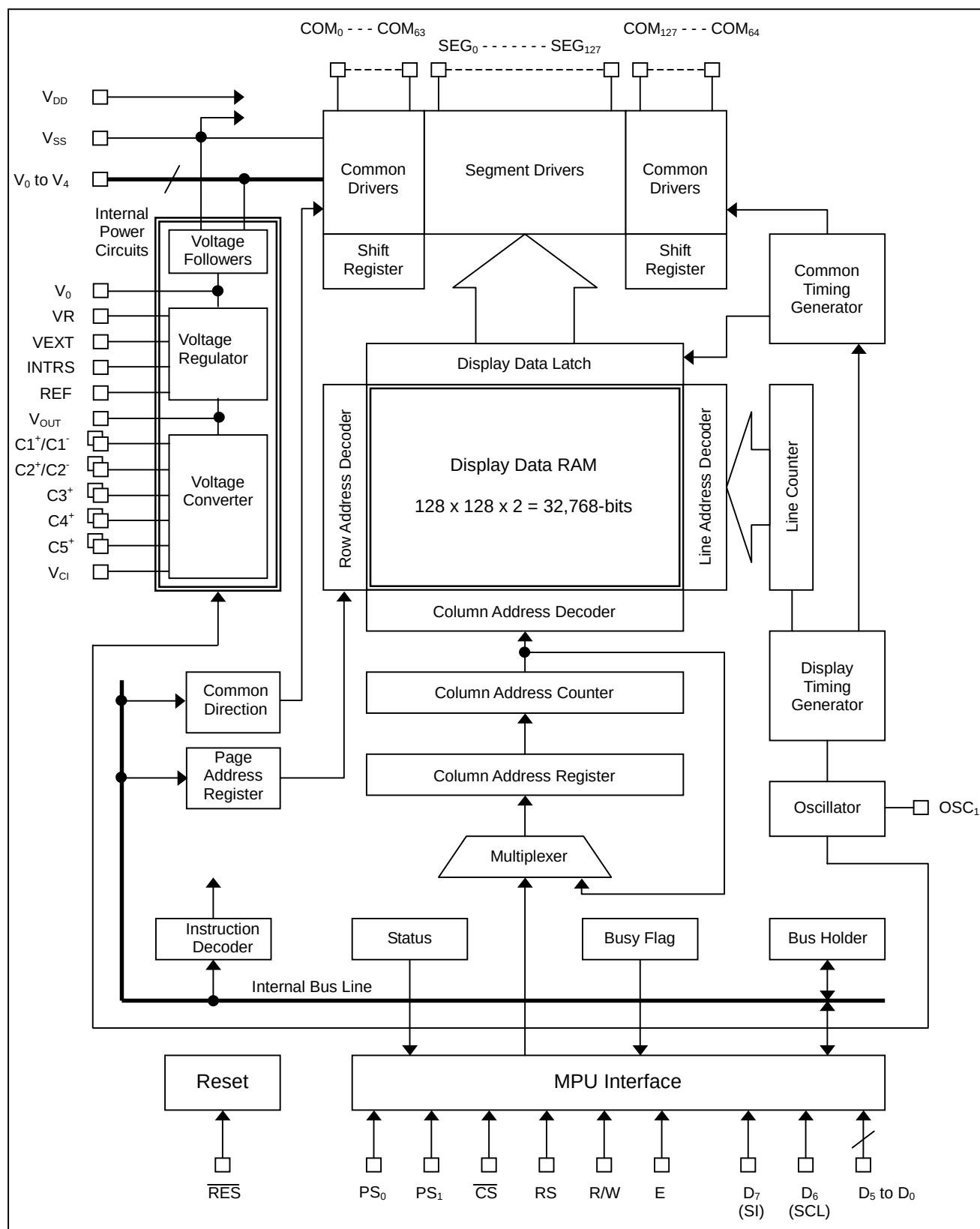
PAD No.	Terminal	X(um)	Y(um)
201	SEG ₁₈	2730	1384
202	SEG ₁₉	2670	1384
203	SEG ₂₀	2610	1384
204	SEG ₂₁	2550	1384
205	SEG ₂₂	2490	1384
206	SEG ₂₃	2430	1384
207	SEG ₂₄	2370	1384
208	SEG ₂₅	2310	1384
209	SEG ₂₆	2250	1384
210	SEG ₂₇	2190	1384
211	SEG ₂₈	2130	1384
212	SEG ₂₉	2070	1384
213	SEG ₃₀	2010	1384
214	SEG ₃₁	1950	1384
215	SEG ₃₂	1890	1384
216	SEG ₃₃	1830	1384
217	SEG ₃₄	1770	1384
218	SEG ₃₅	1710	1384
219	SEG ₃₆	1650	1384
220	SEG ₃₇	1590	1384
221	SEG ₃₈	1530	1384
222	SEG ₃₉	1470	1384
223	SEG ₄₀	1410	1384
224	SEG ₄₁	1350	1384
225	SEG ₄₂	1290	1384
226	SEG ₄₃	1230	1384
227	SEG ₄₄	1170	1384
228	SEG ₄₅	1110	1384
229	SEG ₄₆	1050	1384
230	SEG ₄₇	990	1384
231	SEG ₄₈	930	1384
232	SEG ₄₉	870	1384
233	SEG ₅₀	810	1384
234	SEG ₅₁	750	1384
235	SEG ₅₂	690	1384
236	SEG ₅₃	630	1384
237	SEG ₅₄	570	1384
238	SEG ₅₅	510	1384
239	SEG ₅₆	450	1384
240	SEG ₅₇	390	1384
241	SEG ₅₈	330	1384
242	SEG ₅₉	270	1384
243	SEG ₆₀	210	1384
244	SEG ₆₁	150	1384
245	SEG ₆₂	90	1384
246	SEG ₆₃	30	1384
247	SEG ₆₄	-30	1384
248	SEG ₆₅	-90	1384
249	SEG ₆₆	-150	1384
250	SEG ₆₇	-210	1384

PAD No.	Terminal	X(um)	Y(um)
251	SEG ₆₈	-270	1384
252	SEG ₆₉	-330	1384
253	SEG ₇₀	-390	1384
254	SEG ₇₁	-450	1384
255	SEG ₇₂	-510	1384
256	SEG ₇₃	-570	1384
257	SEG ₇₄	-630	1384
258	SEG ₇₅	-690	1384
259	SEG ₇₆	-750	1384
260	SEG ₇₇	-810	1384
261	SEG ₇₈	-870	1384
262	SEG ₇₉	-930	1384
263	SEG ₈₀	-990	1384
264	SEG ₈₁	-1050	1384
265	SEG ₈₂	-1110	1384
266	SEG ₈₃	-1170	1384
267	SEG ₈₄	-1230	1384
268	SEG ₈₅	-1290	1384
269	SEG ₈₆	-1350	1384
270	SEG ₈₇	-1410	1384
271	SEG ₈₈	-1470	1384
272	SEG ₈₉	-1530	1384
273	SEG ₉₀	-1590	1384
274	SEG ₉₁	-1650	1384
275	SEG ₉₂	-1710	1384
276	SEG ₉₃	-1770	1384
277	SEG ₉₄	-1830	1384
278	SEG ₉₅	-1890	1384
279	SEG ₉₆	-1950	1384
280	SEG ₉₇	-2010	1384
281	SEG ₉₈	-2070	1384
282	SEG ₉₉	-2130	1384
283	SEG ₁₀₀	-2190	1384
284	SEG ₁₀₁	-2250	1384
285	SEG ₁₀₂	-2310	1384
286	SEG ₁₀₃	-2370	1384
287	SEG ₁₀₄	-2430	1384
288	SEG ₁₀₅	-2490	1384
289	SEG ₁₀₆	-2550	1384
290	SEG ₁₀₇	-2610	1384
291	SEG ₁₀₈	-2670	1384
292	SEG ₁₀₉	-2730	1384
293	SEG ₁₁₀	-2790	1384
294	SEG ₁₁₁	-2850	1384
295	SEG ₁₁₂	-2910	1384
296	SEG ₁₁₃	-2970	1384
297	SEG ₁₁₄	-3030	1384
298	SEG ₁₁₅	-3090	1384
299	SEG ₁₁₆	-3150	1384
300	SEG ₁₁₇	-3210	1384

PAD No.	Terminal	X(um)	Y(um)
301	SEG ₁₁₈	-3270	1384
302	SEG ₁₁₉	-3330	1384
303	SEG ₁₂₀	-3390	1384
304	SEG ₁₂₁	-3450	1384
305	SEG ₁₂₂	-3510	1384
306	SEG ₁₂₃	-3570	1384
307	SEG ₁₂₄	-3630	1384
308	SEG ₁₂₅	-3690	1384
309	SEG ₁₂₆	-3750	1384
310	SEG ₁₂₇	-3810	1384
311	COM ₆₄	-3870	1384
312	COM ₆₅	-3930	1384
313	COM ₆₆	-3990	1384
314	COM ₆₇	-4050	1384
315	COM ₆₈	-4110	1384
316	COM ₆₉	-4170	1384
317	COM ₇₀	-4230	1384
318	COM ₇₁	-4290	1384
319	COM ₇₂	-4350	1384
320	COM ₇₃	-4410	1384
321	COM ₇₄	-4470	1384
322	COM ₇₅	-4530	1384
323	COM ₇₆	-4590	1384
324	COM ₇₇	-4650	1384
325	COM ₇₈	-4710	1384
326	COM ₇₉	-4770	1384
327	COM ₈₀	-4830	1384
328	COM ₈₁	-4890	1384
329	COM ₈₂	-4950	1384
330	COM ₈₃	-5010	1384
331	COM ₈₄	-5070	1384
332	COM ₈₅	-5130	1384
333	COM ₈₆	-5190	1384
334	COM ₈₇	-5250	1384
335	COM ₈₈	-5310	1384
336	COM ₈₉	-5370	1384
337	COM ₉₀	-5430	1384
338	COM ₉₁	-5490	1384
339	DUMMY ₄₇	-5550	1384
340	DUMMY ₄₈	-5610	1384
341	DUMMY ₄₉	-5670	1384
342	DUMMY ₅₀	-5730	1384
343	DUMMY ₅₁	-5790	1384
344	DUMMY ₅₂	-5850	1384
345	DUMMY ₅₃	-5910	1384
346	DUMMY ₅₄	-5970	1384
347	DUMMY ₅₅	-6030	1384
348	DUMMY ₅₆	-6090	1384
349	DUMMY ₅₇	-6150	1384
350	DUMMY ₅₈	-6210	1384

PAD No.	Terminal	X(um)	Y(um)
351	DUMMY ₅₉	-6270	1384
352	DUMMY ₆₀	-6400	1307
353	DUMMY ₆₁	-6400	1247
354	DUMMY ₆₂	-6400	1187
355	COM ₉₂	-6400	1127
356	COM ₉₃	-6400	1067
357	COM ₉₄	-6400	1007
358	COM ₉₅	-6400	947
359	COM ₉₆	-6400	887
360	COM ₉₇	-6400	827
361	COM ₉₈	-6400	767
362	COM ₉₉	-6400	707
363	COM ₁₀₀	-6400	647
364	COM ₁₀₁	-6400	587
365	COM ₁₀₂	-6400	527
366	COM ₁₀₃	-6400	467
367	COM ₁₀₄	-6400	407
368	COM ₁₀₅	-6400	347
369	COM ₁₀₆	-6400	287
370	COM ₁₀₇	-6400	227
371	COM ₁₀₈	-6400	167
372	COM ₁₀₉	-6400	107
373	COM ₁₁₀	-6400	47
374	COM ₁₁₁	-6400	-13
375	COM ₁₁₂	-6400	-73
376	COM ₁₁₃	-6400	-133
377	COM ₁₁₄	-6400	-193
378	COM ₁₁₅	-6400	-253
379	COM ₁₁₆	-6400	-313
380	COM ₁₁₇	-6400	-373
381	COM ₁₁₈	-6400	-433
382	COM ₁₁₉	-6400	-493
383	COM ₁₂₀	-6400	-553
384	COM ₁₂₁	-6400	-613
385	COM ₁₂₂	-6400	-673
386	COM ₁₂₃	-6400	-733
387	COM ₁₂₄	-6400	-793
388	COM ₁₂₅	-6400	-853
389	COM ₁₂₆	-6400	-913
390	COM ₁₂₇	-6400	-973
391	DUMMY ₆₃	-6400	-1033
392	TEST ₄	-6400	-1153
393	DUMMY ₆₄	-6400	-1213
394	TEST ₅	-6400	-1273

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

• Power Supply

No.	Terminal	Description
19-21, 27-29, 36-38, 45-48, 57-60, 71-73, 77,87	V _{DD}	Power Supply
23-25, 31-33, 41-43, 62,75, 79,86	V _{SS}	Ground, 0V

• Internal Power Circuits

No.	Terminal	Description
61	V _{CI}	Voltage converter input terminal
63	V _{OUT}	Voltage converter output terminal
84 83 82 81 80	V ₀ V ₁ V ₂ V ₃ V ₄	LCD driving voltage terminals - When the internal power circuits are used, the LCD driving voltages (V₀ to V₄) are enabled by the "Power control set" instruction and an LCD bias ratio is selected by the "LCD bias set" instruction. - When the internal power circuits are not used, the external voltages (V₀ to V₄) are required on these terminals. The external voltages should be maintained in the relationship: V_{SS} ≤ V₄ ≤ V₃ ≤ V₂ ≤ V₁ ≤ V₀.
67 66	C1 ⁺ C1 ⁻	Capacitor terminals for voltage converter
68 69	C2 ⁺ C2 ⁻	Capacitor terminals for voltage converter
65	C3 ⁺	Capacitor terminal for voltage converter
70	C4 ⁺	Capacitor terminal for voltage converter
64	C5 ⁺	Capacitor terminal for voltage converter
85	VR	V0 voltage adjustment terminal
74	REF	Internal or external reference voltage select terminal "H": Internal "L": External
76	VEXT	External reference voltage input terminal This terminal is valid when the REF terminal is connected to "L".
78	INTRS	Internal resistor select terminal "H": Internal "L": External

• MPU Interface Circuits

No.	Terminal	Description
26	PS ₀	Parallel or serial interface select terminal PS ₀ ="L", PS ₁ ="L": 3-line serial PS ₀ ="L", PS ₁ ="H": 4-line serial PS ₀ ="H", PS ₁ ="L": 80 type MPU parallel interface PS ₀ ="H", PS ₁ ="H": 68 type MPU parallel interface
30	PS ₁	
34	$\overline{CS}$	Chip select terminal Active "L"
56-49	D ₇ -D ₀	Data bus terminals Parallel interface: D ₇ to D ₀ Serial interface: SI (D ₇ terminal), SCL (D ₆ terminal)
39	RS	Register select terminal • This signal distinguishes instruction data or display data when the LSI is used in the 4-line serial or parallel interface mode. RS="H": D ₇ to D ₀ are Display data RS="L": D ₇ to D ₀ are Instruction data
44	$\overline{E}$ (RD)	68 type MPU: Active "H" 80 type MPU: Active "L"
40	R/W (WR)	68 type MPU: R/W="H": Read operation R/W="L": Write operation 80 type MPU: Active "L"
35	$\overline{RES}$	Reset terminal Active "L"
88	OSC ₁	OSC terminal • When the internal oscillator is used, the external resistor, R _f , is required between this terminal and the V _{DD} . R _f =270kΩ: Frame frequency=165Hz (typ.)

• LCD drivers

No.	Terminal	Description
182-155, 138-103, 311-338, 355-390	COM ₀ -- COM ₁₂₇	Common (row) drivers COM ₀ -COM ₁₂₇
182-310	SEG ₀ -- SEG ₁₂₇	Segment (column) drivers SEG ₀ -SEG ₁₂₇

• Dummy

No.	Terminal	Description
1-18, 89-98, 100,102 139-154, 339-354, 391,393	DUMMY ₁ -- DUMMY ₆₄	No connections. Dummy pads

• Test terminals

No.	Terminal	Description
22,99, 101,392, 394	TEST ₁ -- TEST ₅	No connections. Used for maker test

■ Functional Description

(1) Description of each blocks

(1-1) Busy Flag (BF)

The BF is used to indicate whether the LSI is busy or not. During the busy status, the LSI cannot accept any instruction except the "Status read" instruction, which reads out the BF through the D₇ terminal. When the cycle time (tcyc) mentioned in "AC characteristics" is satisfied, the BF is not required after each instruction so that it is possible to improve the process performance of an MPU.

(1-2) Initial display line register

The initial display line register is used to specify the DDRAM line address corresponding to the COM₀ by the "Initial display line set" instruction. It is used not only for normal display but also vertical scrolling and page switching displays without changing the display data in the DDRAM.

(1-3) Line Counter

The line counter is used to provide the DDRAM line address. The line address is initialized whenever the polarity of an internal frame signal (FR) is switched, and then it is counted up in synchronization of a common timing signal.

(1-4) Column Address Counter

An MPU can access only 7-bit [C6:C0] "column address" by the "Column address LSB set" and "Column address MSB set" instructions. When both 4-bit LSB and 3-bit MSB data is set into the column address register, 8-bit "internal column address" is established in the LSI as illustrated in the following figure, and accordingly, 2-bit display data must be written for each pixel with two successive bytes.

The column address automatically increases by 1 (+1) after each 2-byte display data and wraps around to the column address (00)_H in the same page after the last column is addressed. The assignment of the column address for the segment drivers can be reversed by the "ADC set" instruction.

Segment outputs	SEG ₀	SEG ₁	SEG ₂	SEG ₃		SEG ₁₂₄	SEG ₁₂₅	SEG ₁₂₆	SEG ₁₂₇
Internal Column address	(00) _H (01) _H	(02) _H (03) _H	(04) _H (05) _H	(06) _H (07) _H		(F8) _H (F9) _H	(FA) _H (FB) _H	(FC) _H (FD) _H	(FE) _H (FF) _H
Column address (ADC=0)	(00) _H	(01) _H	(02) _H	(03) _H		(7C) _H	(7D) _H	(7E) _H	(7F) _H
Display data	1 1	0 0	0 1	1 0		0 1	1 0	1 1	0 0
Display image									

Column address (ADC=1)	(7F) _H	(7E) _H	(7D) _H	(7C) _H		(03) _H	(02) _H	(01) _H	(00) _H
Display data	0 0	1 1	1 0	0 1		1 0	0 1	0 0	1 1
Display image									

(1-5) Page Address Register

The page address register is used to provide the DD RAM page address.

(1-6) Display data RAM (DD RAM)

The Display data RAM (DD RAM) is the bit map RAM consisting of 32,768-bit to store the display data corresponding to 128x128 pixels on LCD panel. Each LCD pixel corresponds to two bits in the display data RAM in gray scale mode and to one bit in black & white mode, display data respectively.

The DD RAM data : "00" = Gray Scale Level 0 (Set by the "Gray Scale Level Select" instruction)
 The DD RAM data : "01" = Gray Scale Level 1 (")
 The DD RAM data : "10" = Gray Scale Level 2 (")
 The DD RAM data : "11" = Gray Scale Level 3 (")

The DD RAM data and the state of the LCD in Black & White Mode:

In Normal Display : "1"=Turn-On Display, "0" =Turn-Off Display

In Reverse Display : "1"=Turn-Off Display, "0" =Turn-On Display

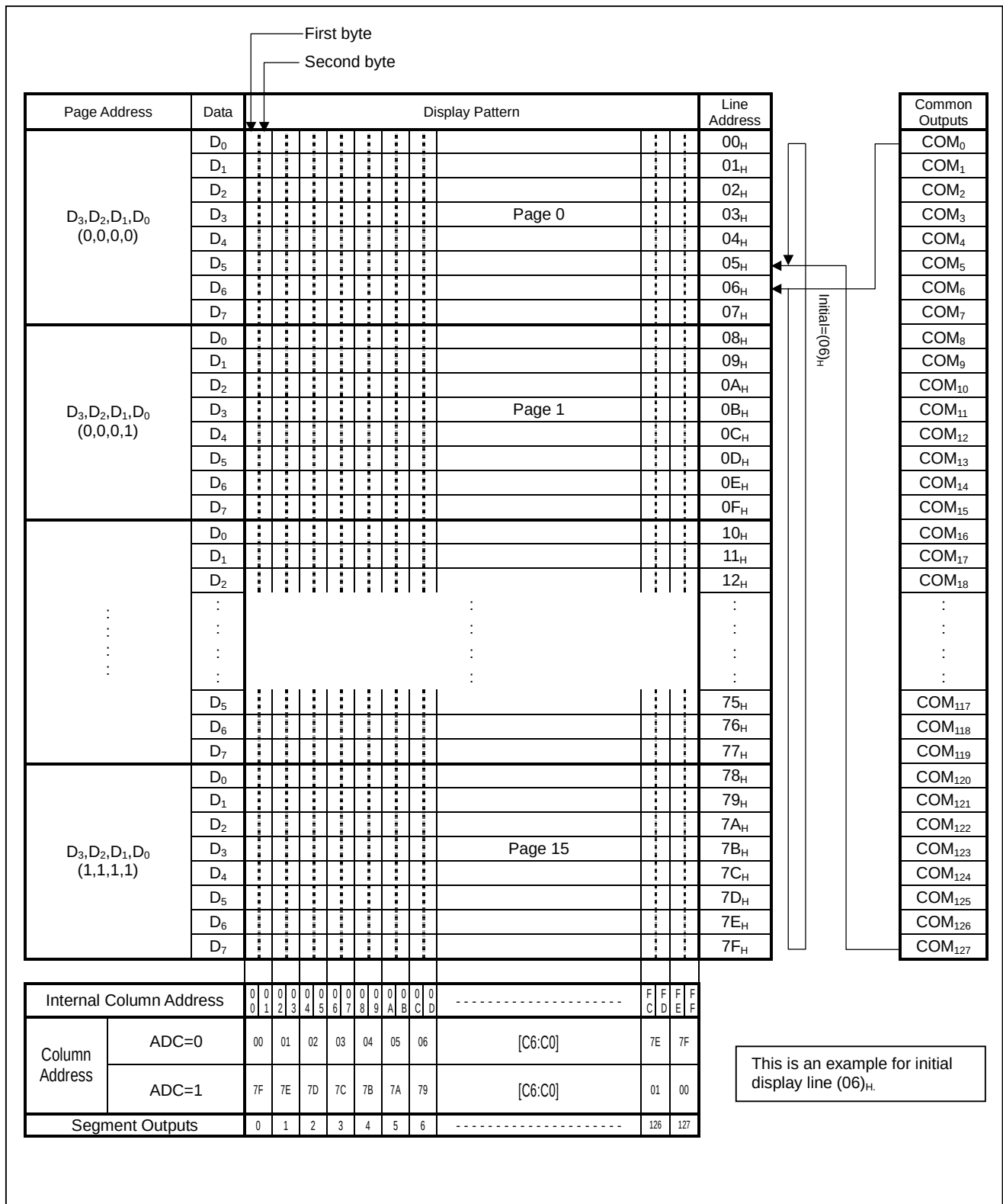


Fig.1 Display data RAM (DDRAM) Map

(1-7) Common Direction Register

The common direction register is used to select a common scan direction by setting the S_0 in the "COM scan direction select" instruction.

S_0	COM scan direction
0	COM ₀ to COM ₁₂₇
1	COM ₁₂₇ to COM ₀

(1-8) Reset Circuit

The reset circuit is used to initialize the LSI to the following default status by setting the $\overline{\text{RES}}$ terminal to "0" level.

Default status by using of the $\overline{\text{RES}}$ terminal

1. Page address : (0) page
2. Column address : (00)_H
3. COM scan direction : $S_0=0$
4. ADC select : $S_0=0$
5. Initial display line : (00)_H
6. Initial COM0 line : (00)_H
7. Display ON/OFF : OFF
8. Reverse display ON/OFF : OFF
9. Entire display ON/OFF : OFF
10. N-line inversion ON/OFF : OFF
11. Partial display duty ratio : 1/128 duty
12. Power control register : (VC,VR,VF)=(0,0,0)
13. Boost level : 3x boost
14. Contrast level : 32 level
15. LCD bias : 1/12 bias
16. Internal resistor ratio : $1+R_b/R_a=2.3$
17. Internal oscillator ON/OFF : OFF
18. Power save mode ON/OFF : OFF
19. Display data length : (0,0,0,0)
20. White mode set : OFF
21. White palette register : (0,0,0,0)
22. Light gray mode set : OFF
23. Light gray palette register : (0,0,0,0)
24. Dark gray mode set : OFF
25. Dark gray palette register : (1,1,1,1)
26. Black mode set : OFF
27. Black palette register : (1,1,1,1)
28. FRC & PWM mode : 4-frame, 9-level
29. Display mode set : Gray scale mode

The $\overline{\text{RES}}$ terminal is usually connected to the MPU's reset terminal in order that the LSI is initialized at the same timing of the MPU reset. The reset time must be at least 10us or longer, as mentioned in "DC characteristics". The LSI will return to normal operation after about 1us from the rising edge of the reset signal. In case that an external power supply is used for the LCD driving voltage, the $\overline{\text{RES}}$ terminal is required to be maintained in the "0" level when the external power supply is turned on.

The "Reset" instruction in Table 3 cannot be substituted for the reset operation by the $\overline{\text{RES}}$ terminal. It can execute only 1,2,5,14,16,19 to 28 items listed above.

(1-9) LCD display circuits

(a) Common and segment drivers

The common and segment drivers are used to generate LCD driving waveforms in accordance with the combination of display data, common timing signal (CL) and internal frame signal (FL).

(b) Display timing generator

The display timing generator is used to generate the common timing signal (CL) and the internal frame signal (FR). The FR signal adopts the 2-frame AC driving method, in which the FR signal is toggled to alternate the crystal polarization on an LCD panel. It toggles on every frame in the default setting or once every N frames in the N-line inversion mode setting, as illustrated in Fig.2-1 and Fig.2-2.

(c) Display Data Latch Circuit

The display data latch circuit is used to temporally store the 128-bit display data transferred from the DDRAM and output these display data onto the segment drivers in synchronization of the CL signal. The output timing for the display data, from display latch circuits to segment drivers, is independent of the access timing from MPU to DDRAM. As a result, the LCD display is not affected by the DDRAM access.

The “Display ON/OFF”, “Reverse display ON/OFF” and “Entire display ON/OFF” instructions control the display data in the display data latch circuit, however they do not change the display data in the DDRAM.

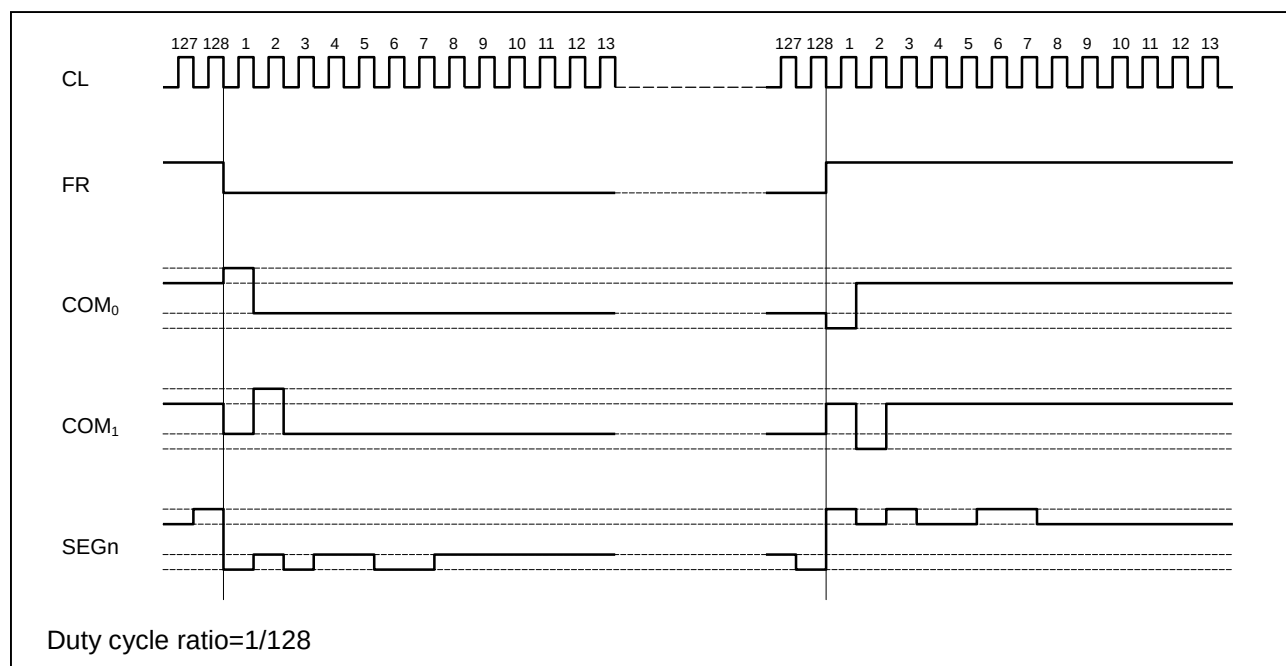


Fig.2-1 LCD driving Waveforms

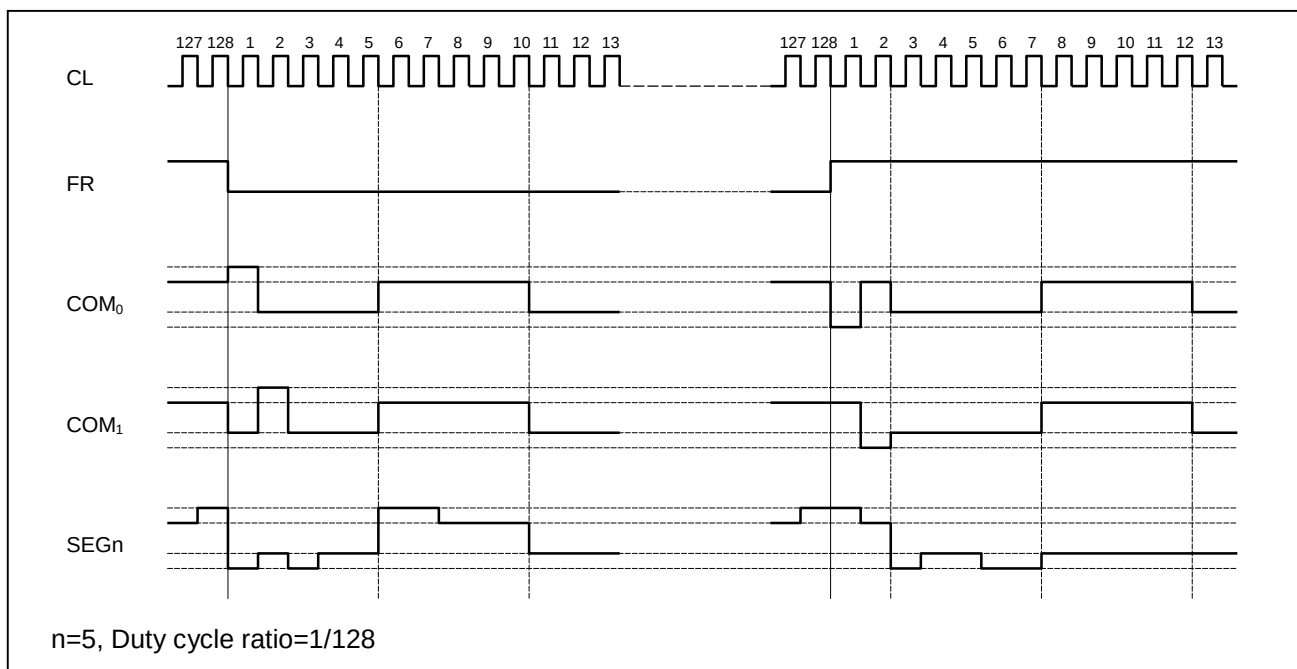


Fig. 2-2. LCD driving waveforms in the n-line inversion mode

(d) Oscillator

The internal oscillator is used to create internal clocks for the display timing signals (CL, FR) and the voltage converter.

(e) Internal Power Circuits

The internal power circuits are composed of the voltage converter, voltage regulator with 64-level EVR, and voltage followers. The status of the internal power circuits is arranged by the "Power control set" instruction, as shown in Table 1. For this arrangement, the part of the internal power circuits can be used in combination with an external power supply, as shown in Table 2.

The internal power circuits require the optimum values for the passive components, such as V_0 to V_4 capacitors and external feedback resistors in accordance with an LCD panel; and accordingly should be evaluated by using of actual LCD module samples to decide these values.

Table 1. Power control set

Bits	Portions	Status	
VC	Voltage converter	1: ON	0: OFF
VR	Voltage regulator	1: ON	0: OFF
VF	Voltage followers	1: ON	0: OFF

Table 2. Power supply combinations

Combination	Instruction			Power supply circuits			Output terminals		
	VC	VR	VF	Voltage converter	Voltage regulator	Voltage followers	V_{OUT}	V_0	V_1-V_4
Using all internal power circuits	1	1	1	ON	ON	ON	Open	Open	Open
Using voltage regulator and voltage followers	0	1	1	OFF	ON	ON	External	Open	Open
Using voltage followers	0	0	1	OFF	OFF	ON	Open	External	Open
Using only external power Supply	0	0	0	OFF	OFF	OFF	Open	External	External

Note) De coupling capacitors on the V_0 to V_4 terminals are required when the voltage followers are enabled.

● Power Supply Circuits example

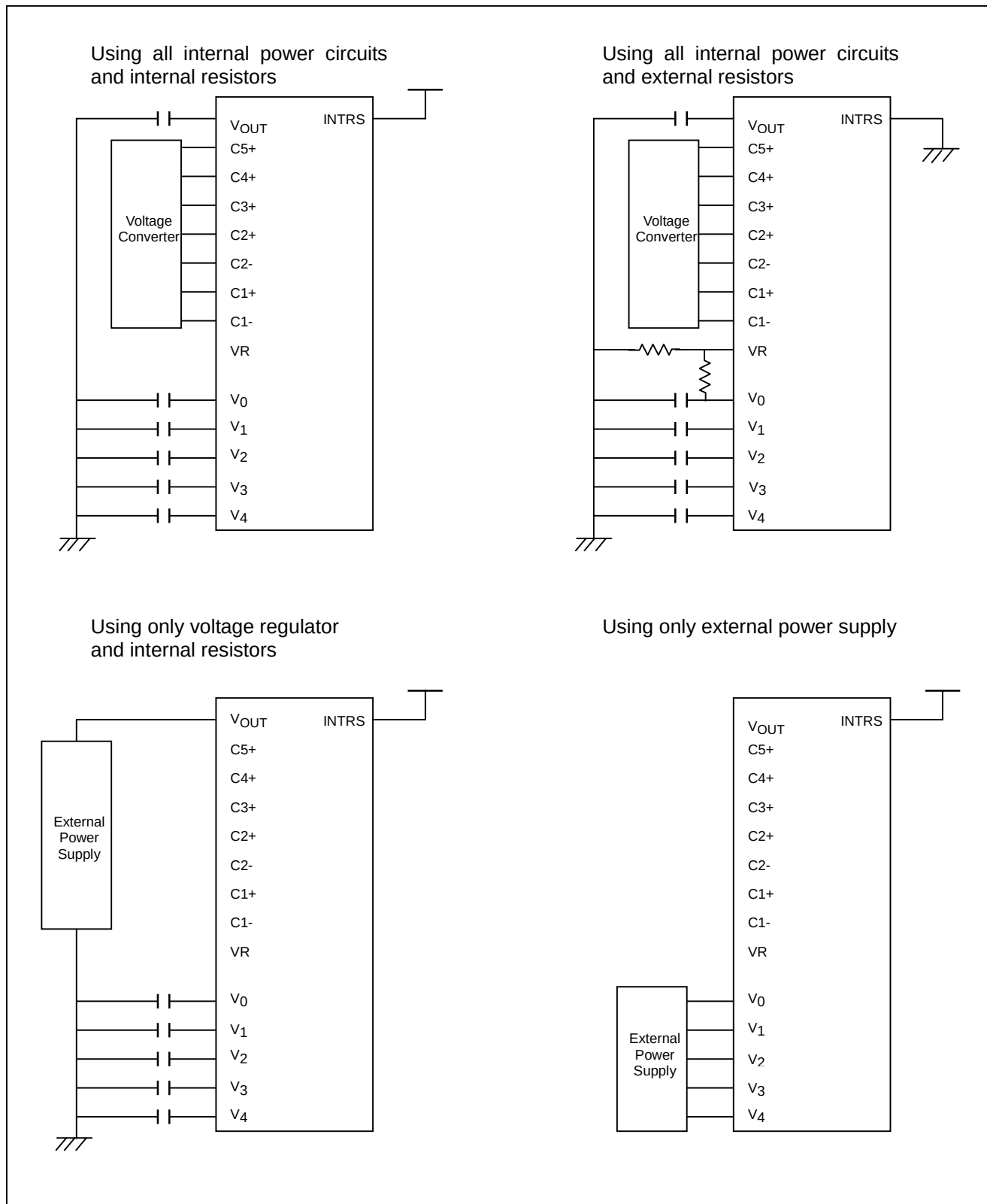


Fig. 3. Power circuits configuration

(2) Instructions

The **NJU6680** distinguishes the data on the data bus D₀ to D₇ as an instruction by combination of RS and R/W signals. The decoding of the instruction and execution performs with only high speed internal timing without relation to the external clock.

In case of the serial interface, the data input as MSB(D₇) first serially.

Table.3-1, 3-2 shows the instruction codes of the **NJU6680**

Table 3-1. Instruction Codes

Instruction		Code										Descriptions
		RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
(a)	Status read	0	1	Busy	ON	RES	0	0	0	0	0	-
(b)	Display data write	1	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	-
(c)	Column address LSB set	0	0	0	0	0	0	C ₃	C ₂	C ₁	C ₀	Lower 4-bit
	Column address MSB set	0	0	0	0	0	1	0	C ₆	C ₅	C ₄	Upper 3-bit
(d)	Internal resistor ratio set	0	0	0	0	1	0	0	R ₂	R ₁	R ₀	-
(e)	Power control set	0	0	0	0	1	0	1	VC	VR	VF	-
(f)	Initial display line set (Dual instructions)	0	0	0	1	0	0	0	0	*	*	Set initial display line mode
		0	0	*	L ₆	L ₅	L ₄	L ₃	L ₂	L ₁	L ₀	Specify line address
(g)	Initial COM ₀ line set (Dual instructions)	0	0	0	1	0	0	0	1	*	*	Set initial COM ₀ line mode
		0	0	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	Specify line address
(h)	Partial display duty set (Dual instructions)	0	0	0	1	0	0	1	0	*	*	Set partial display mode
		0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Specify duty cycle ratio
(i)	N-line inversion set (Dual instructions)	0	0	0	1	0	0	1	1	*	*	Set N-line inversion mode
		0	0	*	*	*	N ₄	N ₃	N ₂	N ₁	N ₀	Specify the number of N-line
(j)	LCD bias set	0	0	0	1	0	1	0	B ₂	B ₁	B ₀	-
(k)	Boost level set	0	0	0	1	1	0	0	1	B ₁	B ₀	-
(l)	Contrast level set (Dual instructions)	0	0	1	0	0	0	0	0	0	1	Set contrast level mode
		0	0	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	Specify contrast level
(m)	ADC select	0	0	1	0	1	0	0	0	0	S ₀	Select segment direction
(n)	Entire display ON/OFF	0	0	1	0	1	0	0	1	0	E ₀	E ₀ =0: OFF, E ₀ =1: ON
(o)	Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	R ₀	R ₀ =0: OFF, R ₀ =1: ON
(p)	Power save mode ON	0	0	1	0	1	0	1	0	0	1	Power save mode
(q)	Internal oscillator ON	0	0	1	0	1	0	1	0	1	1	-
(r)	Display ON/OFF	0	0	1	0	1	0	1	1	1	D ₀	D ₀ =0: OFF, D ₀ =1: ON
(s)	Page address set	0	0	1	0	1	1	P ₃	P ₂	P ₁	P ₀	-
(t)	COM scan direction select	0	0	1	1	0	0	S ₀	*	*	*	Select common direction
(u)	Power save mode OFF	0	0	1	1	1	0	0	0	0	1	-
(v)	Reset	0	0	1	1	1	0	0	0	1	0	-
(w)	N-line inversion OFF	0	0	1	1	1	0	0	1	0	0	-
(x)	Display data length set (Dual instructions)	0	0	1	1	1	0	1	0	0	0	Set display data length
		0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Specify the data length
(y)	FRC & PWM set	0	0	1	0	0	1	0	FRC	PWM ₁	PWM ₀	-

(*:Don't Care)

Table 3-2. Instruction Codes

Instruction		Code										Descriptions
		RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
(z)	White mode set, 1st/2nd frame	0	0	1	0	0	0	1	0	0	0	Specify mode & frame
				WB ₃	WB ₂	WB ₁	WB ₀	WA ₃	WA ₂	WA ₁	WA ₀	Sets 4-bit pallet registers
	White mode set, 3rd/4th frame	0	0	1	0	0	0	1	0	0	1	Specify mode & frame
				WD ₃	WD ₂	WD ₁	WD ₀	WC ₃	WC ₂	WC ₁	WC ₀	Sets 4-bit pallet registers
	Light gray mode set, 1st/2nd frame	0	0	1	0	0	0	1	0	1	0	Specify mode & frame
				LB ₃	LB ₂	LB ₁	LB ₀	LA ₃	LA ₂	LA ₁	LA ₀	Sets 4-bit pallet registers
	Light gray mode set, 3rd/4th frame	0	0	1	0	0	0	1	0	1	1	Specify mode & frame
				LD ₃	LD ₂	LD ₁	LD ₀	LC ₃	LC ₂	LC ₁	LC ₀	Sets 4-bit pallet registers
(z)	Dark gray mode set, 1st/2nd frame	0	0	1	0	0	0	1	1	0	0	Specify mode & frame
				DB ₃	DB ₂	DB ₁	DB ₀	DA ₃	DA ₂	DA ₁	DA ₀	Sets 4-bit pallet registers
	Dark gray mode set, 3rd/4th frame	0	0	1	0	0	0	1	1	0	1	Specify mode & frame
				DD ₃	DD ₂	DD ₁	DD ₀	DC ₃	DC ₂	DC ₁	DC ₀	Sets 4-bit pallet registers
	Black mode set, 1st/2nd frame	0	0	1	0	0	0	1	1	1	0	Specify mode & frame
				BB ₃	BB ₂	BB ₁	BB ₀	BA ₃	BA ₂	BA ₁	BA ₀	Sets 4-bit pallet registers
	Black mode set, 3rd/4th frame	0	0	1	0	0	0	1	1	1	1	Specify mode & frame
				BD ₃	BD ₂	BD ₁	BD ₀	BC ₃	BC ₂	BC ₁	BC ₀	Sets 4-bit pallet registers
(aa)	Display mode set	0	0	1	1	1	0	1	1	1	DM ₀	DM ₀ =0: Gray scale mode DM ₀ =1: Black & White mode
(bb)	Test mode	0	0	1	1	1	1	*	*	*	*	Don't use.

(*:Don't Care)

(2-1) Descriptions of the Instruction Codes

(a) Status read

The "Status read" instruction is used to read out an LSI internal status. It is available only in the parallel interface mode.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	BUSY	ON	RES	0	0	0	0	0

BUSY 0: The LSI is idle.
 1: The LSI is busy and cannot accept any instruction except the "Status read".

ON 0: Display OFF
 1: Display ON

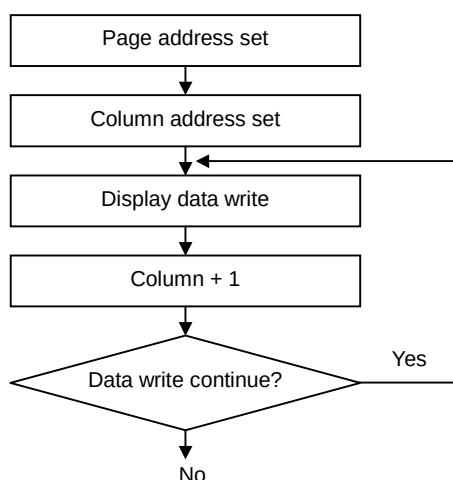
RES 0: The LSI is idle.
 1: The LSI is executing the reset operation.

(b) Display data write

The "Display data write" instruction is used to write display data into the DDRAM, which address is designated by the "Column address set" and "Page address set" instructions. The column address automatically increases by 1 (+1) after each 2-byte display data and wraps around to the column address 00_H in the same page after the last column is addressed. In case that the LSI is used in the 3-line serial interface mode, the "Display data length set" instruction is required before the "Display data write" instruction.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	Display data							

Sequence for the display data writing



(c) Column address set

The “Column address set” instruction is used to specify the column address for display data. It is required before the “Display data write” instruction. An MPU can access only 7-bit [C6:C0] “column address” by the “Column address LSB set” and “Column address MSB set” instructions. When both 4-bit LSB and 3-bit MSB data is set into the column address register, 8-bit “internal column address” is established in the LSI. For this reason, 2-bit display data must be written for each pixel with two successive bytes.

The column address automatically increases by 1 (+1) after each 2-byte display data and wraps around to the column address 00_H in the same page after the last column is addressed, and therefore, the DDRAM can be continuously accessed without another “Column address set” instruction.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	0	0	0	0	C ₃	C ₂	C ₁	C ₀	LSB column address
0	0	0	0	0	1	0	C ₆	C ₅	C ₄	MSB column address

C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	Column address	Internal Column address
0	0	0	0	0	0	0	00 _H	00 _H
								01 _H
0	0	0	0	0	0	1	01 _H	02 _H
								03 _H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	7E _H	FC _H
								FD _H
1	1	1	1	1	1	1	7F _H	FE _H
								FF _H

(d) Internal resistor ratio set

The “Internal resistor ratio set” instruction is used to determine the internal resistor ratio (1+R_b/R_a) for the voltage regulator. For more information, refer to (3-3) “Setting for internal resistor ratio”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	1	0	0	R ₂	R ₁	R ₀

R ₂	R ₁	R ₀	1+(R _b /R _a)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

(e) Power control set

The “Power control set” instruction is used to configure the internal power circuits. For more information, refer to (3) “Internal power circuits”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	
0	-	-	Voltage converter OFF
1	-	-	Voltage converter ON
-	0	-	Voltage regulator OFF
-	1	-	Voltage regulator ON
-	-	0	Voltage followers OFF
-	-	1	Voltage followers ON

(f) Initial display line set

The “Initial display line set” instruction is used to specify the line address, which corresponds to the initial COM₀ line (COM₀).

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	0	1	0	0	0	0	*	*	Set initial display line
0	0	*	L ₆	L ₅	L ₄	L ₃	L ₂	L ₁	L ₀	Specify line address

L ₆	L ₅	L ₄	L ₃	L ₂	L ₁	L ₀	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

(g) Initial COM₀ line set

The “Initial COM₀ line set” instruction is specify the common driver, which starts scanning the display data in the DDRAM.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	0	1	0	0	0	1	*	*	Set initial COM ₀ line
0	0	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	Specify initial COM ₀

C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	Initial COM ₀
0	0	0	0	0	0	0	COM ₀
0	0	0	0	0	0	1	COM ₁
0	0	0	0	0	1	0	COM ₂
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	COM ₁₂₅
1	1	1	1	1	1	0	COM ₁₂₆
1	1	1	1	1	1	1	COM ₁₂₇

(h) Partial display duty set

The “Partial display duty set” instruction is used to specify the duty cycle ratio for the partial display. The LSI can be programmed to select not only the duty cycle ratio, but also the LCD bias ratio, boost level and contrast level by the instructions so that it is possible to optimize the LSI's condition in accordance with the partial display status. For more information, refer to (7) “Partial display function”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	0	1	0	0	1	0	*	*	Set partial display duty
0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Specify duty cycle ratio

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Duty
0	0	0	0	0	0	0	0	Invalid
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	1/16
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	0	0	0	1/128
1	0	0	0	0	0	0	1	Invalid
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	1	1	

(i) N-line inversion register set

The “N-line inversion register set” instruction is used to control the alternate rates of the crystal polarization on an LCD panel. In the N-line inversion mode, the FR signal toggles once every N frames, which number is selected in between 3 and 33 lines, and therefore, prevents a cross talk. If the N-line inversion is disabled by the “N-line inversion mode OFF” instruction, the FR signal toggles by the frame.

The number of the N-line should not be set to 1/2 of the display duty cycle ratio in order to avoid generating a DC bias when the partial display is used.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	0	0	1	1	*	*
0	0	*	*	*	N ₄	N ₃	N ₂	N ₁	N ₀

Set N-line inversion
Specify N-line number

N ₄	N ₃	N ₂	N ₁	N ₀	Number of N-line
0	0	0	0	0	0
0	0	0	0	1	3 lines
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	32 lines
1	1	1	1	1	33 lines

(j) LCD bias set

The “LCD bias set” instruction is used to select the LCD bias ratio. For more information, refer to (3-8) “Voltage followers”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	0	1	0	B ₂	B ₁	B ₀

B ₂	B ₁	B ₀	Bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(k) Boost level set

The “Boost level set” instruction is used to select the multiple for the voltage converter. For detailed information, refer to (3-1) “Voltage converter”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	1	0	0	1	B ₁	B ₀

B ₁	B ₀	Boost
0	0	3x
0	1	4x
1	0	5x
1	1	6x

(l) Contrast level set

The “Contrast level set” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) in accordance with an LCD panel. For detailed information, refer to (3-2) “Voltage regulator”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	0	0	0	0	0	1
0	0	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀

Set contrast level
Specify contrast level

(m) ADC select

The “ADC select” instruction is used to reverse the column address assignment for the segment drivers, so that it is possible to reduce the restriction for the placement of the LSI in an LCD module. For more information, refer to “- Connection between the LSI and LCD panel”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	0	0	0	S ₀

S ₀	Segment direction
0	SEG ₀ to SEG ₁₂₇
1	SEG ₁₂₇ to SEG ₀

(n) Entire display ON/OFF

The “Entire display ON/OFF” instruction is used to enable or disable the entire display, which turns on all pixels without changing the display data in the DDRAM.

The “Entire display ON/OFF” instruction has a priority over the “Reverse display ON/OFF” instruction and the “Display ON/OFF” instruction has the priority over the “Entire display ON/OFF” instruction. As a result, even though the “Entire display ON” can be accepted during the “Display OFF”, the visual state of the LCD panel does not change.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	0	1	0	E ₀

E ₀	Mode
0	Entire display OFF (Normal)
1	Entire display ON

(o) Reverse display ON/OFF

The “Reverse display ON/OFF” instruction is used to enable or disable the reverse display, which reverses the illumination of each pixel without changing the display data in the DDRAM.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	0	1	1	R ₀

R ₀	Mode
0	Reverse display OFF (Normal)
1	Reverse display ON

Reverse display OFF (Normal)

Display data	1	1	1	0	0	1	0	0
Illumination								

Reverse display ON

Display data	1	1	1	0	0	1	0	0
Illumination								

(p) Power save mode ON

The “Power save mode ON” instruction is used to enable the power save mode, where it is possible to reduce the power consumption down to stand-by current level. Both of the LSI’s internal status and the display data in the DDRAM before the “Power save mode ON” instruction are maintained during the power save mode, in which it is possible to access to the DDRAM. The internal status of the LSI in the power save mode is listed below.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	1	0	0	1

Mode	Description
Power save mode	Oscillator OFF LCD power supply OFF COM/SEG outputs V _{SS}

(q) Internal oscillator ON

The “Internal oscillator ON” instruction is used to enable the internal oscillator. Since the oscillator always turns off after the reset operation, this instruction must be executed for the initialization.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	1	0	1	1

(r) Display ON/OFF

The “Display ON/OFF” instruction is used to control the display ON or OFF without changing the display data in the DDRAM.

The “Display ON/OFF” instruction has a priority over the “Entire display ON/OFF” and “Reverse display ON/OFF” instructions. Accordingly, even though the “Entire display ON” and “Reverse display ON” instructions can be accepted during the “Display OFF”, the visual state of the LCD panel does not change.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	0	1	1	1	D ₀

D ₀	Mode
0	Display OFF
1	Display ON

(s) Page address set

The “Page address set” instruction is used to specify the page address for display data. It is required before the “Display data write” instruction.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	1	1	P ₃	P ₂	P ₁	P ₀

(t) COM scan direction select

The “COM scan direction select” is used to select the COM scan direction, so that it is possible to reduce the restriction for the placement of the LSI in an LCD module. For more information, refer to “-Connection between the LSI and LCD panel”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	0	0	S ₀	*	*	*

S ₀	COM scan direction
0	COM ₀ to COM ₁₂₇
1	COM ₁₂₇ to COM ₀

(u) Power save mode OFF

The "Power save mode OFF" instruction is used to release the LSI from the power save mode.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	0	0	0	1

(v) Reset

The "Reset" instruction is used to reset the LSI to the following status. It doesn't change the display data in the DDRAM. It cannot be substituted for the reset operation by the RES terminal. For more information regarding to the reset operation by the RES terminal, refer to (1-8) "Reset circuits".

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	0	0	1	0

Reset status by "Reset" instruction

1. Page address : (0) page
2. Column address : (00)_H
3. Initial display line : (00)_H
4. Contrast level set : 32 level
5. Internal resistor ratio : $1+R_b/R_a=2.3$
6. Display data length : (0,0,0,0)
7. White mode set : OFF
8. White palette register : (0,0,0,0)
9. Light gray mode set : OFF
10. Light gray palette register : (0,0,0,0)
11. Dark gray mode set : OFF
12. Dark gray palette register : (1,1,1,1)
13. Black mode set : OFF
14. Black palette register : (1,1,1,1)
15. FRC, PWM mode : 4-frame, 9-level

(w) N-line inversion mode OFF

The "N-line inversion mode OFF" instruction is used to disable the n-line inversion.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	0	1	0	0

(x) Display data length set

The "Display data length set" instruction is used in the 3-line serial interface mode in order to specify the data length in between 1 and 256 bytes for the display data transferred to the DDRAM. The next transferred data after the display data is distinguished as instruction data.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	1	0	0	0
0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Set display data length
Specify the data length

(y) FRC & PWM set

The “FRC & PWM set” instruction is used to specify the configuration of PWM and FRC for the 4 gray scale display.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	0	1	0	FRC	PWM ₁	PWM ₀

FRC	Frame rate
0	4-frame
1	3-frame

PWM ₁	PWM ₀	PWM level
0	0	9-level
0	1	9-level
1	0	12-level
1	1	15-level

(z) Gray scale mode and register set

The “Gray scale mode and register set” instruction is composed of two bytes and is used to specify the contrast level for each of the gray scale modes. The first byte specifies the gray scale mode and the frame number, and then the second byte sets pallet values into the specified 4-bit pallet register. For detailed information regarding the gray scale function, refer to (5) “Gray scale function”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	1	0	0	0	1	0	0	0	White mode set, 1st/2nd frame
0	0	WB ₃	WB ₂	WB ₁	WB ₀	WA ₃	WA ₂	WA ₁	WA ₀	4-bit pallet registers
0	0	1	0	0	0	1	0	0	1	White mode set, 3rd/4th frame
0	0	WD ₃	WD ₂	WD ₁	WD ₀	WC ₃	WC ₂	WC ₁	WC ₀	4-bit pallet registers
0	0	1	0	0	0	1	0	1	0	Light gray mode set, 1st/2nd frame
0	0	LB ₃	LB ₂	LB ₁	LB ₀	LA ₃	LA ₂	LA ₁	LA ₀	4-bit pallet registers
0	0	1	0	0	0	1	0	1	1	Light gray mode set, 3rd/4th frame
0	0	LD ₃	LD ₂	LD ₁	LD ₀	LC ₃	LC ₂	LC ₁	LC ₀	4-bit pallet registers
0	0	1	0	0	0	1	1	0	0	Dark gray mode set, 1st/2nd frame
0	0	DB ₃	DB ₂	DB ₁	DB ₀	DA ₃	DA ₂	DA ₁	DA ₀	4-bit pallet registers
0	0	1	0	0	0	1	1	0	1	Dark gray mode set, 3rd/4th frame
0	0	DD ₃	DD ₂	DD ₁	DD ₀	DC ₃	DC ₂	DC ₁	DC ₀	4-bit pallet registers
0	0	1	0	0	0	1	1	1	0	Black mode set, 1st/2nd frame
0	0	BB ₃	BB ₂	BB ₁	BB ₀	BA ₃	BA ₂	BA ₁	BA ₀	4-bit pallet registers
0	0	1	0	0	0	1	1	1	1	Black mode set, 3rd/4th frame
0	0	BD ₃	BD ₂	BD ₁	BD ₀	BC ₃	BC ₂	BC ₁	BC ₀	4-bit pallet registers

(aa) Display mode set

The “Display mode set” instruction is used to select either “Gray scale mode” or “Black & White mode”. For more information, refer to (6) “Black & White mode”.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	1	1	1	DM ₀

DM ₀	Display mode
0	Gray scale mode
1	Black & White mode

(bb) Test mode

This instruction is used only for manufacturer's tests.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	1	*	*	*	*

(3) Internal power circuits

The internal power circuits are composed of the voltage converter, voltage regulator with 64-level EVR, and voltage followers. The status of the internal power circuits is arranged by the "Power control set" instruction, as shown in Table 4. For this arrangement, the part of the internal power circuits can be used in combination with an external power supply, as shown in Table 5.

The internal power circuits require the optimum values for the passive components, such as V₀ to V₄ capacitors and external feedback resistors in accordance with an LCD panel; and accordingly should be evaluated by using of actual LCD module samples to decide these values.

Table 4. Power control set

Bits	Portions	Status	
V _C	Voltage converter	1: ON	0: OFF
V _R	Voltage regulator	1: ON	0: OFF
V _F	Voltage followers	1: ON	0: OFF

Table 5. Power supply combinations

Combination	Instruction			Power supply circuits			Output terminals		
	V _C	V _R	V _F	Voltage converter	Voltage regulator	Voltage followers	V _{OUT}	V ₀	V ₁ -V ₄
Using all internal power circuits	1	1	1	ON	ON	ON	Open	Open	Open
Using voltage regulator and voltage followers	0	1	1	OFF	ON	ON	External	Open	Open
Using voltage followers	0	0	1	OFF	OFF	ON	Open	External	Open
Using only external power Supply	0	0	0	OFF	OFF	OFF	Open	External	External

Note) Decoupling capacitors on the V₀ to V₄ terminals are required when the voltage followers are enabled.

(3-1) Voltage converter

The voltage converter is designed to generate a maximum 6x voltage from the voltage difference between the V_{CI} and V_{SS} terminals. It is programmed so that the boost level can be selected out of 3x, 4x, 5x or 6x by the "Boost level set" instruction. Since the voltage converter operates by using of the internal clocks supplied from the oscillator, the oscillator is required to be working during the voltage converter operation. The boosted voltage V_{OUT} must not exceed beyond the 18.0V described in "Absolute maximum ratings". Otherwise, the voltage stress may cause a permanent damage to the LSI. Fig.4 illustrates the capacitor connections for the voltage converter.

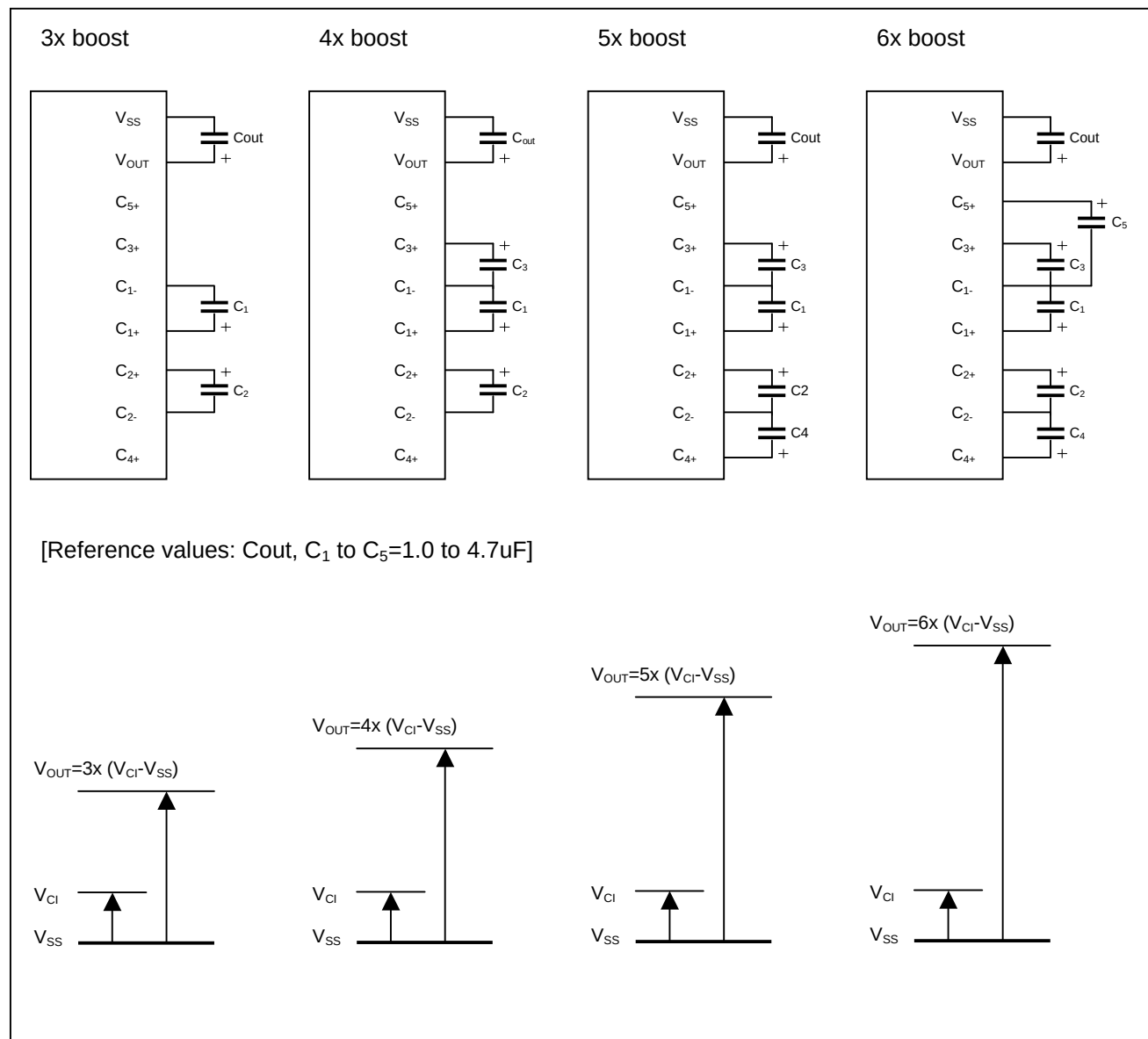
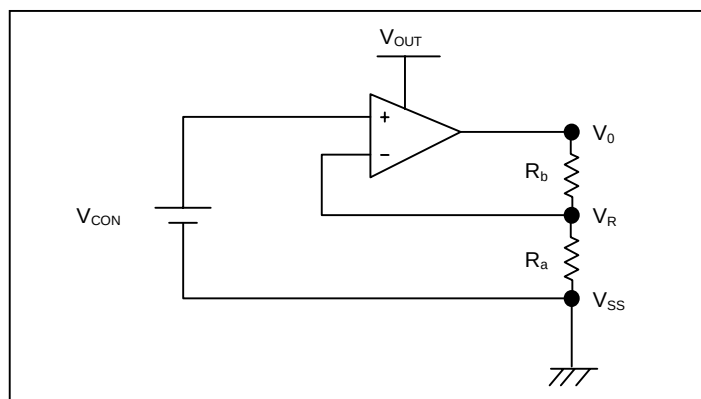


Fig.4 Capacitors connections for the voltage converter

(3-2) Voltage regulator

The voltage regulator is composed of the reference voltage generator, 64-level EVR, operational amplifier, and internal (or external) feedback resistors, as illustrated in Fig.5 and used to generate the LCD driving voltage V_0 . In the voltage regulator, the reference voltage V_{REF} is gained with the EVR to produce regulated voltage V_{CON} , which is used for the input voltage of the internal operational amplifier. Namely, the V_0 is determined in accordance with the setting for the EVR and internal (or external) resistor ratio, as calculated by the following equations [1] and [2].



$$V_0 = (1 + R_b/R_a) \times V_{CON} \quad [1]$$

$$V_{CON} = (1 - (63 - n)/210) \times V_{REF} \quad [2]$$

V_0 : LCD driving voltage
 R_a, R_b : Feed back resistors
 V_{CON} : Contrast control voltage
 n : Parameter decided instruction
 V_{REF} : Reference voltage

Fig.5 Voltage regulator

(3-3) Setting for internal resistor ratio

Either external or internal feedback resistors can be selected by setting the INTRS terminal to "0" or "1", as shown in Table 6. In case that the internal resistors are used, the resistor ratio $(1 + R_b/R_a)$ can be selected by the "Internal resistor ratio" instruction, as listed in Table 7.

Table 6. Setting for the INTRS terminal

INTRS	R_a, R_b
0	External resistors
1	Internal resistors

Table 7. Setting for the internal resistor ratio

R_2	R_1	R_0	$1 + (R_b/R_a)$
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

(3-4) Contrast control voltage VCON

In the equation [2], the VCON depends on the parameter "n", which is determined in between 0 and 63 by the "Contrast level set" instruction.

Table 8. Setting for the contrast level

C5	C4	C3	C2	C1	C0	n	V_{CON}
0	0	0	0	0	0	0	MIN.
:	:	:	:	:	:	:	:
1	1	1	1	1	1	63	MAX.

(3-5) Reference voltage V_{REF}

Either external or internal reference voltage V_{REF} is selected by setting the REF terminal to "0" or "1", as shown in Table 9. When the internal reference voltage V_{REF} is selected, the V_{REF} is designed to be 2.1V Typ. and its temperature coefficient becomes -0.125%/°C Typ.

Table 9. Setting for the REF terminal

REF	V_{REF} (V)	Temperature coefficient
0	External voltage on the VEXT terminal	-
1	Internal voltage ($V_{REF}=2.1V$ Typ.)	-0.125%/°C Typ.

(3-6) Range for the contrast control

The LCD driving voltage V_0 is determined in accordance with the setting for the EVR and the internal (or external) resistor ratio. Fig.6 graphs the range for the contrast control using the "Contrast level set" and "Internal resistor set" instructions.

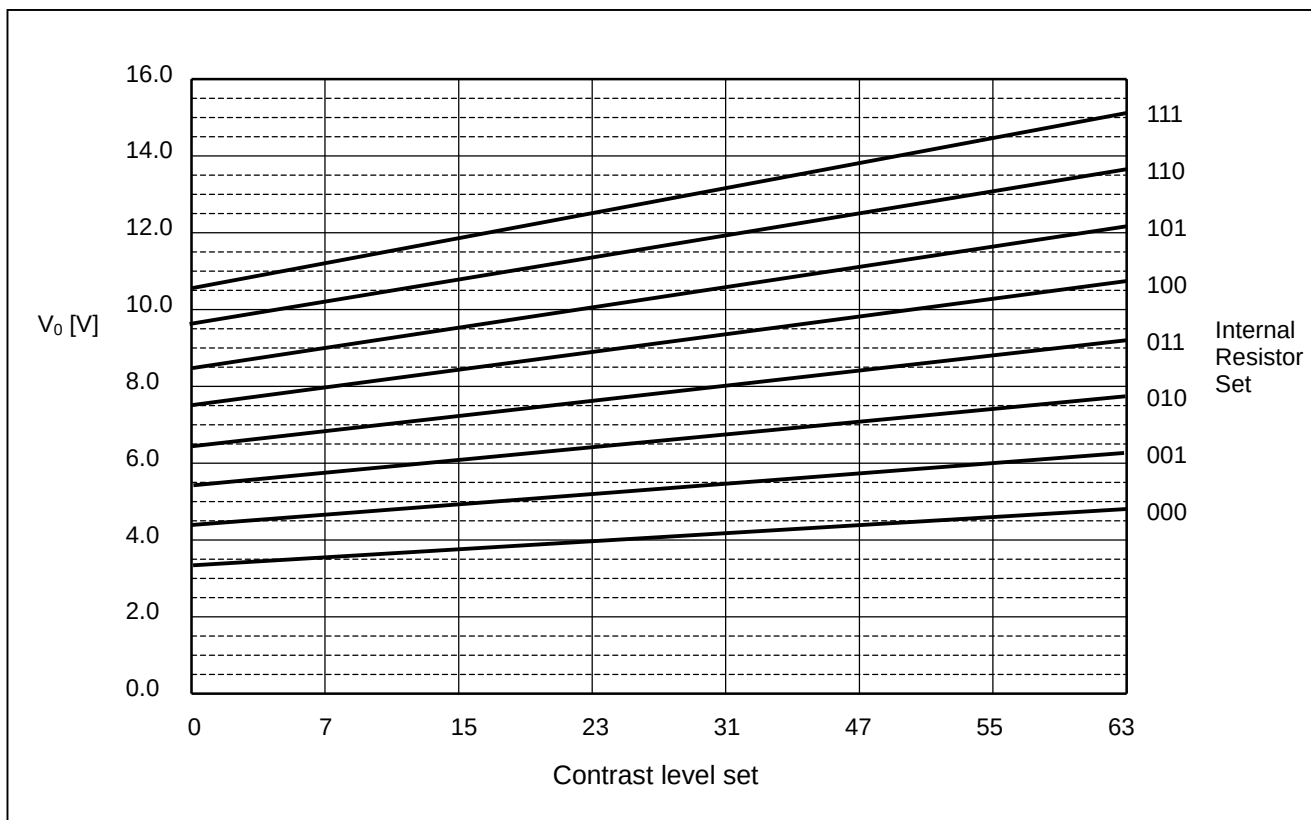


Fig.6 Range for the contrast control

(3-7) Using external Ra and Rb resistors

In case that the external feedback resistors (Ra, Rb) are used by setting the INTRS terminal to "0", these external resistors are required to be placed between the V_{SS} and V_R and between the V_R and V₀ terminals. The LCD driving voltage V₀ is determined in accordance with the setting for the EVR and the external resistor ratio (1+Rb/Ra) in the following equations [1] and [2], as well as the setting in using the internal resistors Ra and Rb.

$$V_0 = (1+R_b/R_a) \times V_{CON} \quad [1]$$

$$V_{CON} = (1-(63-n)/210) \times V_{REF} \quad [2]$$

V₀ : LCD driving voltage
 Ra, Rb : Feed back resistors
 V_{CON} : Contrast control voltage
 n : Parameter decided instruction
 V_{REF} : Reference voltage

The following calculations describe the setting example to decide the external resistors Ra and Rb values.

Requirements:

1. LCD driving voltage V₀=14.0V (when the contrast level parameter "n"=32)
2. The maximum current flowing through the external Ra and Rb = 5uA

Calculations:

Following the equation [2],

$$V_{CON} = (1-(63-32)/210) \times 2.1V = 1.79V$$

Following the equation [1],

$$R_b/R_a = V_0/V_{CON} - 1 = 14.0V/1.79V - 1 = 6.821 \text{ -----[A]}$$

Following the requirement 2,

$$R_a+R_b = 14.0V/5uA = 2.8M \text{ ohm -----[B]}$$

Finally, the values for the Ra and Rb are determined by the results [A] and [B],

Ra = 0.358M ohm

Rb = 2.442M ohm

Contrast level [n]	V ₀ [V]
0	11.5V
:	:
32	14.0V
:	:
63	16.4V

(3-8) Voltage followers

The voltage followers are used to stabilize and output the LCD driving voltages (V₀, V₁, V₂, V₃ and V₄), which are produced by the internal bleeder resistors. It can be programmed to select the LCD bias in the range of 1/5 and 1/12 by the "LCD bias set" instruction. Generally, the optimum bias ratio is determined by the following equation: LCD bias ratio=1/(1+(√duty ratio)). For instance, in case of 1/80 duty cycle ratio, it should be 1/10 in accordance with the calculation: 1/(1+(√80)).

When the voltage followers are used, the capacitors for the V₀ to V₄ terminals are required in order to stabilize the LCD driving voltages and should be in between 0.47uF and 2.0uF.

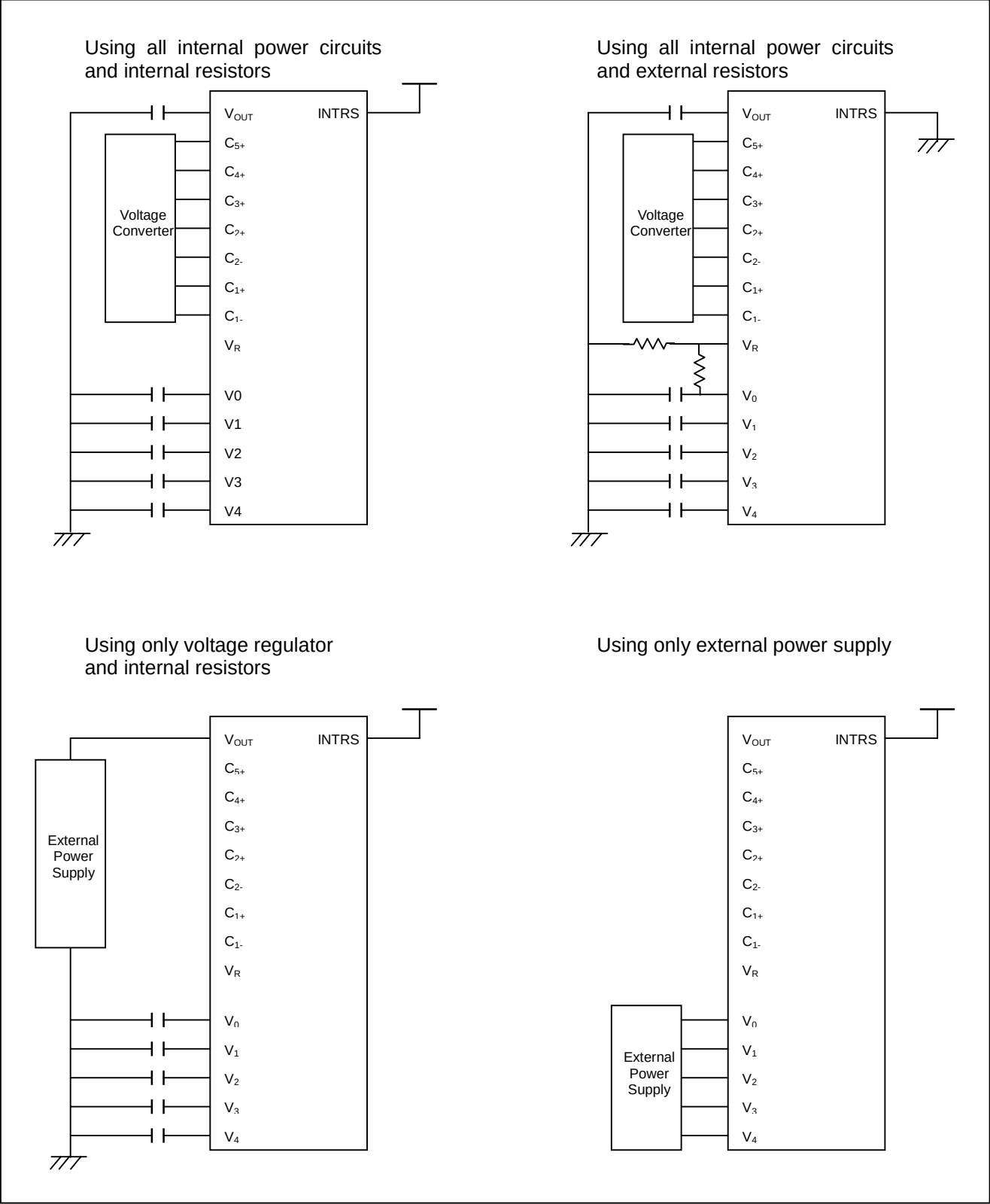


Fig.7 Power circuits configuration

(4) MPU Interface

(4-1) Interface type selection

The interface type (the parallel or serial interface) is determined by the condition of the PS_0 and PS_1 terminals connecting to "H" or "L" level as shown in Table 10. In the 3- or 4- line serial interface mode, the "Status read" instruction cannot be used.

Table 10

PS_0	PS_1	Type	$\overline{CS}$	RS	E	W/R	Data bus terminals
L	L	3-line serial	$\overline{CS}$	*	*	*	SI, SCL
L	H	4-line serial	$\overline{CS}$	RS	*	*	SI, SCL
H	L	80-type MPU parallel	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D_7 to D_0
H	H	68-type MPU parallel	$\overline{CS}$	RS	E	R/W	D_7 to D_0

*:Don't care

(4-2) Parallel interface

In the 68- or 80- type PU parallel inter face mode, the transferred data on the D_7 to D_0 terminals is processed in accordance with the polarities of the RS, $E(\overline{RD})$, and R/W(WR) signals as shown in table 11.

Table 11 Data Distinction

$\overline{CS}$	RS	68 type		80 type		Operation
		E	R/W	$\overline{RD}$	WR	
L	H	H	H	L	H	None
L	H	H	L	H	L	Write display data
L	L	H	H	L	H	Read out status read
L	L	H	L	H	L	Write instruction data

(4-3) Serial Interface

In the serial interface mode, when the chip select is active ($\overline{CS}=0$) the SI and SCL are enabled. While the chip select is not active ($\overline{CS}=1$), the SI & SCL are disabled and the internal 8-bit shift register and the 3-bit counter are being initialized. The 8-bit serial data on the SI terminal is fetched at the at the rising edge of the SCL signals in order of $D_7, D_6 \dots D_0$ data, and the fetched data is converted into 8-bit parallel data on the 8th SCL signals.

(a) 4-line serial interface

In the 4-line serial interface mode, the transferred data on the SI terminal is distinguished as display data or instruction data in accordance with the polarity of the RS signal at the 8th SCL signal, as illustrated in Fig. 8-1.

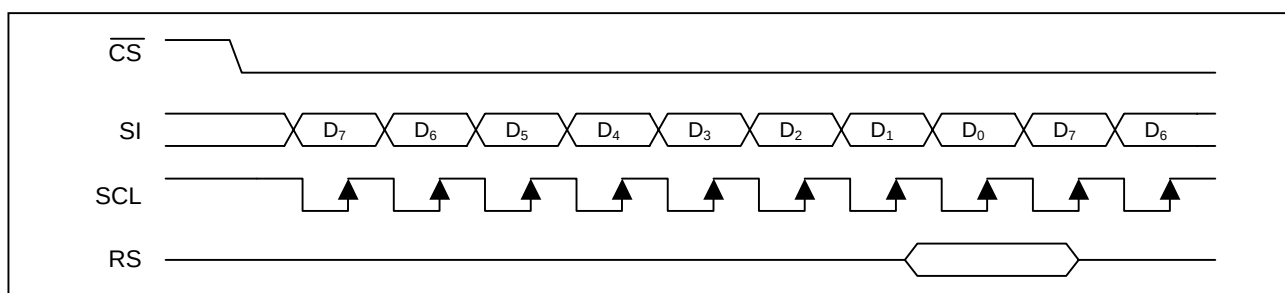


Fig. 8-1 4-line serial interface timing

(b) 3-line serial interface

In the 3-line serial interface mode, the “Display data length set” instruction is used to specify the data length in between 1 and 256 bytes for the display data transferred to the DDRAM. The “Display data length set” instruction is executed by 2 bytes data, after which the display data can be continuously transferred. The next transferred data after the display data is distinguished as instruction data. Fig 8-2 illustrates the timing and setting example for the data transmission in the 3-line serial interface mode.

When the chip select becomes non-active ($\overline{CS}$ ="1") during a serial display data stream, the interrupted byte data is invalid, however all previous transferred display data is valid and next transferred data will be distinguished as instruction data.

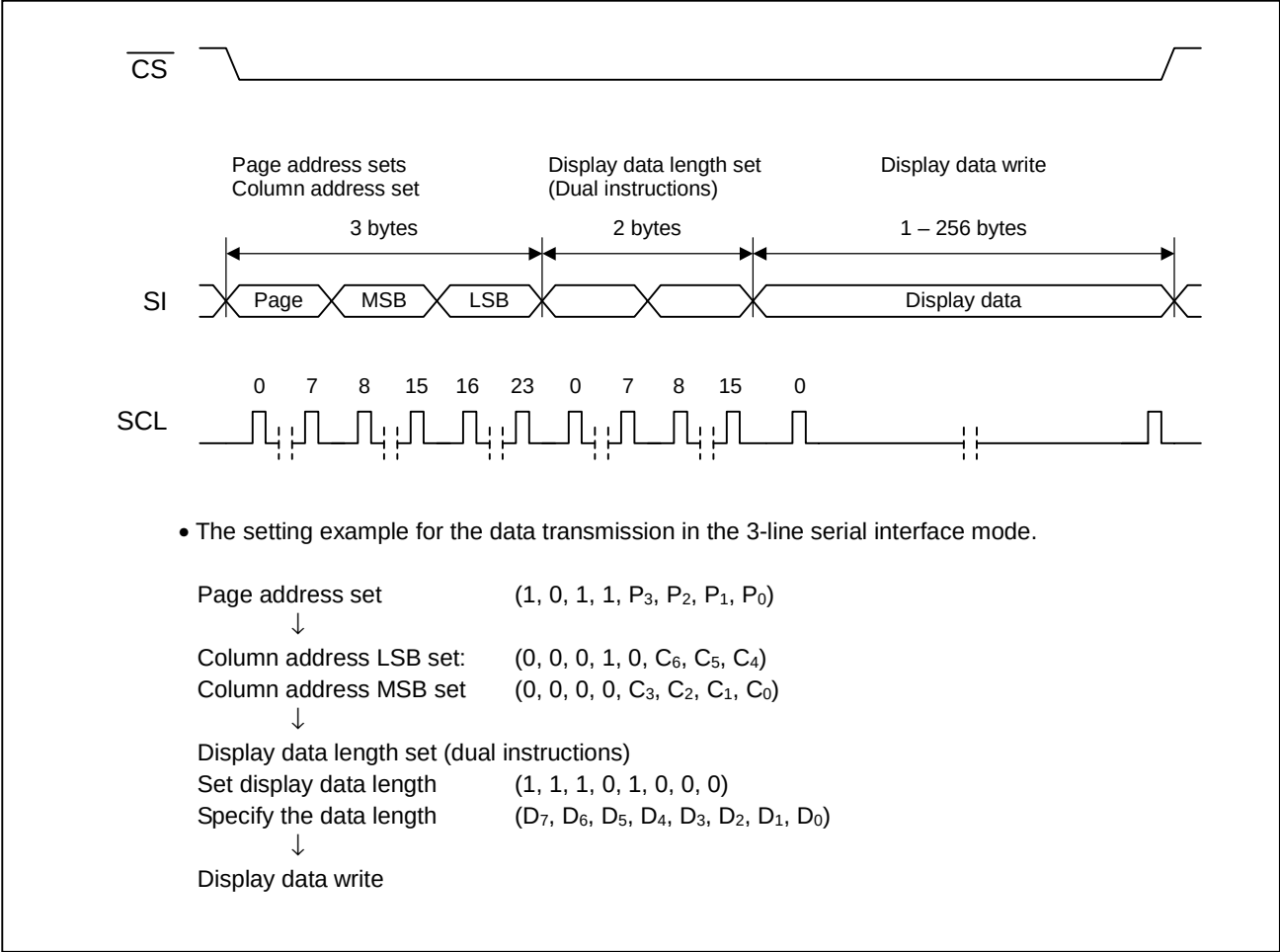


Fig 8-2 3-line serial interface timing

(5) Gray scale function

(5-1) FRC (Frame Rate Control) and PWM (Pulse Width Modulation)

The 4-gray scale function is controlled by the setting for the FRC and PWM configurations and the palette values into the 4-bit palette registers, and provides required gray scale levels. This setting is executed by the “FRC & PWM set” and “Gray scale mode and register set” instructions, as described in the following.

(5-2) FRC & PWM set

The “FRC & PWM set” instruction is used to specify the PWM and FRC configurations.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	0	1	0	FRC	PWM ₁	PWM ₀

FRC	Frame rate
0	4-frame
1	3-frame

PWM ₁	PWM ₀	PWM level
0	0	9-level
0	1	9-level
1	0	12-level
1	1	15-level

(5-3) Gray scale mode & Register set

The “Gray scale mode and register set” instruction is composed of two bytes and used to specify the contrast level for each of the gray scale modes. The first byte specifies the gray scale mode and frame number and then the second byte sets the pallet value into the specified 4-bit pallet register.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	0	0	1	GM ₂	GM ₁	GM ₀
0	0	4-bit pallet register				4-bit pallet register			

Gray scale mode & frame
4-bit pallet register set

GM ₂	GM ₁	GM ₀	Gray scale mode & Frame	
0	0	0	White mode	1st/2nd frame
0	0	1		3rd/4th frame
0	1	0	Light gray mode	1st/2nd frame
0	1	1		3rd/4th frame
1	0	0	Dark gray mode	1st/2nd frame
1	0	1		3rd/4th frame
1	1	0	Black mode	1st/2nd frame
1	1	1		3rd/4th frame

(5-4) Setting tables for the FRC and PWM

Table 12-1. Gray scale table for the 4-FRC

Gray scale level	Display data	MSB (D ₇ to D ₄)	LSB (D ₃ to D ₀)
White	00	2nd frame	1st frame
		4th frame	3rd frame
Light gray	01	2nd frame	1st frame
		4th frame	3rd frame
Dark gray	10	2nd frame	1st frame
		4th frame	3rd frame
Black	11	2nd frame	1st frame
		4th frame	3rd frame

Table 12-2. Gray scale table for the 3-FRC

Gray scale level	Display data	MSB (D ₇ to D ₄)	LSB (D ₃ to D ₀)
White	00	2nd frame	1st frame
		*	3rd frame
Light gray	01	2nd frame	1st frame
		*	3rd frame
Dark gray	10	2nd frame	1st frame
		*	3rd frame
Black	11	2nd frame	1st frame
		*	3rd frame

Note) *: Don't care.

Table 13. Gray scale table for the PWM

4-bit palett register	9-PWM	12-PWM	15-PWM
0,0,0,0	0	0	0
0,0,0,1	1/9	1/12	1/15
0,0,1,0	2/9	2/12	2/15
0,0,1,1	3/9	3/12	3/15
0,1,0,0	4/9	4/12	4/15
0,1,0,1	5/9	5/12	5/15
0,1,1,0	6/9	6/12	6/15
0,1,1,1	7/9	7/12	7/15
1,0,0,0	8/9	8/12	8/15
1,0,0,1	1	9/12	9/15
1,0,1,0	0	10/12	10/15
1,0,1,1	0	11/12	11/15
1,1,0,0	0	1	12/15
1,1,0,1	0	0	13/15
1,1,1,0	0	0	14/15
1,1,1,1	0	0	1

(6) Black & White mode

As an extended function, the LSI is designed to support the black & white mode, which can be switched from the gray scale mode by the "Display mode set" instruction. The gray scale mode is set in the default status.

(6-1) Display mode set instruction

The "Display mode set" instruction is used to select either gray scale or black & white mode. It is required that the "Display OFF" instruction and DDRAM initialization are executed before the "Display mode set" instruction.

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	1	0	1	1	1	DM ₀

DM ₀	Display mode
0	Gray scale mode
1	Black & White mode

(6-2) Display data RAM (DDRAM)

Although the DDRAM's capability in the gray scale mode is 32,768-bit (128-line by 256-column) for the LCD panel with up to 128x128 pixels, the capability in the black & white mode is 16,384-bit out of the total memory area, as illustrated in the Fig 9. In the black and white mode, 1-bit display data is used for 1-pixel.

(6-3) Column address set

In the black & white mode, an MPU can access 7-bit [C6:C0] column address by the "Column address LSB set" and "Column address MSB set" instructions. The column address automatically increases by 1 (+1) after each 1-byte display data.

(6-4) Display data length set

The "Display data length set" instruction is used in the 3-line serial interface mode in order to specify the data length in between 1 and 128 bytes in the black & white mode. The D₇ bit in the "Display data length set" instruction must be "0".

RS	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	1	0	1	0	0	0
0	0	(D ₇)	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Set display data length
Specify the data length

(D₇) : Must be "0" in the black & white mode

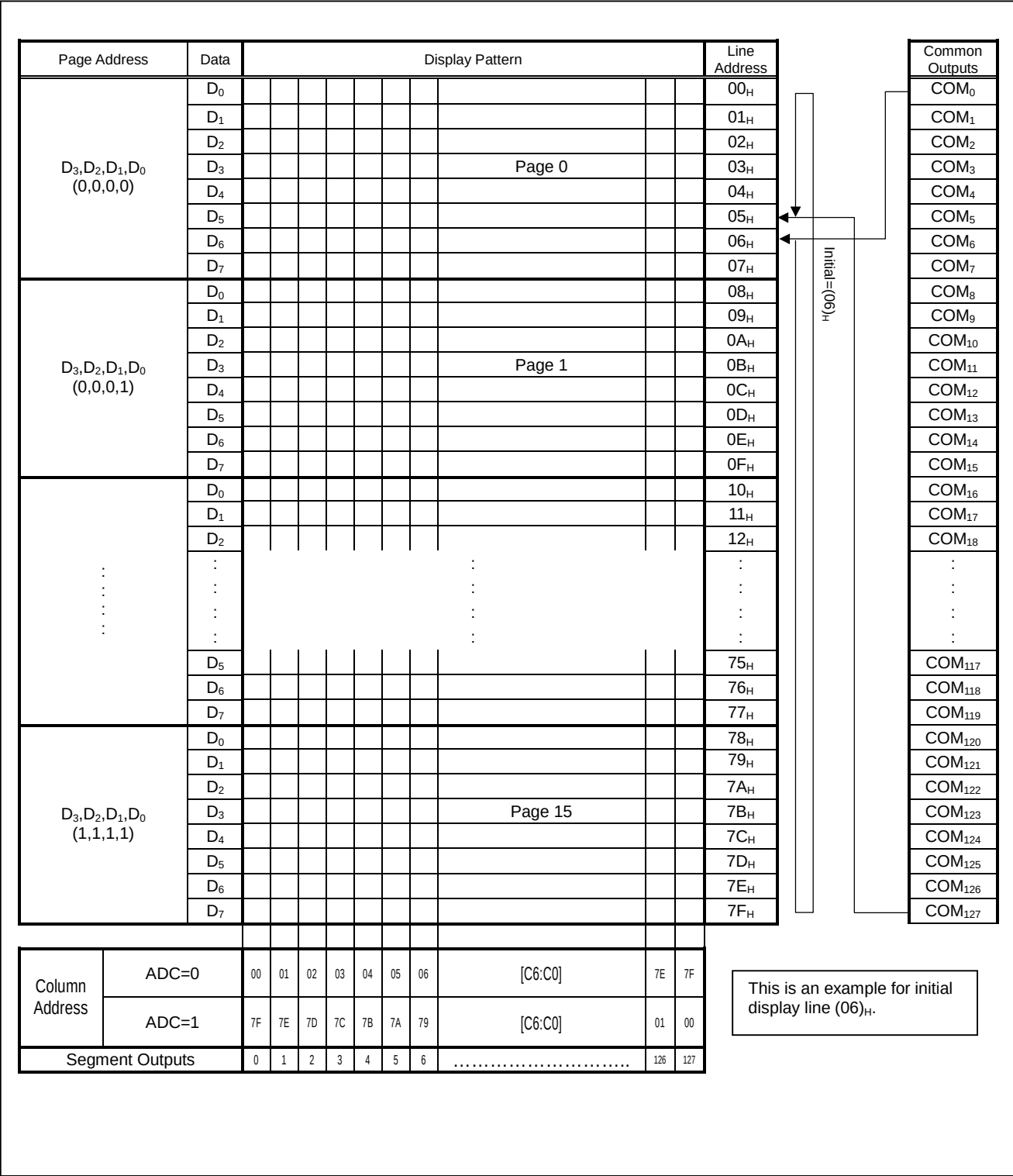


Fig.9 Display data RAM (DDRAM) Map in the Black & White mode

(7) Partial display function

The partial display function is used to specify optimum duty cycle ratio, LCD bias ratio, boost level and LCD driving voltage to partially display active area on an LCD panel, so that it is possible to display the time and calendar under extremely low power consumption state. It can be programmed to select the duty cycle ratio, LCD bias ratio, boost level and EVR level by the instructions. Fig.10-1 illustrates normal display image and Fig.10-2, 10-3 and 10-4 illustrate the partial display images. The setting sequence for the partial display is described in Fig.15.

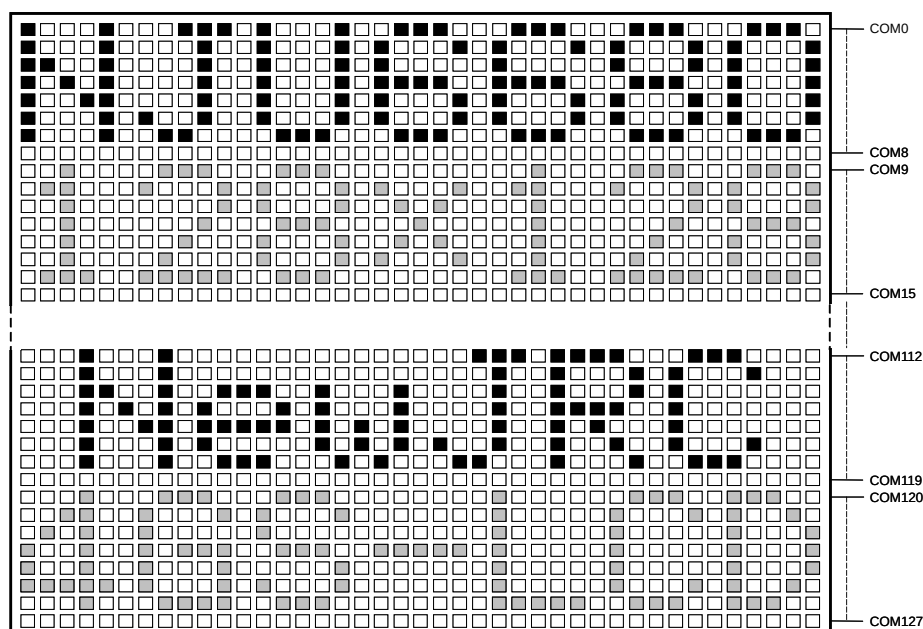


Fig.10-1 Normal display image (duty cycle ratio=1/128, COM₀=0)

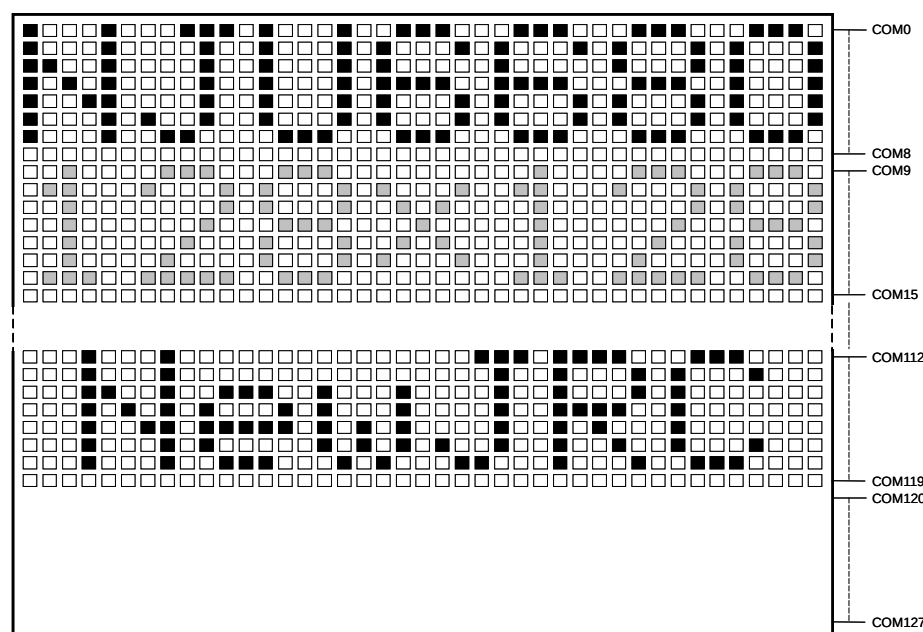


Fig.10-2 Partial display image 1 (duty cycle ratio=1/120, COM₀=0)

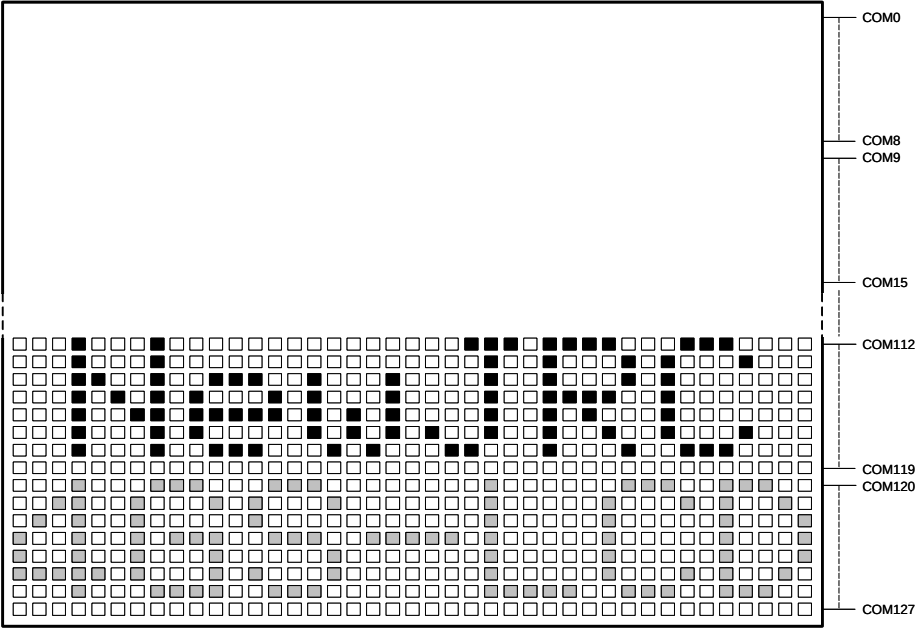


Fig.10-3 Partial display image 2 (duty cycle ratio=1/16, COM₀=112)

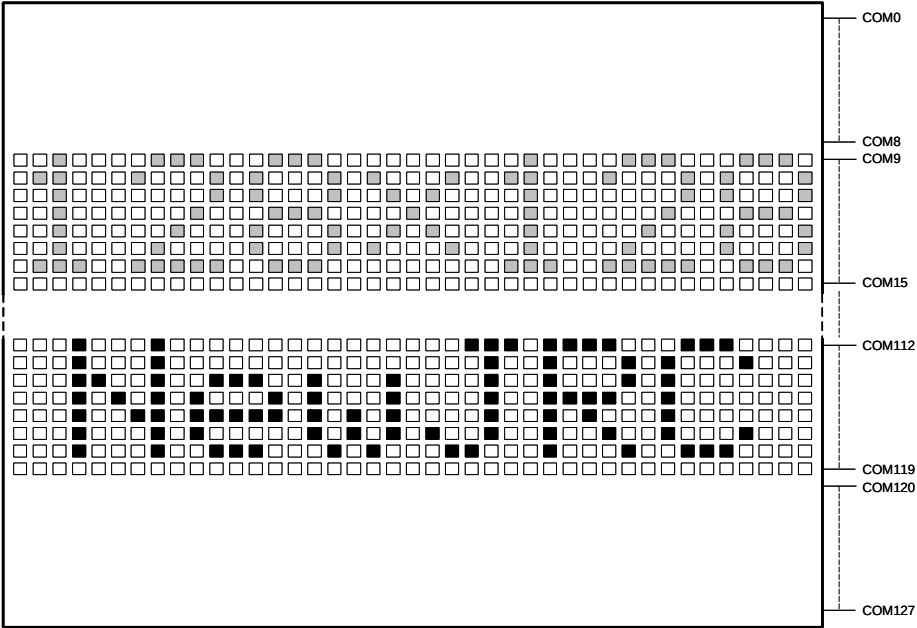


Fig.10-4 Partial display image 3 (duty cycle ratio=1/112, COM₀=9)

■ Examples for instruction sequence

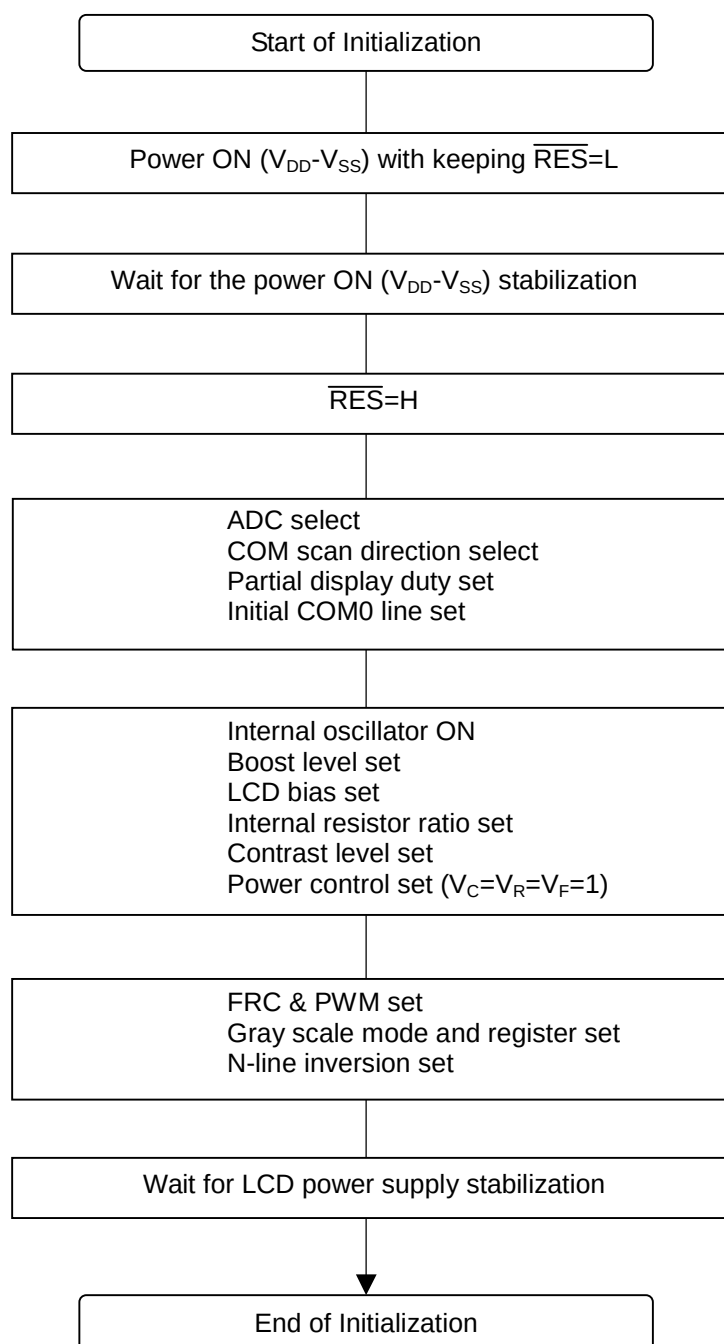


Fig.11 Initialization in using the internal power circuits

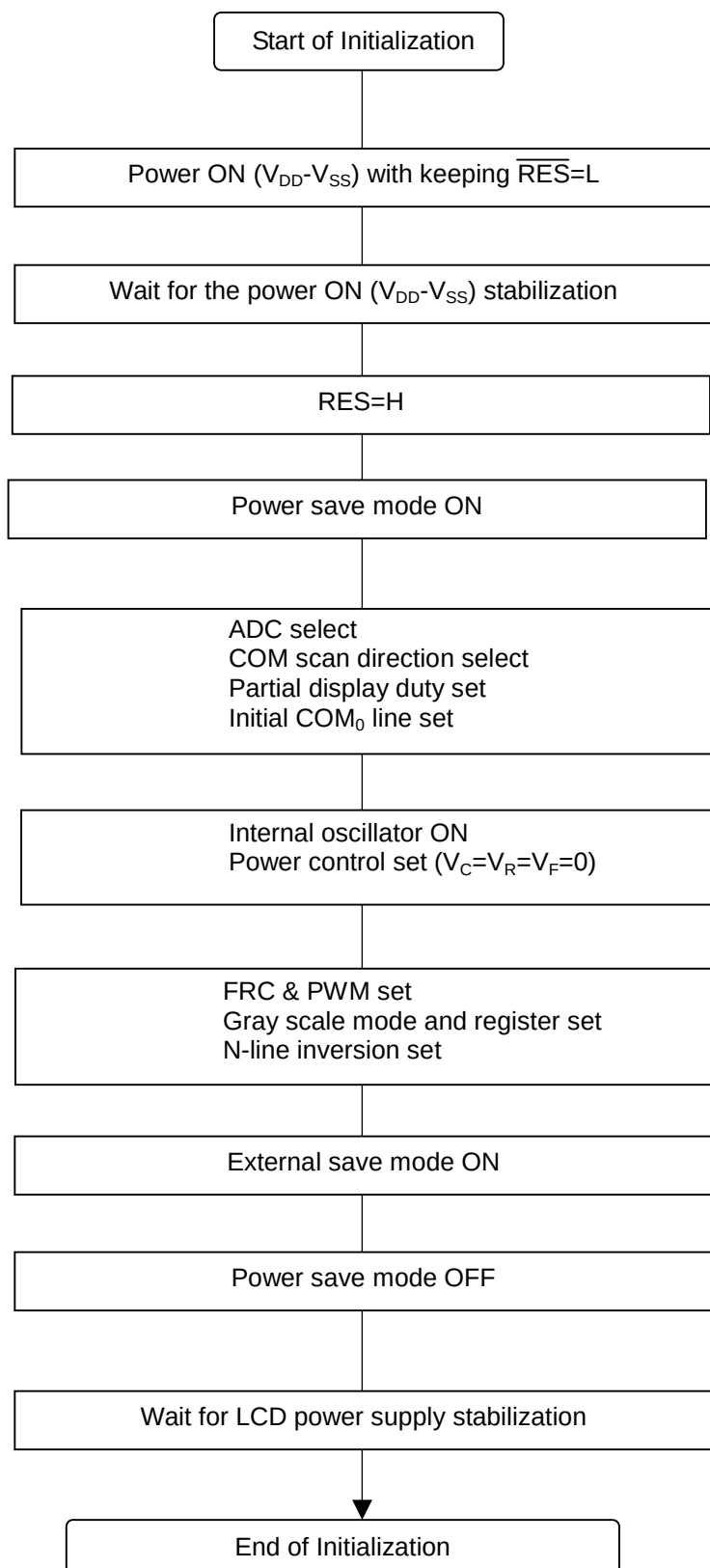


Fig.12 Initialization in using the external power supply

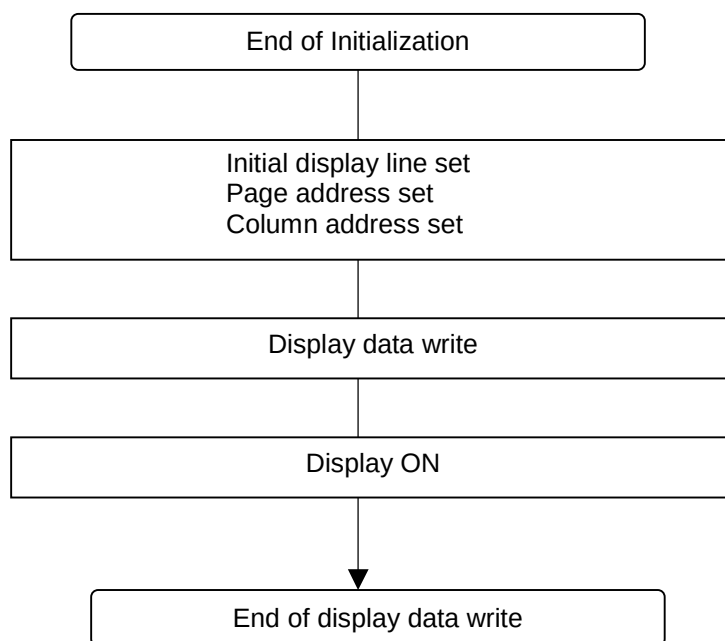


Fig.13 Display data write sequence

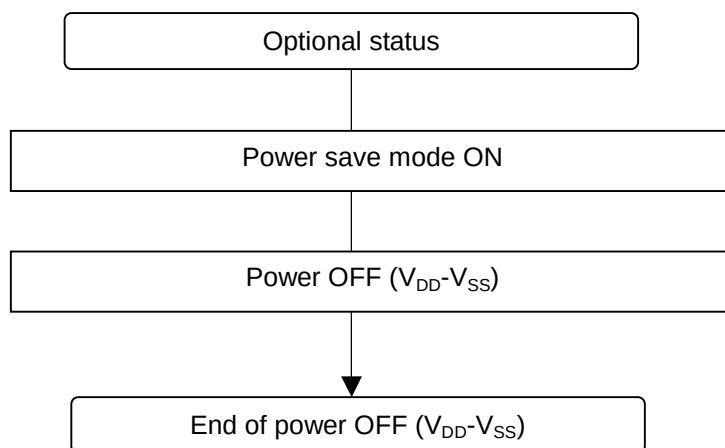


Fig.14 Power OFF sequence

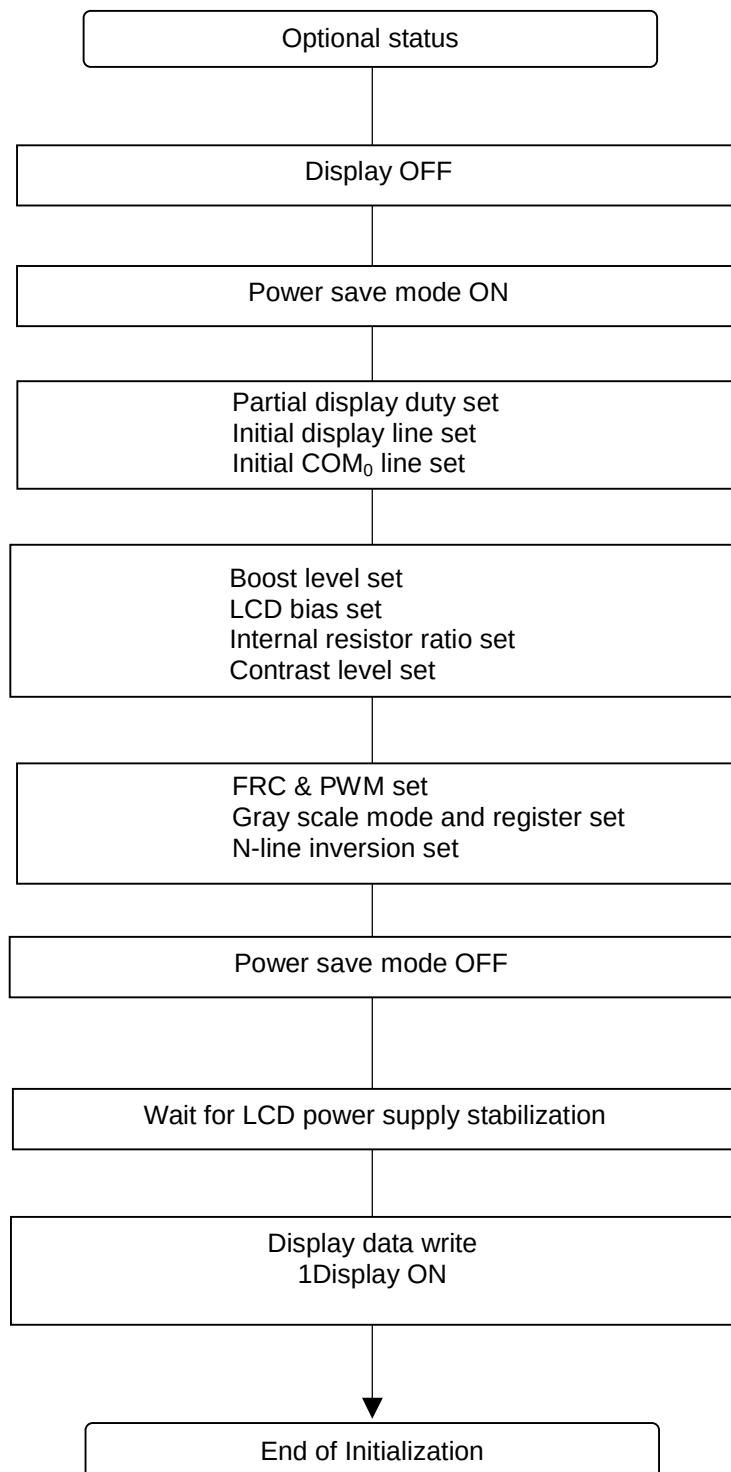
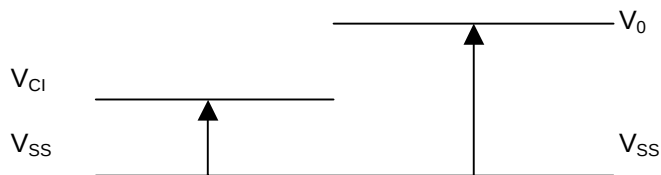


Fig.15 Partial display sequence

■ ABSOLUTE MAXIMUM RATING

(Ta=25°C)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage(1)		V_{DD}, V_{CI}	-0.3 to +4.0	V
Supply Voltage(2)		V_0, V_{OUT}	$V_{SS}-0.3$ to $V_{SS}+18.0$	V
Supply Voltage(3)		V_1, V_2, V_3, V_4	-0.3 to $V_0+0.3$	V
Input Voltage		V_{IN}	-0.3 to $V_{DD}+0.3$	V
Operating Temperature		T_{OPR}	-40 to +85	°C
Storage Temperature	TCP	T_{STG}	-55 to +100	°C
	Chip		-55 to +125	



Note 1) All voltages are relative to $V_{SS}=0V$ reference.

The relationship among the supply voltages should be maintained in the following condition:

$$V_{SS} \leq V_4 \leq V_3 \leq V_2 \leq V_1 \leq V_0 \leq V_{OUT}$$

Note 2) When the external power supply is used for the LCD driving voltages, the external power supply should be turned on at the same timing or after the timing that the V_{DD} is turned on.

Note 3) The LSI should be operated inside of the "Absolute maximum ratings" in order to prevent excessive stress. Otherwise, the stresses beyond the "Absolute Maximum Ratings" may cause a permanent damage to the LSI.

Note 4) The decoupling capacitors between the V_{DD} , V_{CI} , and V_{SS} terminals are required in order to stabilize the LSI operation.

ELECTRICAL CHARACTERISTICS

($V_{DD}=2.2$ to $3.6V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$)

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Operating voltage(1)		V_{DD}	-		2.2	-	3.6	V	5
			$V_{DD}=2.7V$		2.7	2.775	2.875		
Operating voltage(2)		V_{CI}	6-times boost $V_{DD}=2.2$ to $3.0V$		V_{DD}	-	3.0	V	-
			3,4,5-times boost $V_{DD}=2.2$ to $3.6V$		V_{DD}	-	3.6		
Operating voltage(3)		V_0	$V_{LCD}=V_0-V_{SS}$		6.0	-	15.0	V	-
		V_1, V_2			$0.6V_0$	-	V_0		
		V_3, V_4			V_{SS}	-	$0.4V_0$		
Input Voltage	High Level	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	V	-
	Low Level	V_{IL}			V_{SS}	-	$0.2V_{DD}$		
Output Voltage	High Level	V_{OH}	D ₀ to D ₁ Terminal	$I_{OH}=-0.5mA$	$0.8V_{DD}$	-	V_{DD}	V	-
	Low Level	V_{OL}		$I_{OL}=0.5mA$	V_{SS}	-	$0.2V_{DD}$		
Input Leakage Current		I_{LI}	-		-1.0	-	1.0	μA	-
Output Leakage Current		I_{LO}	-		-3.0	-	3.0	μA	-
Driver On-resistance		R_{ON}	$V_0=8.0V$		-	3.0	4.5	$k\Omega$	6
Stand-by Current		I_{sleep}	In Power Save Mode		-	-	2.0	μA	7
Input Terminal Capacitance		C_{IN}	$T_a=25^{\circ}C$		-	10	-	pF	8
Frame Frequency		f_{FR}	$R_f=270k\Omega$		150	-	180	Hz	-
Reset Time		t_R	RES terminal		1.0	-	-	μS	9
Reset "L" level pulse Width		t_{RW}	-		10	-	-	μS	10

Input Voltage	V_{CI}	$V_{DD}-V_{SS}$ $V_{DD}=2.2$ to $3.0V$ 6-times boost	V_{DD}	-	3.0	V	11
Voltage converter efficiency	$V_{REG}\%$	No-load	95	99	-	%	-
Voltage Follower operating voltage	V_0	Voltage regulator "OFF"	6.0	-	16.5	V	-
Voltage converter output on resuistance	R_{STEP}	C_1 to C_5 , $C_{OUT}=1.0\mu F$ 6-times boost	-	2.0	4.0	$k\Omega$	-
Operating Current	I_{OUT1}	$T_a=25^{\circ}C$, $V_{DD}=2.75V$ (Checker board display, No access from MPU, All COM/SEG open)	-	400	550	μA	13
Reference Voltage	V_{REF}	$T_a=25^{\circ}C$	2.04	2.10	2.16	V	-
External reference voltage	V_{EXT}	-	2.0	-	V_{DD}	V	-
V_{REF} temp.Coefficient	TC	$V_{DD}=3.0V$	-	-0.125	-	$\%/^{\circ}C$	-

Note 5) This parameter cannot be guaranteed for the spike voltage during an MPU access.

Note 6) Apply to the resistance between each driver (COM, SEG) and power supply (V_1, V_2, V_3, V_4) terminals when the voltage difference 0.1V is supplied between these terminals.

Note 7) Apply to the condition when the internal power circuits are not used and MPU doesn't access to the LSI.

Note 8) Apply to the D_7 to D_0 , E, R/W, RS, $\overline{CS}$, PS_0 and PS_1 terminals.

Note 9) Specified the time between the rising edge of the $\overline{RES}$ signal and the completion of the reset operation.

Note 10) Specify the minimum pulse width of the $\overline{RES}$ signal.

Note 11) Apply to the V_{DD} when 6x boost level is used.

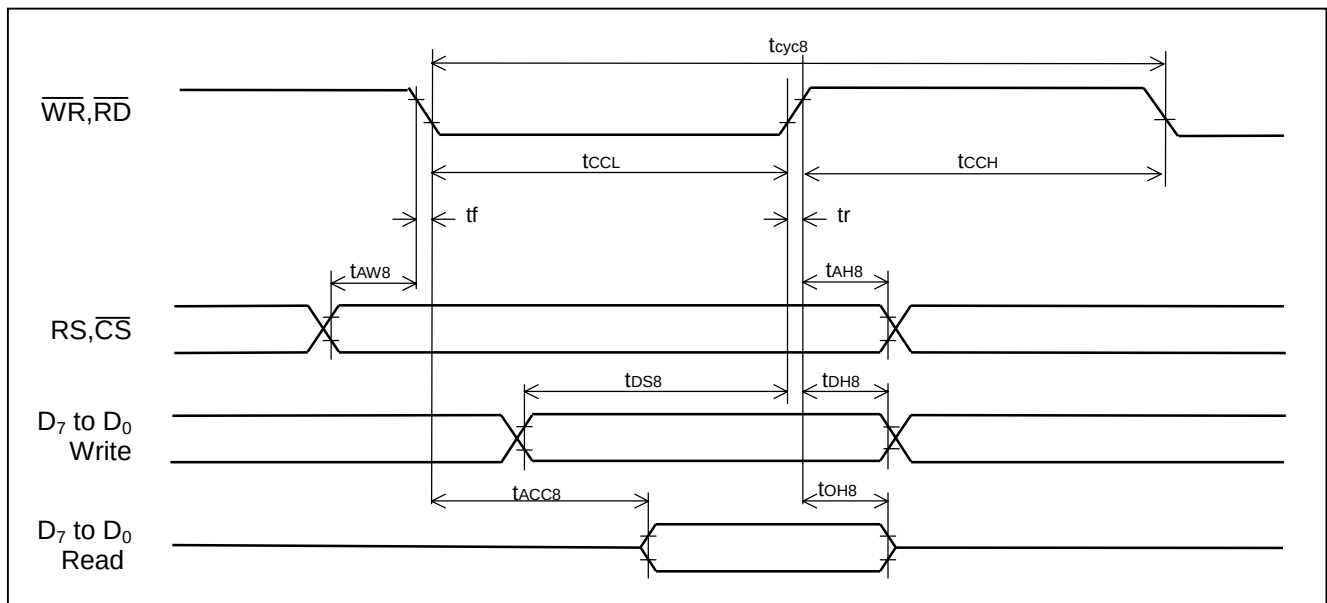
Note 12) The LCD driving voltage can be adjusted within the operating range of the voltage converter.

Note 13) Each of the values is specified by each of the following conditions.

SYMBOL	POWER SUPPLY SET INSTRUCTION			OPERATING CONDITION		
	VC	VR	VF	Voltage converter	Voltage regulator	Voltage follower
I_{OUT1}	1	1	1	ON (5 times)	ON	ON

BUS TIMING CHARACTERISTICS

- Read/Write operation sequence(80 type MPU)



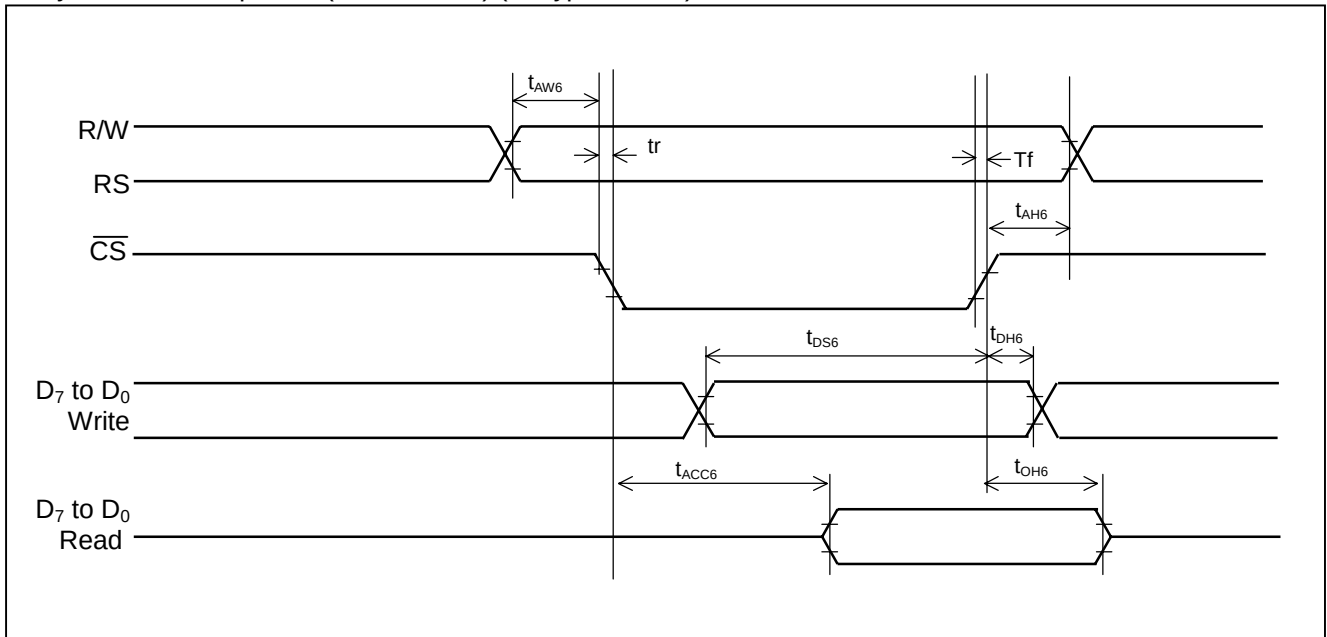
(V_{SS}=0V, V_{DD}=2.2V, Ta=-40 to +85°C)

PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Address set up time		RS, $\overline{CS}$	t _{AW8}	-	0	-	ns
Address hold time			t _{AH8}		0	-	
System cycle time			t _{cyc8}		330	-	
Control “H” pulse width	Read	$\overline{WR},\overline{RD}$	t _{CCHR}	-	210	-	
	Write		t _{CCHW}		210	-	
Control “L” pulse width	Read		t _{CCLR}		120	-	
	Write		t _{CCLW}		60	-	
Data set up time		D ₇ to D ₀	t _{DS8}	-	40	-	
Data hold time			t _{DH8}		15	-	
RD access time			t _{ACC8}	CL=100pF	-	114	
Output disable time			t _{OH8}		5	50	
Input signal rising, falling edge		-	tr,tf	-	-	15	

(V_{SS}=0V, V_{DD}=3.0V, Ta=-40 to +85°C)

PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Address set up time		RS, $\overline{CS}$	t _{AW8}	-	0	-	ns
Address hold time			t _{AH8}		0	-	
System cycle time			t _{cyc8}		166	-	
Control “H” pulse width	Read	$\overline{WR}, \overline{RD}$	t _{CCHR}	-	70	-	
	Write		t _{CCHW}		70	-	
Control “L” pulse width	Read		t _{CCLR}		70	-	
	Write		t _{CCLW}		30	-	
Data set up time		D ₇ to D ₀	t _{DS8}	-	30	-	
Data hold time			t _{DH8}		10	-	
RD access time			t _{ACC8}	CL=100pF	-	50	
Output disable time			t _{OH8}		5	50	
Input signal rising, falling edge			-		tr,tf	-	

• System BUS Sequence (Read / Write) (68-type 1 MPU)



($V_{SS}=0V$, $V_{DD}=2.2V$, $T_a=-40$ to $+85^{\circ}C$)

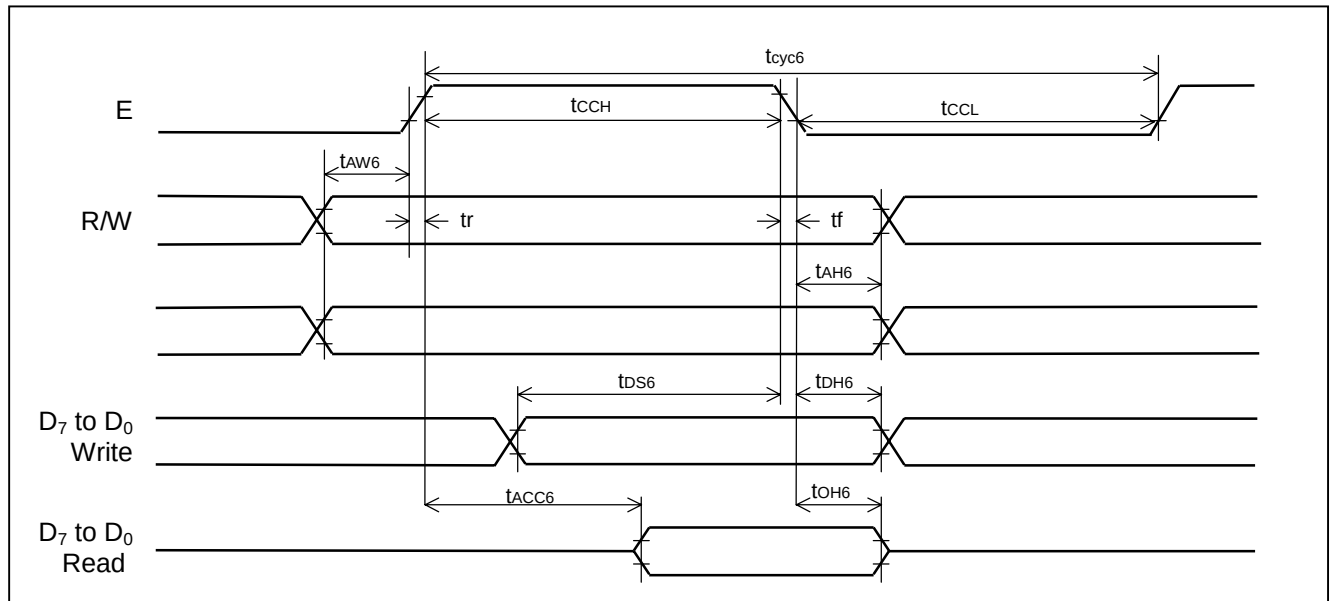
PARAMETER	SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Address set up time	RS, $\overline{CS}$	t_{AW6}	-	0	-	ns
Address hold time		t_{AH6}	-	0	-	
System cycle time		t_{cyc6}	-	350	-	
Data set up time	D ₇ to D ₀	t_{DS6}	-	40	-	
Data hold time		t_{DH6}	-	10	-	
RD access time		t_{ACC6}	CL=100pF	-	128	
Output disable time		t_{OH6}		5	50	
Input signal rising, falling edge	-	tr,tf	-	-	15	

($V_{SS}=0V$, $V_{DD}=3.0V$, $T_a=-40$ to $+85^{\circ}C$)

PARAMETER	SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Address set up time	RS, $\overline{CS}$	t_{AW6}	-	0	-	ns
Address hold time		t_{AH6}	-	0	-	
System cycle time		t_{cyc6}	-	166	-	
Data set up time	D ₇ to D ₀	t_{DS6}	-	30	-	
Data hold time		t_{DH6}	-	10	-	
RD access time		t_{ACC6}	CL=100pF	-	52	
Output disable time		t_{OH6}		5	50	
Input signal rising, falling edge	-	tr,tf	-	-	15	

Note 14) Apply to the condition that E pin is always fixed to "H".

• System BUS Sequence (Read / Write) (68-type 2 MPU)



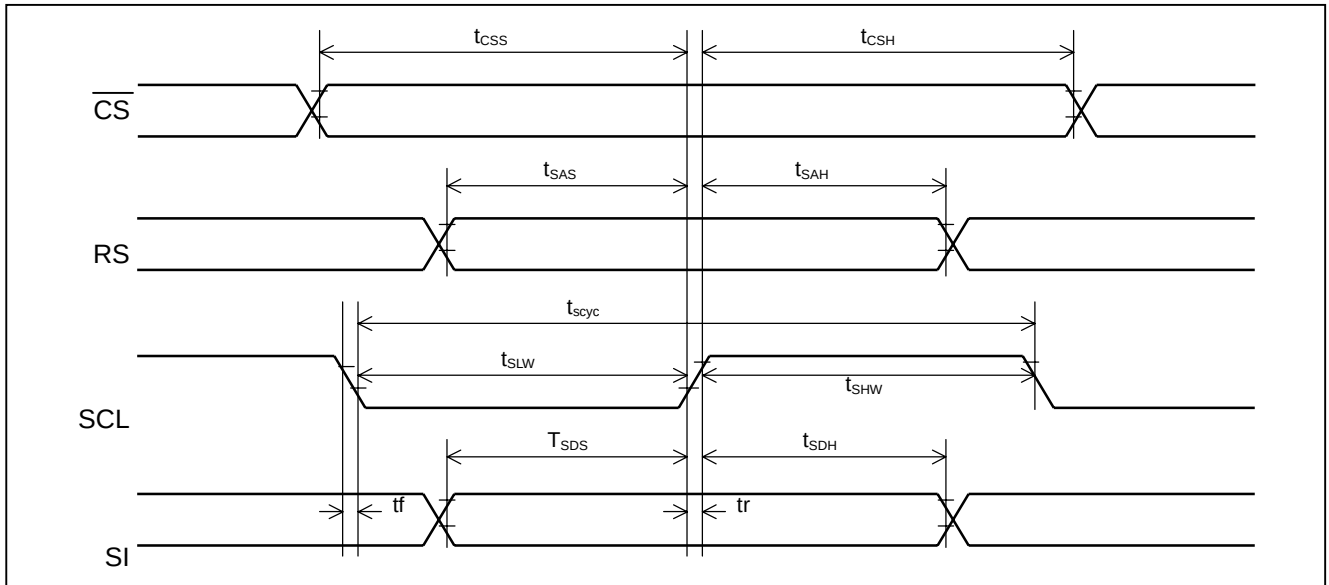
($V_{SS}=0V$, $V_{DD}=2.2V$, $T_a=-40$ to $+85^{\circ}C$)

PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Address set up time		RS,CS	t _{AW6}	-	0	25	ns
Address hold time			t _{AH6}		0	-	
System cycle time			t _{CYC6}		350	-	
Enable “H” pulse width	Read	E	t _{CCHR}	-	140	-	
	Write		t _{CCHW}		60	-	
Enable “L” pulse width	Read		t _{CCLR}		140	-	
	Write		t _{CCLW}		60	-	
Data set up time		D ₇ to D ₀	t _{DS6}	-	40	-	
Data hold time			t _{DH6}		10	-	
RD access time			t _{ACC6}	CL=100pF	15	-	
Output disable time			t _{OH6}		5	50	
Input signal rising, falling edge		-	tr, tf	-	-	15	

($V_{SS}=0V$, $V_{DD}=3.0V$, $T_a=-40$ to $+85^{\circ}C$)

PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT		
Address set up time		RS,CS	t _{AW6}	-	0	-	ns		
Address hold time			t _{AH6}		0	-			
System cycle time			t _{CYC6}		166	-			
Enable “H” pulse width	Read	E	t _{CCHR}	-	70	-			
	Write		t _{CCHW}		70	-			
Enable “L” pulse width	Read		t _{CCLR}		40	-			
	Write		t _{CCLW}		40	-			
Data set up time			D ₇ to D ₀		t _{DS6}	-		30	-
Data hold time					t _{DH6}			10	-
RD access time		t _{ACC6}		CL=100pF	15	-			
Output disable time		t _{OH6}			5	50			
Input signal rising, falling edge		-		tr,tf	-			15	

• Serial Interface



($V_{SS}=0V$, $V_{DD}=2.2V$, $T_a=-40$ to $+85^{\circ}C$)

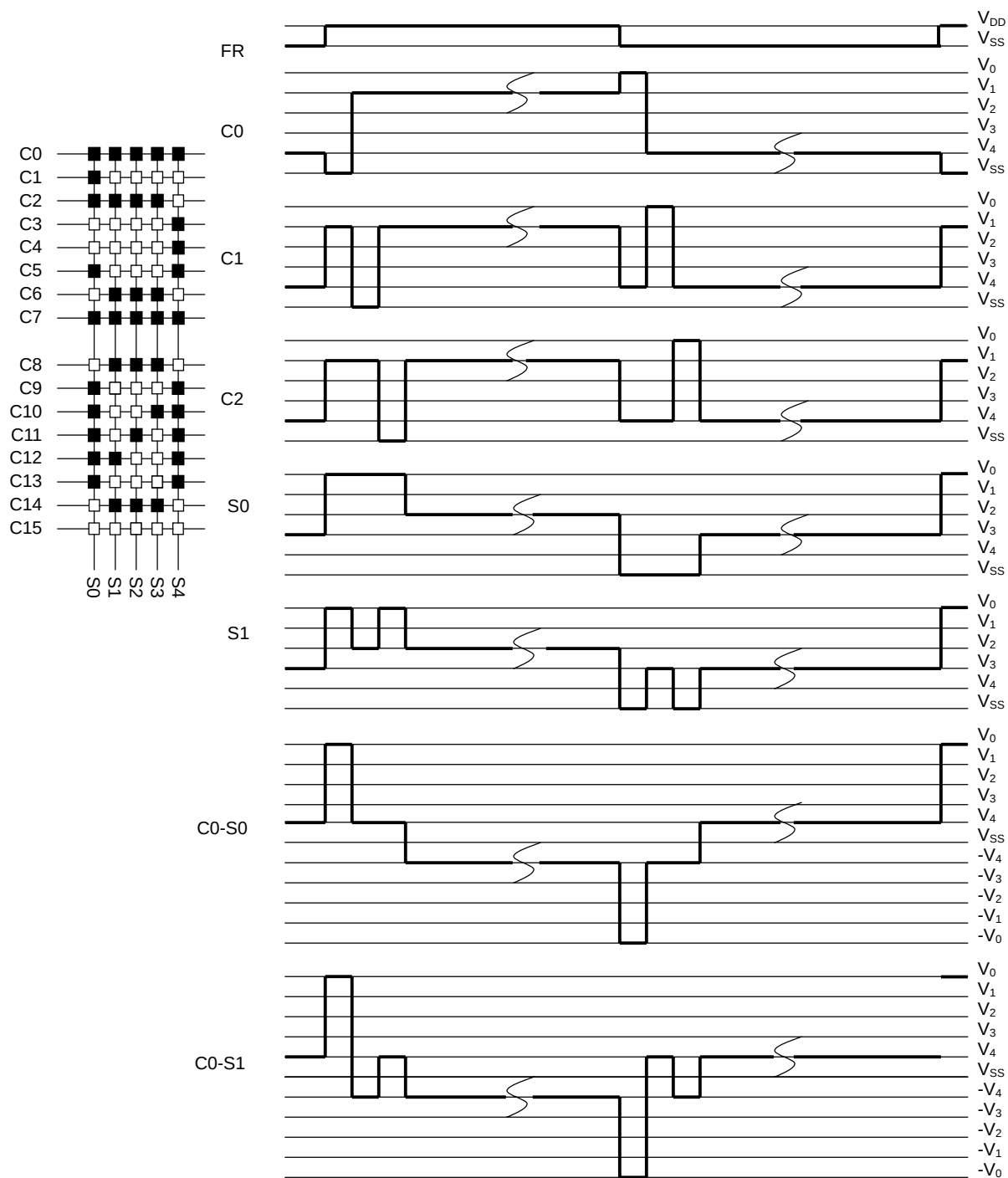
PARAMETER	SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Serial clock cycle	SCL	t_{scyc}	-	110	-	ns
SCL "H" pulse width		t_{SHW}	-	40	-	
SCL "L" pulse width		t_{SLW}	-	40	-	
Address set up time	RS	t_{SAS}	-	60	-	
Address hold time		t_{SAH}	-	60	-	
Data set up time	SI	t_{SDS}	-	50	-	
Data hold time		t_{SDH}	-	60	-	
CS-SCL time	$\overline{CS}$	t_{CSS}	-	60	-	
		t_{CSH}	-	55	-	
Rising, falling edge	-	t_r, t_f	-	-	15	

($V_{SS}=0V$, $V_{DD}=3.0V$, $T_a=-40$ to $+85^{\circ}C$)

PARAMETER	SIGNAL	SYMBOL	Measurement Condition	MIN.	MAX.	UNIT
Serial clock cycle	SCL	t_{scyc}	-	55	-	ns
SCL "H" pulse width		t_{SHW}	-	20	-	
SCL "L" pulse width		t_{SLW}	-	20	-	
Address set up time	RS	t_{SAS}	-	30	-	
Address hold time		t_{SAH}	-	30	-	
Data set up time	SI	t_{SDS}	-	25	-	
Data hold time		t_{SDH}	-	30	-	
CS-SCL time	$\overline{CS}$	t_{CSS}	-	30	-	
		t_{CSH}	-	27	-	
Rising, falling edge	-	t_r, t_f	-	-	15	

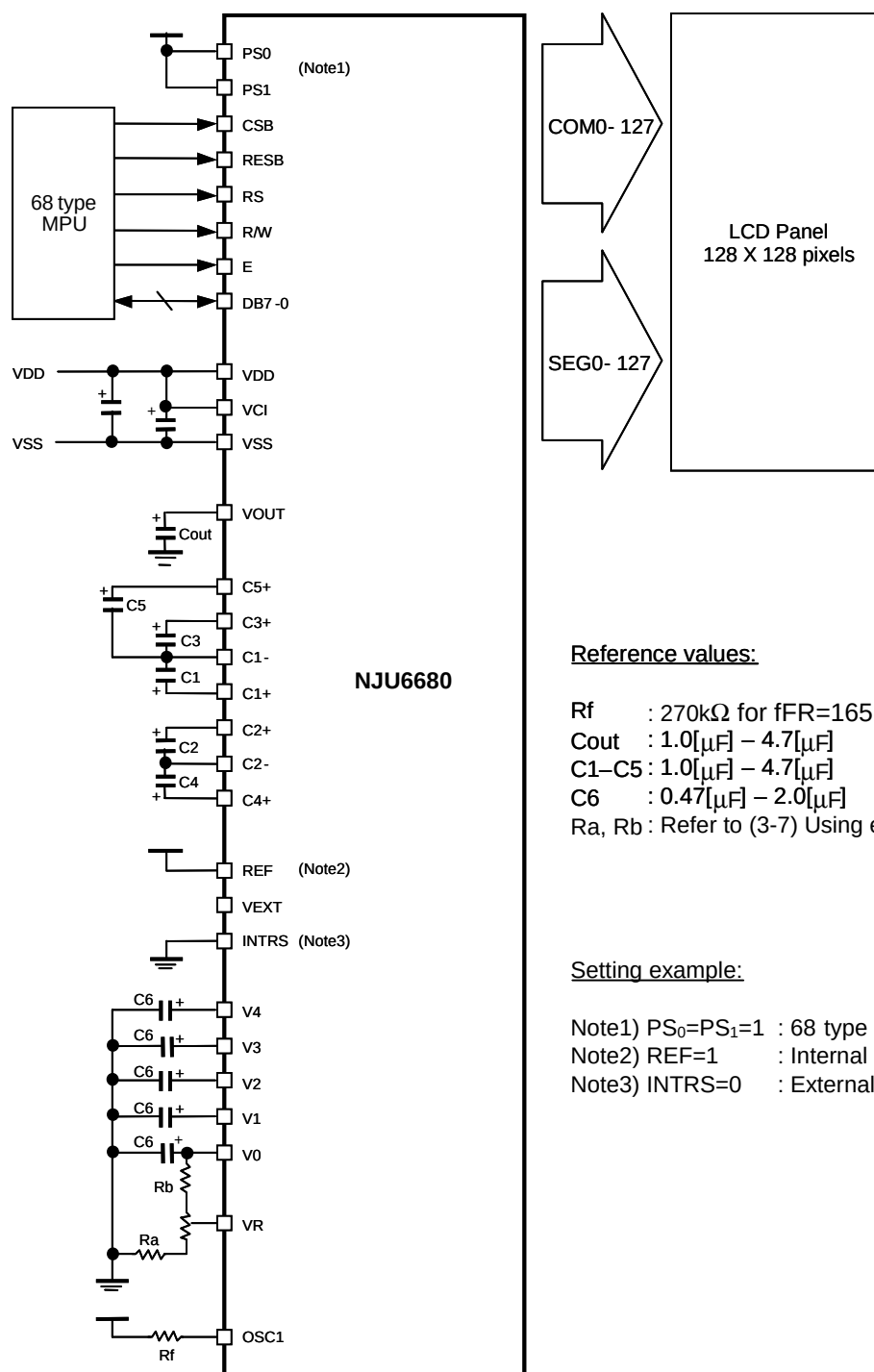
Note 15) SPI clock tolerance is $\pm 2ppm$.

■ LCD Driving Wave Form (Black & White Mode)



APPLICATION CIRCUIT

Example for the application circuits in using the internal power circuits (VC=VR=VF=1)



Reference values:

R_f : 270k Ω for $f_{FR}=165\text{Hz}$ (typ.)
 C_{out} : 1.0[μF] – 4.7[μF]
 $C1-C5$: 1.0[μF] – 4.7[μF]
 $C6$: 0.47[μF] – 2.0[μF]
 R_a, R_b : Refer to (3-7) Using external R_a and R_b resistors

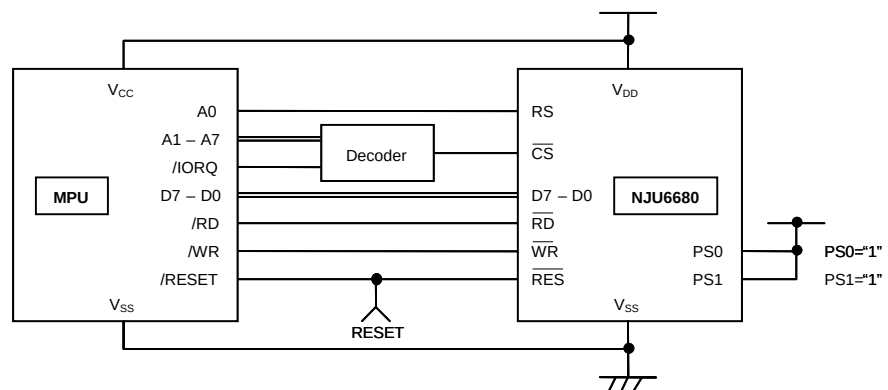
Setting example:

Note1) $PS_0=PS_1=1$: 68 type MPU interface
 Note2) $REF=1$: Internal reference voltage
 Note3) $INTRS=0$: External R_a and R_b resistors

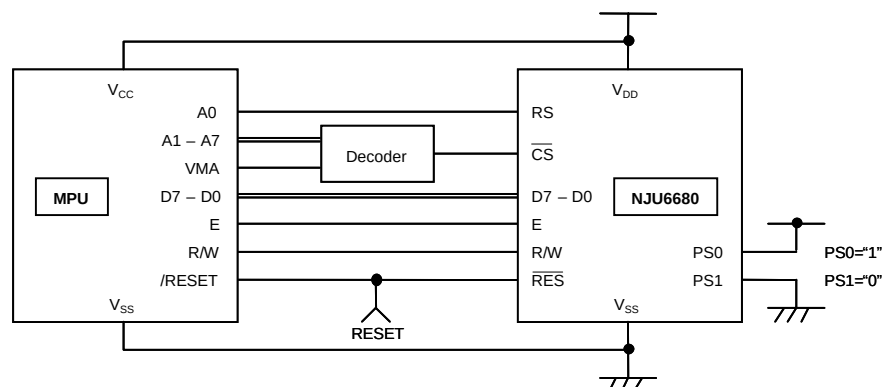
Fig.16

• MPU Interface Example

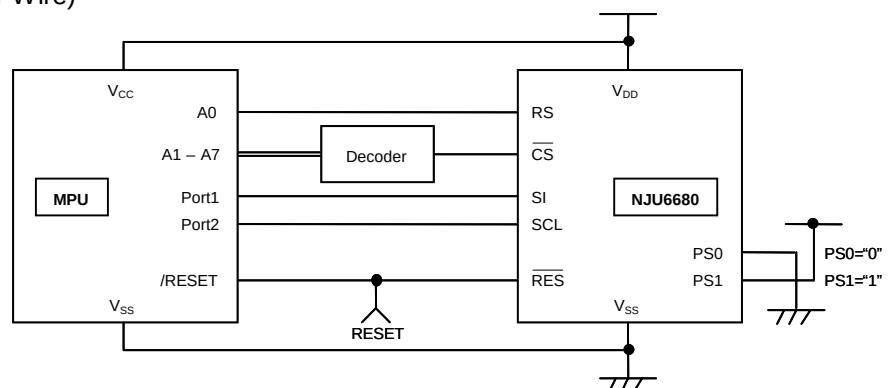
• 80 type MPU



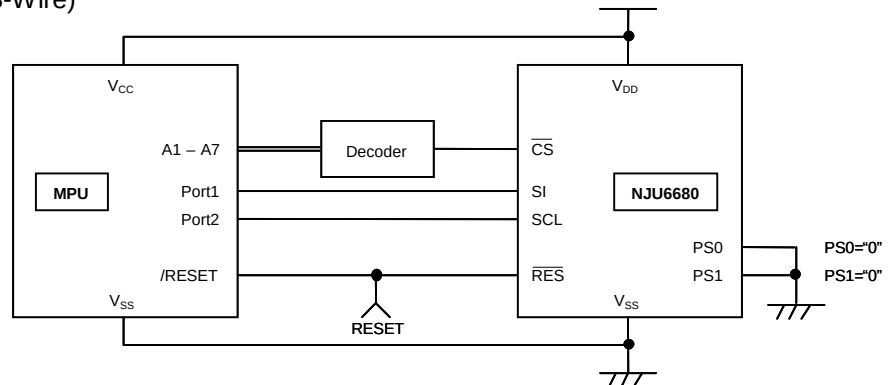
• 68 type MPU



• Serial Interface (4-Wire)

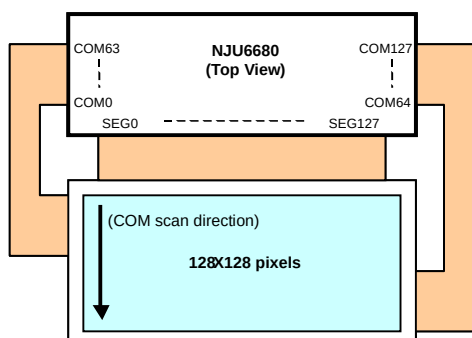


• Serial Interface (3-Wire)

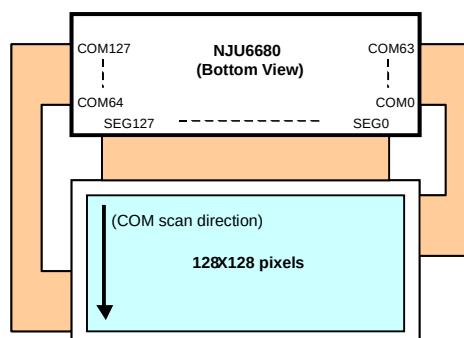


- Connections between the LSI and LCD panel

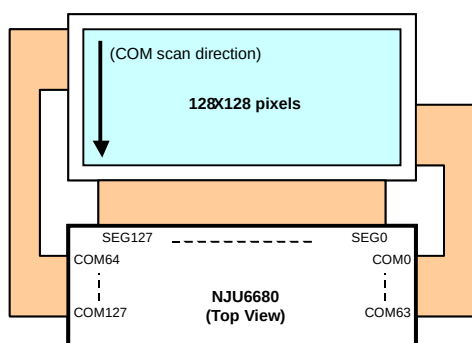
(1) ADC=0, COM scan direction=0



(2) ADC=1, COM scan direction=0



(3) ADC=1, COM scan direction=1



(4) ADC=0, COM scan direction=1

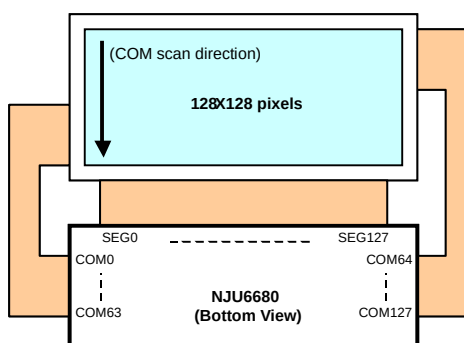


Fig. 17

MEMO

[CAUTION]

The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.