Si5381/82 Data Sheet

Multi-DSPLL Wireless Jitter Attenuating Clocks

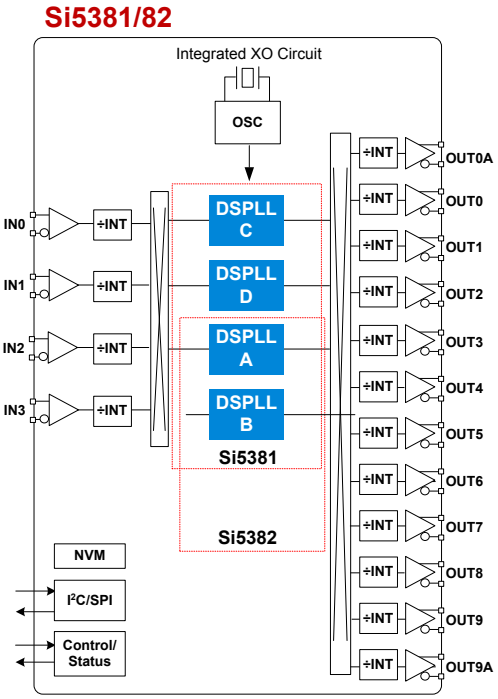
The Si5381/82 is a wireless multi-PLL, jitter-attenuating clock that leverages Silicon Labs' latest fourth-generation DSPLL technology to address the form factor, power, and performance requirements demanded by radio area network equipment, such as small cells, baseband units, and distributed antenna systems (DAS). The Si538x is the industry's first multi-PLL wireless clock generator family capable of replacing discrete, high-performance, VCXO-based clocks with a fully integrated CMOS IC solution. The Si5381/82 features a multi-PLL architecture that supports independent timing paths for JESD wireless clocks with less than 85 fs typical phase jitter as well as Ethernet and other low-jitter, general-purpose clocks. DSPLL technology also supports free-run and holdover operation as well as automatic and hitless input clock switching. This unparalleled integration reduces power and size without compromising the stringent performance and reliability demanded in wireless applications.

Applications

- Pico cells, small cells
- Mobile backhaul
- Multiservice Distributed Access Systems (MDAS)

KEY FEATURES

- Supports simultaneous wireless and general-purpose clocking in a single device
- Jitter performance: 85 fs RMS typ (12 kHz–20 MHz)
- Input frequency range:
  - Differential: 8 kHz – 750 MHz
  - LVCMOS: 8 kHz – 250 MHz
- Output frequency range:
  - JESD204B: 480 kHz - 2.94912 GHz
  - Differential: 1 Hz – 712.5 MHz
  - LVCMOS: 480 kHz – 250 MHz

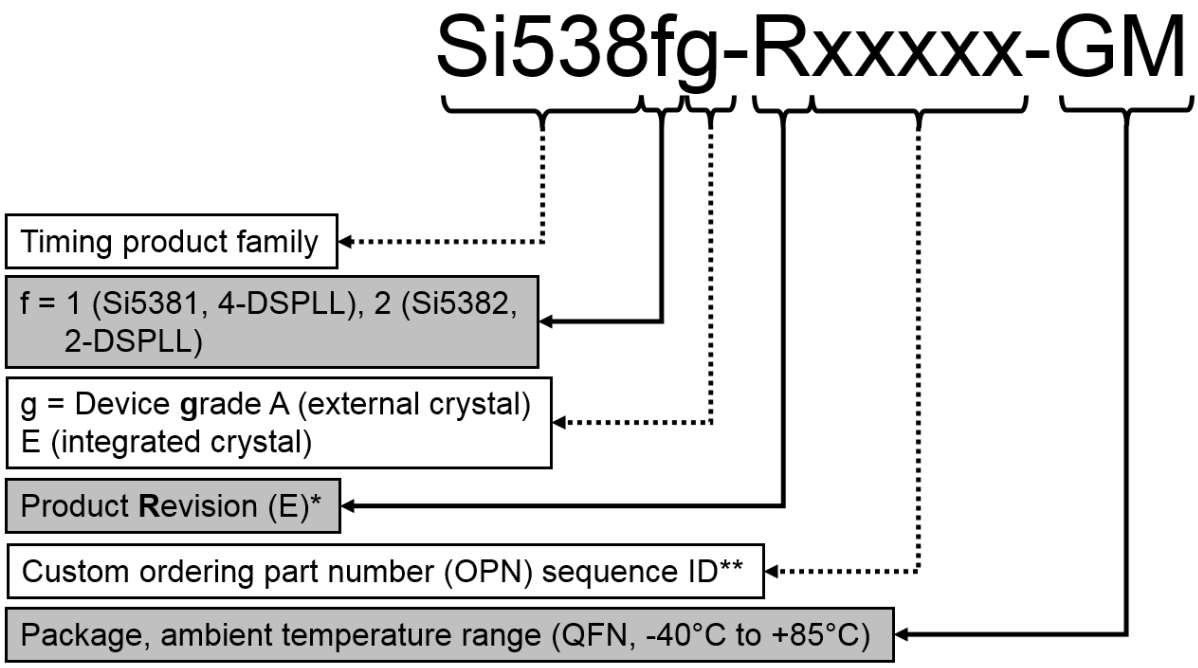


1. Feature List

The Si5381/82 highlighted features are listed below.

- Digital frequency synthesis eliminates external VCXO and analog loop filter components
- DSPLL_B supports high-frequency, wireless clocking. Remaining three DSPLLs support general-purposing clocking
- Integrated crystal option (Grade E)
- Input frequency range:
  - Differential: 7.68 MHz–750 MHz
  - LVCMOS: 10 MHz–250 MHz
- Output frequency range (DSPLL_B):
  - Differential: up to 2.94912 GHz
  - LVCMOS: up to 250 MHz
- Output frequency range (DSPLL_A/C/D):
  - Differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
- Excellent jitter performance:
  - DSPLL_B: 85 fs typ (12 kHz - 20 MHz)
  - DSPLL_A/C/D: 150 fs typ (12 kHz - 20 MHz)
- Phase noise floor: –165 dBc/Hz
- Spur performance: –95 dBc max (relative to a 122.88 MHz carrier)
- Flexible crosspoints route any input to any output clock
- Configurable outputs:
  - Compatible with LVDS, LVPECL, LVCMOS, CML, HCSL
  - Programmable signal amplitude
- Adjustable output-output delay: 68 ps/step, ±128 steps
- Independent output supply pins: 3.3, 2.5, or 1.8 V
- Core voltage:
  - VDD = 1.8 V ±5%
  - VDDA = 3.3 V ±5%
- Automatic free-run, lock, and holdover modes
- Digitally selectable loop bandwidth: DSPLL_B: 1 Hz to 4 kHz
- Hitless switching between input clocks
- Status monitoring (LOS, OOF, LOL)
- Serial interface: I^2C or SPI in-circuit programmable with non-volatile OTP memory
- ClockBuilder™ Pro software tool simplifies device configuration
- 4 input, 12 output, 64QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Guide



*See Ordering Guide table for current product revision.
** (Optional) 5 digits; assigned by ClockBuilder Pro for Custom, factory-preprogrammed OPN devices only; (The "xxxxx" field is not included for "Base" OPNs).

Table 2.1. Ordering Guide

Ordering Part Number	Reference	# DSPLL	Number of Clock Inputs/ Outputs	Maximum Output Frequency		Package	RoHS-6, Pb-Free	Temperature Range
				4G/LTE JESD204B Clocks	General Purpose Clocks			
Si5381A-E-GM	External	4	4 / 12	2.94912 GHz	735 MHz	64-Lead 9x9 mm QFN	Yes	–40 to +85 °C
Si5382A-E-GM	External	2	4 / 12	2.94912 GHz	735 MHz			
Si5381E-E-GM	Internal Crystal	4	4 / 12	2.94912 GHz	735 MHz	64-Lead 9x9 mm LGA		
Si5382E-E-GM	Internal Crystal	2	4 / 12	2.94912 GHz	735 MHz			
Si5381E-E-EVB	Evaluation Board							
Si5382E-E-EVB	Evaluation Board							

Note:

1. Add an "R" at the end of the device to denote tape and reel options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by ClockBuilder Pro. Part number format is: Si5381E-Exxxxx-GM, where "xxxxx" is a unique numerical sequence representing the pre-programmed configuration.

Table of Contents

3. Functional Description

The Si5381/82 integrates four/two independent any-frequency DSPLLs in a monolithic IC for applications that require a combination of 4G/LTE and general-purpose clocking. Any clock input can be routed to any DSPLL. The output of any DSPLL can be routed to any of the device clock outputs. Based on 4th generation DSPLL technology, the Si5381/82 provides a clock-tree-on-a-chip solution for applications that need a mix of 4G/LTE and general-purpose frequencies.

3.1 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. DSPLL_B generates 4G/LTE frequencies. For DSPLL_A/C/D, fractional frequency multiplication (Mn/Md) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.The Si5382 supports one general-purpose DSPLL (DSPLL_A).

3.1.1 Si5381/82 4G/LTE Frequency Configuration

The device's frequency configuration is fully programmable through the serial interface and can also be stored in non-volatile memory. The combination of flexible integer dividers and a high frequency VCO allows the device to generate multiple output clock frequencies for applications that require ultra-low phase noise and spurious performance. The table below shows a list of possible output frequencies for LTE applications. Note that these 4G/LTE frequencies may be generated with an Ethernet input clock to DSPLL_B. These frequencies are distributed to the output dividers using a configurable crosspoint mux. The R dividers allow further division for up to 10 unique integer-ratio related frequencies on the Si5381/82. The ClockBuilder Pro software utility provides a simple means of automatically calculating the optimum divider values (P, M, N and R) for the frequencies listed in the table below.

Table 3.1. Example of Possible 4G/LTE Clock Frequencies

4G/LTE Device Clock Frequencies Fout (MHz)
15.36
19.20
30.72
38.40
61.44
76.80
122.88
153.60
184.32
245.76
307.20
368.64
491.52
614.40
737.28
983.04
1228.80
1474.56
2949.12

3.1.2 Si5381/82 Configuration for Wireless Clock Generation

The Si5381/82 can be used as a high performance, fully integrated wireless jitter cleaner while eliminating the need for discrete VCXO and loop filter components. The Si5381/82 supports JESD204B subclass 0 and subclass 1 clocking by providing both device clocks (DCLK) and system reference clocks (SYSREF). The clock outputs can be independently configured as device clocks or SYSREF clocks to drive JESD204B converters, FPGAs, or other logic devices. An example frequency configuration is shown in the figure below. In this case, the N dividers determine the device clock frequency and the R dividers provide the divided SYSREF clock which is used as the lower frequency frame clock. The SYSREF clock is always periodic and can be controlled (on/off) without glitches by enabling or disabling its output through register writes.

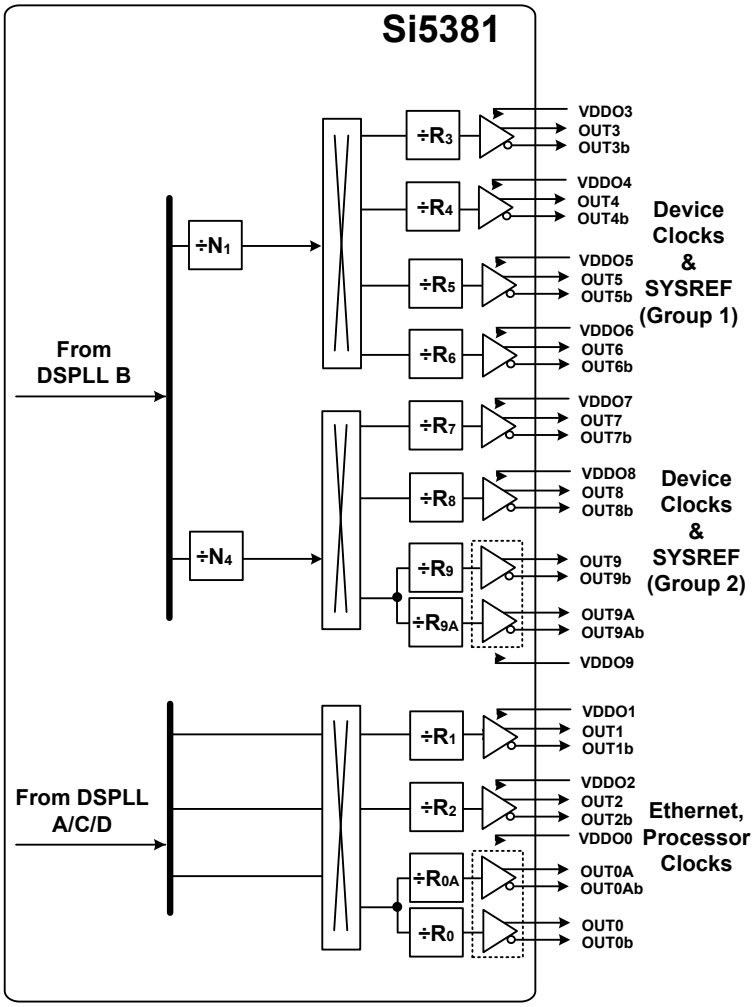


Figure 3.1. Example Divider Configuration for Generating JESD204B Subclass 1 Clocks

3.1.3 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and support a digitally selectable loop bandwidth ranging from 1 Hz to 4000 Hz. DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the DSPLL loop bandwidth selection.

3.1.4 Fastlock

Selecting a low DSPLL loop bandwidth (e.g., 1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 1 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting as described in section 3.1.3 DSPLL Loop Bandwidth. The fastlock feature can be enabled or disabled independently for each of the DSPLLs.

3.1.5 Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

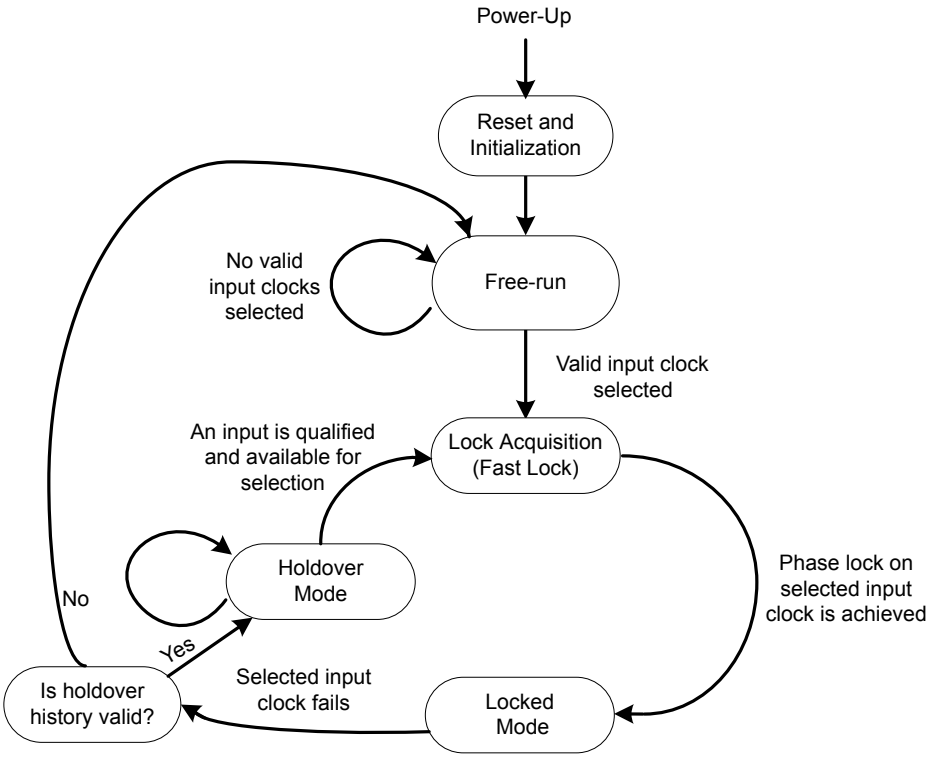


Figure 3.2. Modes of Operation

3.1.6 Initialization and Reset

When power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RST pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can either affect all or each DSPLL individually.

3.1.7 Free-run Mode

Once power is applied to the Si5381/82 and initialization is complete, all DSPLLs will automatically enter Free-run Mode. The frequency accuracy of the reference clock (internal crystal or external reference on XA/XB pins). Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that require better frequency accuracy and stability while in Free-run Mode or Holdover Mode.

3.1.8 Lock Acquisition

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process. If the fastlock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition, the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

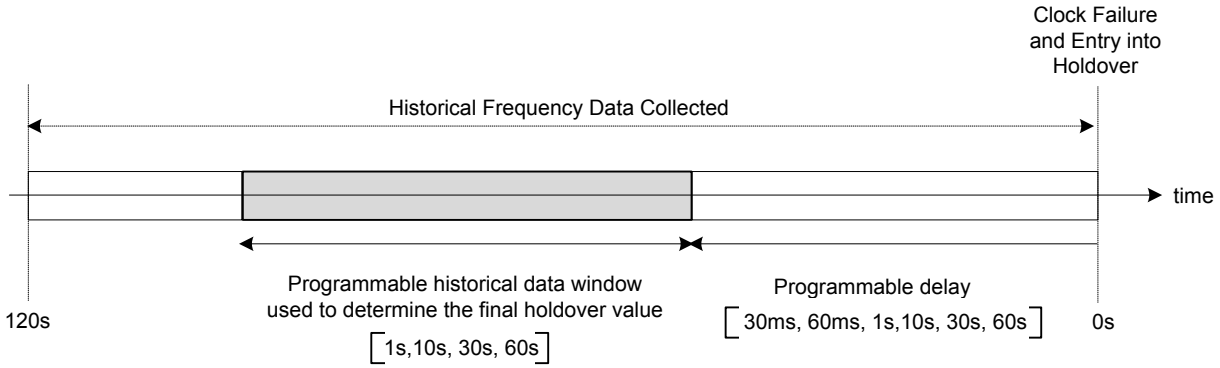
3.1.9 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own status bit to indicate when lock is achieved. See 3.4.6 LOL Detection for more details on the operation of the loss of lock circuit.

3.1.10 Holdover Mode

Any of the DSPLLs will automatically enter Holdover Mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

Figure 3.3. Programmable Holdover Window



When entering Holdover Mode, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover Mode, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, a DSPLL will automatically exit the Holdover Mode and reacquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless, and its rate is controlled by the DSPLL bandwidth or the fastlock bandwidth. These options are register programmable.

3.2 External Reference (XA/XB) (Grade A Only)

An external crystal (XTAL) can be used on Grade A parts in combination with the internal oscillator (OSC) to produce an ultra-low phase noise reference clock for the DSPLLs and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in the figure below. The Si5381/82 includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to the Si5381/82 Datasheet for crystal specifications. A crystal frequency of 54 MHz is required, with a total accuracy of ±100 ppm* recommended for best performance. The Si5381/82 includes built-in XTAL load capacitors (C_L) of 8 pF, which are switched out of the circuit when using an external XO. The Si5381/82 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. The Si5381/82 can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. It is important to note that when using the REFCLK option the close-in phase noise of the outputs is directly affected by the phase noise of the external XO reference. Refer to the Si5381/82 Datasheet for REFCLK signal requirements when using this mode.

Note: Including initial frequency tolerance and frequency variation over the full operating temperature range, voltage range, load conditions, and aging.

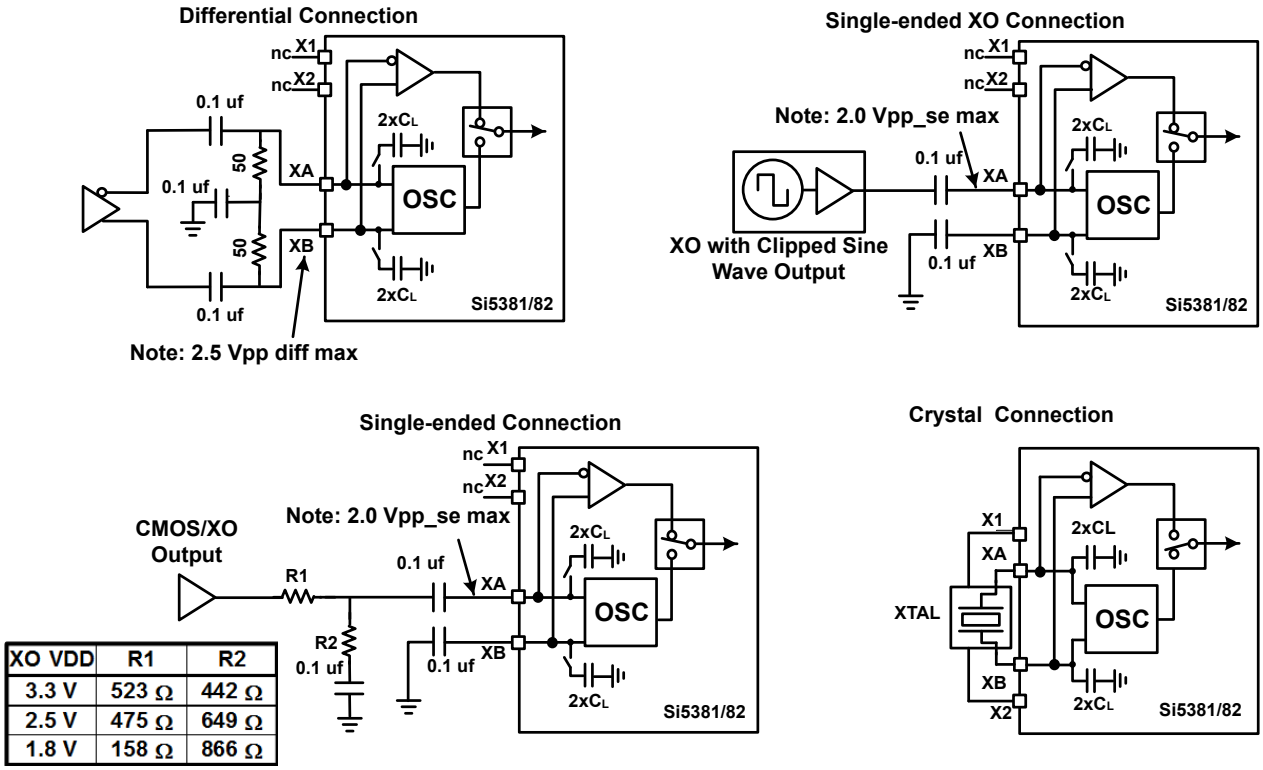


Figure 3.4. XAXB Crystal Resonator and External Reference Clock Connection Options

3.3 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in the figure below.

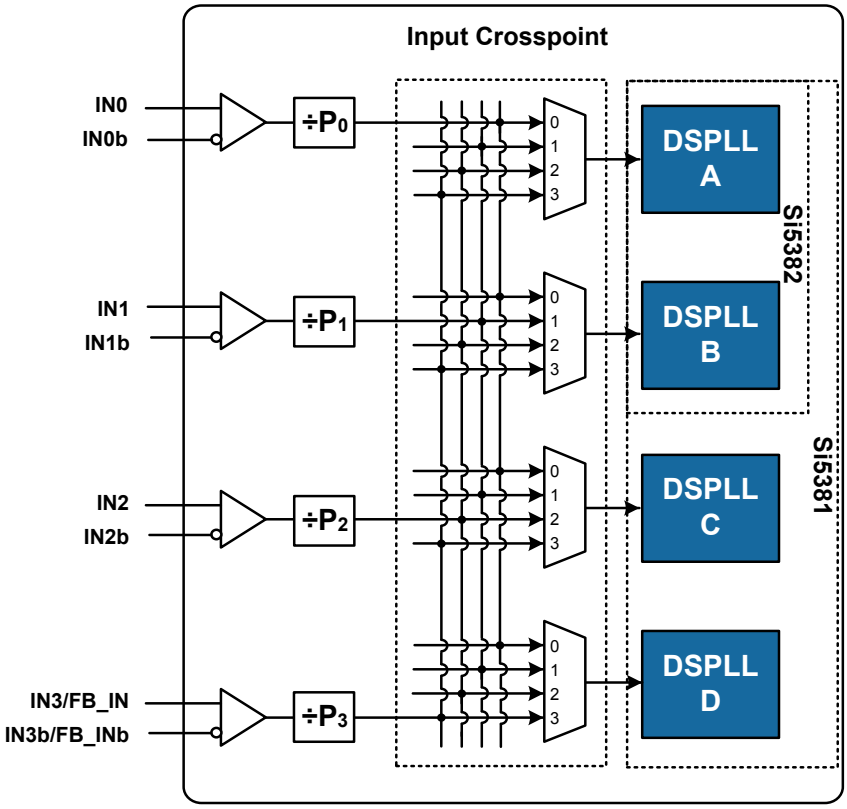


Figure 3.5. DSPLL Input Selection Crosspoint

3.3.1 Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in the figure below. Standard 50% duty cycle signals must be ac-coupled, while low duty cycle pulsed CMOS signals can be dc-coupled. Unused inputs can be disabled and left unconnected when not in use.

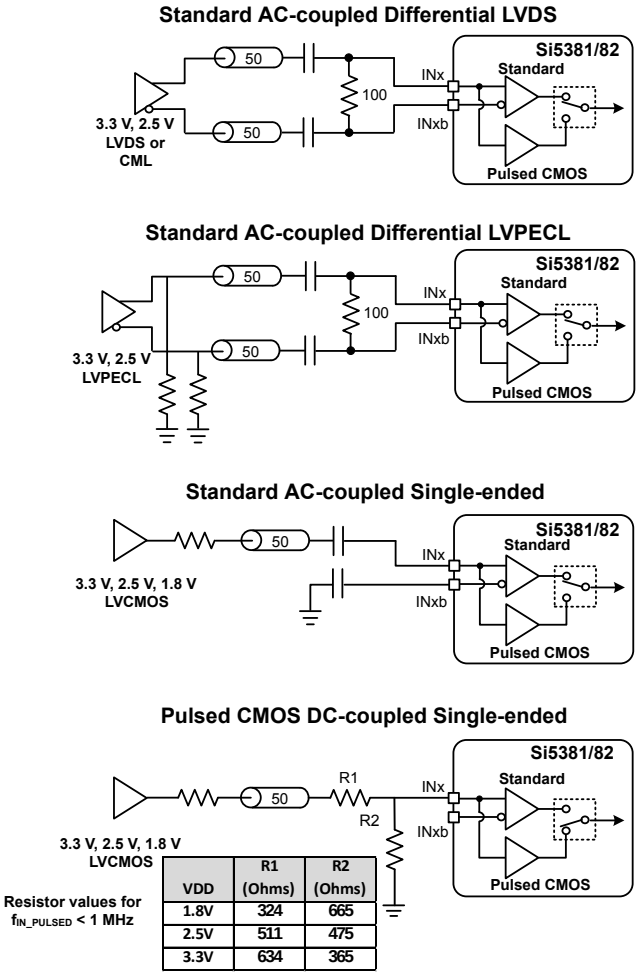


Figure 3.6. Termination of Differential and LVCMOS Input Signals

3.3.2 Manual Input Selection (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins for DSPLL_B or through a register for all DSPLLs. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode.

Table 3.2. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input to DSPLL_B
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

3.3.3 Automatic Input Switching (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on reference qualification, input priority, and the revertive option. Only references which are valid can be selected by the automatic state machine. If there are no valid references available, the DSPLL will enter the Holdover Mode. With revertive switching enabled, the highest priority input with a valid reference is always selected. If an input with a higher priority becomes valid, then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid, an automatic switchover to a valid input with the highest priority will be initiated.

3.3.4 Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two frequency locked clock inputs that have a fixed phase difference between them. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or have an integer frequency relationship to each other. When this feature is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled (normal switching), the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL loop bandwidth.

3.3.5 Glitchless Input Switching

Each DSPLL has the ability of switching between two input clocks that are up to ±20 ppm apart in frequency. The DSPLL will pull-in to the new frequency using the DSPLL loop bandwidth or using the Fastlock loop bandwidth if it is enabled. The loss of lock (LOL) indicator will be asserted while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output. Glitchless input switching is available regardless of whether the hitless switching feature is enabled or disabled.

3.3.6 Zero Delay Mode (ZDM)

Zero delay mode is configured for DSPLL B by opening the internal feedback loop through software configuration and closing the loop externally around as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any output generated by DSPLL B can be fed back to the IN3/FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9A and IN3/FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. The order of the OUT9A and FB_IN polarities is such that they may be routed on the device side of the PCB without requiring vias or needing to cross each other. Zero delay mode is not available on Si5381/82 A, C, or D DSPLLs.

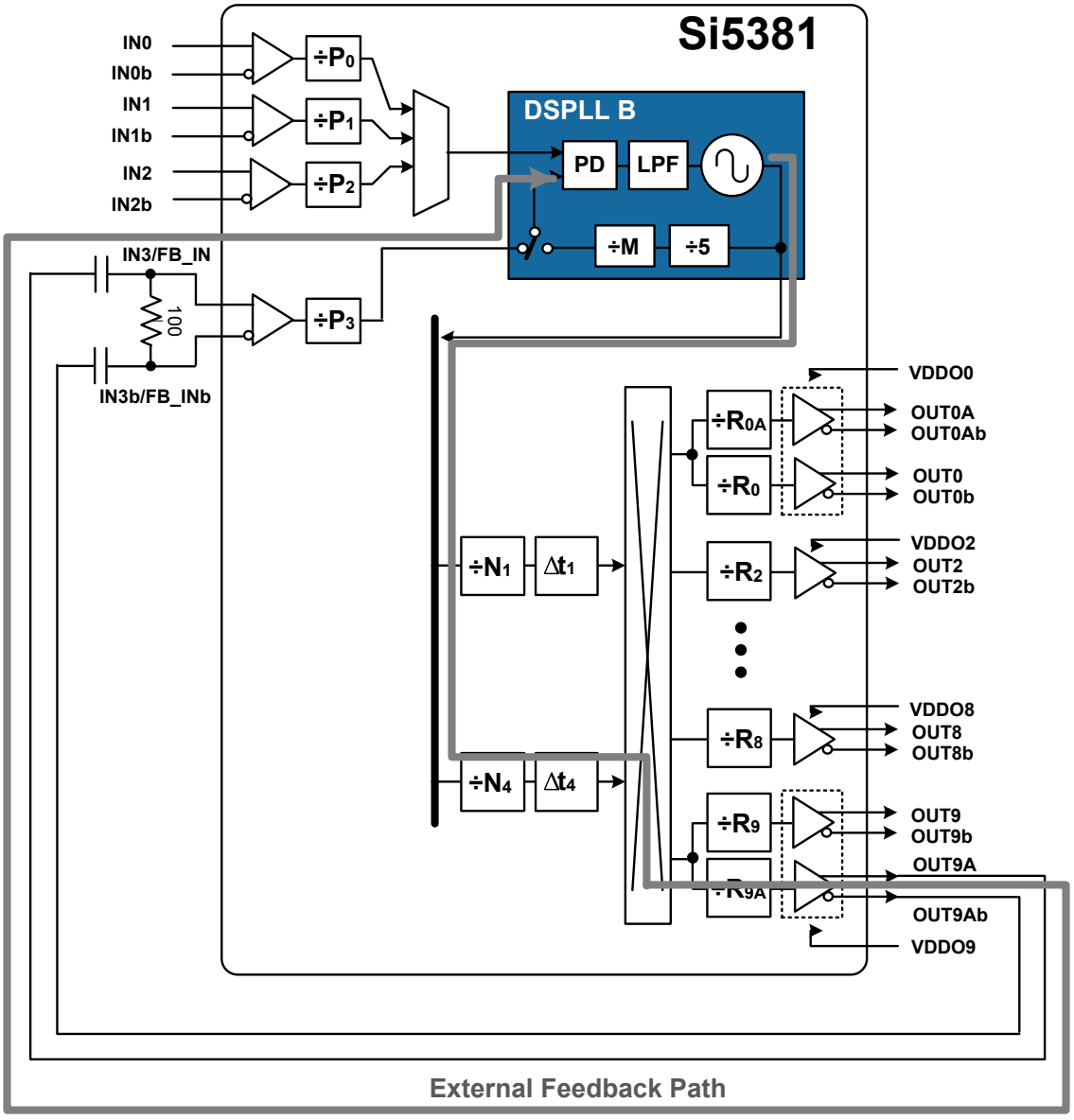


Figure 3.7. Zero Delay Mode (ZDM) Setup

3.4 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical clock for the DSPLLs (external XA/XB pins on grade A only). Each DSPLL also has a Loss Of Lock (LOL) indicator, which is asserted when the DSPLL has lost synchronization with the selected input clock.

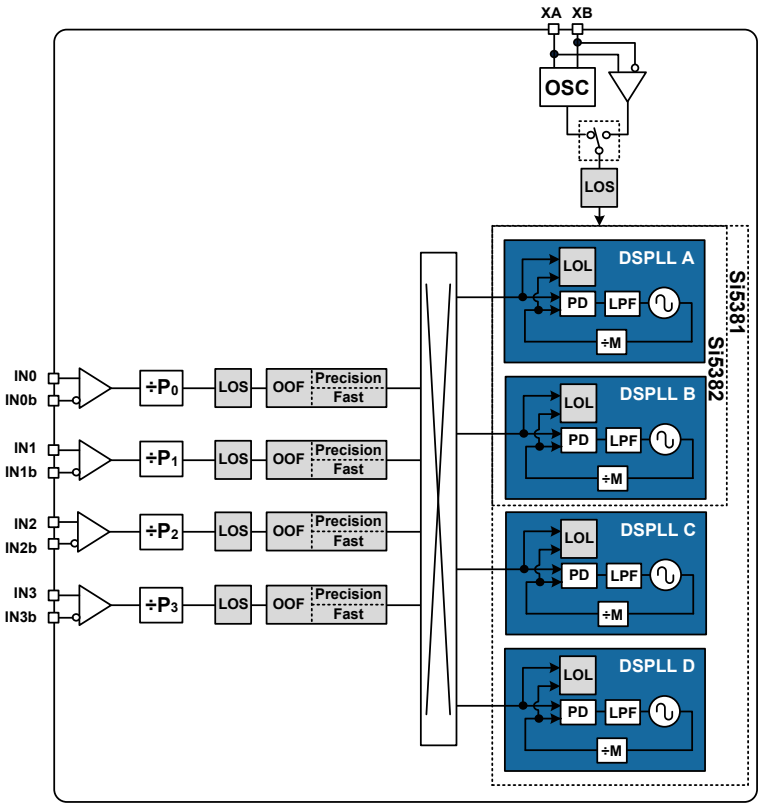


Figure 3.8. Si5381/82 Fault Monitors (Grade A Shown)

3.4.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits have their own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

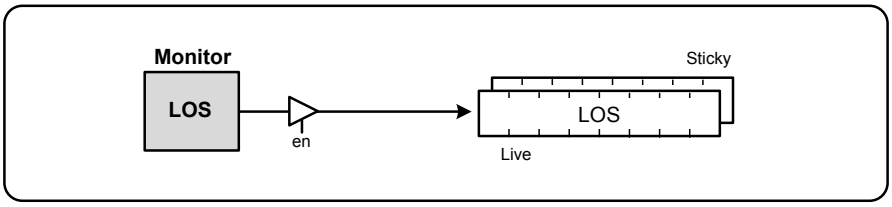


Figure 3.9. LOS Status Indicators

3.4.2 Reference LOS Detection

An LOS monitor is available to ensure that the reference clock (REFCLK) XA/XB external reference (grade A) or internal crystal (grade E) is valid. By default, the output clocks are disabled when reference LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when reference LOS is detected. See the 3.5.11 Output Disable During Reference LOS (XAXB, Internal Crystal) section for details.

3.4.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either: XA/XB/internal crystal, IN0, IN1, IN2 or IN3. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

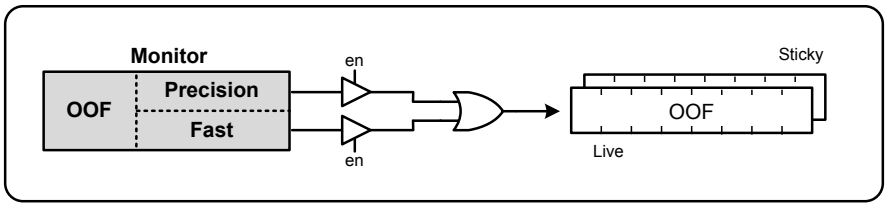


Figure 3.10. OOF Status Indicator

3.4.4 Precision OOF Monitor

The Precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the reference clock (XA/XB on Grade A and internal crystal on Grade E). The OOF monitor considers the frequency at the reference pins as its 0 ppm OOF reference. A valid input frequency is one that remains within the OOF frequency range which is register configurable from ±2 ppm to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

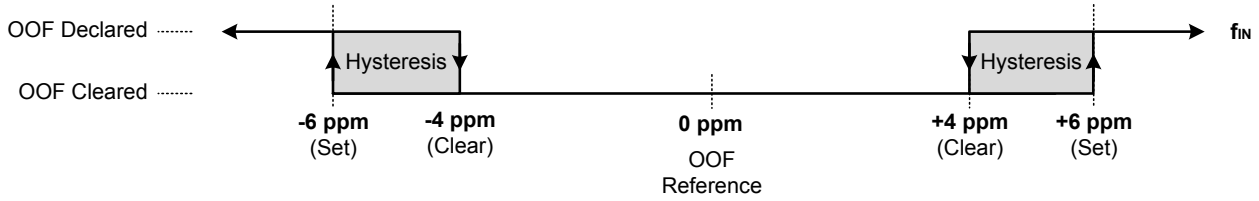


Figure 3.11. Example of Precise OOF Monitor Assertion and De-assertion Triggers

3.4.5 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by 1,000 to 16,000 ppm.

3.4.6 LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts an LOL register bit when a DSPLL has lost synchronization with its selected input clock. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared.

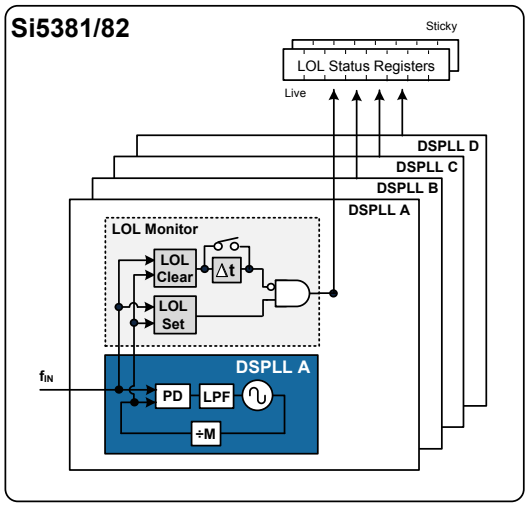


Figure 3.12. LOL Status Indicators

Each of the frequency monitors have adjustable sensitivity which is register configurable from 0.1 ppm to 10000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 2 ppm frequency difference is shown in the figure below.

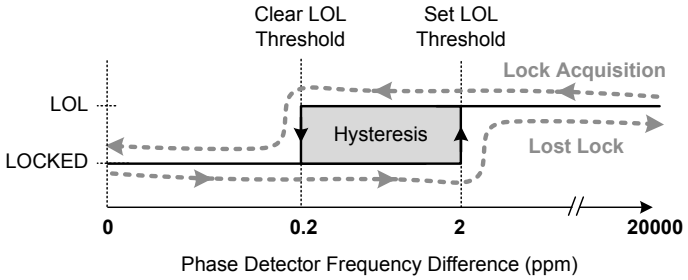


Figure 3.13. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely phase lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.4.7 Interrupt Pin INTRb

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

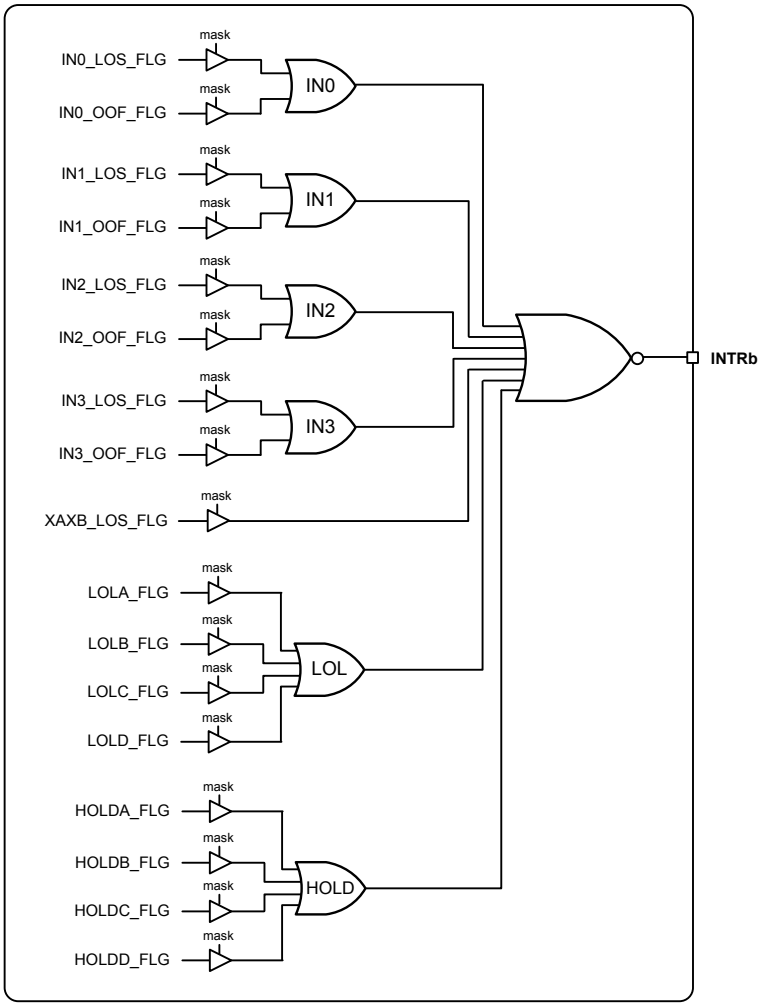


Figure 3.14. Interrupt Triggers and Masks

3.5 Outputs

The Si5381/82 supports up to twelve differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.5.1 Output Crosspoint

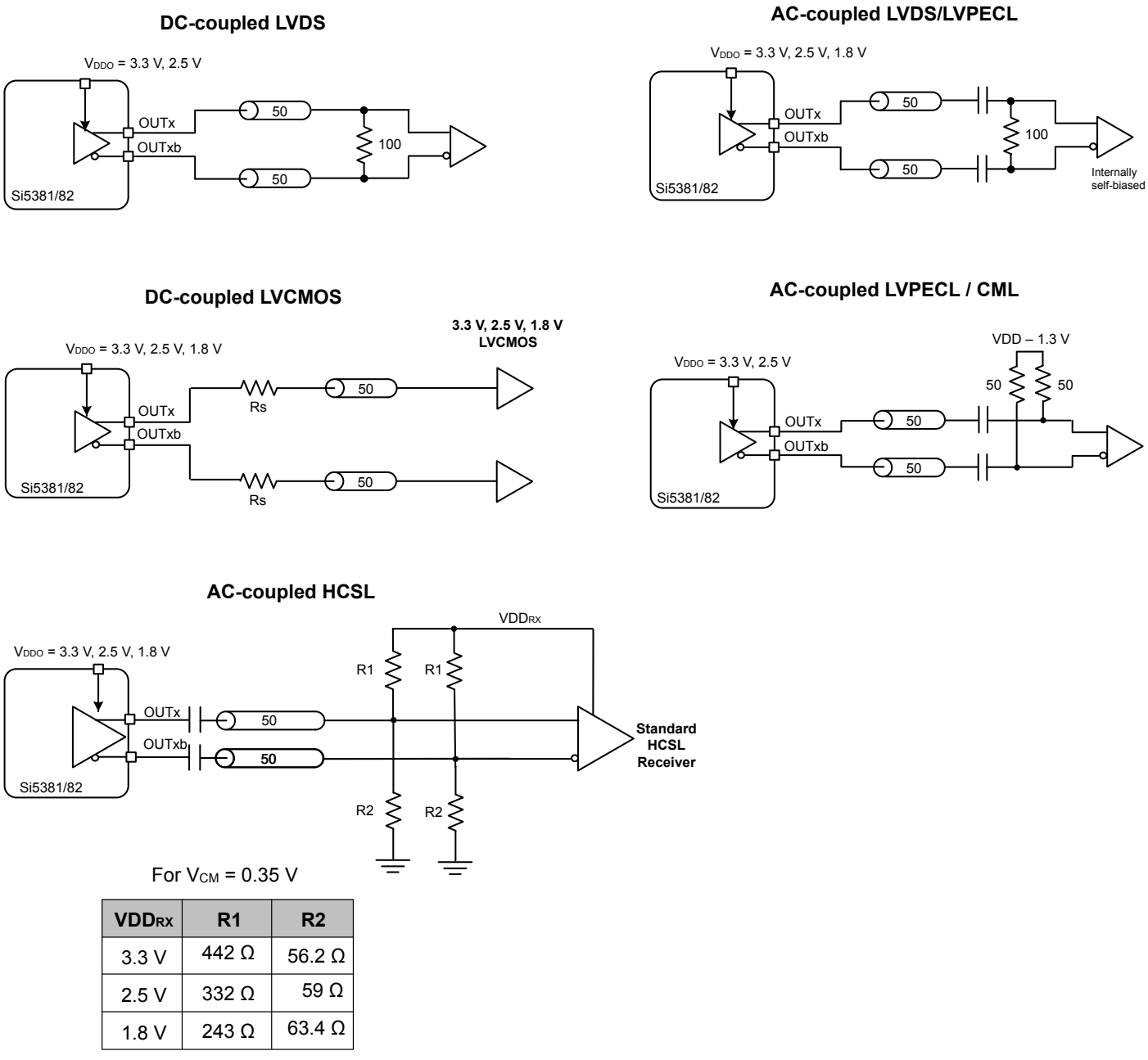
A crosspoint allows any of the output drivers to connect with any of the DSPLLs. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.

3.5.2 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable covering a wide variety of signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.5.3 Output Terminations

The output drivers support both ac-coupled and dc-coupled terminations as shown in the following figure.



For V_{CM} = 0.35 V

VDDRX	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 3.15. Supported Output Terminations

3.5.4 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential normal and low power modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

3.5.5 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled with source-side series termination as shown in the figure below.

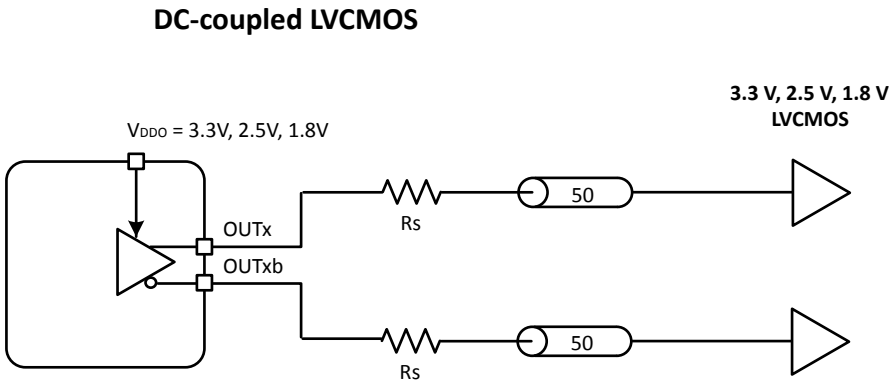


Figure 3.16. LVCMOS Output Terminations

3.5.6 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below.

Table 3.3. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA
Note: Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.			

3.5.7 LVCMOS Output Signal Swing

The signal swing (VOL/VOH) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. OUT0 and OUT0A share the same VDDO pin. OUT9 and OUT9A also share the VDDO pin. All other outputs have their own individual VDDO pins. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage. By default, both output pins carry the output clock signal, generating two CMOS output signals for each output driver. It is possible to configure the device to have only one of the output pins active to reduce power consumption.

3.5.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

3.5.9 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling all of the output drivers at the same time. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will all be enabled. Outputs in the enabled state can still be individually disabled through register control.

3.5.10 Output Disable During LOL

By default, a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.5.11 Output Disable During Reference LOS (XAXB, Internal Crystal)

The internal oscillator circuit (OSC) in combination with the external XA/XB reference (Grade A) internal crystal (Grade E) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure, the device will assert an XAXB_LOS alarm. By default, all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition. The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs.

3.5.12 Output Driver State When Disabled

The disabled state of an output driver is configurable as either disable low or disable high.

3.5.13 Synchronous Enable/Disable Feature

The output drivers provide a selectable synchronous enable/disable feature. Output drivers with this feature active will wait until a clock period has completed before the driver is disabled or enabled. This prevents unwanted runt pulses from occurring when enabling or disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.5.14 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the reset bit will have the same result. Asserting the sync register bit provides another method of realigning the R dividers without resetting the device.

3.6 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the ClockBuilder Pro configuration utility for details.

3.6.1 Power Down Pin (PDNb)

A power down pin is provided to force the device in a low power mode. The device's configuration will be maintained but no output clocks will be generated. Most of the internal blocks will be shut down but device communication via the serial interface will still be available. When the PDNb pin is pulled low the outputs will shut down without glitching (the clock's complete period will be generated before shutting down). When PDNb is released the device will start generating clocks without glitches. The device will generate free-running clocks until each DSPLL has acquired lock to the selected input clock source.

3.7 In-Circuit Programming

The Si5381/82 is fully configurable using the serial interface (I2C or SPI). At power-up, the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins. The NVM is writable two times. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5381/82 Family Reference Manual for a detailed procedure for writing registers to NVM.

3.8 Serial Interface

Configuration and operation of the Si5381/82 is controlled by reading and writing registers using the I2C or SPI interface. The I2C_SEL pin selects I2C or SPI operation. The Si5381/82 supports communication with a 3.3 V or 1.8 V host by setting the IO_VDD_SEL configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit.

3.9 Custom Factory Preprogrammed Devices

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed device will generate clocks at power-up. Custom, factory-pre-programmed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you typically within two weeks.

3.10 How to Enable Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at www.silabs.com and opting in for updates to software, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is NOT yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. Examples of this type of feature or custom setting are the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and custom requirements, a Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled, using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown below:

Table 3.4. Setting Overrides

Location	Customer Name	Engineering Name	Type	Target	Dec Value	Hex Value
0x0435[0]	FORCE_HOLD_PLLA	OLA_HO_FORCE	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	OOF_DIV_CLK_DIS	User	OPN and EVB	0	0x00

Once you receive the updated design file, simply open it in CBPro. After you create a custom OPN, the device will begin operation after startup with the values in the NVM file, including the Silicon Labs-supplied override settings.

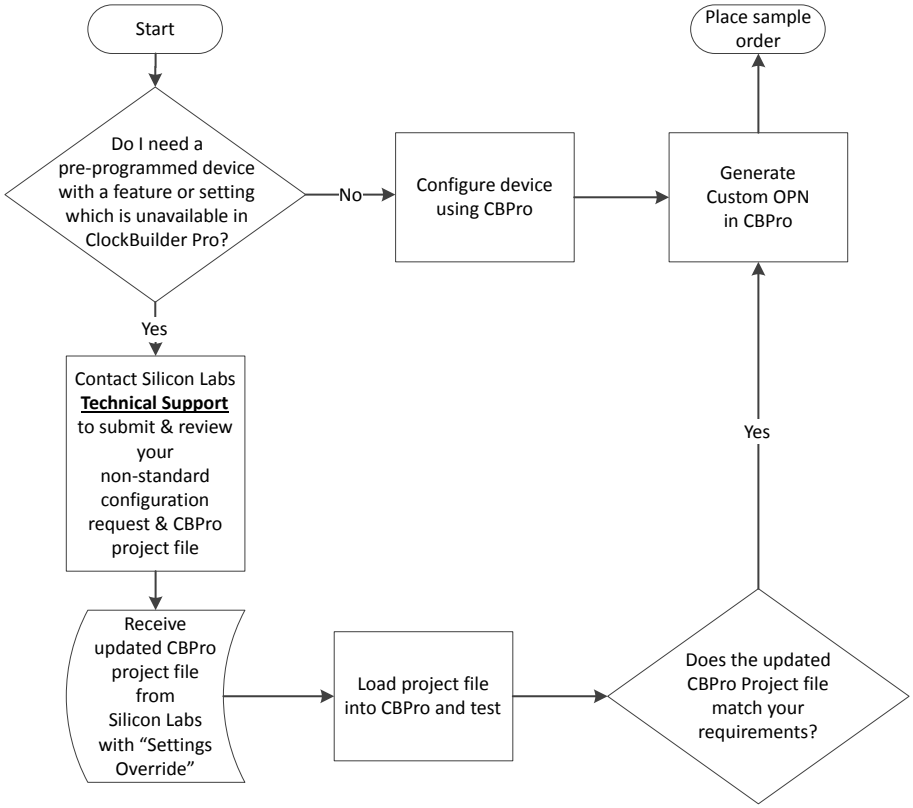


Figure 3.17. Flowchart to Order Custom Parts with Features not Available in CBPro

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessed registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration and general device settings. Refer to the Si5381/82 Family Reference Manual for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Maximum Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

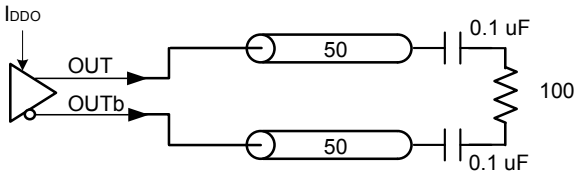
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Si5381	—	175	—	mA
	I_{DDA}	Notes 1, 2	—	120	—	mA
Output Buffer Supply Current	I_{DDO}	LVPECL Output[3] @ 156.25 MHz	—	21	25	mA
		LVDS Output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] Output @ 156.25 MHz	—	21	25	mA
		2.5 V LVCMOS[4] Output @ 156.25 MHz	—	16	18	mA
		1.8 V LVCMOS[4] Output @ 156.25 MHz	—	12	13	mA
Total Power Dissipation	P_d	Note 1,5	—	1125	—	mW

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Si5381 test configuration: 8 clock outputs enabled (2 x 983.04 MHz, 2 x 491.52 MHz, 1 x 245.76 MHz, 3 x 122.88 MHz; 2.5 LVDS). Excludes power in termination resistors.
2. VDDO0 supplies power to both OUT0 and OUT0A buffers. Similarly, VDDO9 supplies power to both OUT9 and OUT9A buffers.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 6-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

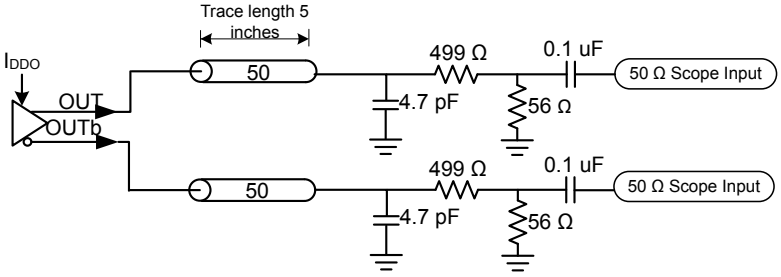


Table 5.3. Input Clock Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended/LVCMOS — AC-coupled (IN0, IN1, IN2, IN3)						
Input Frequency Range	f_{IN_DIFF}	Differential	0.008	—	750	MHz
	f_{IN_SE}	Single-ended/ LVCMOS	0.008	—	250	
Input Voltage Amplitude	V_{IN_DIFF}	f_{IN_DIFF} < 250 MHz	100	—	1800	mVpp_se
		250 MHz < f_{IN_DIFF}< 750 MHz	225	—	1800	mVpp_se
Single-Ended Input Swing	V_{IN_SE}	f_{IN_SE}< 250 MHz	100	—	3600	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
Pulsed CMOS — DC-coupled (IN0, IN1, IN2, IN3)[3]						
Input Frequency	f_{IN_CMOS}		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Clock Input	40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB) (Grade A Only)						
REFCLK	f_{IN_REF}	4G/LTE	—	54	—	MHz
Total Frequency Tolerance	f_{RANGE}		-100	—	+100	ppm
Input Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
	V_{IN_DIFF}		365	—	2500	mVpp_diff
Slew Rate[1, 2]	SR	Imposed for phase noise performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%
Integrated Crystal REFCLK (Grade E)						
Crystal Frequency	f_{IN_XTAL}		—	48.0231	—	MHz
Frequency Stability	f_{STABLE}	10 years of aging at 70 °C	—	TBD	—	ppm
Frequency Perturbation	f_{PERT}		—	—	TBD	ppm

Note:

1. Imposed for phase noise performance.
2. Rise and fall times can be estimated using the following simplified equation: tr/tf80-20 = ((0.8 - 0.2) * VIN_Vpp_se) / SR.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks <1 MHz, which must be dc-coupled, having a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (VIL, VIH) of this buffer are non-standard, refer to the input attenuator circuit for dc-coupled Pulsed LVCMOS in the Si5381/82 Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the “AC-coupled Singled-Ended” mode as shown in Figure 3.6 Termination of Differential and LVCMOS Input Signals on page 12.

Table 5.4. Serial and Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial and Control Input Pins (IN_SEL[1:0], RSTb, OEb, PDNb, I2C_SEL, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage Thresholds	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, PDNb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5381/82 Family Reference Manual for more details on the register settings.

Table 5.5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}	Outputs connected to DSPLL_B		0.48	—	2949.12	MHz
		Outputs connected to DSPLL_A/C/D		0.0001	—	735	MHz
Duty Cycle	DC	fOUT < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 800 MHz		45	—	55	%
		800 MHz < f_{OUT} < 1474.56 MHz		40	—	60	%
		f > 1474.56 MHz		35	—	65	
Output-Output Skew	T_{SK}	Differential Outputs Normal Mode		—	20	50	ps
		Differential Outputs		—	20	100	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Voltage Amplitude[1]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	470	550	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	660	810	1000	
Common Mode Voltage [1,2]	VCM	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.35	V
			LVPECL	1.90	2.05	2.15	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.15	1.25	1.35	
		V_{DDO} = 1.8 V [5]	sub-LVDS	0.87	0.93	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
Differential Output Impedance[2]	Z_O	Normal Mode		—	100	—	Ω
Power Supply Noise Rejection	PSRR	10 kHz sinusoidal noise		—	–93	—	dBc
		100 kHz sinusoidal noise		—	–93	—	
		500 kHz sinusoidal noise		—	–84	—	
		1 MHz sinusoidal noise		—	–79	—	
Output-Output Crosstalk[4]	XTALK			—	–75	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Refer to the Si5381/82 Family Reference Manual for recommended output settings.
2. Not all combinations of voltage amplitude and common mode voltages settings are possible.
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, http://www.silabs.com/Support%20Documents/TechnicalDocs/AN862.pdf, guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.
5. VDDO = 2.5 V or 3.3V required for f_{OUT} > 1474.56 MHz.

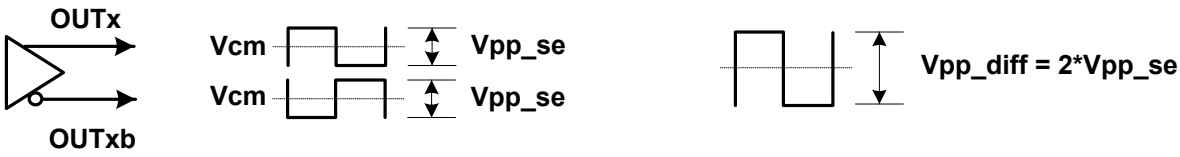


Table 5.6. LVCMOS Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

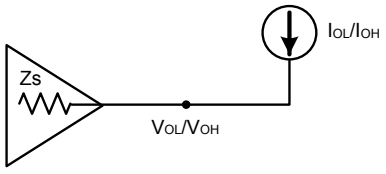
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}	Outputs connected to DSPLL_B		0.48	—	250	MHz
		Outputs connected to DSPLL_A/C/D		0.0001	—	250	MHz
Duty Cycle	DC	fOUT <100 MHz		47	—	53	%
		100 MHz < fOUT < 250 MHz		44	—	55	
Output-to-Output	T_{SK}	LVCMOS, integer related from the same Multi-Synth		—	—	100	ps
Output Voltage High[1, 2, 3]	V_{OH}	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOH = –10 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –12 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –17 mA		—	—	
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOH = –6 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –8 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –11 mA		—	—	
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOH = –4 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=3	IOH = –5 mA		—	—	

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Low[1, 2, 3]	V_{OL}	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOL = 10 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 12 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 17 mA	—	—		
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOL = 6 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 8 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 11 mA	—	—		
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOL = 4 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=3	IOL = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	420	550	ps
		VDDO = 2.5 V		—	475	625	ps
		VDDO = 1.8 V		—	525	705	ps

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5381/82 Family Reference Manual for more details on register settings.
2. IOL/IOH is measured at VOL/VOH as shown in the dc test configuration.
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



AC Output Test Configuration

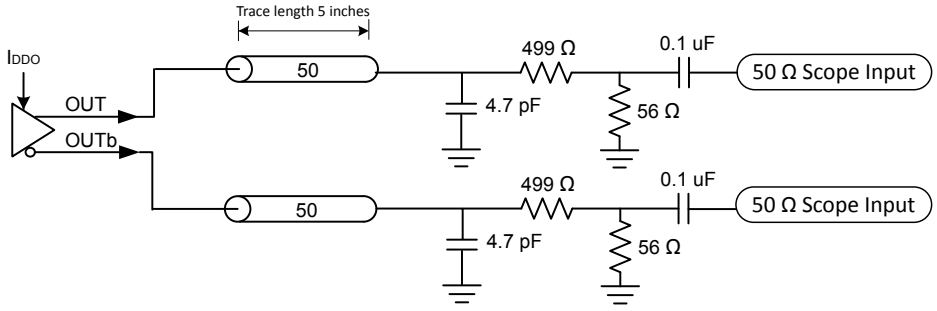


Table 5.7. Output Serial and Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial and Status Output Pins (INTRb, SDA/SDIO[2], A1/SDO)						
Output Voltage	V_{OH}	IOH = –2 mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	IOL = 2 mA	—	—	V_{DDIO}1 x 0.15	V

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as VDDA or VDD. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5381/82 Family Reference Manual for more details on register settings.
2. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high internally. V_{OL} remains valid in all cases.

Table 5.8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up or de-assertion of PDNb to when the device generates free-running clocks	—	385	—	ms
PLL Lock Time	t_{ACQ}	Fastlock enabled, f_{IN} = 19.44 MHz[2]	—	500	600	ms
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	25 MHz input, 25 MHz output, loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Only valid for a single automatic switch between two input clocks at the same frequency.	—	—	2.0	ns
		Only valid for a single manual switch between two input clocks at the same frequency.	—	—	1.3	ns
Pull-in Range	ω_P		–20	—	+20	ppm
Input-to-Output Delay Variation	$t_{IODELAY}$[4]	Through a given DSPLL, for DSPLLs A/C/D only.	—	—	1.8	ns
	t_{ZDELAY}		—	110	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RMS Jitter Generation[6]	J_{GEN}[5]	DSPLL_B, 12 kHz to 20 MHz	—	85	—	fs RMS
		DSPLL_A/C/D, 12 kHz to 20 MHz	—	150	—	fs RMS
Phase Noise Performance (122.88 MHz Carrier Frequency)	PN	10 Hz	—	TBD	—	dBc/Hz
		100 Hz	—	TBD	—	dBc/Hz
		1 kHz	—	TBD	—	dBc/Hz
		10 kHz	—	TBD	—	dBc/Hz
		100 kHz	—	TBD	—	dBc/Hz
		1 MHz	—	TBD	—	dBc/Hz
		10 MHz	—	TBD	—	dBc/Hz
Spur Performance (122.88 MHz Carrier Frequency)	SPUR	Up to 1 MHz offset	—	-103	—	dBc
		From 1 MHz to 30 MHz offset	—	-95	—	dBc

Note:

1. Actual loop bandwidth may be lower; please refer to CBPro for actual value on your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths, both set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Measured between a common 2 MHz input and 2 MHz output with different N-dividers on the same unit and a loop bandwidth of 4 kHz. These output frequencies are generated using non-production engineering modes only for test.
5. Delay between reference and feedback input both clocks at 10 MHz and same slew rate. Ref clock rise time must be <200 ps. These output frequencies are generated using non-production engineering modes only for test.
6. Jitter generation test conditions: f_{IN} = 30.72 MHz, 3.3V LVPECL, DSPLL LBW = 100 Hz. Jitter integrated from 12 kHz to 20 MHz offset. Does not include jitter from PLL input reference.

Table 5.9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
			Standard Mode 100 kbps		**Fast Mode 400 kbps**		
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

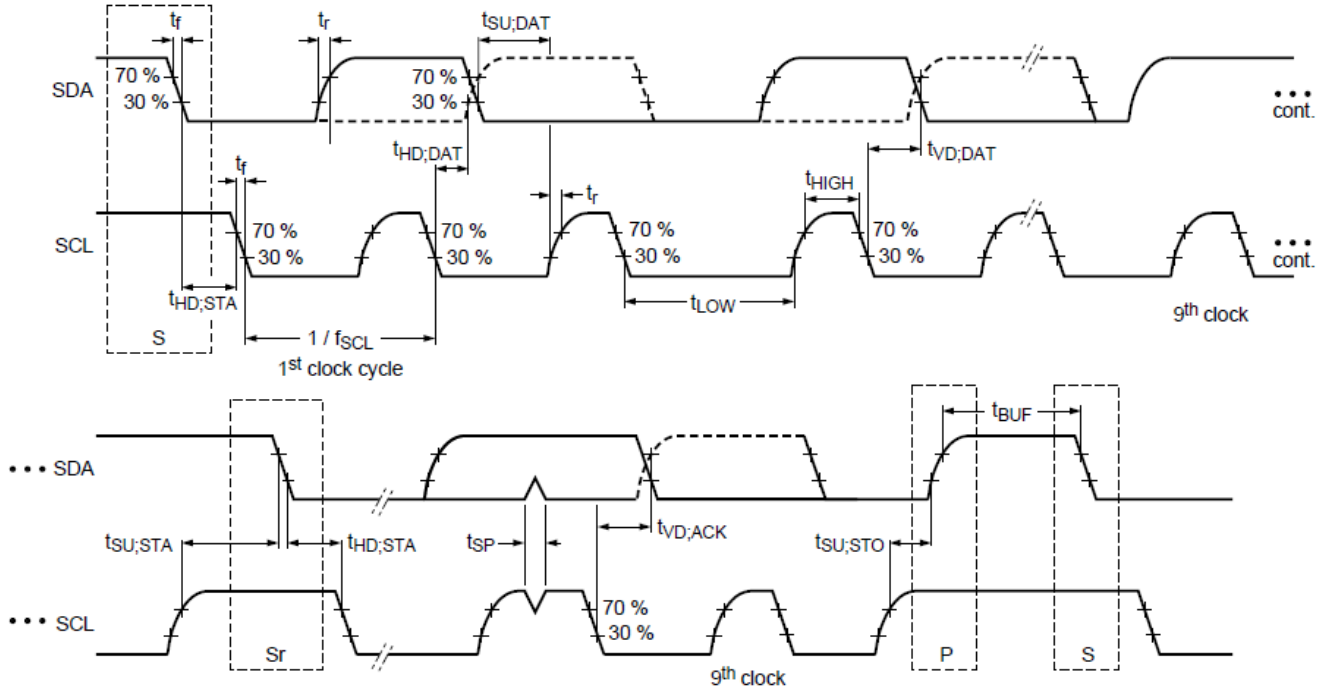


Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	—	15	ns

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_c

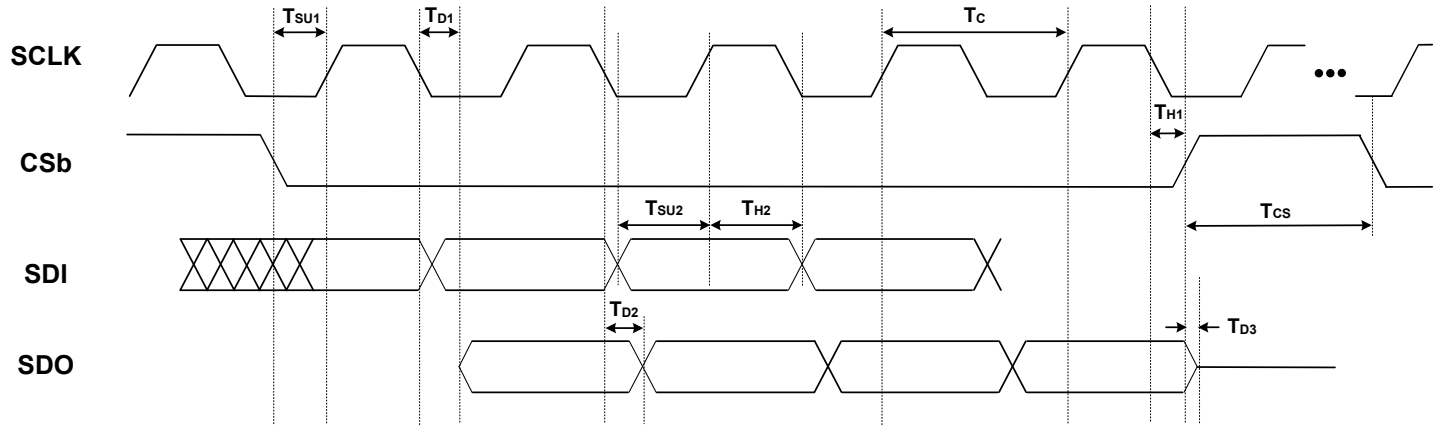


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_c

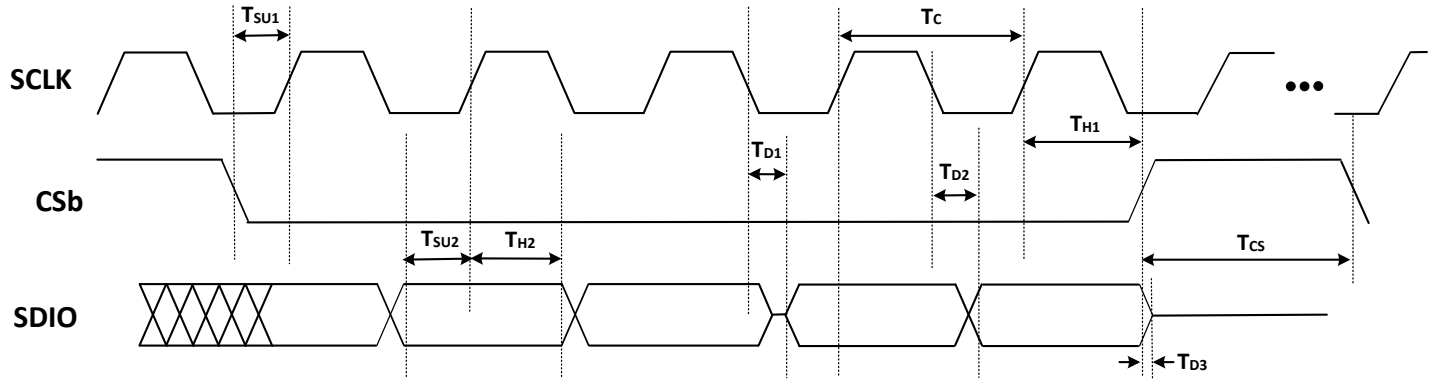


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. External Crystal Specifications (Grade A Only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Crystal Frequency[1]	f_{XTAL}		—	54	—	MHz
Total Frequency Tolerance[2]	f_{RANGE}		–100	—	+100	ppm
Load Capacitance	C_L		—	8	—	pF
Crystal Output Capacitance	C_O		—	—	2	pF
Crystal Drive Level	d_L		—	—	300	µW
Equivalent Series Resistance	R_{ESR}		—	—	23	Ω

Note:
1. The Si5381/82 is designed to work with crystals that meet the frequencies and specifications in Table 12.
2. Includes initial tolerance, drift after reflow, change over temperature (–40 °C to +85 °C), VDD variation, load pulling and aging.

Table 5.13. Thermal Characteristics (Grade A, QFN-64)

Parameter	Symbol	Test Condition[1]	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	

Note:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.14. Thermal Characteristics (Grade E, LGA-64)

Parameter	Symbol	Test Condition[1]	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	TBD	°C/W
		Air Flow 1 m/s	TBD	
		Air Flow 2 m/s	TBD	
Thermal Resistance Junction to Case	θ_{JC}		TBD	
Thermal Resistance Junction to Board	θ_{JB}		v	
	Ψ_{JB}		TBD	
Thermal Resistance Junction to Top Center	Ψ_{JT}		TBD	

Note:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.15. Absolute Maximum Ratings[1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	VDD		–0.5 to 3.8	V
	VDDA		–0.5 to 3.8	V
	VDDO		–0.5 to 3.8	V
Input Voltage Range	VI1	IN0 – IN3	–0.85 to 3.8	V
	VI2	IN_SEL[1:0], RSTb, PDNb, OEb, I2C_SEL, SDA/SDIO, A1/SDO, SCLK, A0/CSb	–0.5 to 3.8	V
	VI3	XA/XB (Grade A only)	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Storage Temperature Range	T_{STG}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Temperature Time at TPEAK(Pb-free profile)[4]	T_P		20–40	sec

Parameter	Symbol	Test Condition	Value	Unit

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN is RoHS-6 compliant.
3. For detailed MSL and packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

6. Typical Application Diagram

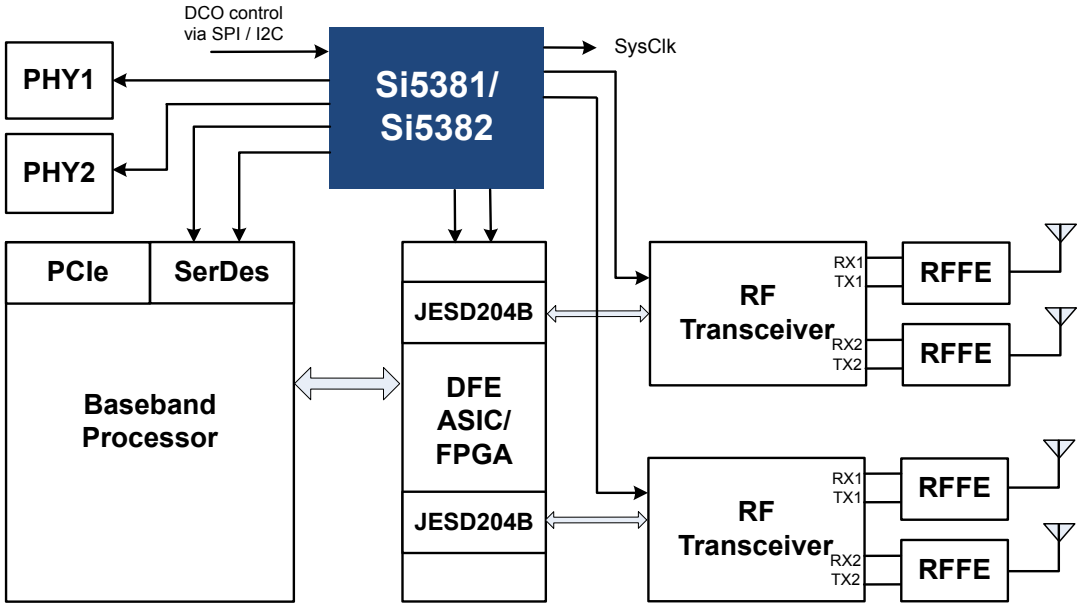


Figure 6.1. Si5381/82 Typical Application

7. Detailed Block Diagram

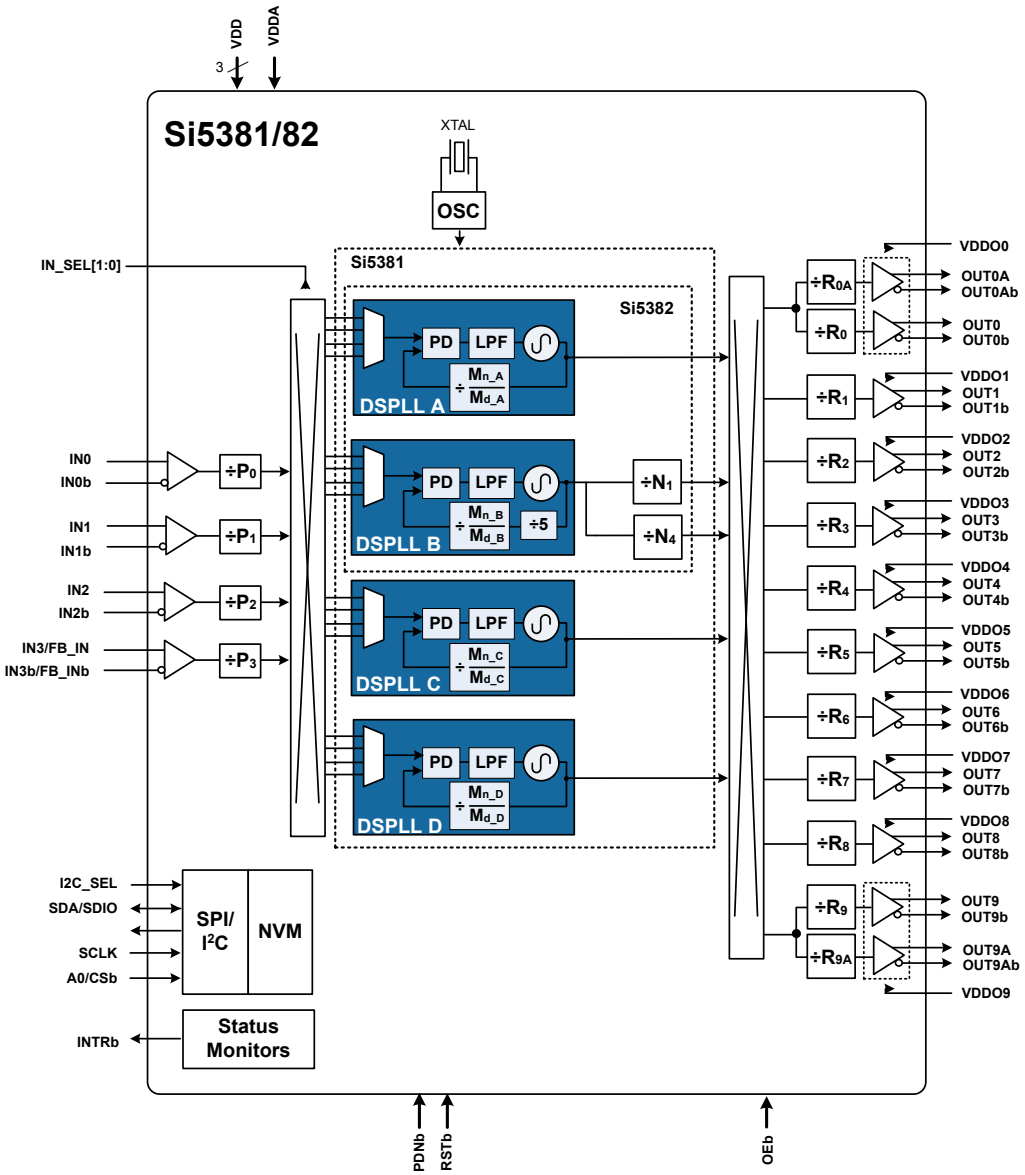


Figure 7.1. Si5381/82 Block Diagram (Grade E Shown)

8. Typical Operating Characteristics (Phase Noise and Jitter)

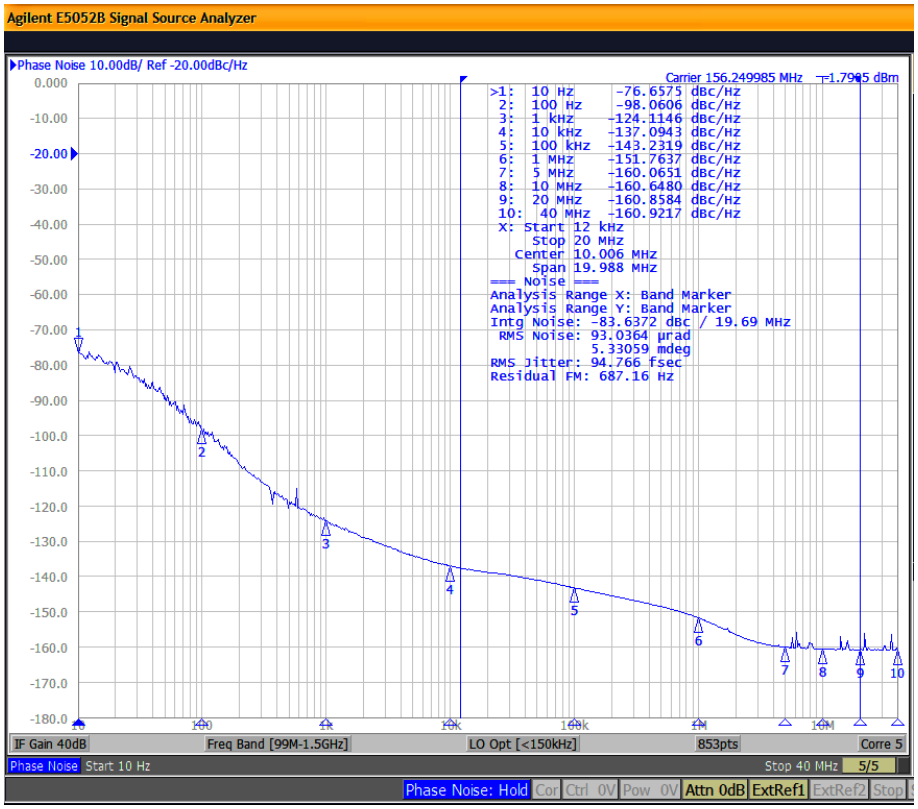


Figure 8.1. Typical Phase Noise (156.25 MHz)

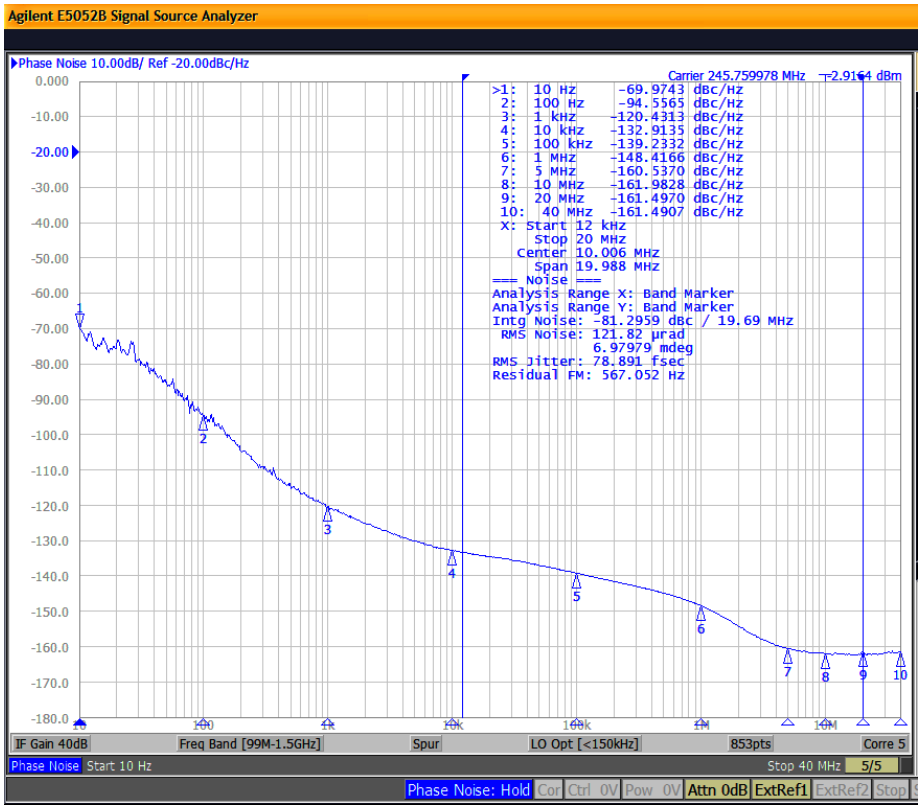


Figure 8.2. Typical Phase Noise (245.76 MHz)

9. Pin Descriptions

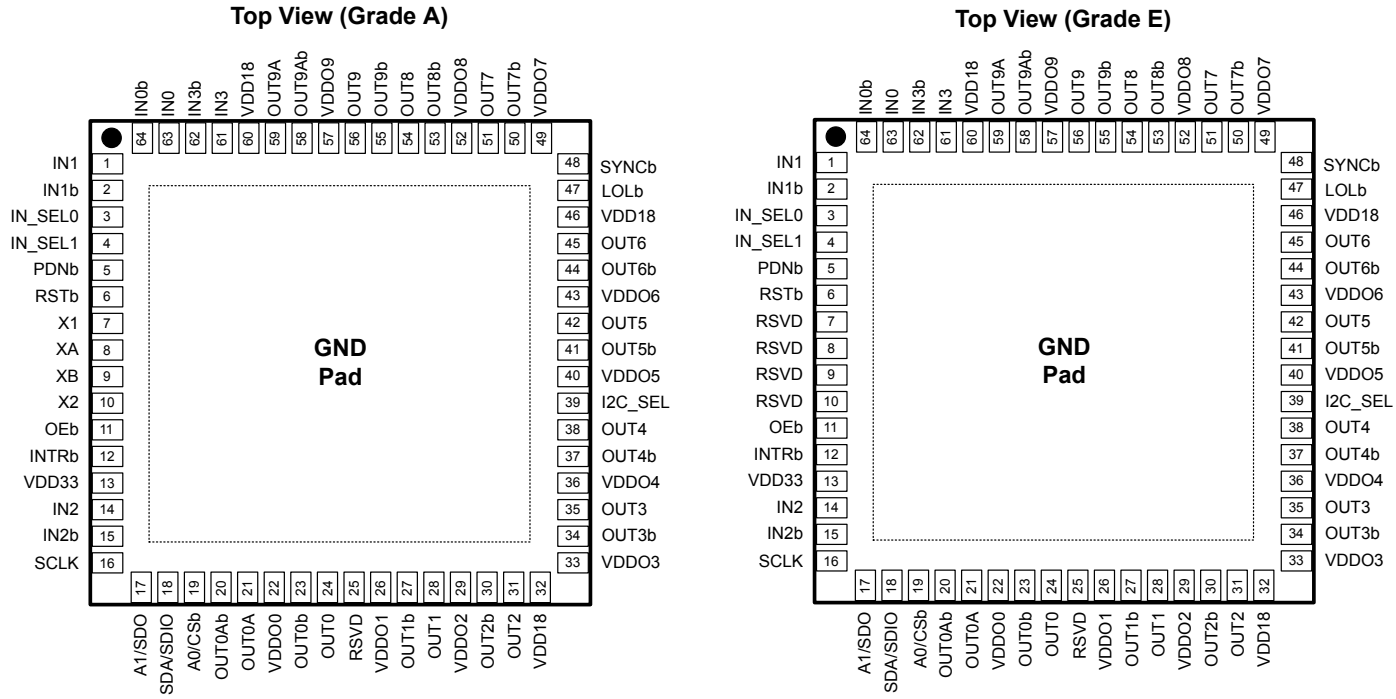


Figure 9.1. Si5381/82 64-QFN Top View

Table 9.1. Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	8	I	**Crystal Input (Grade A Only)** Input pin for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode. Single-ended inputs must be connected to the XA pin, with the XB pin appropriately terminated. **For Grade E (integrated crystal) these pins are reserved and should be left unconnected)**.
XB	9	I	
X1	7	I	**XTAL Shield (Grade A Only)** Connect these pins directly to the crystal ground pins. Both the X1/X2 pins and Crystal ground pins should be separated from the PCB ground plane. Refer to the Si5381/82 Family Reference Manual for layout guidelines. **For Grade E (integrated crystal) these pins are reserved and should be left unconnected)**.
X2	10	I	

Pin Name	Pin Number	Pin Type[1]	Function
IN0	63	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to section 3.3.1 Input Configuration and Terminations for input termination options. These pins are high-impedance and must be terminated externally, when being used. The negative side of the differential input must be ac-grounded when accepting a single-ended clock. Unused inputs may be left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	
IN3	61	I	
IN3b	62	I	
Outputs			
OUT0A	21	O	**Output Clocks.** These output clocks support programmable signal amplitude and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in the sections, and 3.5.5 LVCMOS Output Terminations. Unused outputs should be left unconnected.
OUT0Ab	20	O	
OUT0	24	O	
OUT0b	23	O	
OUT1	28	O	
OUT1b	27	O	
OUT2	31	O	
OUT2b	30	O	
OUT3	35	O	
OUT3b	34	O	
OUT4	38	O	
OUT4b	37	O	
OUT5	42	O	
OUT5b	41	O	
OUT6	45	O	
OUT6b	44	O	
OUT7	51	O	
OUT7b	50	O	
OUT8	54	O	
OUT8b	53	O	
OUT9	56	O	
OUT9b	55	O	
OUT9A	59	O	
OUT9Ab	58	O	
Serial Interface			
I2C_SEL	39	I	**I²C Select.** This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.

Pin Name	Pin Number	Pin Type[1]	Function
SDA/SDIO	18	I/O	**Serial Data Interface.** This is the bidirectional data pin (SDA) for the I^2C mode, the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode or unused, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A1/SDO	17	I/O	**Address Select 1/Serial Data Output.** In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode, this is the serial data output (SDO) pin. This pin is 3.3 V tolerant. This pin must be pulled-up externally when unused.
SCLK	16	I	**Serial Clock Input.** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode or unused, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A0/CSb	19	I	**Address Select 0/Chip Select.** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt.** [2] This pin is asserted low when a change in device status has occurred. This pin must be pulled-up externally using a resistor of at least 1 kΩ. It should be left unconnected when not in use.
PDNb	5	I	**Power Down.** [2] The device enters into a low power mode when this pin is pulled low. This pin is internally pulled-up. This pin is 3.3 V tolerant. It can be left unconnected when not in use.
RSTb	6	I	**Device Reset.** [2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. This pin is 3.3 V tolerant.
OEb	11	I	**Output Enable.** [2] This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. This pin is 3.3 V tolerant.
RSVD	47, 48		**Reserved.** Leave disconnected.

Pin Name	Pin Number	Pin Type[1]	Function
IN_SEL0	3	I	**Input Reference Select.** [2] The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 3.2 Manual Input Selection Using IN_SEL[1:0] Pins on page 12. These pins are internally pulled-down and may be left unconnected when unused.
IN_SEL1	4	I	
RSVD	7, 8, 9, 10, 25		**Reserved.** Leave disconnected.
Power			
VDD	32	P	**Core Supply Voltage.** The device operates from a 1.8 V supply. A 1 uF bypass capacitor should be placed very close to each pin.
VDD	46	P	
VDD	60	P	
VDDA	13	P	**Core Supply Voltage 3.3 V.** This core supply pin requires a 3.3 V power source. A 1 uF bypass capacitor should be placed very close to this pin.
VDDO0	22	P	**Output Clock Supply Voltage. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTx, OUTxb Outputs.** Note that VDDO0 supplies power to OUT0 and OUT0A; VDDO9 supplies power to OUT9 and OUT9A. Leave VDDO pins of unused output drivers unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 1 µF bypass capacitor should be placed very close to each connected VDDO pin.
VDDO1	26	P	
VDDO2	29	P	
VDDO3	33	P	
VDDO4	36	P	
VDDO5	40	P	
VDDO6	43	P	
VDDO7	49	P	
VDDO8	52	P	
VDDO9	57	P	
GND PAD		P	**Ground Pad.** This pad provides connection to ground and must be connected for proper operation.

Note:

1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.

10. Packages

10.1 64-LGA Package

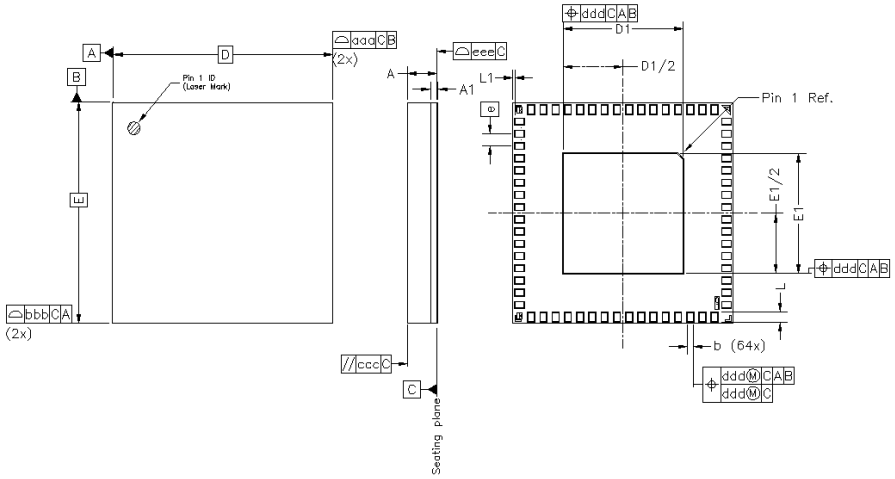


Figure 10.1. Si5381/82 9x9 mm 64-LGA Package Diagram

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	1.00	1.10	1.30
A1		0.26 REF	
b	0.20	0.25	0.30
D		9.00 BSC	
D2	5.40	5.50	5.60
e		0.50 BSC	
E		9.00 BSC	
E2	5.40	5.50	5.60
L	0.35	0.363	0.45
L1	0.03	0.08	0.13
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.15
ddd	—	—	0.05
ddd			0.10
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 64-QFN Package

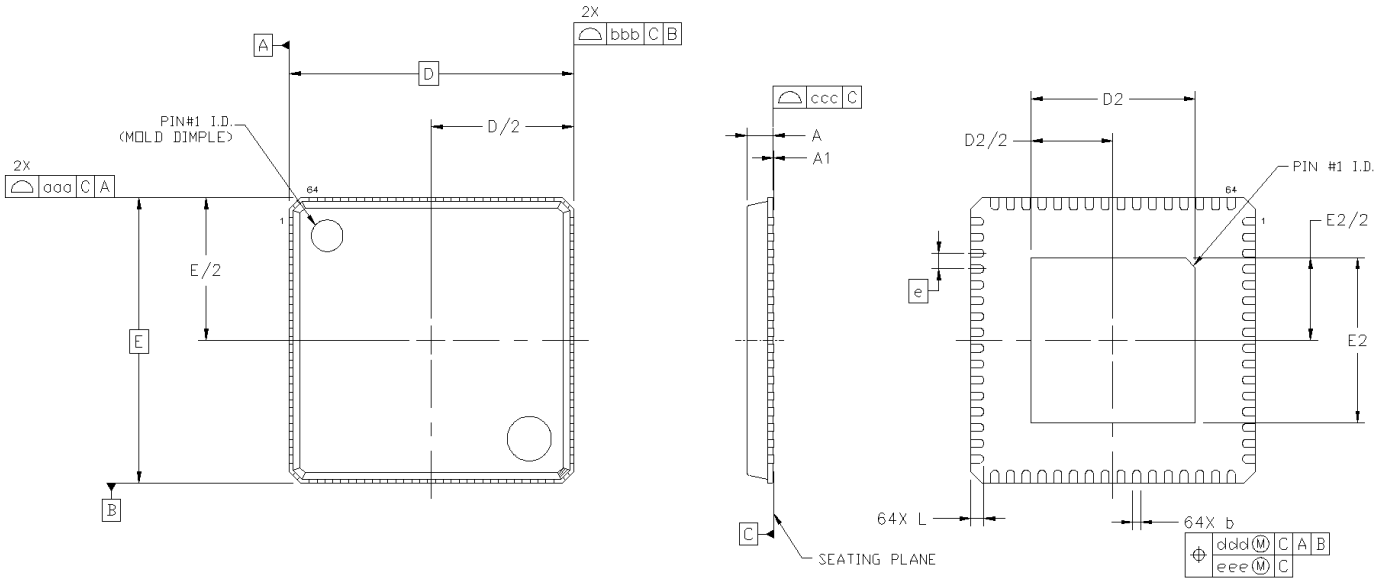


Figure 10.2. Si5381/82 9x9 mm 64-QFN Package Diagram

Table 10.2. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

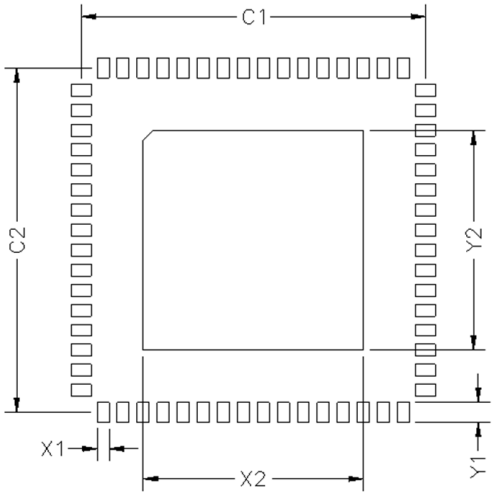


Figure 11.1. 9x9 mm 64-QFN Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Max
C1	8.60
C2	8.60
E	0.50
X1	0.30
Y1	0.50
X2	5.50
Y2	5.50

General

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

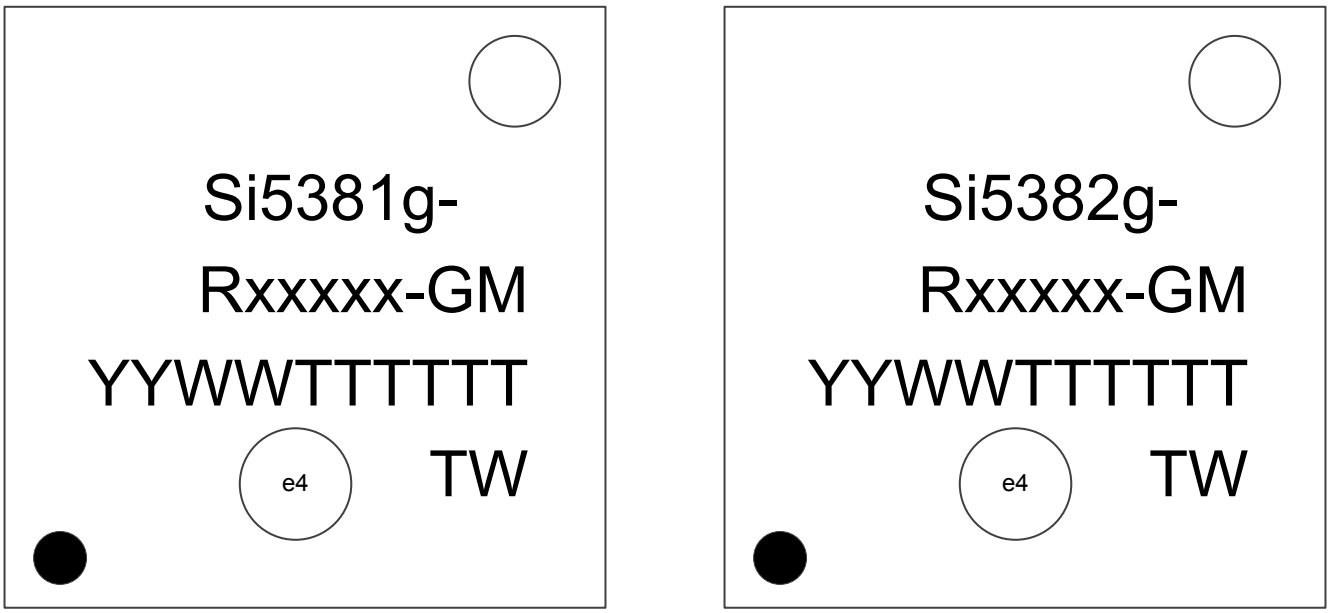


Figure 12.1. Si5381/82 Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
Line 1	Si5381g Si5382g	g = Grade (internal versus external crystal oscillator option) Si5381A = Grade A, 4-DSPLL wireless clock with external XO/Crystal Si5381E = Grade E, 4-DSPLL wireless clock with internal crystal oscillator Si5382A = Grade A, 2-DSPLL wireless clock with external XO/Crystal Si5382E = Grade E, 2-DSPLL wireless clock with internal crystal oscillator
Line 2	Rxxxxx-GM	R = Product revision. (See 2. Ordering Guide for current ordering revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. -GM = Package (QFN) type and temperature range (–40 to +85 °C).
Line 3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
Line 4	Circle w/ 1.6 mm diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

14. Revision History

14.1 Revision 0.9

September 25, 2017

- Initial Public Release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
www.silabs.com/timing

SW/HW
www.silabs.com/CBPro

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com