OV7910 Color CMOS NTSC/PAL CAMERACHIP™
OV7411 B&W CMOS NTSC/PAL CAMERACHIP™

General Description

The OV7910 (color) and OV7411 (black and white) single chip CMOS CAMERACHIPS™ are designed to provide a high level of functionality in a small footprint package. Both devices support NTSC/PAL composite video and S-Video. The OV7910 imager also provides RGB and YCbCr video signals, and each device directly interfaces with a VCR TV monitor or other 75 ohm terminated input. A minimal number of external components are required to complete a fully functional camera subsystem. The OV7910/OV7411 video cameras require only a single 5-volt DC supply and have been designed for very low power operation. These products are ideal for all applications requiring a small footprint, low voltage, low power and low cost color or black and white video camera.

Features

- Single chip 1/3" format video camera
- 628 x 582 pixels (PAL) or 510 x 492 pixels (NTSC)
- Composite video: NTSC, S-Video
- Component video RGB or YUV
- Sensitivity boost (+18 dB)/AGC ON/OFF
- Automatic exposure/gain/white balance
- External frame sync capability
- Aperture correction
- SCCB programmable controls: color saturation, gain, brightness, contrast, white balance, exposure time
- Gamma correction (0.45) ON/OFF
- Low power consumption
- +5 volt only power supply

Ordering Information

Product	Package
OV07910-C10A (Color, NTSC)	CLCC-48
OV07910-C20A (Color, PAL)	CLCC-48
OV07910-P10A (Color, NTSC)	PLCC-48
OV07910-P20A (Color, PAL)	PLCC-48
OV07411-C10A (B&W, NTSC)	CLCC-48
OV07411-C20A (B&W, PAL)	CLCC-48
OV07411-P10A (B&W, NTSC)	PLCC-48
OV07411-P20A (B&W, PAL)	PLCC-48

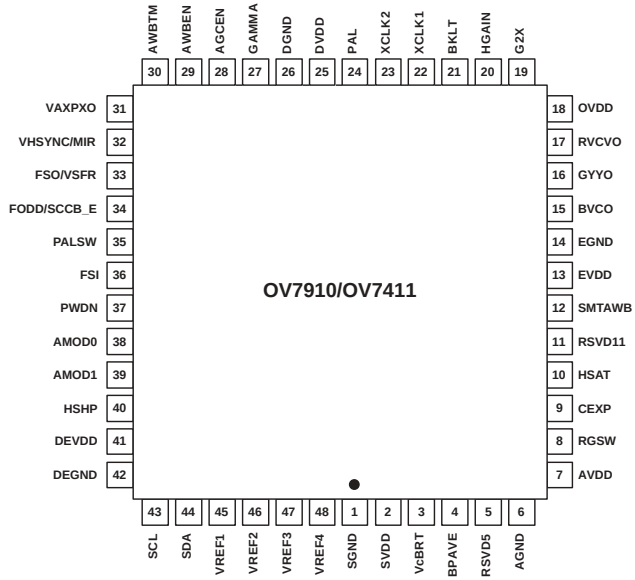
Applications

- Automotive
- PC Multimedia
- Toys
- Security
- Surveillance
- Video phones
- Video conference equipment

Key Specifications

Array Size	**PAL**	628 x 582
	NTSC	510 x 492
Power Supply		5 VDC ± 5%
Power Requirements		200 mW
Image Area	**PAL**	5.78 mm x 4.19 mm
	NTSC	4.69 mm x 3.54 mm
Auto Electronic Exposure Time		1/60s to 1/1500s
Lens Size		1/3"
Min. Illumination (3000K)	**OV7910**	< 5 Lux
	OV7411	< 1 Lux
S/N Ratio		40 dB
Pixel Size		9.2 µm x 7.2 µm
Fixed Pattern Noise		< 0.03% V_{PP}
Package Dimensions		.560 in. x .560 in.

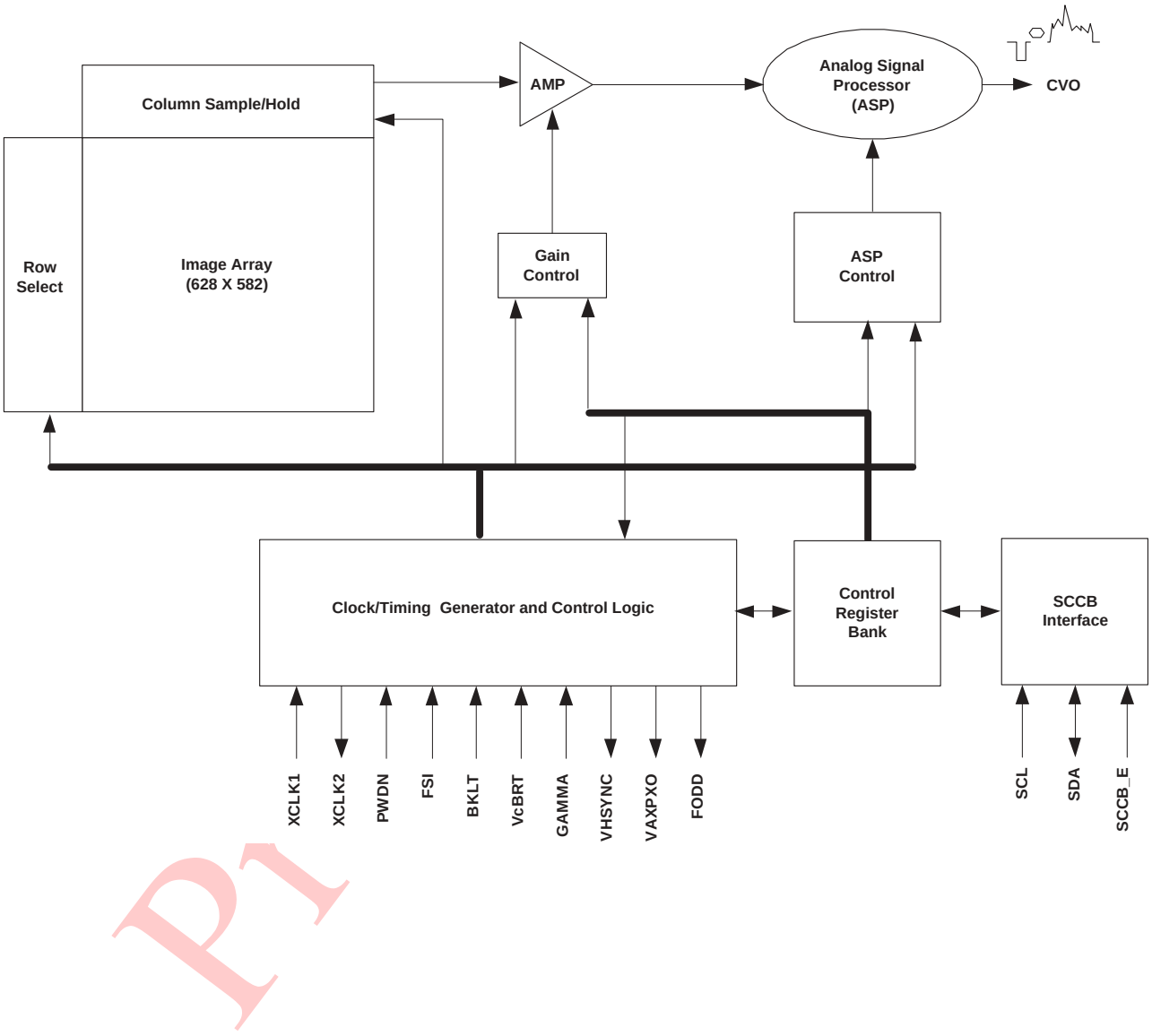
Figure 1 OV7910/OV7411 Pin Diagram



Functional Description

This section describes the various functions of the OV7910/OV7411. Refer to Figure 2 for the functional block diagram of the OV7910/OV7411.

Figure 2 Functional Block Diagram



Video Standards

Two TV standards are implemented and available as output in the OV7910/OV7411 imaging devices, NTSC (M) and PAL (B). Table 1 shows how to configure the standard of choice. Note that the accuracy and stability of the crystal clock frequency is important to avoid unwanted color shift in TV video system.

Table 1 Standard Configurations

Standard	PAL Setting (Pin 24)	Clock	Comments
NTSC	0	14.31818 MHz	Clock in = 4 x F_{SC}
PAL	1	17.734475 MHz	Clock in = 4 x F_{SC}

Video Formats

The OV7910/OV7411 image sensors support a variety of formats including Composite (CVBS), S-Video (YO/CO), RGB components, and YUV components. Composite and S-Video signals are generated from the internal TV encoder and RGB/YUV outputs are generated form the color matrix prior to entering the encoder. The image sensor utilizes the RG/BG Bayer pattern, sending raw pixel data through the color matrix, creating RGB or YUV component signals. At the same time, YUV signals are also processed to generate both composite and S-video signals. Note that color format configuration is valid only for the OV7910 image sensor.

Composite and S-Video

The Composite/S-Video format is the power-up default configuration for the OV7910/OV7411 image sensors. AMOD0 (pin 38) and AMOD1 (pin 39) select composite and S-video formats. In this configuration, RVCVO (pin 17) outputs the YO component of the S-video signal and BVCO (pin 15) outputs the CO component. Table 2 summarizes the available formats and the settings required on the appropriate pins.

RGB Format

Setting AMOD0 = 1 (with AMOD1 = x) selects the RGB format. In this configuration, RVCVO outputs the RED component, GYYO outputs the GREEN component and BVCO provides the BLUE component.

YUV Format

Setting AMOD0 = 0 and AMOD1 = 1 configures the OV7910/OV7411 sensors to operate in YUV mode or B&W mode. In this configuration, GYYO outputs the Y component, RVCVO provides the Cr component, and BVCO outputs the Cb component. On the OV7411 image sensor, only the GYYO (Y component) output is valid.

Configuring the OV7910/OV7411

The OV7910/OV7411 sensors are designed for ease-of-use in many standalone applications. Most of the on-chip functions are configurable by connecting appropriate pins high (logic "1") or low (logic "0") using a 10KΩ resistor. The image sensor reads the input pins at power up which enable user-defined default configurations.

The OV7910/OV7411 sensors also contain a Serial Camera Control Bus (SCCB) interface for programmable access to all register functions. For further details on the SCCB port, see "Serial Camera Control Bus (SCCB)" on page 4. By default, the SCCB interface is disabled. To enable the SCCB interface for controlling the sensor, a 10KΩ. pull-up resistor must be connected to the FODD/SCCB_E pin (pin 34). With the FODD/SCCB_E pin pulled high at power-up, the OV7910/OV7411 image sensors will enable the SCCB port for access.

White Balance

The White Balance function in the OV7910/OV7411 image sensor is used to adjust and calibrate the image device sensitivity on the primary (RGB) colors to match the color cast of the light source. The Auto White Balance (AWB) can be enabled or disabled through either the AWBEN pin (pin 29) or through the SCCB port. If AWB is enabled, the image sensors continuously perform white balancing. A fast or slow mode of white balancing may be user-selected through the AWBTM pin (pin 30). Fast AWB updates color every 2 fields while slow AWB updates every 16 fields.

By using the SCCB port, the color temperature may be further fine tuned to the requirement of the application. Note that the "blue" (BLUE and BBS registers) and "red" (RED and RBS registers) bias control are only available through the SCCB port. This function enables the user to define a "cooler" or "warmer" background for image capture.

Table 2 Video Format Options

Format Type	RVCVO (Pin 17)	GYYO (Pin 16)	BUCO (Pin 15)	Pin Settings
Composite/S-Video	CVBS	YO	CO	AMOD0 = 0, AMOD1 = 0
RGB Component	RED	GREEN	BLUE	AMOD0 = 1, AMOD1 = x
YUV Component	Cr	Y	Cb	AMOD0 = 0, AMOD1 = 1
Black and White	—	Y	—	AMOD0 = 0, AMOD1 = 1 ***Note:*** *Pins 15 and 17 are undefined in the OV7411 sensor.*

Additional Picture Control

A number of functions/registers are available which enable the user to configure OV7910/OV7411 image capturing parameters. These functions include Automatic Gain Control (AGC), AGC Gain, Automatic Exposure Control (AEC), GAMMA, and Backlight control.

AGC Gain can be set at 2x normal by programming pin 20, HGAIN. This function may be configured through the SCCB port as well. GAMMA (pin 27) can be used to set the color correction. BKLT (pin 21) controls how the OV7910/OV7411 image sensors manage backlight conditions. These functions may also be controlled by the SCCB interface.

At power up, AGC and AEC are enabled. AGC can be disabled at power-up by configuring the AGCEN pin (pin 28) as required. AEC cannot be enabled/disabled externally and must be programmed through the SCCB port.

Other Image Sensor Control Functions

Additional programmable functions for OV7910/OV7411 image sensors include sharpness adjustment, brightness level fine tune, color saturation adjustment, hue adjustment. All these functions (except for power down) can be configured by either an external pin or through the SCCB interface.

Serial Camera Control Bus (SCCB)

Many of the functions and configuration registers in the OV7910/OV7411 image sensors are available through the SCCB interface. The SCCB port is enabled by asserting the SCCB_E line (pin 34, see "FODD/SCCB_E" on page 8) through a 10KΩ resistor to V_{DD}. When the SCCB capability is enabled (SCCB_E = 1), the OV7910/OV7411 image sensor operates as a slave device that supports up to 400 kbps serial transfer rate using a 7-bit address/data transfer protocol.

NOTE: When the SCCB interface is enabled, the OV7410/OV7411 will output in color by default. To output in B&W mode, set register COMB[1:0] = 10b.

SCCB Protocol Format

In SCCB operation (see Figure 5), the master must perform the following operations:

- Generate the Start/Stop condition
- Provide the serial clock on SCL
- Place the 7-bit slave address (RW bit) and the 8-bit sub-address on SDA

The receiver must pull down SDA during the acknowledgement bit time. During the write cycle, the OV7910/OV7411 device returns the acknowledgement and, during the read cycle, the master returns the acknowledgement, indicating to the slave that the read cycle can be terminated. Note that the restart feature is not supported here.

Within each byte, the MSB is transferred first. The read/write control bit is the LSB of the first byte. Standard SCCB communications require only two pins, SCL and SDA. SDA is configured as an open drain for bidirectional purposes. A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions.

Except for these two special conditions, the protocol that SDA remain stable during the HIGH period of the clock, SCL. Each bit is allowed to change state only when SCL is LOW (see Figure 3 and Figure 4).

The OV7910/OV7411 SCCB interface supports multi-byte write and multi-byte read. The master must supply the sub-address in the write cycle, but not in the read cycle. Therefore, the OV7910/OV7411 takes the read sub-address from the previous write cycle. In multi-byte write or multi-byte read cycles, the sub-address automatically increments after the first data byte so that

continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original sub-address; therefore, if a read cycle immediately follows a multi-byte cycle, a single byte write cycle that provides a new address must be inserted.

The OV7910/OV7411 supports a single slave ID. The ID is preset to 80 for write and 81 for read.

In the write cycle, the second byte in the SCCB is the sub-address for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to the unimplemented sub-address is ignored.

In the read cycle, the second byte is the data associated with the previously stored sub-address. Reading of an unimplemented sub-address returns unknown.

Figure 3 Bit Transfer on the SCCB

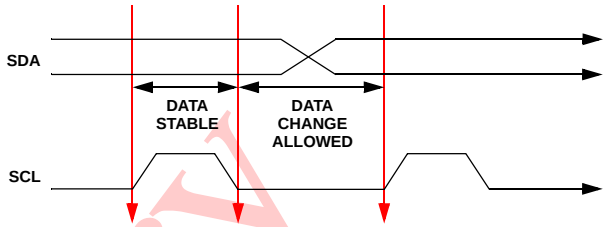


Figure 4 Data Transfer on the SCCB

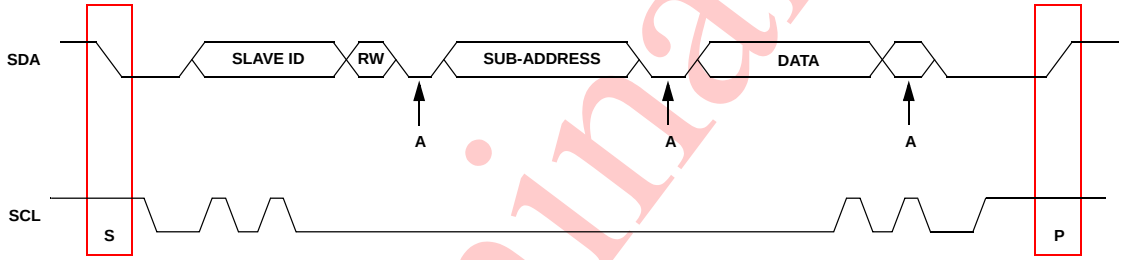
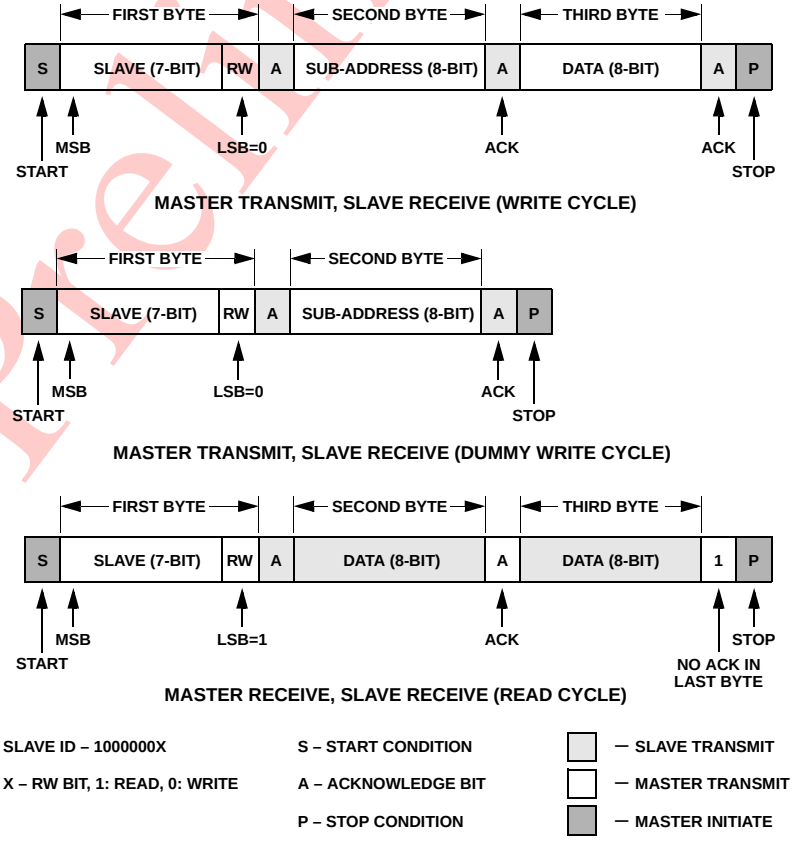


Figure 5 SCCB Protocol Format



Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	SGND	V_{IN}	Analog ground
02	SVDD	V_{IN}	Analog Power (+5 VDC)
03	VcBRT	1.2V	Image brightness adjustment - default set by internal resistor (~50KΩ). Default may be changed by applying an external bias to this pin.
04	BPAVE	Function (default = 0)	Internal 3-point average selection 0: Use internal 3-point averaging 1: Bypass internal 3-point averaging
05	RSVD5	V_{REF}	Internal reference
06	AGND	V_{IN}	Analog ground
07	AVDD	V_{IN}	Analog power (+ 5 VDC)
08	RGSW	Function (default = 0)	"Raw" data pixel selection 0: Select "raw" pixel data 1: Select non-"raw" pixel data
09	CEXP	Function (default = 0)	Central exposure selection 0: Select normal mode 1: Select central exposure mode
10	HSAT	Function (default = 0)	Color saturation selection 0: Select normal color saturation 1: Select increase color saturation by 25%
11	RSVD11	NC	Reserved
12	SMTAWB	Function (default = 0)	Automatic White Balance (AWB) smart mode selection 0: Disable smart mode 1: Enable smart mode - count pixels which contain a luminance signal between 10-80% of maximum value
13	EVDD	V_{IN}	Analog power (+5 VDC)
14	EGND	V_{IN}	Analog ground
15	BVCO	Output	Video output - output format determined by pin 38 (AMOD0) and pin 39 (AMOD1) AMOD0 AMOD1 Format Output Component 0 0 Composite S-video CO channel 0 1 YUV or B&W Cb component 1 0 RGB Blue component 1 1 RGB Blue component
16	GYYO	Output	Video output - output format determined by pin 38 (AMOD0) and pin 39 (AMOD1) AMOD0 AMOD1 Format Output Component 0 0 Composite S-video YO channel 0 1 YUV or B&W Y component 1 0 RGB Green component 1 1 RGB Green component

Table 3 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
17	RVCVO	Output	Video output - output format determined by pin 38 (AMOD0) and pin 39 (AMOD1) AMOD0 AMOD1 Format Output Component 0 0 Composite CVBS 0 1 YUV or B&W Cr component 1 0 RGB Red component 1 1 RGB Red component
18	OVDD	V_{IN}	Analog power for video output (+5 VDC)
19	G2X	Function (default = 0)	Enhanced gain selection for Automatic Gain Control (AGC) 0: Select normal AGC gain (no additional 2x gain) 1: Select additional 2x AGC gain
20	HGAIN	Function (default = 0)	AGC gain range selection 0: Select normal AGC range 1: Select AGC range x2 (4x to 8x)
21	BKLT	Function (default = 0)	Backlight selection 0: Disable backlight compensation 1: Enable backlight compensation
22	XCLK1	Input	Crystal clock input - frequency is 4 x F_{SC} to meet NTSC/PAL subcarrier standards
23	XCLK2	Output	Crystal clock output (4 x F_{SC} for NTSC = 14.318181 MHz, 4 x F_{SC} for PAL = 17.73265 MHz)
24	PAL	Function (default = 0)	NTSC/PAL selection 0: Select NTSC mode 1: Select PAL mode
25	DVDD	V_{IN}	Digital power
26	DGND	V_{IN}	Digital ground
27	GAMMA	Function (default = 1)	GAMMA selection 0: Disable GAMMA correction 1: Enable GAMMA correction
28	AGCEN	Function (default = 1)	AGC selection 0: Disable AGC 1: Enable AGC
29	AWBEN	Function (default = 1)	Automatic White Balance (AWB) selection 0: Disable AWB 1: Enable AWB
30	AWBTM	Function (default = 0)	AWB speed selection 0: Select normal AWB 1: Select "fast" AWB
31	VAXPXO	Output	Valid pixel detect output - CLK is asserted on this pin during active image period
32	VHSYNC/MIR	Output/Function (default = 0)	Vertical/horizontal sync output - adding a pull-up resistor on this pin enables mirror image

Table 3 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
33	FSO/VSFR	Output/Function (default = 0)	Vertical field/frame sync output - (default = field sync) adding a pull-up resistor on this pin enables frame sync
34	FODD/SCCB_E	Output/Function (default = 0)	Even/Odd field flag - adding a pull-up resistor on this pin enables SCCB control
35	PALSW	Output	PAL switch clock output
36	FSI	Input	Field sync input
37	PWDN	Function	Power down mode selection 0: Disable power down mode 1: Enable power down mode
38	AMOD0	Function	Mode output selection - determined with pin 39 (AMOD1) AMOD0 AMOD1 Mode 0 0 YO/CO/CVO 0 1 RGB 1 0 Y/U/V 1 1 RGB
39	AMOD1	Function	Mode output selection - determined with pin 38 (AMOD0) AMOD0 AMOD1 Mode 0 0 YO/CO/CVO 0 1 RGB 1 0 Y/U/V 1 1 RGB
40	HSHP	Function	Sharpness level selection 0: Select normal sharpness 1: Select x2 sharpness
41	DEVDD	V_{IN}	Analog power
42	DEGND	V_{IN}	Analog ground
43	SCL	I/O	SCCB control
44	SDA	I/O	SCCB data/address
45	VREF1	V_{REF}	Internal reference - must be decoupled with 0.1 µF capacitor to analog ground
46	VREF2	V_{REF}	Internal reference - must be decoupled with 0.1 µF capacitor to analog ground
47	VREF3	V_{REF}	Internal reference - must be decoupled with 0.1 µF capacitor to analog ground
48	VREF4	V_{REF}	Internal reference - must be decoupled with 0.1 µF capacitor to analog ground

Electrical Characteristics

Table 4 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 5 Electrical Characteristics (0°C to 70°C, all voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD}	Supply voltage (VDD, DVDD)	4.75	5.0	5.25	V
V_{DDO}	Supply voltage (DOVDD)	3		5.25	V
I_{DD1}	Supply current in VDDs			25	mA
I_{DD2}	Supply current in DOVDD with 50 pF load at digital output		TBD		mA/MHz
I_{DD3}	Standby supply current (CMOS level at inputs)			100	µA
Digital Input Pin					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2.0			V
C_{IN}	Input capacitor			10	pF
t_r, t_f	Digital input rise/fall time			25	ns
Digital Output - Standard Load 50 pF, 1.2 KΩ to 3.0 V					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
Video Bus - at 60Hz fps					
t_{PCLK}	PCLK cycle time		74		ns
t_P	PCLK pulse width		32		ns
t_{DS}	Data to PCLK setup time		t_P - 10		ns
t_{DH}	Data to PCLK hold time		t_P - 10		ns
SCCB					
f_{scl}	SCL clock frequency			400	KHz
t_f	SDA fall time	20 + 0.1C_{sda}		300	ns
t_{idle}	Bus idle time	1.3			µs

Table 5 Electrical Characteristics (0°C to 70°C, all voltages referenced to GND)

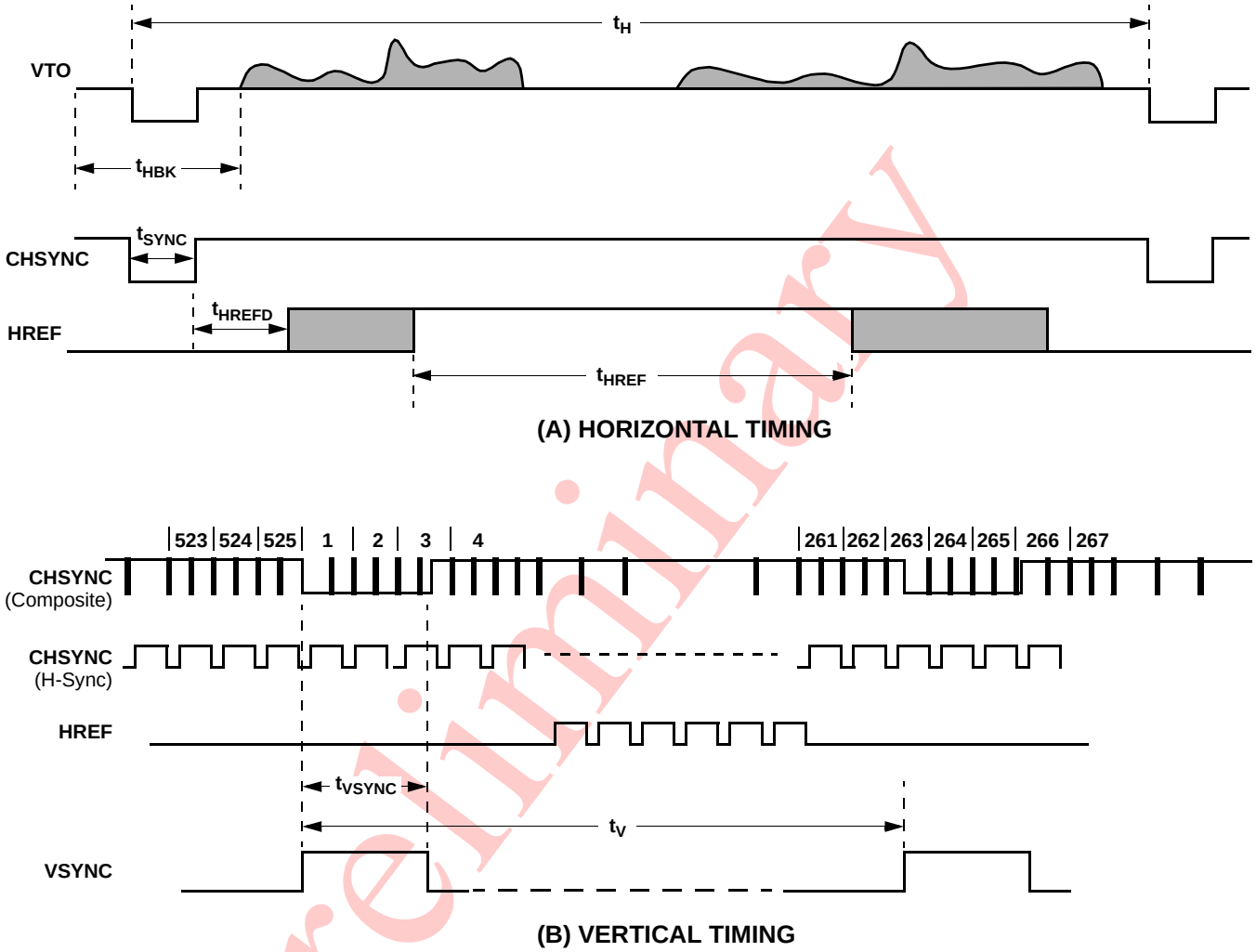
Symbol	Parameter	Min	Typ	Max	Unit
t_{hdsta}	START hold time	0.6			µs
t_{stps}	STOP setup time	0.6			µs
t_{ds}	SDA setup time	100			µs
t_{dh}	SDA hold time	0			µs
Clock Input/Crystal Oscillator					
f_{OSC}	Resonator frequency	TBD	TBD	TBD	MHz
	Load capacitor		10		pF
	Parallel resistance		1M		Ω
	Rise/fall time for external clock input		5		ns
	Duty cycle for external clock input	40		60	%
Miscellaneous Timing					
t_{SYNC}	External FSI cycle time		2		frame
t_{PU}	Chip power up time			100	µs
t_{PD}	Power up delay time		10		µs
t_{PZ}	Power up low-z delay		1000		ns
VTO Analog Video Output Parameters					
V_{TO-P}	Video peak signal level		2.8		V
V_{TO-B}	Video black signal level		0.7		V
V_{SYNC}	Y video sync pulse amplitude		0.7		V
Ro	Video output load		75		Ω
t_H	Horizontal line width				pclk
t_{HSYNC}	Horizontal sync width				pclk
t_{HBK}	Horizontal blank width				pclk
t_V	Vertical field width		262.5		t_H
t_{VSYNC}	Vertical sync width				t_H
t_{VF1}	Field 1 vertical front equalization width				t_H
t_{VB1}	Field 1 vertical back equalization width				t_H
t_{VBK1}	Field 1 blank line outside equalization region				t_H
t_{VF2}	Field 2 vertical front equalization width				t_H
t_{VB2}	Field 2 vertical back equalization width				t_H
t_{VBK2}	Field 2 blank line outside equalization region				t_H

Table 6 Sensor Characteristics (temp 27°C, illumination 3200°K, AEC maximum, AGC off, γ = 1)

Parameter	Value	Unit	Description
Dark current	50	mV/sec	Photo diode leakage induced signal - the leakage roughly doubles for every 10°C temperature rise
Sensitivity	1	V/lux.sec	
Random noise	TBD		Measured rms value at 75% signal illumination level versus full scale
Fix pattern noise	< 0.03	%	Measured rms value at 75% signal illumination level versus full scale
Smear	< 0.01	%	
Blooming	TBD	%	
Uniformity	1	%	Average signal variation over 9 equal size blocks at 50% signal illumination level

Timing Specifications

Figure 6 Video Timing Diagram

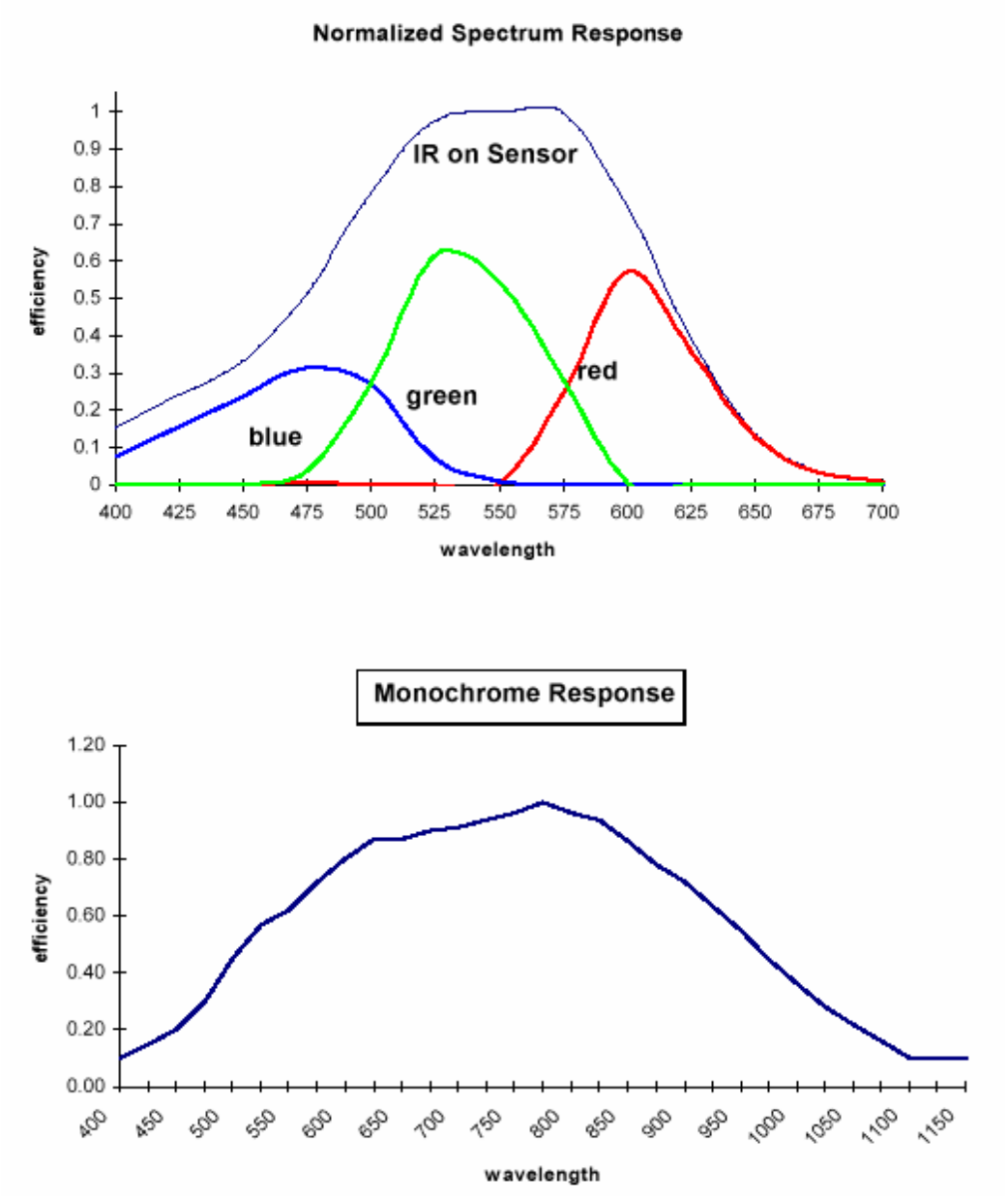


(A) HORIZONTAL TIMING

(B) VERTICAL TIMING

OV7910/OV7411 Light Response

Figure 7 OV7910/OV7411 Light Response



Register Set

Table 7 provides a list and description of the Device Control registers contained in the OV7910/OV7411. The device slave addresses are 80 for write and 81 for read.

Table 7 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Setting Bit[7]: Reserved Bit[6:0]: Storage for current AGC gain setting This register is updated automatically. If AGC is enabled, the internal control stores the optimal gain value in this register. If AGC is not enabled, a "00" is stored in this register.
01	BLUE	80	RW	Storage for the current blue channel setting for white balance control Bit[7]: Adjustment direction 0: Decrease gain 1: Increase gain Bit[6:0]: Blue channel gain balance value
02	RED	80	RW	Storage for the current red channel setting for white balance control Bit[7]: Adjustment direction 0: Decrease gain 1: Increase gain Bit[6:0]: Red channel gain balance value
03	SAT	D0	RW	Saturation Control Bit[7:0]: Saturation adjustment • Range: [00] lowest to [FF] highest
04	CNT	00	RW	Contrast Control Bit[7:0]: Contrast adjustment • Range: [00] lowest to [FF] highest
05	BRT	80	RW	Brightness Control Bit[7:0]: Brightness adjustment • Range: [00] lowest to [FF] highest
06	RSVD	XX	–	Reserved
07	BBS	20	RW	B Channel Offset Bit[7:6]: Reserved (BBS[7:6] = 00) Bit[5:0]: Blue channel bias value This value defines the fine tune adjustment for the blue tint in the white balance control. This register is the manual control portion of the AWB control.
08	RBS	20	RW	R Channel Offset Bit[7:6]: Reserved (RBS[7:6] = 00) Bit[5:0]: Red channel bias value This value defines the fine tune adjustment for the red tint in the white balance control. This register is the manual control portion of the AWB control.
09-0F	RSVD	XX	–	Reserved

Table 7 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	VER	03	R	Version number
11	MIDH	7F	R	Manufacturer ID Byte -- High (Read only = 0x7F)
12	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
13	AEC	82	RW	Exposure Control Value Bit[7:0]: Manual exposure setting • Range: [00] lowest to [82] highest
14	COMA	9F	RW	Common Control A Bit[7]: CEXP 0: Selects central exposure Bit[6:4]: Reserved Bit[3]: GAMMA selection 0: Select GAMMA = 1.0 1: Select GAMMA = 0.45 Bit[2]: AGC enable 1: Enable auto gain control Bit[1]: AWB enable 1: Enable auto channel balance Bit[0]: AEC enable - if AEC[0] = 1, AEC[7:0] (register 0x13) is updated automatically. If AEC[0] = 0, AEC[7:0] remains unchanged. 0: Disable 1: Enable
15	COMB	00	RW	Common Control B Bit[7]: SRST 1: Initiates soft reset. All registers are set to default values after which the chip resumes normal operation. Bit[6]: Mirror image selection 0: Normal 1: Output mirror image Bit[5]: VSFR 0: Enables field sync output to VSYNC (pin 32) 1: Enables frame sync output to VSYNC Bit[4]: Backlight exposure mode selection 0: OFF 1: ON Bit[3]: FREX 0: Exposure and gain values automatically updated 1: Disable update of exposure and gain values Bit[2]: HGAIN, AGC gain range selection 0: AGC normal range 1: Enable AGC 2x gain boost Bit[1:0]: AMOD - selects video output modes 00: S-Video and CVBS 01: RGB 10: YUV (for OV7410/OV7411, bit[1:0] must be set to 10) 11: RGB

Table 7 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
16	COMC	20	RW	Common Control C Bit[7]: Smart AWB selection 0: Disabled SMTAWB 1: Enables SMTAWB Bit[6]: Reserved Bit[5]: Automatic level control (ALC) 0: Disabled 1: Enabled Bit[4:0]: Reserved
17	COMD	34	RW	Common Control D Bit[7:4]: Reserved Bit[3]: BPSHP 0: Enables sharpness control 1: Disables sharpness control Bit[2]: Reserved Bit[1]: AWBTM 1: Selects "fast" AWB update Bit[0]: Reserved
18-1C	RSVD	XX	–	Reserved
1D	COME	34	RW	Common Control E Bit[7]: Reserved Bit[6]: G2XA 1: Enables additional 2x gain (not controlled by AGC) Bit[5:0]: Reserved
1E-3B	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7910/OV7411 uses 48-pin ceramic package. Refer to Figure 8 for ceramic package information and Figure 9 for the array center on the chip.

Figure 8 OV7910/OV7411 Package Specifications

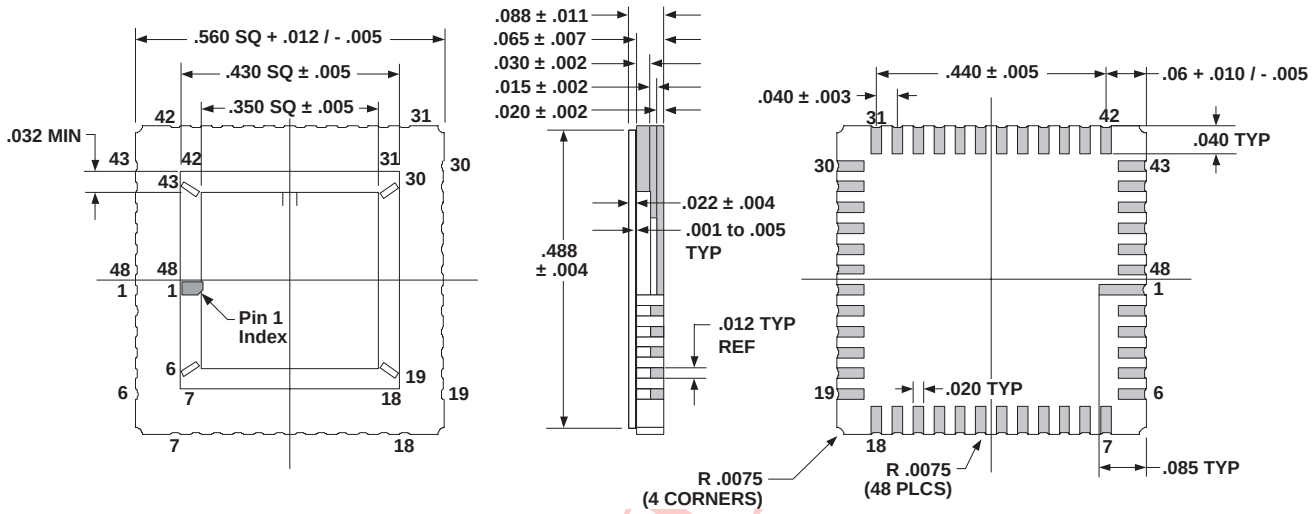
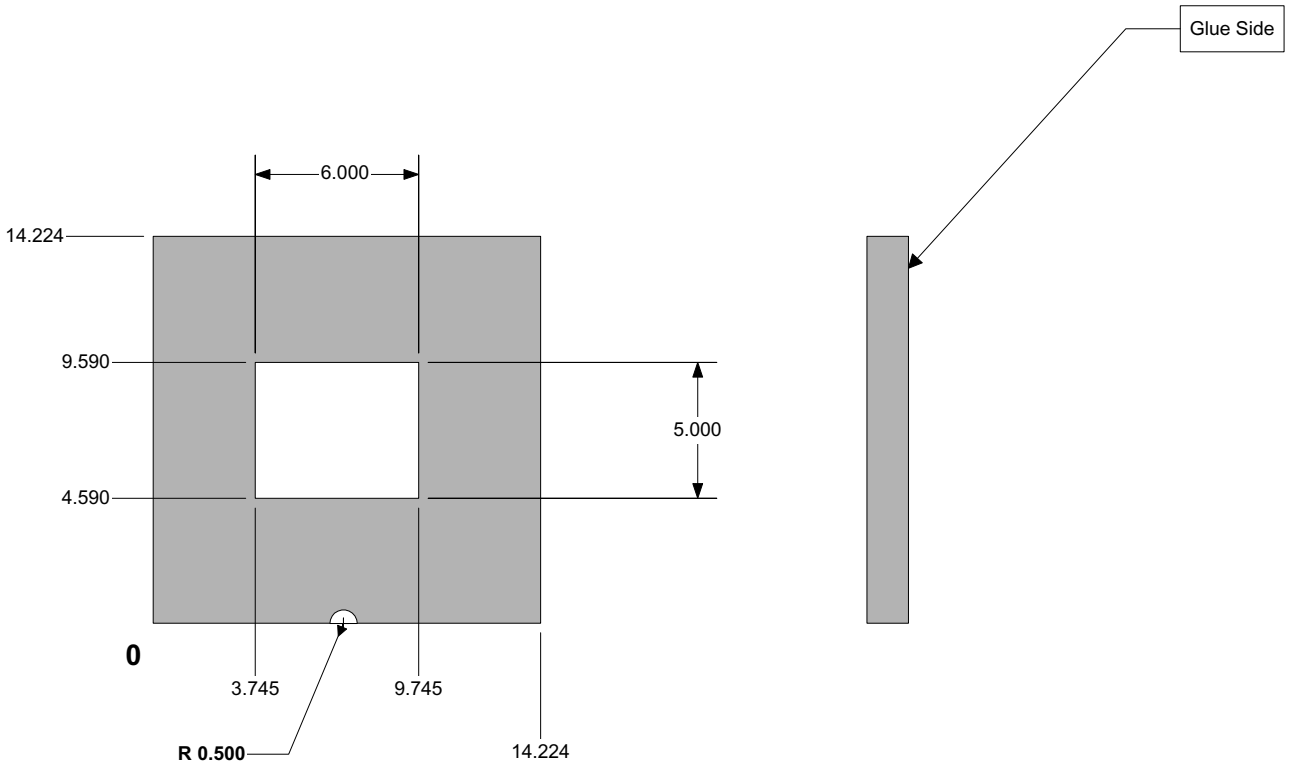


Table 8 OV7910/OV7411 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Mask Specifications

Figure 9 OV7910/OV7411 Mask Drawing

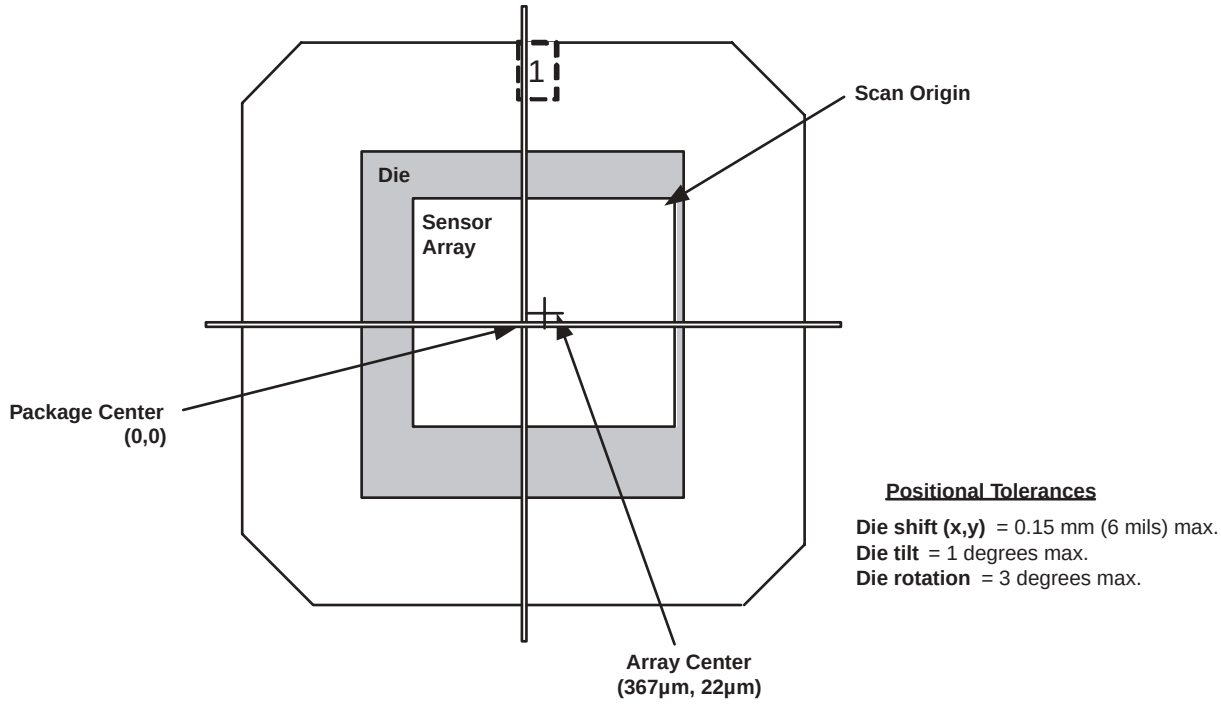


NOTE:

Due to a stray light path in the OV7910, you may encounter situations where you will see a slight red flare and or red flashes in the image. This behavior will be present in conditions of strong scene lighting such as outdoors and with wider than standard FOV lenses. The remedy for this behavior is to shield the die from strong oblique light rays by applying a mask to the window of the chip. Construct the mask to the dimensions as shown in Figure 9 above using some opaque self-adhesive material. To apply the mask on the top window, ensure that you have the pin one notch on the mask aligned with pin one on the bottom of the package and that the edges of the mask are even with the edges of the top window glass. This will ensure proper alignment of the opening in the mask with the photo array on the die. Lightly adhere the mask in place and double check the alignment before applying firm even pressure to the adhesive to achieve a permanent bond.

Sensor Array Center

Figure 10 OV7910/OV7411 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pin one oriented down on the PCB.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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