

Description

The PAM8304 is a mono filter-less Class-D amplifier with high SNR and differential input that helps eliminate noise. The PAM8304 supports 2.8V to 6V operation make it idea for up to 4 cells alkaline battery applications. The PAM8304 is capable of driving speaker loads as low as 3Ω speaker with a 5V supply maximizing the output power.

Features like greater than 90% efficiency and small PCB area make the PAM8304 Class-D amplifier ideal for portable applications. The output uses a filter-less architecture minimizing the number of external components and PCB area whilst providing a high performance, simple and lower cost system.

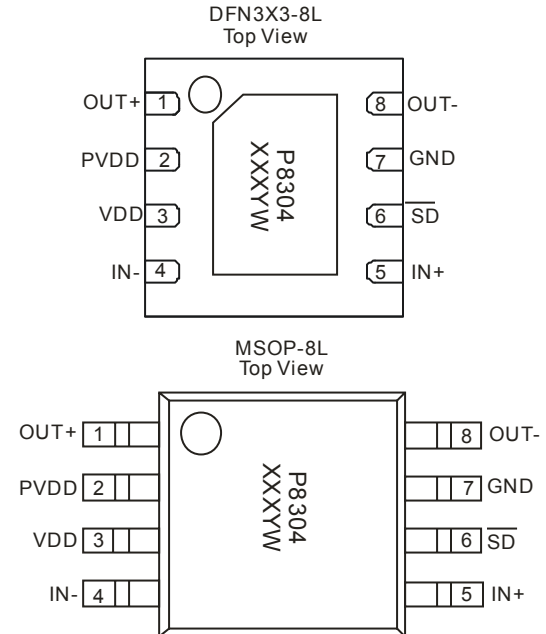
The PAM8304 features short circuit protection, thermal shutdown and under voltage lock-out.

The PAM8304 is available in DFN3030-8L and MOP-8L packages.

Features

- Supply Voltage from 2.8V to 6.0 V
- 3Ω Driving Capability
- 3.0W@10% THD Output with a 4Ω Load and 5V Supply
- High Efficiency up to 90% @1W with an 8Ω Load
- Shutdown Current <1μA
- Superior Low Noise without Input
- Short Circuit Protection
- Thermal Shutdown
- Available in Space Saving DFN3030-8L and MSOP-8L Packages
- Pb-Free Package

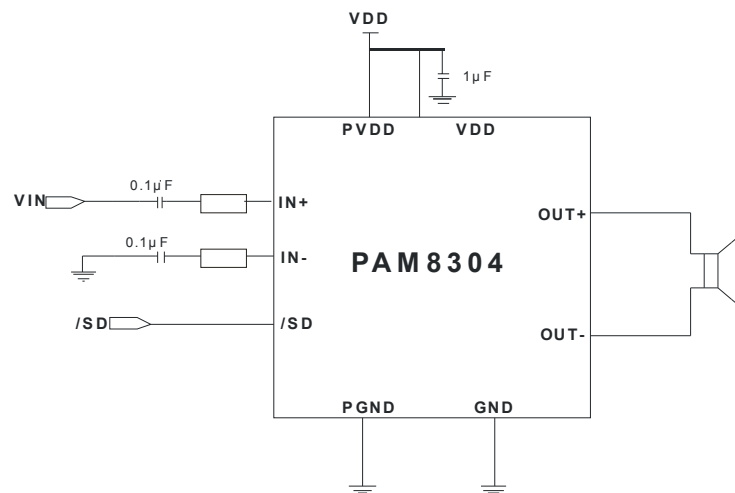
Pin Assignments



Applications

- MP4/MP3
- GPS
- Set-Top-Box
- Tablets/Digital Photo Frame
- Electronic Dictionary
- Portable Game Machines

Typical Applications Circuit



Pin Name	MSOP-8L/DFN3x3-8L	Function
OUT+	1	Positive BTL Output
PVDD	2	Power Supply
VDD	3	Analog Power Supply
IN-	4	Negative Differential Input
IN+	5	Positive Differential Input
/SD	6	Shutdown Terminal, Active Low
GND	7	Ground
OUT-	8	Negative BTL Output
Exposed Pad	—	NC

The block diagram illustrates the internal architecture of the motor driver IC, enclosed in a dashed box. The supply voltage is VDD and ground is GND. The input stage consists of a differential pair with inputs IN+ and IN-, and a sense input SD. The sense input SD is connected to a sense divider (SD) block. The differential pair's output is connected to a PWM Modulator block. The PWM Modulator's output is connected to two Gate Drive blocks, which drive the motor's OUT+ and OUT- terminals. The motor's other terminal is connected to PVDD. The internal architecture also includes a Bias and Vref block, an OSC block, and a protection block containing UVLO, SC Protect, Startup Protection, and OTP blocks. The sense divider (SD) block is connected to the PWM Modulator and the OSC block. The OSC block is connected to the PWM Modulator and the Bias and Vref block. The protection block is connected to the PWM Modulator and the Bias and Vref block.

Parameter	Rating	Unit
Supply Voltage (VDD)	6.5	V
Input Voltage (IN+, IN-, /SD)	-0.3 to V _{DD} +0.3	V
Storage Temperature	-65 to +150	°C
Maximum Junction Temperature	150	°C

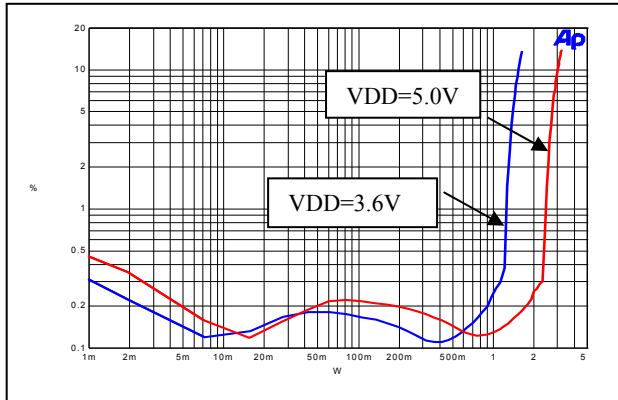
Symbol	Parameter	Min	Max	Unit
V _{DD}	Supply Voltage	2.8	6.0	V
T _A	Operating Ambient Temperature Range	-40	+85	°C
T _J	Junction Temperature Range	-40	+125	°C

Electrical Characteristics (@TA=25°C, VDD=5V, Gain=18dB, RL=L(33μH)+R+L(33μH), unless otherwise noted.)

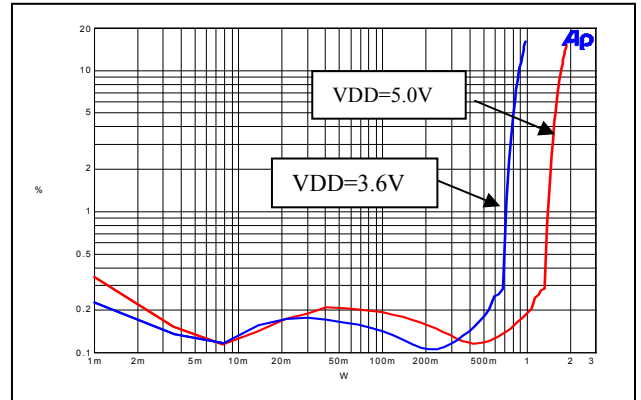
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			2.8		6.0	V
Po	Output Power	THD+N = 10%, f = 1kHz, R = 4Ω	VDD = 5.0V		3.0		W
			VDD = 3.6V		1.5		
			VDD = 3.2V		1.2		
		THD+N = 1%, f = 1kHz, R = 4Ω	VDD = 5.0V		2.4		W
			VDD = 3.6V		1.25		
			VDD = 3.2V		1.0		
		THD+N = 10%, f = 1kHz, R = 8Ω	VDD = 5.0V		1.75		W
			VDD = 3.6V		0.90		
			VDD = 3.2V		0.70		
		THD+N = 1%, f = 1kHz, R = 8Ω	VDD = 5.0V		1.40		W
			VDD = 3.6V		0.72		
			VDD = 3.2V		0.60		
THD+N	Total Harmonic Distortion Plus Noise	VDD = 5.0V, Po = 1W, R = 8Ω	f = 1kHz		0.17		%
		VDD = 3.6V, Po = 0.1W, R = 8Ω			0.16		
		VDD = 3.2V, Po = 0.1W, R = 8Ω			0.14		
		VDD = 5.0V, Po = 0.5W, R = 4Ω	f = 1kHz		0.14		%
		VDD = 3.6V, Po = 0.2W, R = 4Ω			0.16		
		VDD = 3.2V, Po = 0.1W, R = 4Ω			0.17		
PSRR	Power Supply Ripple Rejection	VDD = 3.6V, Inputs ac-grounded with C = 1μF	f=217Hz		-68		dB
			f=1kHz		-70		
			f=10kHz		-67		
Dyn	Dynamic Range	VDD = 5V, THD = %, R = 8Ω	f=1kHz		95		dB
Vn	Output Noise	Inputs ac-grounded	No A weighting		170		μV
			A-weighting		130		
η	Efficiency	RL = 8Ω, THD = 10%	f=1kHz		93		%
		RL = 4Ω, THD = 10%			86		
IQ	Quiescent Current	VDD = 5V	No Load		5		mA
Isd	Shutdown Current	VDD = 2.8V to 5V	/SD=0V			1	μA
Rdson	Static Drain-to Source On-state Resistor	High Side PMOS, I = 500mA	VDD=5.0V		325		mΩ
		Low Side NMOS, I = 500mA	VDD=5.0V		200		mΩ
fsw	Switching Frequency	VDD = 2.8V to 5V			400		kHz
Gv	Closed-loop Gain	VDD = 2.8V to 5V			300K/Rin		V/V
Vos	Output Offset Voltage	Input ac-ground, VDD = 5V				50	mV
VIH	SD Input High Voltage	VDD = 5V		1.4			V
VIL	SD Input Low Voltage	VDD = 5V				1.0	

Performance Characteristics (@TA=25°C, VDD=5V, Gain=18dB, RL=L(33μH)+R+L(33μH), unless otherwise noted.)

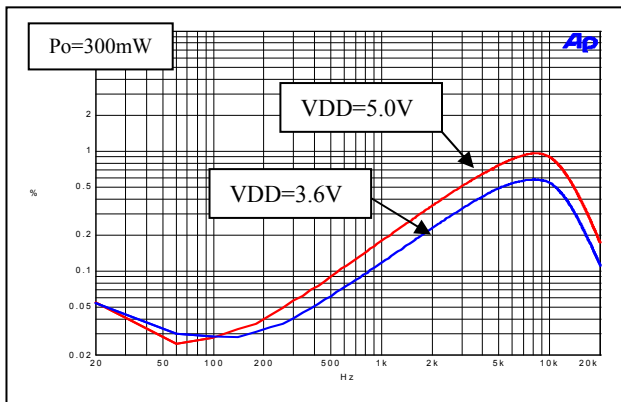
THD+N Vs. Output Power (RL=4Ω)



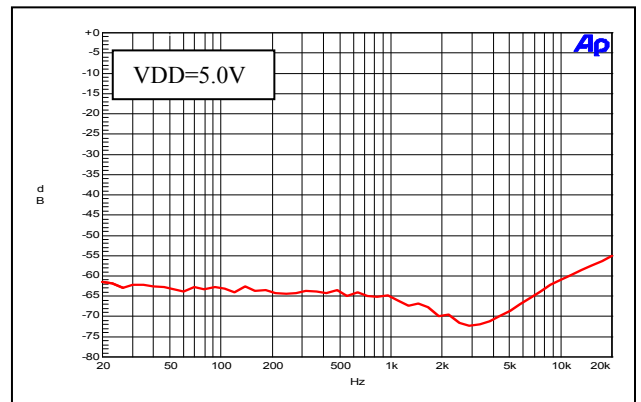
THD+N Vs. Output Power (RL=8Ω)



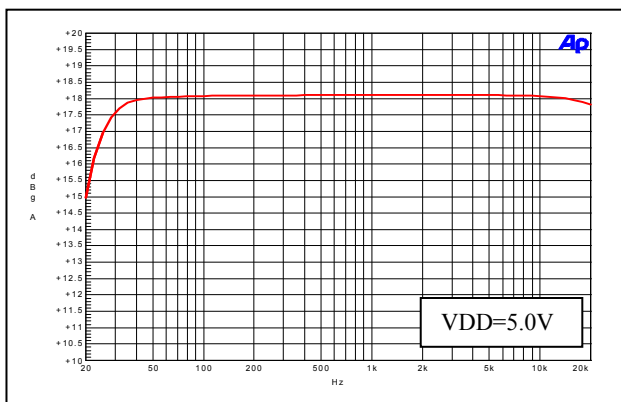
THD+N Vs. Frequency



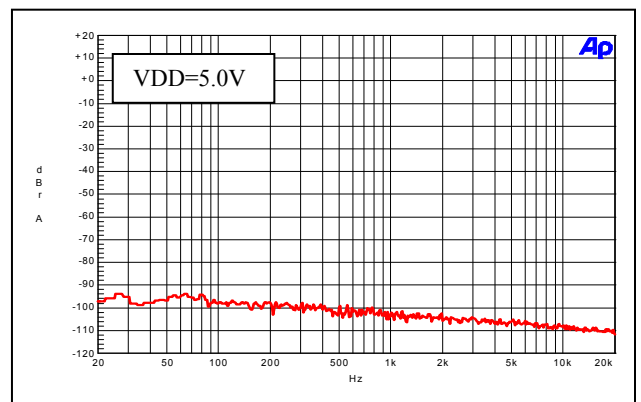
PSRR Vs. Frequency



Frequency Response

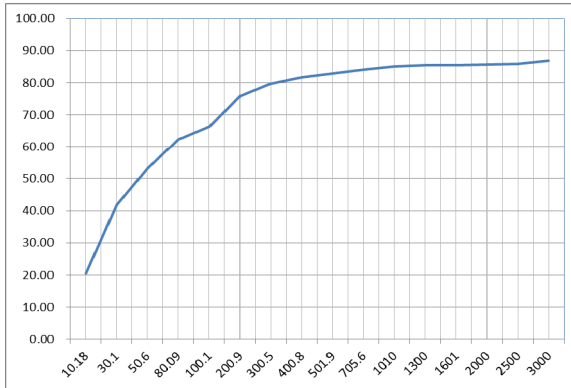


Noise Floor

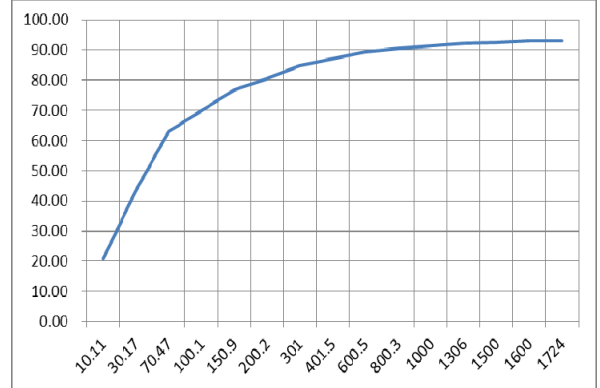


Performance Characteristics (@TA=25°C, VDD=5V, Gain=18dB, RL=L(33μH)+R+L(33μH), unless otherwise noted.)

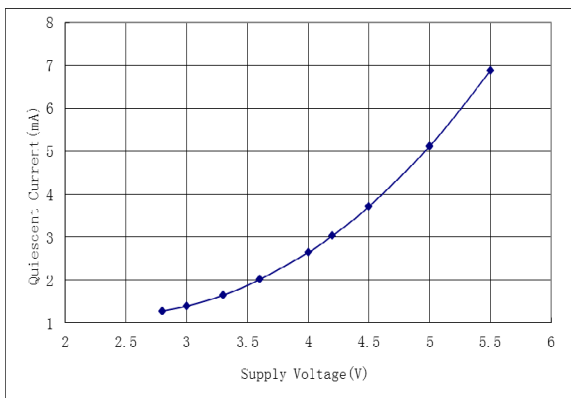
Efficiency Vs. Output Power (RL=4Ω)



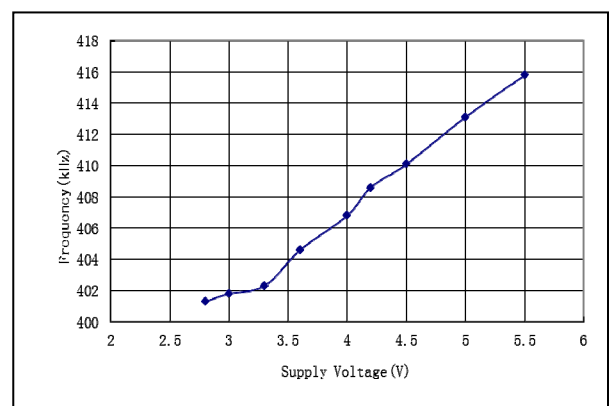
Efficiency Vs. Output Power (RL=8Ω)



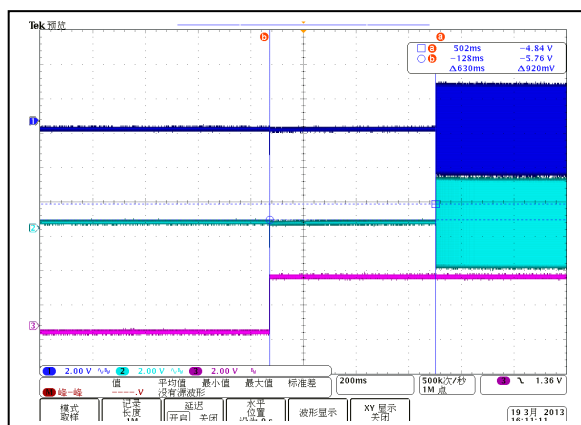
Quiescent Current Vs. Supply Voltage



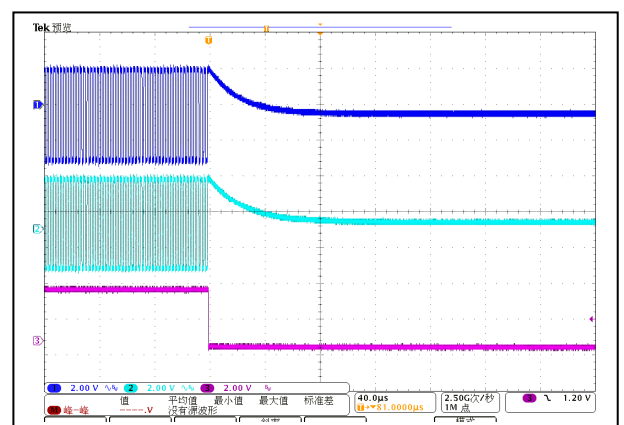
OSC Frequency Vs. Supply Voltage



Start-up Response



Shutdown Response



Application Information

Input Capacitors (C_i)

In the typical application an input capacitor C_i is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i form a high-pass filter with the corner frequency determined in the follow equation:

$$f_c = \frac{1}{(2\pi R_i C_i)}$$

It is important to consider the value of C_i as it directly affects the low frequency performance of the circuit. For example, when R_i is 150kΩ and the specification calls for a flat bass response down to 150Hz. The equation is reconfigured as followed to determine the value of C_i:

$$C_i = \frac{1}{(2\pi R_i f_c)}$$

When input resistance variation is considered, if C_i is 7nF one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i, R_i and R_f) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at VDD/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The PAM8304 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

Optimum decoupling is achieved by using two different types of capacitors that target different types of noise on the power supply leads. Higher frequency transients, spikes or digital hash should be filtered with a good low equivalent-series-resistance (ESR) ceramic capacitor with a value of typically 1μF. This capacitor should be placed as close as possible to the VDD pin of the device. Lower frequency noise signals should be filtered with a large ceramic capacitor of 10μF or greater. It's recommended to place this capacitor near the audio power amplifier.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination as shown in Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead it should be chosen with high impedance at high frequencies but low impedance at low frequencies.

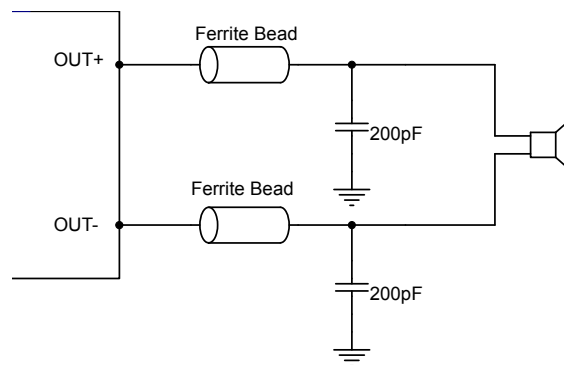


Figure 1 Ferrite Bead Filter to Reduce EMI

Application Information (cont.)

Shutdown Operation

In order to reduce power consumption while not in use the PAM8304 contains amplifier shutdown circuitry. When a logic low or ground is applied to the /SD pin the PAM8304 will enter a standby mode and supply current drawn will be minimized.

Under Voltage Lock-out (UVLO)

The PAM8304 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.0V or below, the PAM8304 goes into a state of shutdown. The device returns to normal operation only when VDD is higher than 2.5V.

Short Circuit Protection (SCP)

The PAM8304 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed the device will be reactivated.

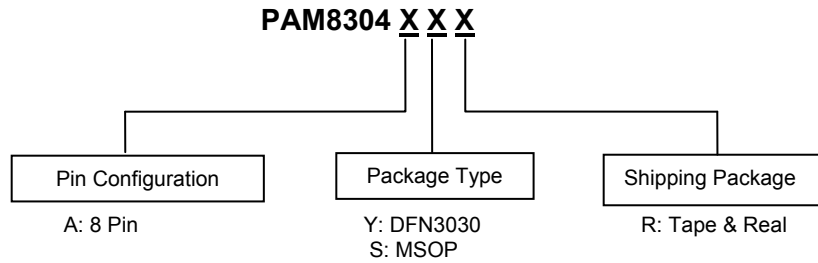
Over Temperature Protection (OTP)

Thermal protection prevents the device from damage. When the internal die temperature exceeds a typical of 150°C the device will enter a shutdown state and the outputs are disabled. This is not a latched fault, once the thermal fault is cleared and the temperature of the die decreased by 40°C the device will restart with no external system interaction.

Anti-POP and Anti-Click Circuitry

The PAM8304 contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Ordering Information



Part Number	Package	Standard Package
PAM8304AYR	DFN3030-8L	3,000Units/Tape&Real
PAM8304ASR	MSOP-8L	2,500Units/Tape&Real

Marking Information

DFN3030 /MOP8



PAM8304: Product Code

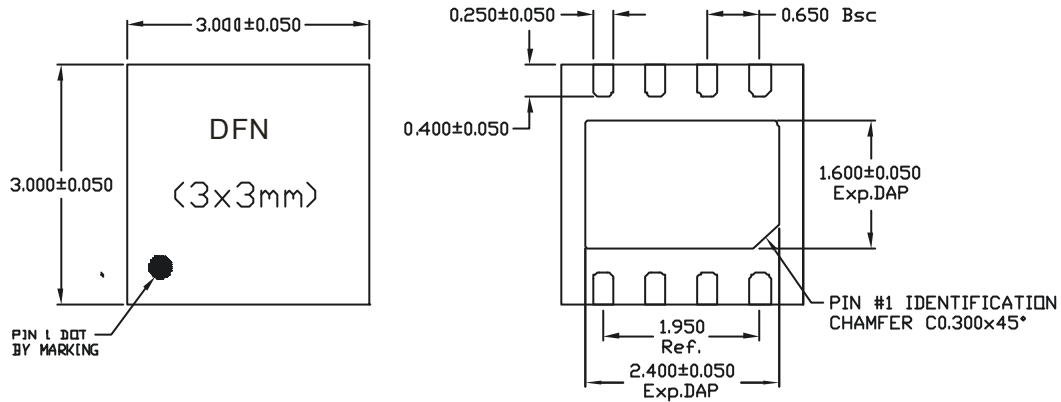
X: Internal Code

Y: Year

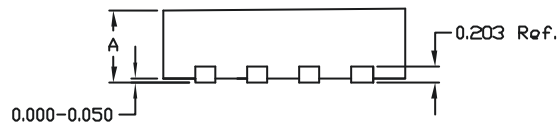
W: Week

Package Outline Dimensions (All dimensions in mm.)

Package: DFN3030



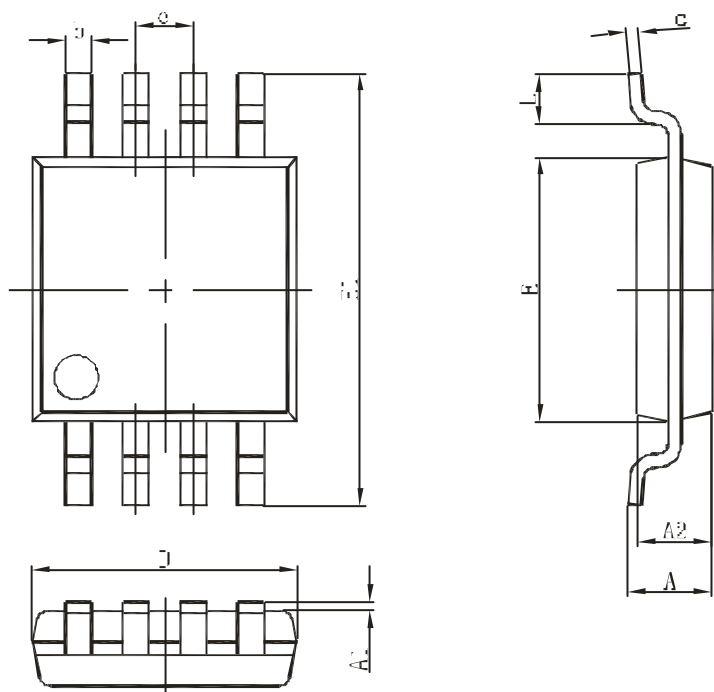
A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700



Unit: Millimeter

Package Outline Dimensions (All dimensions in mm.)

Package: MSOP



REF	Millimeter	
	Min	Max
A	--	1.10
A1	0.05	0.15
A2	0.78	0.94
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.75	5.05
e	0.65BSC	
L	0.40	0.70

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